Genesys Logic, Inc.

GL816E

USB 2.0 9-in-1
Card Reader Controller

Datasheet
Revision 1.33
Mar. 06, 2005

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Revision History

Revision	Date	Description
1.00	10/06/2003	First formal release
1.10	10/15/2003	Added 128-pin PQFP package data
1.11	11/05/2003	Added USB2.0 certified Test ID in Chapter 2 Features
1.12	04/06/2004	Changed pin 45 and pin 118 pin description
1.13	04/09/2004	1. Changed pin no. for NVMA15, XO, XI and AVDD2 in table 3.2 2. Added Company Logo in Package Dimension.
1.14	05/28/2004	Updated DC Characteristics in Chapter 6
1.15	06/16/2004	1. Added media memory card type in Chapter 1 And 2. 2. Removed NAND flash memory interface. 3. Changed Table 6.2 - DC Characteristics value.
1.20	06/25/2004	1. Changed Table 6.1 - Absolute Maximum Ratings value. 2. Added Reset Timing in Chapter 6.3.
1.21	07/15/2004	1. Added CF card information in Chapter 2. 2. Added CF Timing in Chapter 6.3.
1.22	11/18/2004	Removed PCMCIA interface. a. Changed PCCE2Z to CFCE2Z; PCMCIA CE2# to CF CE2#. b. Changed PCCE1Z to CFCE1Z; PCMCIA CE1# to CF CE1#. c. Removed PCMCIA address 10~3.
1.23	12/06/2004	1. Changed Chapter 6.3.8 Reset Timing 2. Changed 54 pin name from SD_WPZ to SD_WP 3. Changed Chapter 3.3 Pin Descriptions
1.30	01/18/2005	1. Changed Table 6.1 - Absolute Maximum Ratings 2. Added Table 6.2 - Operating Conditions 3. Added AC Characteristics Chapter 6.4.4 xD-Picture
1.31	01/21/2005	Added Chapter 6.4.10 93C46 Timing
1.32	02/01/2005	Changed power pin description in Table 3.2
1.33	03/06/2005	Changed pin# 32,33 pin description

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CHAPTER 1 GENERAL DESCRIPTION

The GL816E is a highly integrated, flexible application USB 2.0 Multi-Interface Flash Card Reader controller. It supports USB 2.0 high-speed transmission to CompactFlash™ (CF) Type I/II, Micro Drive, Secure Digital™ (SD), Mini SD™, MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick Pro™ (MS Pro), Memory Stick Pro™ Duo (MS Pro Duo) Memory Stick ROM, SmartMedia™ (SM) 5V/3.3V, and xD-Picture Card™ (xD) on one chip. Besides the flash card interface controller each, the GL816E integrates Genesys Logic own design USB 2.0 high-speed UTMI (**U**SB 2.0 **T**ransceiver **M**acrocell **I**nterface) transceiver. As a single chip solution for USB 2.0 multi flash card reader, the GL816E complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL816E can support different kinds of multi-interface combinations. For the best performance consideration, the GL816E integrates high efficiency card interface hardware engine for data transfer, and the 48MHz feature-enhanced 8051 micro-controller. The GL816E also supports firmware upgrade via USB interface, and external flash read/ write for firmware upgrade and other applications.

The GL816E pin assignment design fits to card sockets to provide easier PCB layout. With two package types, the 128-pin LQFP (14mm x 14mm) and the 128-pin PQFP (14mm x 20mm), the GL816E can fit your various design in both standalone and PC embedded USB 2.0 multi-interface flash card reader/ writer applications.

CHAPTER 2 FEATURES

- USB specification compliance
  - Complies with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Complies with USB Storage Class specification rev. 1.0.
  - Supports 1 device address and up to 10 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/ Interrupt (3), and 3 optional Bulk Read/ Write endpoints pair.
- Integrated USB building blocks
  - Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).
  - Build-in power-on reset (POR) and low-voltage detector (LVD).
- Embedded 8051 micro-controller
  - Operate @ 48 MHz clock.
  - Embedded 32K Byte mask ROM and internal 256 byte SRAM.
  - Supports up to external 64K ROM/ Flash for design flexibility.
- Support firmware upgrade to external flash via USB interface
- USB 2.0 certified (TestID=40390389)
- Support all kinds of flash card interface
  - SmartMedia / xD-Picture Card Interface
  - Memory Stick / Memory Stick Pro Card Interface
  - Secure Digital / MultiMediaCard Interface
  - CompactFlash Type I/II
- 3.3V operation
- Flexible pin utilization
  - Dedicated power control pins and programmable card-enable pins.
  - Supports 4(or more) GPIO pins for design flexibility.
  - Pin assignment fits to card sockets for easy PCB layout.
  - Shared pins for SmartMedia™ interface.
- SmartMedia™ interface
  - Address support up to 4 bytes, 8 bit data width and different speed
  - Supports different page size, and automatic append redundant area data (8 / 16 bytes)
  - Hardware ECC encoding and decoding capability
  - Supports firmware correct page ECC error capability
  - Compliant with xD-Picture Card
- xD-Picture Card™ interface
  - Complies with xD-Picture™ interface specification
  - Compliant SmartMedia™ interface
- Memory Stick™ (MS) / Memory Stick Duo™ (MS Duo) / High Speed Memory Stick™ (HS MS) / Memory Stick Pro™ (MS Pro) / Memory Stick Pro™ Duo (MS Pro Duo) Memory Stick ROM interface
  - Complies with Memory Stick Standard Memory Stick PRO Format Specifications ver 1.00-01
  - Complies with Memory Stick Format Specifications ver 1.40-00
  - Hardware support 4-bit HS Memory Stick PRO interface
  - Supports INS signal
  - Supports automatic CRC16 generation and verification
  - Supports different clock rate up to 40 MHz
- Secure Digital™ , Mini SD™ and MultiMediaCard™
  - Complies with Secure Digital™ / MultiMediaCard™ interface specification
  - Supports both SD / MMC mode access CLK/CMD/DAT0/DAT1/DAT2/DAT3
  - Command transmit and response receive can be enabled separately

- Automatic CRC7 generation for command and CRC7 verification for response on CMD
- Support automatic CRC16 generation and verification on DAT3-0
- In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
- Data processing in block or byte
- Supports different clock rate from 375 KHz to 24 MHz

- High efficient hardware engine
  - Automatic data read / write with card by hardware engine
  - Easier firmware development
  - Media interface signals output low automatically when suspend
- Inter-Media transfer capability
  - Support data copy between flash cards or in the same flash memory card
- Support external ICE / micro-controller interface
  - Easy firmware development environment
  - Easy operate by external robust microprocessor
- Available in 128-pin LQFP and 128-pin PQFP package

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

Figure 3.1 - 128 Pin LQFP Pinout Diagram

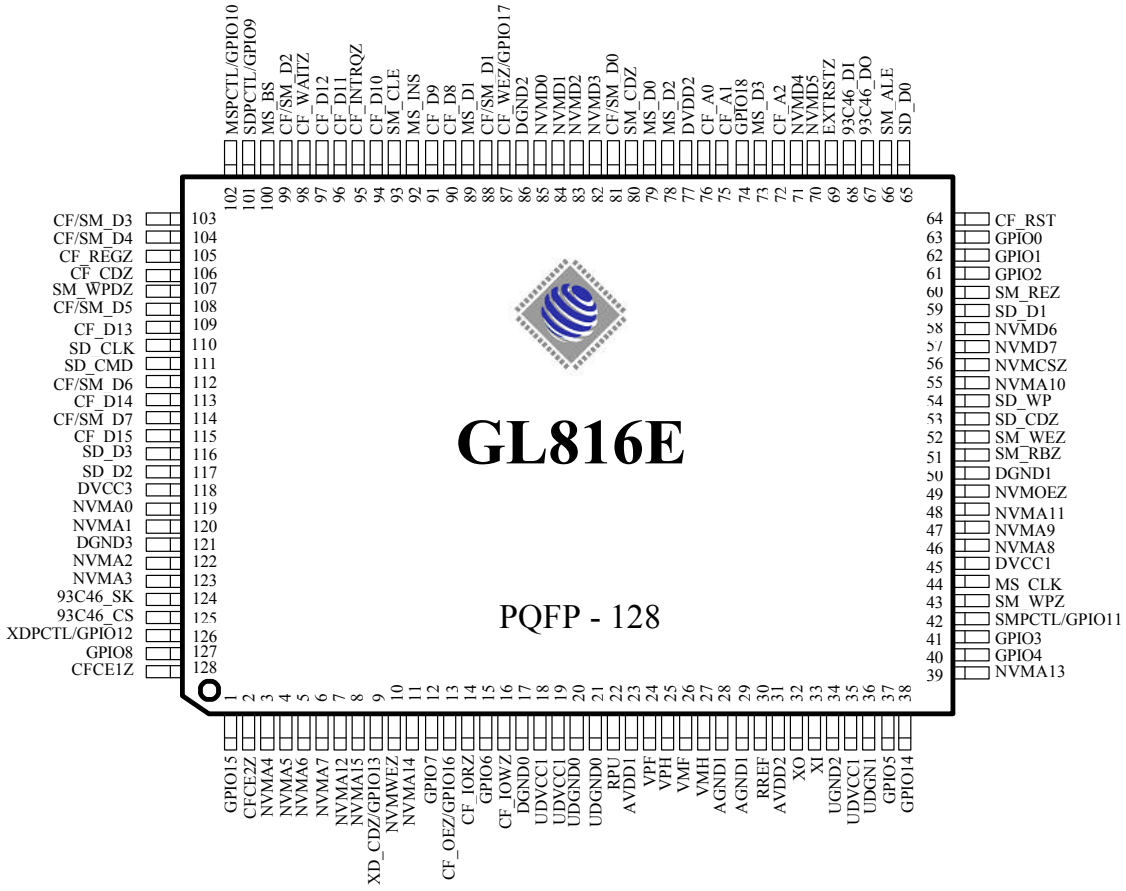


Figure 3.2 - 128 Pin PQFP Pinout Diagram

3.2 Pin List

Table 3.1 - Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	GPIO15	B	33	XI	I	65	SD_D0	B/SO	97	CF_D12	B
2	CFCE2Z	B/O	34	UGND2	P	66	SM_ALE	O	98	CF_WAITZ	I/SO
3	NVMA4	O	35	UDVCC1	P	67	93C46_DO	B/I	99	CF/SM_D2	B
4	NVMA5	O	36	UDGND1	P	68	93C46_DI	B/O	100	MS_BS	O
5	NVMA6	O	37	GPIO5	B/O	69	EXTRSTZ	I	101	SDPCTL/ GPIO9	B/O
6	NVMA7	O	38	GPIO14	B	70	NVMD5	O	102	MSPCTL/ GPIO10	B/O
7	NVMA12	O	39	NVMA13	O	71	NVMD4	O	103	CF/SM_D3	B
8	NVMA15	O	40	GPIO4	B/O	72	CF_A2	O	104	CF/SM_D4	B
9	XD_CDZ/ GPIO13	B/I	41	GPIO3	B/O	73	MS_D3	B	105	CF_REGZ	B/O
10	NVMWEZ	O	42	SMPCTL/ GPIO11	B/O	74	GPIO18	B	106	CF_CDZ	B/I
11	NVMA14	O	43	SM_WPZ	O	75	CF_A1	O	107	SM_WPDZ	B/I
12	GPIO7	B/O	44	MS_CLK	O	76	CF_A0	O	108	CF/SM_D5	B
13	CF_OEZ/ GPIO16	B/O	45	DVCC1	P	77	DVDD2	P	109	CF_D13	B
14	CF_IORZ	O	46	NVMA8	O	78	MS_D2	B	110	SD_CLK	O
15	GPIO6	B/O	47	NVMA9	O	79	MS_D0	B	111	SD_CMD	B/SO
16	CF_IOWZ	O	48	NVMA11	O	80	SM_CDZ	B/I	112	CF/SM_D6	B
17	DGND0	P	49	NVMOEZ	O	81	CF/SM_D0	B	113	CF_D14	B
18	UDVCC1	P	50	DGND1	P	82	NVMD3	O	114	CF/SM_D7	B
19	UDVCC1	P	51	SM_RBZ	B/I	83	NVMD2	O	115	CF_D15	B
20	UDGND0	P	52	SM_WEZ	O	84	NVMD1	O	116	SD_D3	B
21	UDGND0	P	53	SD_CDZ	B/I	85	NVMD0	O	117	SD_D2	B
22	RPU	A	54	SD_WP	B/I	86	DGND2	P	118	DVCC3	P
23	AVDD1	P	55	NVMA10	O	87	CF_WEZ/ GPIO17	B/O	119	NVMA0	O
24	VPF	B	56	NVMCSZ	O	88	CF/SM_D1	B	120	NVMA1	O
25	VPH	B	57	NVMD7	O	89	MS_D1	B	121	DGND3	P
26	VMF	B	58	NVMD6	O	90	CF_D8	B	122	NVMA2	O
27	VMH	B	59	SD_D1	B/SO	91	CF_D9	B	123	NVMA3	O
28	AGND1	P	60	SM_REZ	O	92	MS_INS	B/I	124	93C46_SK	B/O
29	AGND1	P	61	GPIO2	B/O	93	SM_CLE	O	125	93C46_CS	B/O
30	RREF	A	62	GPIO1	B/O	94	CF_D10	B	126	XDPCTL/ GPIO12	B/O
31	AVDD2	P	63	GPIO0	B/O	95	CF_INTRQZ	B/I	127	GPIO8	B
32	XO	B	64	CF_RST	B	96	CF_D11	B	128	CFCE1Z	B/O

3.3 Pin Descriptions

Table 3.2 - Pin Descriptions

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
NVMA15~0	8,11,39,7, 48,55,47, 46,6~3, 123,122, 120,119	O	Ext. flash address 15~0
NVMWEZ	10	O	Ext. flash WE#
RPU	22	A	USB resistor pull up
VPF	24	B	FS D+
VPH	25	B	HS D+
VMF	26	B	FS D-
VMH	27	B	HS D-
RREF	30	A	Reference resistor
XO	32	I	12MHz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL/CLK. It may not be used to drive any external circuitry other than the crystal circuit.
XI	33	B	12MHz Crystal This pin can be connected to one terminal of the crystal or can be connected to an external 12MHz clock when a crystal is not used.
NVMOEZ	49	O	Ext. flash OE#
NVMCSZ	56	O (pu)	Ext. flash CS#
NVMD7~0	57,58,70, 71,82~85	B (pd)	Ext. flash Data 7~0
EXTRSTZ	69	I (pu)	External reset #, the active low signal is used by the system to reset the chip. The active low pulse should be at least 1 us wide.

Memory Interface			
Pin Name	**Pin#**	**Type**	**Description**
CFCE2Z	2	B/I (pu)	CF CE2#
XD_CDZ	9	B/I (pu)	XD CD#, this is the card detection signal from xD-Picture device to indicate if the device is inserted, Normal high.
CF_IORZ	14	O	CF IOR#
CF_IOWZ	16	O	CF IOW#
CF_OEZ	13	O	CF OE#
SM_PCTL	42	B/O	SmartMedia power control
SM_WPZ	43	O	SmartMedia WP#, This pin is an active low write protect signal for the SM device, when SMC is enabled. Normal high.

MS_CLK	44	O	Memory Stick SCLK output
SM_RBZ	51	B/I (pu)	SmartMedia RDY/BSY#
SM_WEZ	52	O	SmartMedia WE#
SD_CDZ	53	B/I (pu)	SD Card detection#, this is the card detection signal from SD device to indicate if the device is inserted, Normal high.
SD_WP	54	B/I (pu)	SD Write Protect Detection, this pin is an active high write protect signal for the SD device, when SD is enable. Normal low.
SD_D0~3	65,59,117, 116	B/SO (pu)	SD DAT0~3
SM_REZ	60	O	SmartMedia RE#
CF_RST	64	B (pd)	CF reset
SM_ALE	66	O	SmartMedia ALE
CF_A2~0	72,75,76	O	CF address 2~0
MS_D3~0	73,78,89, 79	B/SO (pu)	MS DAT3~0
SM_CDZ	80	B/I (pu)	SmartMedia CD#, this is the card detection signal from SM device to indicate if the device is inserted, active low.
CF/SM_D0~7	81,88,99, 103,104, 108,112, 114	B/SO (pu)	CF / SmartMedia DAT0~7
CF_WEZ	87	O	CF WE#
CF_D8~15	90,91,94, 96,97,109, 113,115	B/I (pu)	CF DAT8~15
MS_INS	92	B/I (pu)	Memory Stick INS
SM_CLE	93	O	SmartMedia CLE
CF_INTRQZ	95	B/I	CF INTRQ#
CF_WAITZ	98	I/SO (pu)	CF WAIT#
MS_BS	100	O	MemoryStick BS
SD_PCTL	101	B/O	SD/MMC power control
MS_PCTL	102	B/O	Memory Stick power control
CF_REGZ	105	B/O (pu)	CF REG#
CF_CDZ	106	B/I (pu)	CF CD# . CF card detection, this pin is connected to the ground on the CF card, when the CF device is inserted.
SM_WPDZ	107	B/I (pu)	SmartMedia Write Protect Detect, this pin is an active low write protect signal for the SM device, when SM is enable. Normal high.
SD_CLK	110	O	SD/MMC CLK
SD_CMD	111	B/SO (pu)	SD/MMC CMD
XD_PCTL	126	B/O	XD power control
CFCE1Z	128	B/I (pu)	CF CE1#

EEPROM Interface			
Pin Name	**Pin#**	**Type**	**Description**
93C46_DO	67	B/I	93C46 Data out
93C46_DI	68	B/O	93C46 Data in
93C46_SK	124	B/O	93C46 Clock
93C46_CS	125	B/O	93C46 CS

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
GPIO18~0	74,87,13,1, 38,9,126, 42,102,101, 127,12,15, 37,40,41, 61,62,63	B (odpu)	GPIO18~0

Power / Ground			
Pin Name	**Pin#**	**Type**	**Description**
DGND0~3	17,50,86, 121	P	Digital GND #0~3
UDVCC1	18,19,35	P	UTMI Digital VCC
UDGND0~1	20,21,36	P	UTMI Digital GND
AVDD1	23	P	Analog VDD #1
AGND1	28,29	P	Analog GND #1
AVDD2	31	P	Analog VDD #2
UGND2	34	P	UTMI GND
DVCC1,3	45,118	P	Digital VDD #1, 3
DVDD2	77	P	Digital VDD #2

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

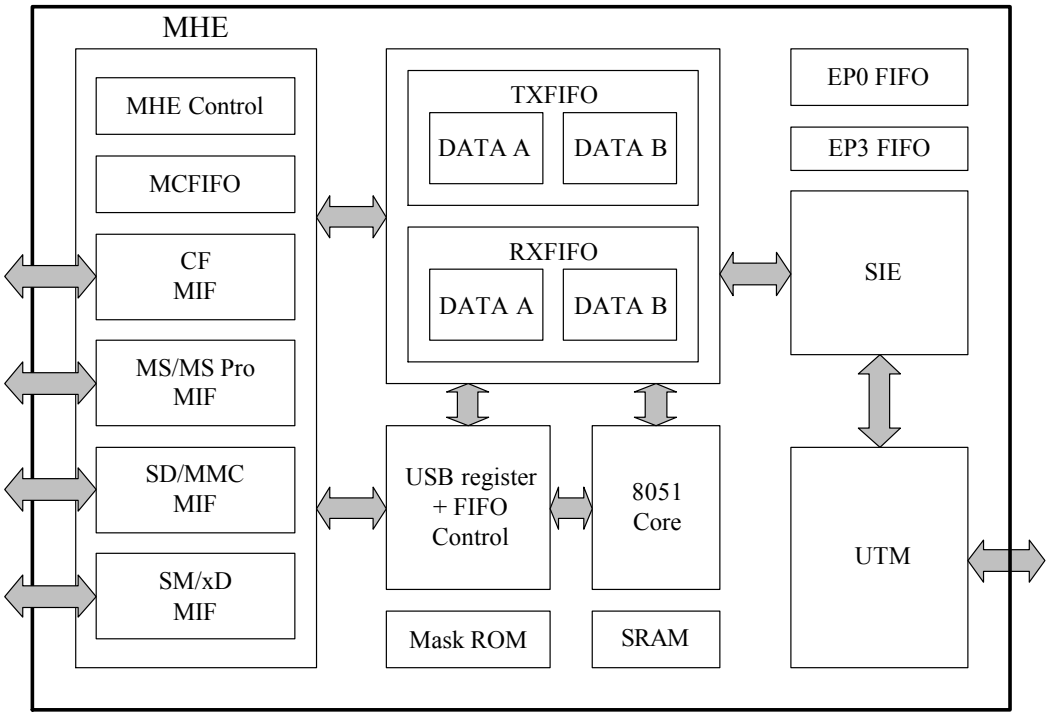


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTIONAL DESCRIPTION

5.1 UTM

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

5.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

5.3 EP0 FIFO

It is composed of TX0FIFO and RX0FIFO, with 64-byte FIFO each, and it is used for endpoint 0 data transfer.

5.4 EP3 FIFO

It's an 8-byte FIFO for endpoint 3.

5.5 Bulk FIFO

It is composed of TXFIFO and RXFIFO for data transmission and receiving respectively, also with different modes support:

TXFIFO:

1. To ensure the continuous data transmission, TXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and two 16 bytes corresponding redundant areas. All can be directly accessed by 8051 µC.
2. Normally SIE popes data, MHE pushes data for DATA A/B FIFOs, and redundant area is pushed by MHE when SmartMedia MIF is enabled and popped by uC.
3. Supports uC single byte access for SmartMedia ECC error correction.
4. At transmit mode SIE won't transmit data filled in TXFIFO before uC complete the data integrity checking.

RXFIFO:

1. To ensure the continuous data transmission, RXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and 16 bytes single redundant area. All can be directly accessed by 8051 µC.
2. Normally MHE popes data, SIE pushes data for DATA A/B FIFOs, and redundant area is pushed by uC and popped by MHE when SmartMedia MIF is enabled.

Buffer Mode:

1. Buffer mode is enabled by firmware and is used to copy data block from source to destination in same card for SmartMedia or Memory Stick applications.
2. Under Buffer mode, firmware can enable MIF to read source data block to TXFIFO, check the data integrity, then enable MIF to write data in TXFIFO to destination data block space on memory card.
3. For SmartMedia application, the redundant data write to destination data block space is from redundant area of RXFIFO.

5.6 MHE (Media Hardware Engine)

The Media Hardware Engine contains 4 MIF (Media Interface), MHE control and MCFIFO.

1. **MIF (Media Interface):** There are CompactFlash MIF, Memory Stick/ Memory Stick PRO MIF, Secure Digital/ MultiMediaCard MIF and SmartMedia/ xD-Picture Card MIF in MHE.
2. **MCFIFO (Media Control FIFO):** It's a 64-byte FIFO that shared by Memory Stick/ Memory Stick PRO and SD/ MMC MIF. In MemoryStick application, the MCFIFO is used for register read and write function; In SD/ MMC application, it is used for command and response.
3. **SMAFIFO (SmartMedia™ Address FIFO):** It's a 4-byte FIFO for SmartMedia address only.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Ambient Temperature	-40°C to +80 °C
Supply Voltage to Ground Potential	-0.5V to +4.0V
DC Input Voltage to Any Pin	-0.5V to +5.8V

6.2 Operating Conditions

Table 6.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.25%

6.3 DC Characteristics

Table 6.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage		2.6	-	5	V
V_{IL}	Input Low Voltage		0.0	-	0.7	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-10	-	10	µA
V_{OH}	Output High Voltage		3.0	-	-	V
V_{OL}	Output Low Voltage		-	-	0.2	V
I_{OH}	Output Current High	VDD=3.3V V_{OH}=2.6V	-	8.3	-	mA
I_{OL}	Output Current Low	VDD=3.3V V_{OL}=0.8V	-	7.8	-	mA
C_{IN}	Input Pin Capacitance		-	-	2.0	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	280	µA
I_{CC}	Supply current	Connect to USB with 8051 operating	-	-	85	mA

6.4 AC Characteristics

6.4.1 UTMI Transceiver

The GL816E is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

6.4.2 External Flash

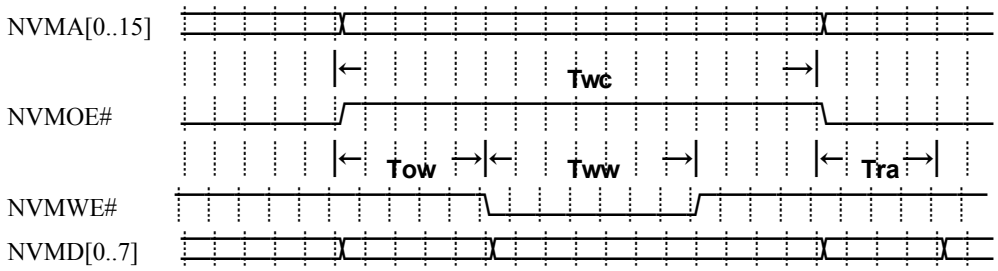
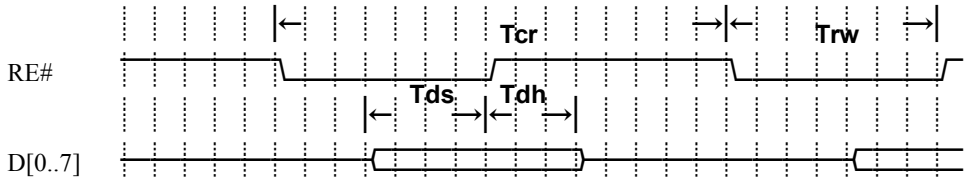


Figure 6.1 - Timing Diagram of External Flash

Parameter	Description	Min	Typ	Max	Unit
T_{WC}	Write data cycle time		102.5		ns
T_{WW}	Write pulse width		41.6		
T_{OW}	OE# to WE# time		38.6		
T_{RA}	Read Access time			90	

6.4.3 SmartMedia

Read



Write

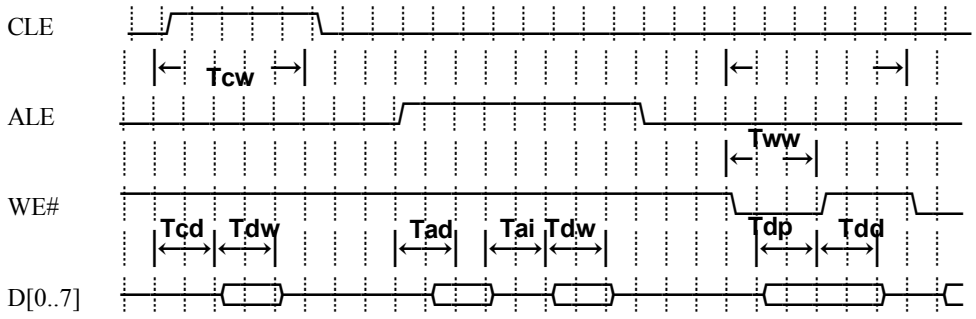
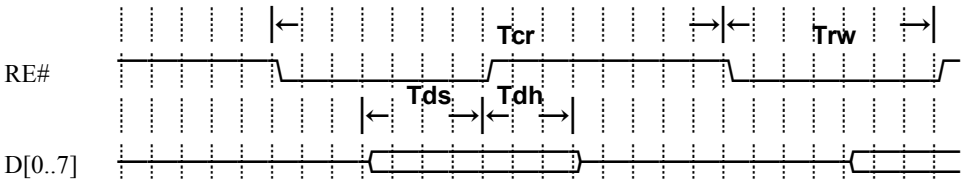


Figure 6.2 - Timing Diagram of SmartMedia

Parameter	Description	Mode	Min	Typ	Max	Unit
Tcw	CLE active width	Normal		165		ns
		Slow		198		
Twc	Write data cycle time	Normal		100		
		Slow		166		
Tww	Write pulse width	Normal		66		
		Slow		100		
Tcd	CLE-to-command delay			33.3		
Tdw	Data width	Normal		67		
		Slow		100		
Tad	ALE-to-address delay			33.3		
Tai	Address data interval time			33.3		
Tdp	Data pre-output delay			33.3		
Tdd	Data delay time			33.3		
Tcr	Read data cycle time	Normal		133.3		
		Slow		166.6		
Trw	Read pulse width			100		
Tds	Data setup time			40		
Tdh	Data hold time			20		

6.4.4 xD-Picture

Read



Write

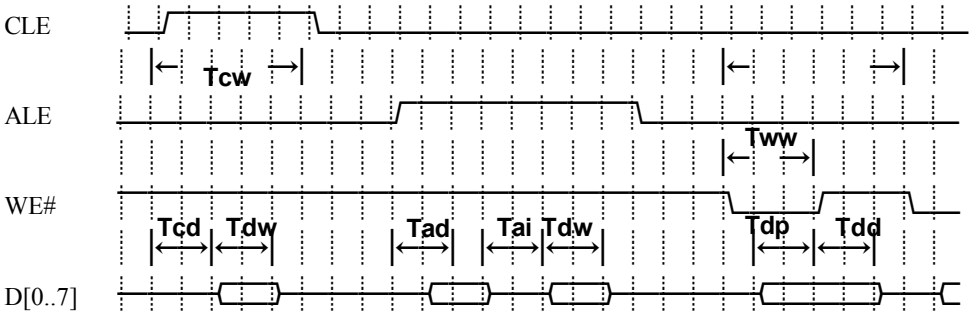


Figure 6.3 - Timing Diagram of xD-Picture

Parameter	Description	Mode	Min	Typ	Max	Unit
Tcw	CLE active width	Normal		165		ns
		Slow		198		
Twc	Write data cycle time	Normal		100		
		Slow		166		
Tww	Write pulse width	Normal		66		
		Slow		100		
Tcd	CLE-to-command delay			33.3		
Tdw	Data width	Normal		67		
		Slow		100		
Tad	ALE-to-address delay			33.3		
Tai	Address data interval time			33.3		
Tdp	Data pre-output delay			33.3		
Tdd	Data delay time			33.3		
Tcr	Read data cycle time	Normal		133.3		
		Slow		166.6		
Trw	Read pulse width			100		
Tds	Data setup time			40		
Tdh	Data hold time			20		

6.4.5 Memory Stick

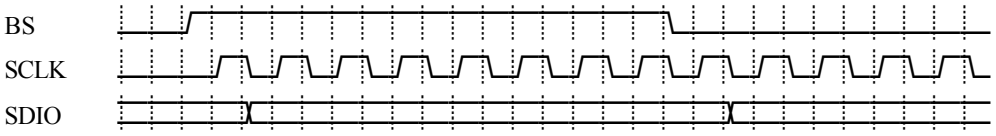


Figure 6.4 - Timing Diagram of MemoryStick

Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	1.5M	Hz	
		1	6M		
		2	15M		
		3	24M		

6.4.6 Memory Stick PRO

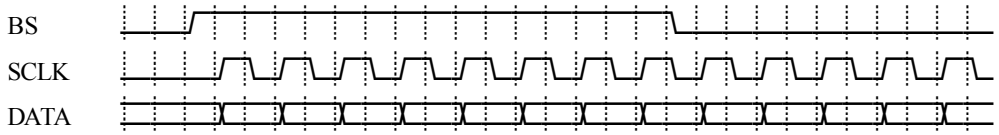


Figure 6.5 - Timing Diagram of MemoryStick PRO

Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	30M	Hz	
		1	40M		

6.4.7 Secure Digital / MultiMedia Card

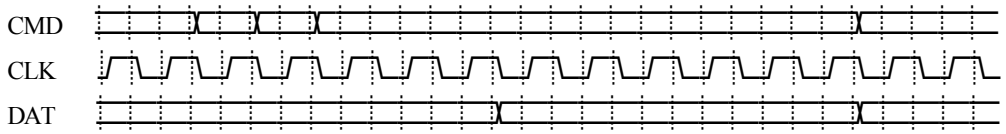


Figure 6.6 - Timing Diagram of SD / MMC

Parameter	Description	Mode	Typ	Unit	Remark
Fck	CLK frequency	0	375K	Hz	
		1	6M		
		2	15M		
		3	24M		

6.4.8 CompactFlash Card

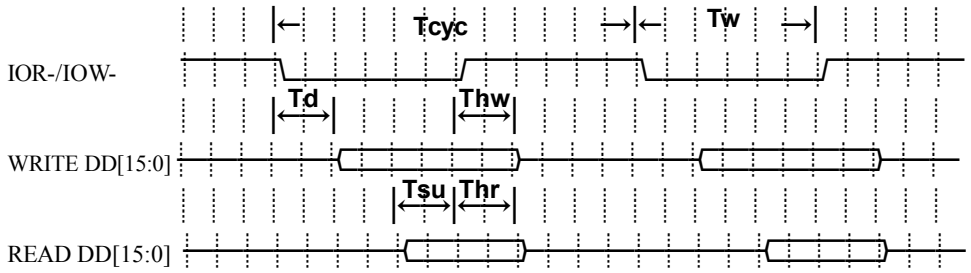


Figure 6.7 - Timing Diagram of CompactFlash

Parameter	Description	Mode	Min	Typ	Max	Unit
Tcyc	Read/Write Cycle Time	0	-	665	-	ns
		1	-	416	-	
		2	-	266	-	
		3	-	199	-	

Tw	Read/Write Active Width	0	-	332	-	
		1	-	166	-	
		2	-	132	-	
		3	-	99	-	
Td	Delay Time for Write Data	0	-	-	0	
		1	-	-	0	
		2	-	-	0	
		3	-	-	0	
Thw	Data Hold Time following IOW-	0	30	-		
		1	30	-	-	
		2	15	-	-	
		3	15	-	-	
Tsu	Data Setup Time before IOR-	0	20	-	-	
		1	20	-	-	
		2	20	-	-	
		3	20	-	-	
Thr	Data Hold Time following IOR-	0	8	-	-	
		1	8	-	-	
		2	8	-	-	
		3	8	-	-	

6.4.9 Reset Timing

Figure 6.8 - Timing Diagram of Reset

Parameter	Description	Minimum	Unit	Remark
Trst	This active low signal is used by the system to reset the chip; the active low pulse should be at least 1us wide.	1	us	

6.4.10 93C46 Timing

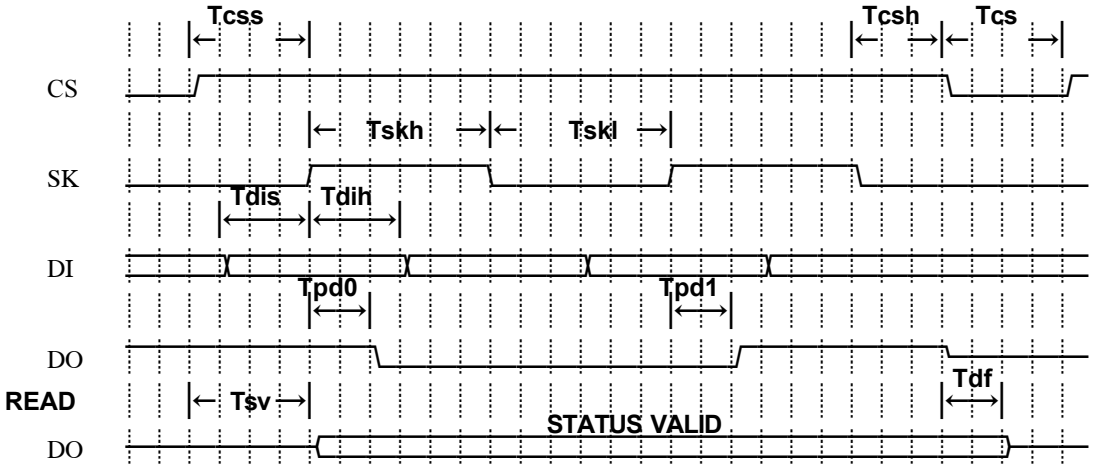
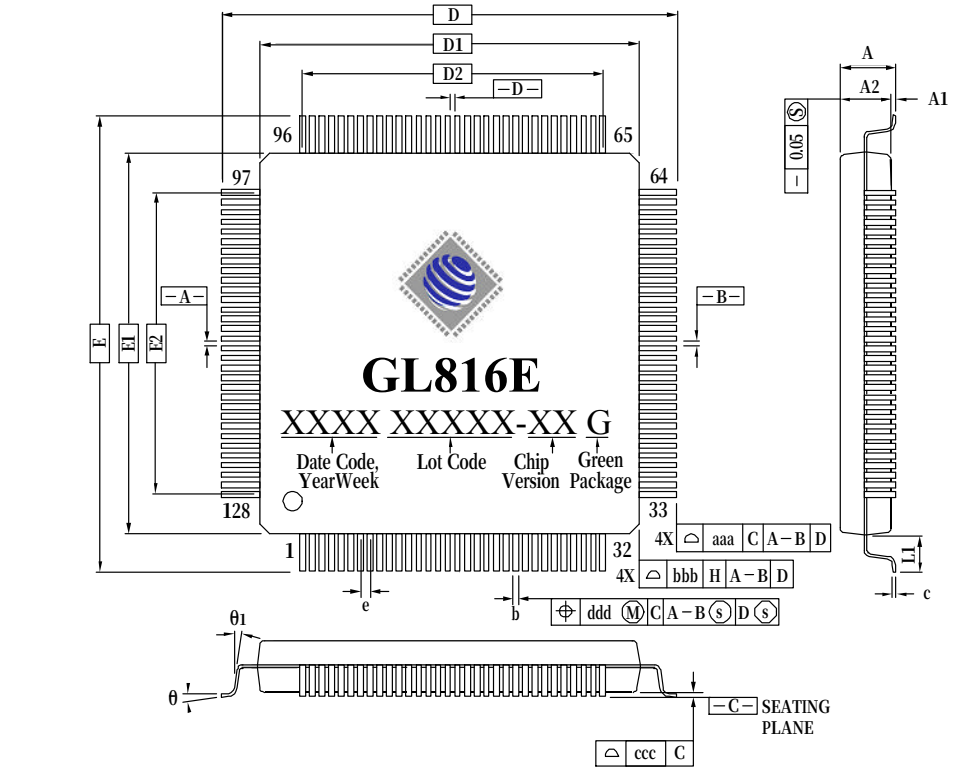
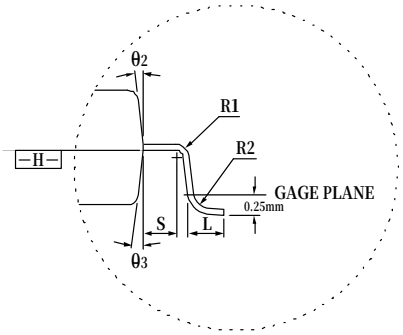


Figure 6.9 - Timing Diagram of 93C46

Parameter	Description	Min	Typ	Max	Unit
Tskh	SK High Time	250	-	-	ns
Tskl	SK Low Time	250	-	-	
Tcs	Minimum CS Low Time	250	-	-	
Tcss	CS Setup Time	50	-	-	
Tdis	DI Setup Time	100	-	-	
Tcsh	CS Hold Time	0	-	-	
Tdih	DI Hold Time	100	-	-	
Tpd1	Output Delay to “1”	-	-	250	
Tpd0	Output Delay to “0”	-	-	250	
Tsv	CS to Status Valid	-	-	250	
Tdf	CS to DO in High Impedance	-	-	100	

CHAPTER 7 PACKAGE DIMENSION





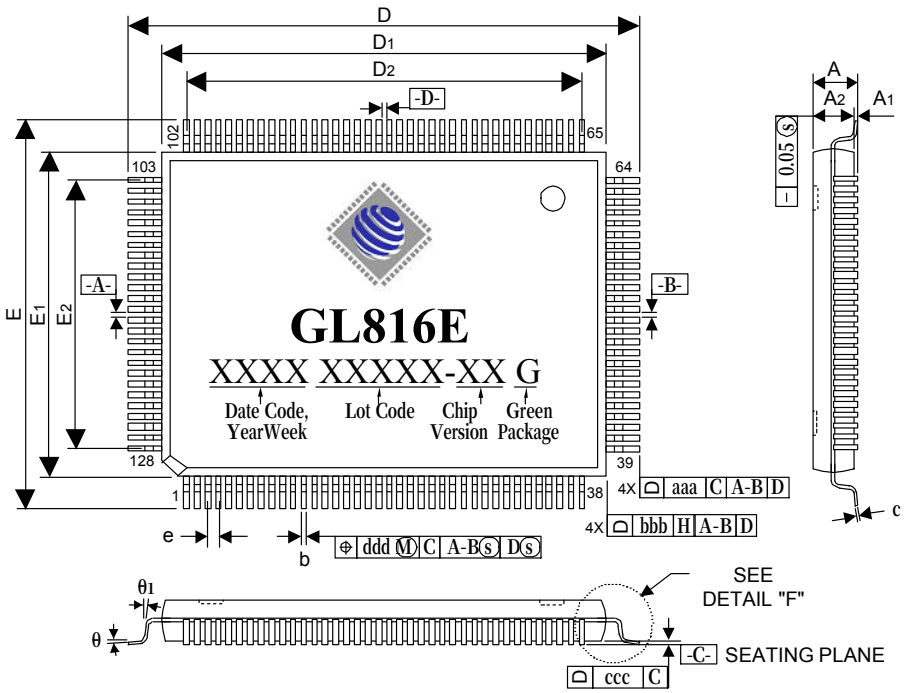
CONTROL DIMENSIONS ARE IN MILLIMETERS.

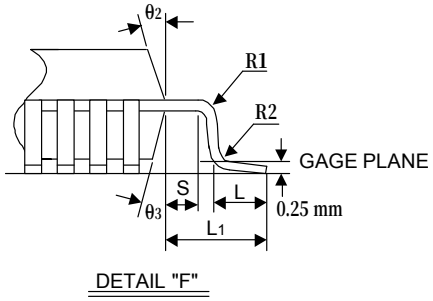
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	12.40 BASIC			0.488 BASIC		
E2	12.40 BASIC			0.488 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BASIC			0.016 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

Figure 7.1 - GL816E 128 Pin LQFP Package





DETAIL "F"

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
E	17.20 BASIC			0.677 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.50 BASIC			0.728 BASIC		
E2	12.50 BASIC			0.492 BASIC		
R1	0.13	—	0.30	0.005	—	0.012
R2	0.13	—	—	0.005	—	—
θ	0	—	7	0	—	7
θ1	0	—	—	0	—	—
θ2	15 REF			15 REF		
θ3	15 REF			15 REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 7.2 - GL816E 128 Pin PQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Status
GL816E	128-pin LQFP	
GL816E	128-pin PQFP	