AK8823
HDTV & NTSC/PAL Multi-Format Encoder
SDTV/HDTV x2 OverSampling 5ch DACs

General Description

The AK8823 is a HD / SD Simultaneous Output Video Encoder with on-chip 5 Channel 10 Bit DACs .
As input data, in SD block, SMPTE-125M-1995 / ITU-R BT. 601, 656 compatible Y / Cb / Cr 4:2:2 formats (8 bit) are accepted and, in HD block, SMPTE-274M-1998 (1080i), SMPTE-296M-2001 (720p) compatible Y / Cb / Cr 4:2:2 formats (8 bit x 2) are accepted.

As input data capture method, either a Synchronous mode to be made by detecting encoded EAV signal or a mode to synchronize with externally-fed H / V SYNC signals is selectable.

Outputs of SDY / SDC and HDY / HDPB / HDPR signals can be independently controlled by turning ON /OFF corresponding DACs.

VBI signal and Macrovision signal can be also superimposed on output in addition to Video signals, by register setting.

Features

HD

- Compatible input data : SMPTE125M-1995 / ITU-R BT601(525i/625i)
  SMPTE274M-1998 (1080i)
  SMPTE296M-2001 (720p)
- Input Signal Formats : Y/Cb/Cr 4:2:2 (8bit x 2)
  - 525i / 625i
  - 525p / 625p
  - 1080i / 720p
  (note) ITU-R656-4 compatible mode in 525i / 625i formats
- Output Signals : Y/Pb/Pr Interlace (EIA 770.1-A) (EIA 770.3-A)
  Y/Pb/Pr Progressive (EIA 770.2-A) (EIA 770.3-A)
- On chip out-put limiter
- Input Signal Synchronization :
  - EAV Decode (*)
  - Slave Operation by HSYNC / VSYNC signals
- VBID (CGMS-A), CC / XDS, WSS
- Macrovision 525i / 625i Rev. 7.1.1L and 525p / 625p Macrovision Progressive 1.2
- On-Chip Color Bar Generator
- On-Chip Black Burst Generator
- Adjustable YPbPr Delay Function

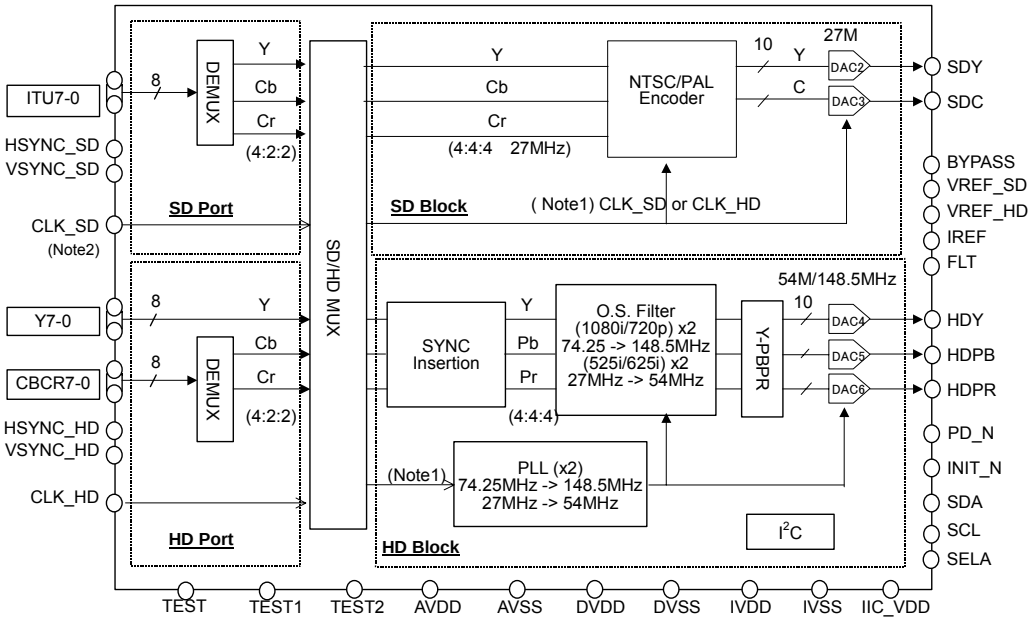
SD NTSC/PAL Encoder

- NTSC-M, PAL-B, D, G, H, I. M, N Encoding
- S-Video Output
- On-chip out-put limiter
- ITU-R BT.656, 4:2:2, 8 Bit Parallel Input (EAV Decoding)
  - Slave Operation by HSYNC / VSYNC Signals
- VBID (CGMS-A), CC / XDS, WSS
- Macrovision Anti-Taping Rev. 7.1.1L

- I2C Bus I / F (400 KHz)
- Power-Down Mode
- On-Chip VREF
- 3.0 V, 1.8 V CMOS
- 65 Pin BGA

(*) Violation of EAV decode is on 625p video mode. Refers to p.38.

Block Diagram



SD Side Input Video Port and HD Side Input Video Port are independently equipped.
525i / 625i signals on SD Input Port can be processed at HD Block ,or D1 signal on HD Input Port can be processed at SD Block.
(Note 1) in the Block diagram, denotes a clock to be used internally.
Either of the two Ports can be selected by register setting. A clock in the selected Port is used which is assigned by bit 7 VPRTSD of Video Process 4 Register at address 0x14 for SD Block or bit 5 VPRT of HD DAC Control Register at address 0x05 for HD Block. Video Signal is processed in the same manner.
(Note 2) When video data on HD port is transferred to SD block, the same clock in CLK_HD pin must be fed to CLK_SD pin.

Table Of Contents

1. Electrical Characteristics

Absolute Maximum Ratings (all voltages are referenced to ground level, AVSS = DVSS = 0V)

Item	Min.	Max.	Units
Power Supplies (VDD) AVDD (DAC,PLL, VREF) DVDD (Digital Core) IVDD (Digital I/O) IIC_VDD (I2C Power Supply)	-0.3	 4.2 2.2 2.2 4.2	V
Input Pin Voltage (VIN)	-0.3	IVDD + 0.3 IIC_VDD + 0.3	V
Input Current (IIN)		+/- 10	mA
Storage Temperature	-40	125	°C

(note) Operation under a condition exceeding above limits may cause permanent damage to the device. Normal operation is not guaranteed under the above, extreme conditions.

Recommended Operating Conditions

Item	Min.	Typ.	Max.	Units
Power Supply (VDD) AVDD DVDD = IVDD IIC_VDD	 2.66 1.65 DVDD	 3.0 1.8 1.8	 3.45 2.0 3.45	V
Operating Temperature (TA)	-20		85	°C

Analog Characteristics and Power Dissipation (AVDD = 3.0V, DVDD = IVDD = IIC_VDD = 1.8V, Ta= 25°C)

Item	Min.	Typ.	Max.	Units	Condition
DAC Resolution		10		bit	
Integral Non-Linearity Error INL		+/- 1.5		LSB	note 1)
Differential Non-Linearity Error DNL		+1.0/- 1.0		LSB	note 1)
Output Full Scale Voltage	1.15	1.28	1.41	V	HDY output = 150 ohms, all other outputs= 300 ohms
DAC SNR		70		dB	50 % Gray Scale
Output Bandwidth		+/- 1		dB	note 2)
Variations among DACs		1.5	TBD	%	note 3)
On-Chip Reference Voltage		1.43		V	
Reference Voltage Drift		350		ppm/°C	
Current Consumption of Analog part		49	70	mA	note 4)
Current Consumption of Digital part		50	79	mA	note 4)
Power-Down Current		100	1000	uA	PD_N : at " L " setting note 5)

note 1) operation at HD DAC : 148 MHz, SD DAC : 27 MHz

note 2) Output Bandwidth 30 MHz : at 148 MHz operation, HDY (load resistor at 150 ohms) channel only, external load capacitance (TBD pF)

note 3) variation when a 700 mV equivalent code is input on DACs. Specified in each of SD and HD groups.

note 4) DAC 5 channels " ON " (SD : on-chip color bar HD : 30 MHz - 1 dB FS)

note 5) values are after initialization of internal filter by either INT_N or by register setting, and before the Power-down.

Digital Input / Output DC Characteristics

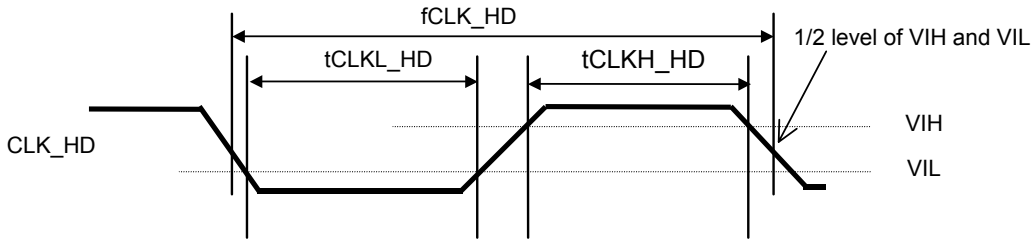
(AVDD = 2.66 ~ 3.45V, IVDD = DVDD = 1.65 ~ 2.0V, IIC_VDD = DVDD ~ 3.45V, Ta= -20~ 85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Units
High Level Input Voltage	VIH	ITU7-0, Y7-0, CBCR7-0 CLK_SD, CLK_HD HSYNC_SD, VSYNC_SD HSYNC_HD, VSYNC_HD INIT_N, PD_N	0.77IVDD			V
Low Level Input Voltage	VIL	ITU7-0, Y7-0, CBCR7-0 CLK_SD, CLK_HD HSYNC_SD, VSYNC_SD HSYNC_HD, VSYNC_HD INIT_N, PD_N			0.21IVDD	V
Input pin Leakage Current	ILIKG	I2C and digital input pins (test pins excluded)			+/-10	uA
I2C High Level Input Voltage	VIH2	SELA, SDA, SCL	0.77IIC_VDD			V
I2C Low Level Input Voltage	VIL2	SELA, SDA, SCL			0.21IIC_VDD	V
I2C Low Level Output Voltage	VOL2	SDA, IOL = 3mA			0.4	V

AC Timing

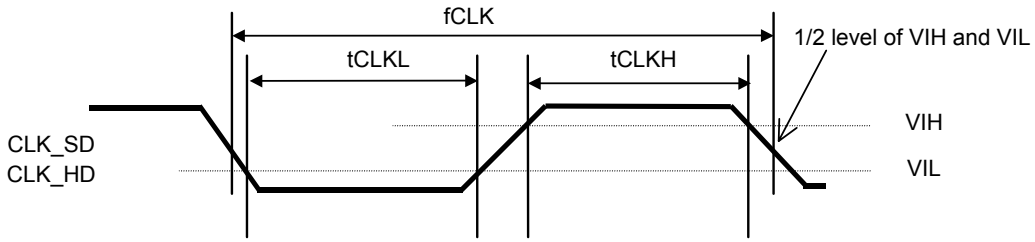
(AVDD = 2.66V ~ 3.45V, DVDD = IVDD = 1.65V ~ 2.0V, Ta = -20 ~ +85°C)

(1) CLK_HD at 74.25 MHz operation



Item	Symbol	Min.	Typ.	Max.	Units	Condition
CLK_HD	fCLK_HD		74.25		MHz	74.25 / 74.175MHz
CLK_HD pulse width H	tCLKH_HD	4.04			nsec	
CLK_HD pulse width L	tCLKL_HD	4.04			nsec	

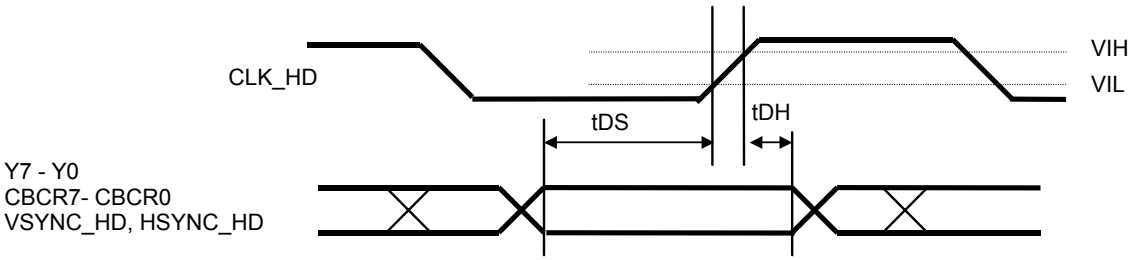
(2) CLK_SD / CLK_HD t 27 MHz operation



Item	Symbol	Min.	Typ.	Max.	Units	Condition
CLK_SD CLK_HD	fCLK_SD fCLK_HD		27		MHz	27MHz (note)
CLK_SD / CLK_HD pulse width H	tCLKH_SD tCLKH_HD	15.0			nsec	
CLK_SD / CLK_HD pulse width L	tCLKL_SD tCLKL_HD	15.0			nsec	

(note) if this frequency shifts, color is not retrieved in SD mode in a display monitor.
The AK8823 operation is not affected, though.

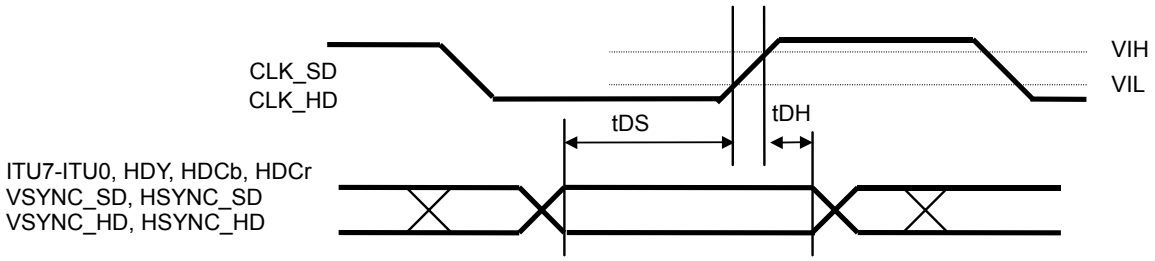
(3) Pixel Data Input Timing -- (1) at 74.25 MHz clock operation



Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Set-up Time	tDS_HD	4.4			nsec
Data Hold Time	tDH_HD	1.45			nsec

(note) polarities of VSYNC_HD, HSYNC_HD are pre-settable by register [Address 0x05 bit 6 HVINV].

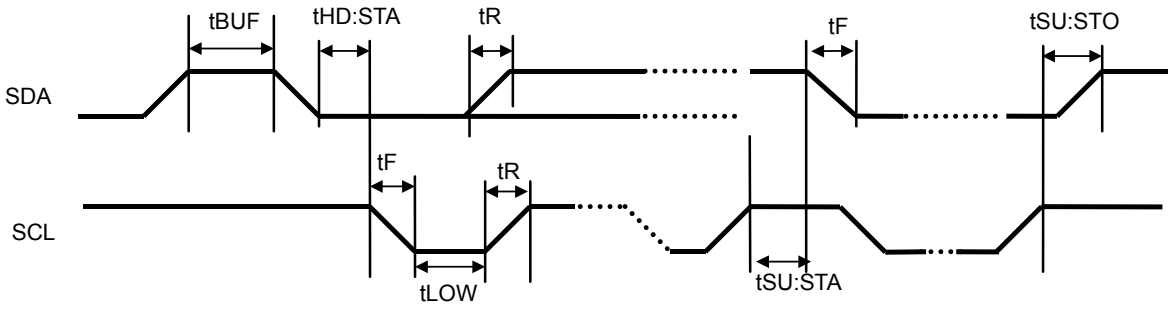
(4) Pixel Data Input Timing (2) at 27 MHz clock operation



(note) polarities of VSYNC_HD, HSYNC_HD are pre-settable by register [Address 0x05 bit 6 HVINV].

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Set-up Time	tDS_SD tDS_HD	5.0			nsec
Data Hold Time	tDH_SD tDH_HD	5.0			nsec

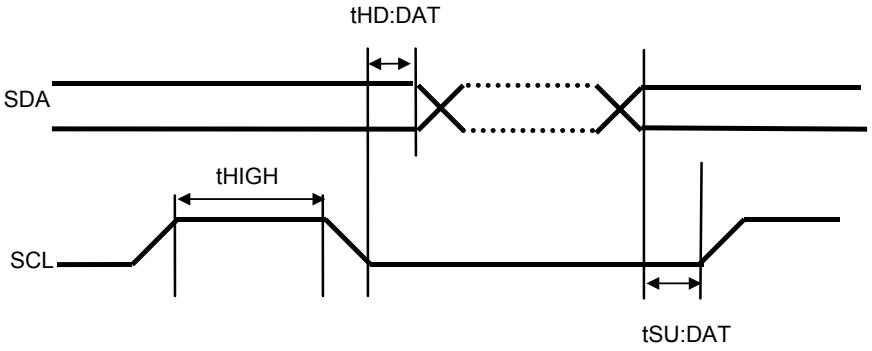
(5) I2C Timing
(5-1) Timing 1



Parameter	Symbol	Min.	Max.	Unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

The above I2C Bus related timings are I2C Bus specifications, and they are not the device limits.
For details, refer to I2C Bus Specifications.

(5-1) Timing 2



Parameter	Symbol	Min.	Max.	Unit
Data Setup Time	tSU:DAT	100 (note1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (note2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

note 1 : when to use in I2C Bus Standard mode, tSU : DAT > = 250nsec must be satisfied.
note 2 : when the AK8823 is used on the not-extended tLOW Bus (used at tLOW = minimum specification), this condition must be satisfied.

No external clock is required to write into / read from registers via I2C interface.
Each operation completes with SCL clock only.
However, a 27MHz clock is required to enable SD block when to access such registers in SD block as VBID / CC / WSS (Addresses 0x18,0x19, 0x26 ~ 0x2B) and Status (at 0x34).
When a 27 MHz clock is stopped once and when to access those registers again, it should be executed after waiting 2 Frame time after the recovery of clock.

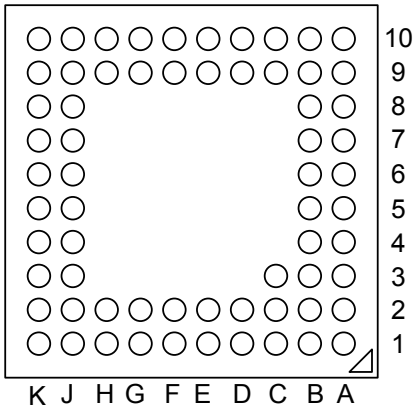
2. Pin Functional Description

Pin name	I/O	Pin No.	Power supply to used	Functional outline
ITU7	I	J8	IVDD	SD Data Input pins (ITU-R. BT.656)
ITU6		K7		
ITU5		J7		
ITU4		K6		
ITU3		J6		
ITU2		J4		
ITU1		K3		
ITU0		J3		
Y7	I	D10	IVDD	Y Data Input pins in HD Block mode
Y6		D9		
Y5		F9		
Y4		G10		
Y3		G9		
Y2		H10		
Y1		H9		
Y0		J10		
CBCR7	I	B3	IVDD	Cb / Cr Time-Division (multiplexed) Data Input pins
CBCR6		A4		
CBCR5		B4		
CBCR4		A5		
CBCR3		B5		
CBCR2		B9		
CBCR1		B10		
CBCB0		C10		
CLK_SD	I	K8	IVDD	Clock Input pin for SD Block. 27MHz
CLK_HD	I	A2	IVDD	Clock Input pin for HD Block. 27MHz / 74.25(74.125)MHz
HSYNC_SD	I	K2	IVDD	HSYNC Timing Input pin for SD Block in Slave Mode operation. Connect to IVSS when not in use
VSYNC_SD	I	J2	IVDD	VSYNC Timing Input pin for SD Block in Slave Mode operation. Connect to IVSS when not in use
HSYNC_HD	I	A7	IVDD	HSYNC Timing Input pin for HD Block in Slave Mode operation. Connect to IVSS when not in use
VSYNC_HD	I	B6	IVDD	VSYNC Timing Input pin for HD Block in Slave Mode operation. Connect to IVSS when not in use
BYPASS	O	H2	AVDD	Output pin to output On-Chip VREF voltage. Should be connected to Analog ground via a larger-than 0.1 uF capacitor.
IREF	O	H1	AVDD	Reference Current Output pin for DACs Should be connected to AVSS via a 3.9kohm (+/-1%) resistor.
FLT	O	B2	AVDD	Filter pin for PLL
HDY	O	D1	AVDD	DAC Output pin for Y signal in HD block
HDPB	O	D2	AVDD	DAC Output pin for Pb signal in HD block
HDPR	O	C1	AVDD	DAC Output pin for Pr signal in HD block
SDY	O	F1	AVDD	DAC Output pin for S-pin Luminance signal in SD block
SDC	O	F2	AVDD	DAC Output pin for S-pin Chroma signal in SD block
SCL	I	B7	IIC_VDD	I2C Bus Clock pin
SDA	I/O	A8	IIC_VDD	I2C Bus Data pin
SELA	I	B8	IIC_VDD	I2C Bus Address Select pin Low : 40H High : 42H
PD_N	I	C3	IVDD	Power-Down Control pin. L : PDN, H : normal operation
INIT_N	I	A3	IVDD	To initialize internal Digital filter. Initialization at " low ". To be pulled-up to IVDD when not in use.
VREF_HD	I	C2	AVDD	To be connected to AVDD via a 0.1 uF capacitor
VREF_SD	I	G1	AVDD	To be connected to AVDD via a 0.1 uF capacitor

Pin name	I/O	Pin No.	Power supply to used	Functional outline
IIC_VDD	P	A9		I2C power supply pin. Decoupling capacitor should be connected between this pin and IVSS pin
IVDD	P	J9		Power Supply pin for I / O part
IVSS	P	K9		Ground pin for I / O part
DVDD	P	F10, K4		Digital Power Supply pins
DVSS	P	E9, E10, J5, K5		Digital Ground pins
AVDD	P	E1		Analog Power Supply pin
AVSS	P	E2, J1		Analog Ground pins
TEST2	I	B1		left open
TEST3	I	G2		left open
TEST	I	A6		Test pin Should be connected to IVSS. This pin has on-chip pull-down resistor (100kohm typ.).
NC		A1, A10, C9,K1, K10		NC pins. left open.

3. Pin Layout

Bottom view



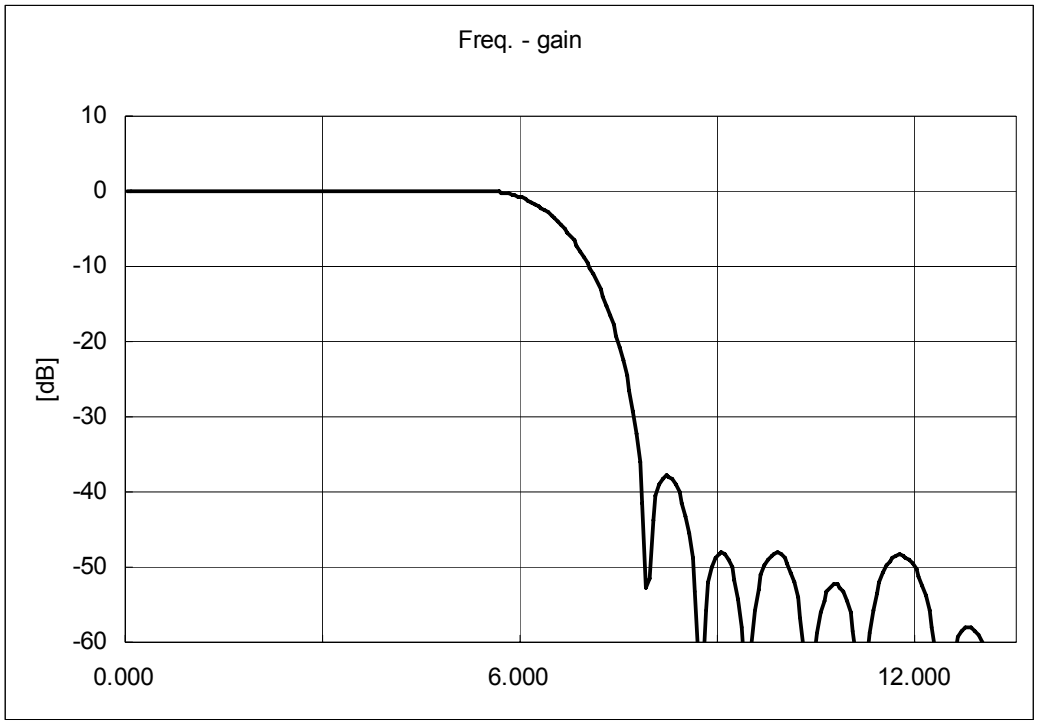
Bottom view

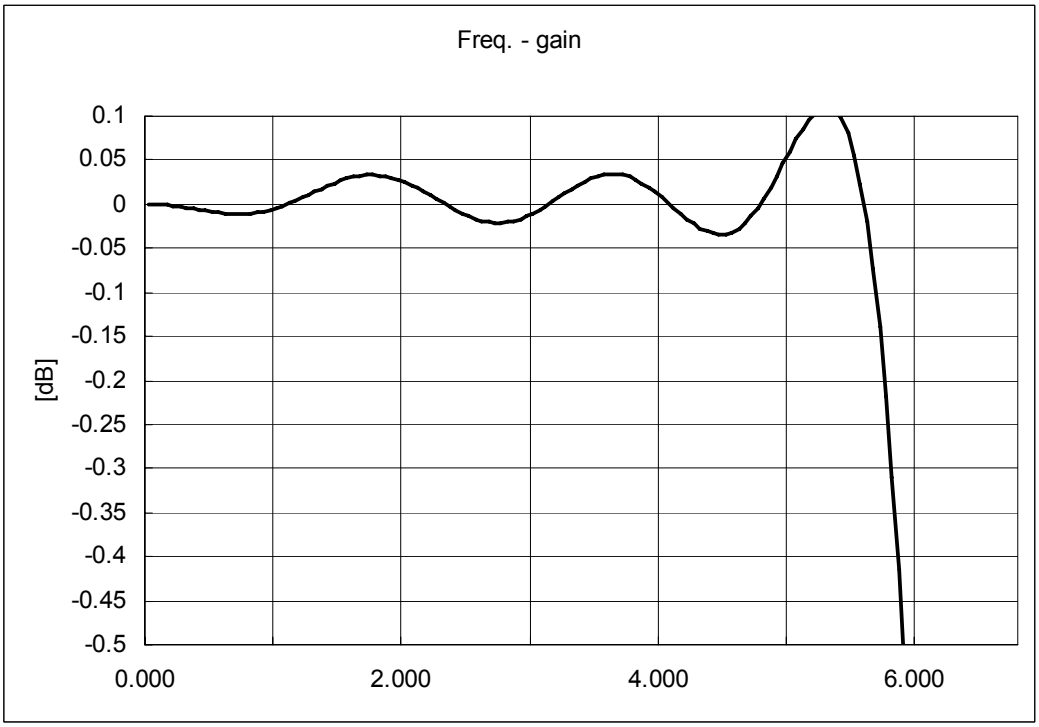
	K	J	H	G	F	E	D	C	B	A
10	NC	Y0	Y2	Y4	DVDD	DVSS	Y7	CBCR0	CBCR1	NC
9	IVSS	IVDD	Y1	Y3	Y5	DVSS	Y6	NC	CBCR2	IIC_VDD
8	CLK_SD	ITU7							SELA	SDA
7	ITU6	ITU5							SCL	HSYNC_HD
6	ITU4	ITU3							VSYNC_HD	TEST
5	DVSS	DVSS							CBCR3	CBCR4
4	DVDD	ITU2							CBCR5	CBCR6
3	ITU1	ITU0						PD_N	CBCR7	INIT_N
2	HSYNC_SD	VSYNC_SD	BYPASS	TEST3	SDC	AVSS	HDPB	VREF_HD	FLT	CLK_HD
1	NC	AVSS	IREF	VREF_SD	SDY	AVDD	HDY	HDPR	TEST2	NC

4. Video Signal Filter HD (HDY/HDPbPr) / SD (SDY)

Shown below is an example of normal over-sampling Filter Characteristics for Y /Pb / Pr and RGB signals for HD, and Luma signal for SD (Figures below show a 13.5MHz example at the right-end frequency scale when Y signal and Luma signal in 525i mode are up-sampled to 27MHz).

Similarly, the right-end frequency scale should be read as 27MHz in 525p mode and 74.25MHz in 1080i / 720p respectively. As for PbPr signal case, the right-end frequency should be scaled to 6.75MHz in 525i / 625i mode, 13.5MHz in 525p / 625p mode, and 37.125MHz in 1080i / 720p mode respectively.

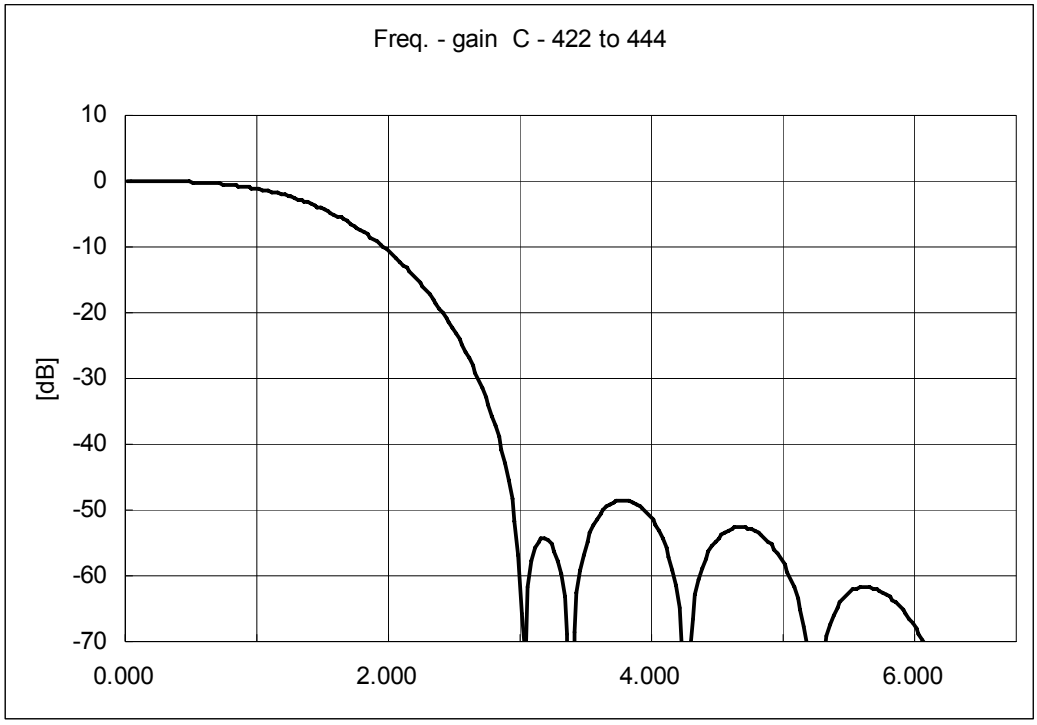


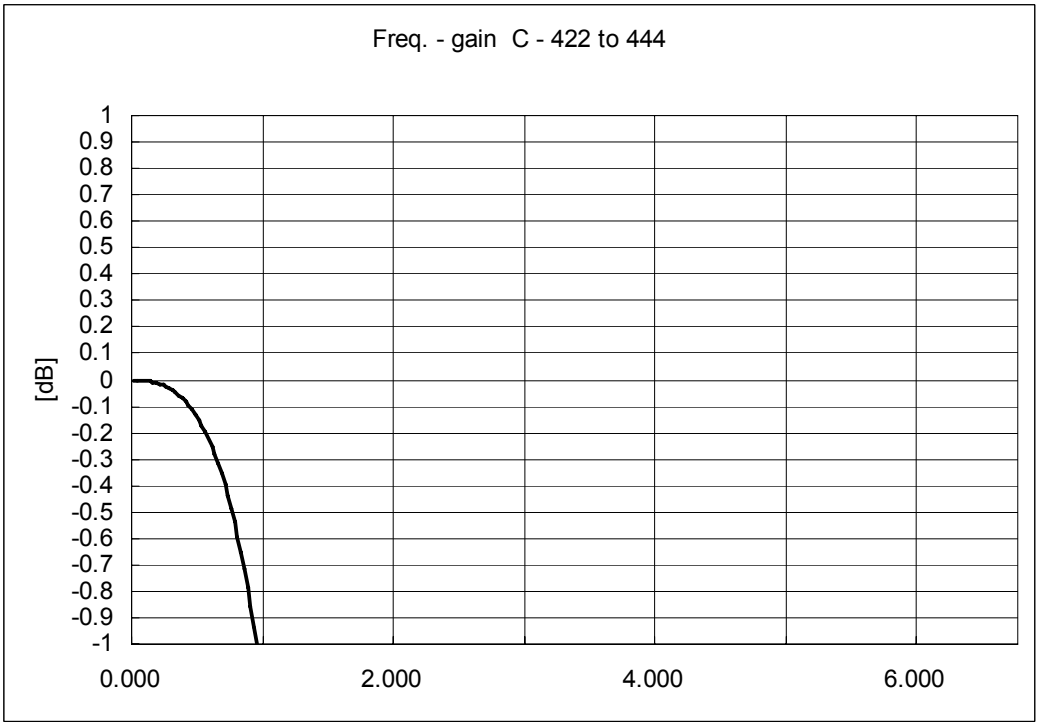


Filter Selection.
Above is the normal filter for Luminance signal pass, another two types filters, Mild and soft could be selected.

5. CbCr (4:2:2 → 4:4:4) Filter (SD)

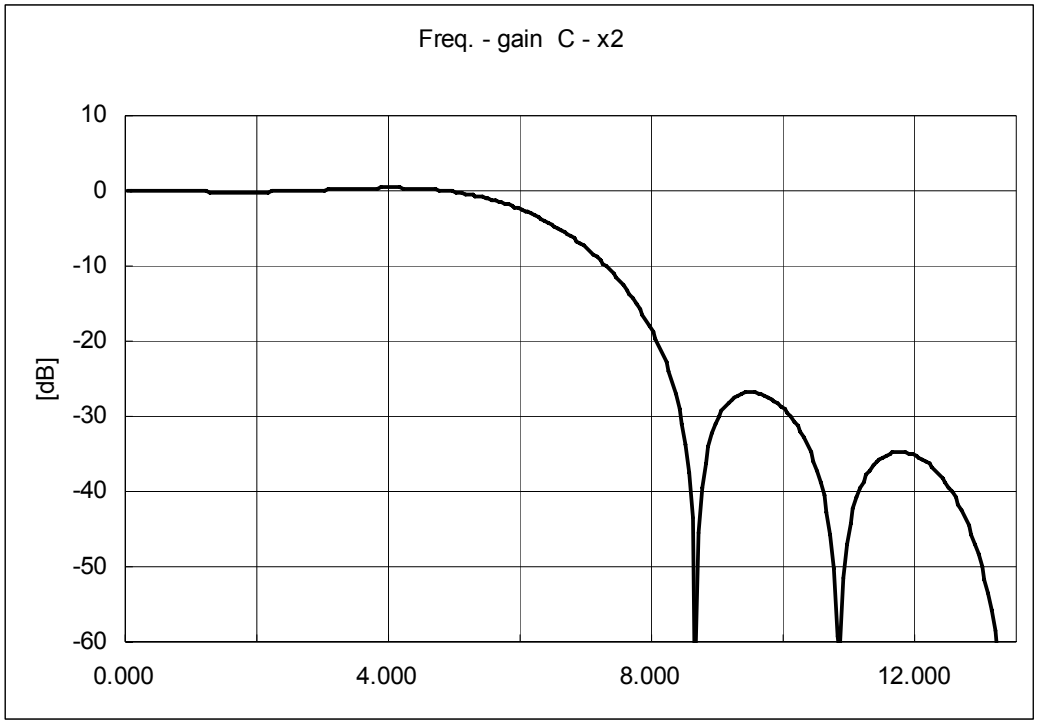
A 6.75 MHz rate CbCr Data is rated up to 13.5 MHz.

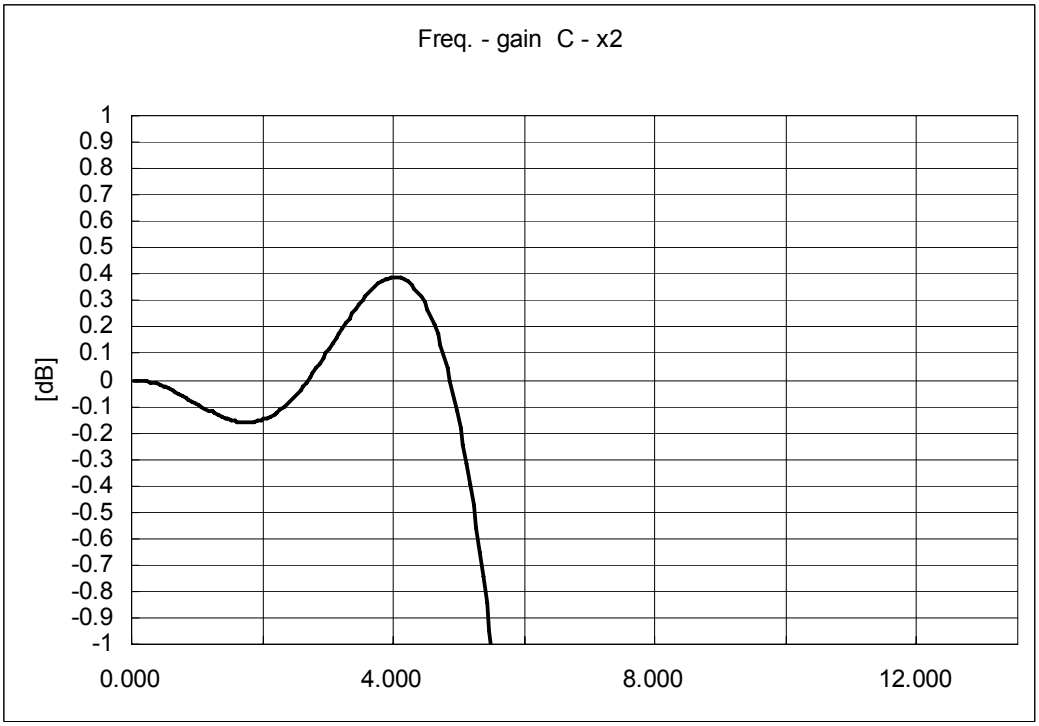




6. C x2 Filter (SD)

A 13.5 MHz rate CbCr signal is balance-modulated by the Color Sub-Carrier and the C signal is generated.





7. Video Input / Output Outline

The AK8823 equips 8Bit SD Input Port (SD Port) at SD Block, and 16Bit HD Input Port (HD Port) at HD Block.
Signal Capture Synchronization is selectable from 2 modes by register setting – one is to decode EAV code which is encoded on Input signal, or the other is to synchronize with HSYNC_SD / VSYNC_SD or HSYNC_HD / VSYNC_HD signals.

SD Block operation sets NTSC / PAL mode, and with HD Video input, input signal types (SD / (525i / 625i) / (525p / 625p) / 1080i / 720p) and Frame Rates (50 Hz / 60 Hz) are set. Signals on SD Port can be transferred to HD Block by proper setting, and vice versa (HD Port signal to SD Block is also possible). But it is only true with D1 signal on HD Input Port
(Note) When video data on HD port is transferred to SD block, the same clock in CLK_HD pin must be fed to CLK_SD pin.

(1) Input pin

Input Format	Bit	Input Pins
SD Port (ITU-R.BT 656)	8	ITU7-ITU0
HD Port	16	Y7-Y0
		CBCR7- CBCR0

(2) Input Rate

Video Mode	Format	CLK	Notes
SD Port			
NTSC/PAL	4:2:2	27MHz	
HD Port			
525i/625i	Y/CBCR 4:2:2	27MHz	
1080i/720p	Y 4 CBCR 2:2	74.25MHz 74.25MHz	

The AK8823 can output SD Video and HD Video signals simultaneously.

Input	SD block		
	DAC2	DAC3	DAC_CLOCK
SD Port	SDY	SDC	27MHz
HD Port	SDY	SDC	27MHz

HD block				
Input	Output			DAC_CLOCK
	DAC 4	DAC 5	DAC 6	
SD Port	HDY	HDPB	HDPR	54MHz (CLK_SD x2)
HD Port 525i/625i	HDY	HDPB	HDPR	54MHz (CLK_HD x2)
HD Port 525p/625p	HDY	HDPB	HDPR	54MHz (CLK_HD x2)
HD Port (1080i/720p)	HDY	HDPB	HDPR	148.5MHz (CLK_HD x2)

The AK8823 has on-chip PLL.
Description with parenthesis (x 2 etc.), following frequency value in DAC_CLOCK column shows an integer- multiple number (multiplier) and the selected input clock source.

8. PLL function

The AK8823 has on-chip PLL for clock multiplier.
When HD block is enabled, frequency-multiplied operation as described above is executed while 27 MHz is used in SD block as its input clock.

9. Video DAC

The AK8823 has 10-bit resolution, discrete 2 channel Current Drive DACs which run at 27MHz, and discrete 3 channel DACs which run at 150MHz.
These DACs are designed to output 1.28V o-p Full Scale with load resistors of 150ohm (+/-1 %) on HDY Output DAC and 300ohm (+/-1 %) on all other DACs when a 3.9kohm (+/-1 %) resistor is connected between IREF pin and ground.

10. Operation Mode [HD Control]

Mode No	SD block	HD block						I2C register settings					
	Mode & output clock	CLK_HD MHz	In Port	Video processing	VBID processing	output clock [MHz]	Macrovision	0x11 bit[3:2] VM	0x00 bit[0] RFRSH	0x00 bit[2:1] MODE1,0	0x06 bit[1;0] BLKCNT	0x07 bit[] VRATIO	0x05 bit[5] VRPT
Refresh rate 60Hz													
1	NTSC or PAL60 27MHz	(CLK_SD)	SD	YpbPr (525i)(*)	CGMA-A/CC	54	7.1.1L	[0:0]or[0:1]	0	[0:0]	[0:0]	1	1
2		(CLK_SD)	SD	YpbPr (525i)	CGMA-A/CC		7.1.1L				[0:0]	0	1
3		27	HD	YpbPr (525i)(*)	CGMA-A/CC		7.1.1L				[0:0]	1	0
4		27	HD	YpbPr (525i)	CGMA-A/CC		7.1.1L				[0:0]	0	0
5		27	HD	YpbPr (525p)	CGMA-A		1.2			[0:1]	[0:0]	0	0
6		74.25(74.175)	HD	YpbPr (1080i)	CGMA-A	148.5	-			[1:0]	[0:0]	0	0
7		74.25(74.175)	HD	YpbPr (720p)	CGMA-A		-			[1:1]	[0:0]	0	0
8	Power Down	(CLK_SD)	SD	YpbPr (525i)(*)	CGMA-A/CC	54	7.1.1L	*	0	[0:0]	[0:1]	1	1
9		(CLK_SD)	SD	YpbPr (525i)	CGMA-A/CC		7.1.1L				[0:1]	0	1
10		27	HD	YpbPr (525i)(*)	CGMA-A/CC		7.1.1L				[0:1]	1	0
11		27	HD	YpbPr (525i)	CGMA-A/CC		7.1.1L				[0:1]	0	0
12		27	HD	YpbPr (525p)	CGMA-A		1.2			[0:1]	[0:1]	0	0
13		74.25(74.175)	HD	YpbPr (1080i)	CGMA-A	148.5	-			[1:0]	[0:1]	0	0
14		74.25(74.175)	HD	YpbPr (720p)	CGMA-A		-			[1:1]	[0:1]	0	0
15	27MHz	Power Down						[0:0]or[0:1]	*	*	[1:0]	*	*
Refresh rate 50Hz													
16	PAL	(CLK_SD)	SD	YpbPr (625i)	WSS/CC	54	7.1.1L	[1:1]	1	[0:0]	[0:0]	0	1
17		27	HD	YpbPr (625i)	WSS/CC		7.1.1L				[0:0]	0	0
18		27	HD	YpbPr (576p)	-		1.2			[0:1]	[0:0]	0	0
19		74.25(74.175)	HD	YpbPr (1080i)	-	148.5	-			[1:0]	[0:0]	0	0
20		74.25(74.175)	HD	YpbPr (720p)	-		-			[1:1]	[0:0]	0	0
21	Power Down	(CLK_SD)	SD	YpbPr (625i)	WSS/CC	148.5	7.1.1L		1	[0:0]	[0:1]	0	1
22		27	HD	YpbPr (625i)	WSS/CC		7.1.1L				[0:1]	0	0
23		27	HD	YpbPr (576p)	-		1.2			[0:1]	[0:1]	0	0
24		74.25(74.175)	HD	YpbPr (1080i)	-	148.5	-			[1:0]	[0:1]	0	0
25		74.25(74.175)	HD	YpbPr (720p)	-		-			[1:1]	[0:1]	0	0
26	27MHz	Power Down						[1:1]	*	*	[1:0]	*	*

(*) mark in the table
In D1 (60 Hz) mode, 286 / 714 amplitude ratio (EIA 770. 1-A Output compatible)

* Do not care bit

11. Operation Mode [SD Control]

Mode No	HD block	SD block				I2C register settings				
	Mode & output clock	CLK_SD MHz	In Port	VBID processing	output clock [MHz]	0x00 bit[2:1] MODE1,0	0x00 bit[0] RFRSH	0x06 bit[1;0] BLKCNT	0x11 bit[3:2] VM3:2	0x14 bit[7] VPRTSD
Refresh rate 60Hz										
1	D1 54MHz	(CLK_HD 27MHz)	HD	VBID/CC	27	[0:0]	0	[0:0]	[0:0]or[0:1]	1
2		27	SD							0
3	D2 54MHz D3 148MHz D4 148MHz	27	SD			[0 :1] [1:0] [1:1]				
4	Power Down	(CLK_HD 27MHz)	HD			*		[1:0]		1
5		27	SD							0
6		Power Down					*	[11]	*	*
Refresh rate 50Hz										
7	D1 54MHz	(CLK_SD) 27MHz	SD	VBID/CC/WSS	27	[0:0]	1	[0:0]	[1:1]	1
8		27	HD							
9	D2 54MHz D3 148MHz D4 148MHz	27	SD			[0 :1] [1:0] [1:1]				
10	Power Down	(CLK_HD 27MHz)	HD			*		[1:0]		1
11		27	SD							0
12		Power Down					*	[11]	*	*

12. Power-Down

PD_N L: Power-Down H : normal operation
PLL clock generator and registers are initialized (into default value setting) at power-down.

Hi-Z input compatible pins are as follows during this power-down.
When device output pins those are connected to the AK8823 input pins become Hi-Z conditions such as a case at the power-on etc., the AK8823 should be powered-up in power-down condition.
This pin controls to power-down all the blocks and puts the device into the minimum power mode (Refer to item 14.Power –up Sequence).

[Hi-Z Compatible Input pins]
ITU7 ~ ITU0, Y7 ~ Y0, CBCR7 ~ CBCR0
HSYNC_SD, VSYNC_SD, HSYNC_HD, VSYNC_HD
INIT_N, CLK_SD, CLK_HD
SCL, SELA

In order to put the device into the minimum power mode in normal operation (PD_N " H "), input clocks (CLK_SD, CLK_HD) should be stopped (either " L " or " H ") in addition to the following register settings.

Register Setting to put into minimum power mode
Address 0x05 bit 2 ~ 0 [000]
Address 0x06 bit 2 [0], bit 1 ~ 0 [11]
Address 0x15 bit 1 ~ 0 [00]

13. Initialization

INIT_N " L " initialization
Video Process Digital Filter is initialized.
PLL Clock Generator and I2C register are not initialized by INIT_N.
Video Process Digital Filter can be also initialized by register (HD_SINIT_N, SD_SINIT_N), instead of INIT_N pin control.
Set INIT_N pin to " H (IVDD) " when it is not used.
PLL can be also reset by register PLL_SPD_N.

[Initialization Registers]
HD_SINIT_N Address 0x05 bit 7
PLL_SPD_N Address 0x06 bit 2
SD_SINIT_N Address 0x15 bit 4

14. Power-up Sequence

Control of Power Supply power-up and power-down

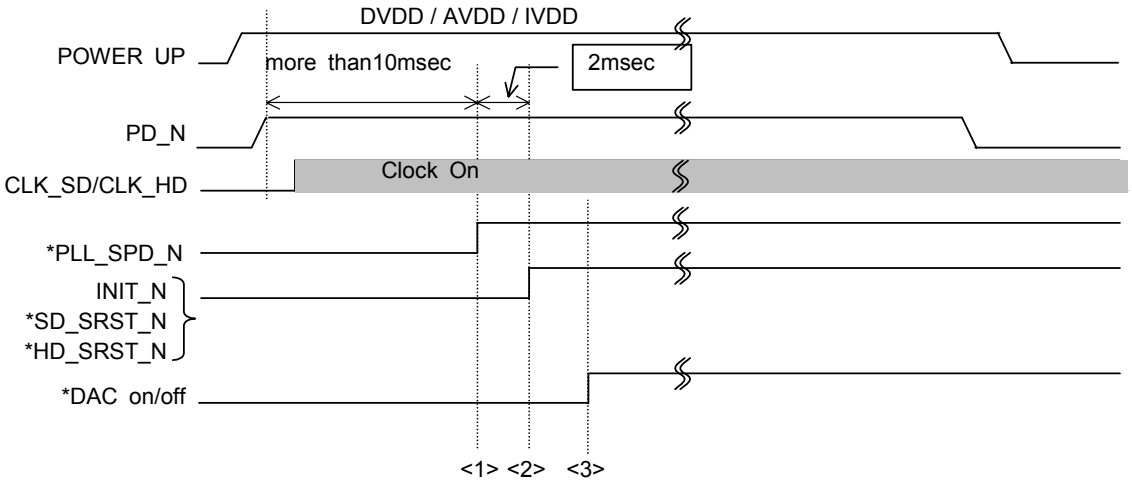
When the power supplies become stable, release PD_N pin and wait for 10 msec.
Set mode of HD / SD Blocks, then enable PLL operation first and turn on DACs.
By releasing PD_N after the power-on, rise time variations of power supplies (DVDD / AVDD / IVDD) are tolerated.
Wait for longer than 10 msec after PD_N is released, then enable PLL.
When to power-down, power supplies should be turned off after PD_N is activated.

When to power-up

Following timing sequence should be made after 10 msec time from the release of power-down and after input clock becomes stable.
A longer than 2 msec transition time is required from sequence <2> to sequence <3> below.

<1> Mode setting → start of PLL operation (PLL_SPD_N : 1)
<2> initialization of internal filter (INIT_N pin " L " or SD_SRST_N / HD_SRST_N : 0) release (note 1) operation which is described below.
<3> turn on DAC

(note 1)
INIT_N pin is used to initialize internal digital filter. Clock input is required.
Initialization at " L " and normal operating condition at " H ".
Instead of controlling this pin, same initialization function is executed by manipulating registers SD_SRST_N, HD_SRST_N.
When to manipulate registers, set INIT_N pin to " H ".

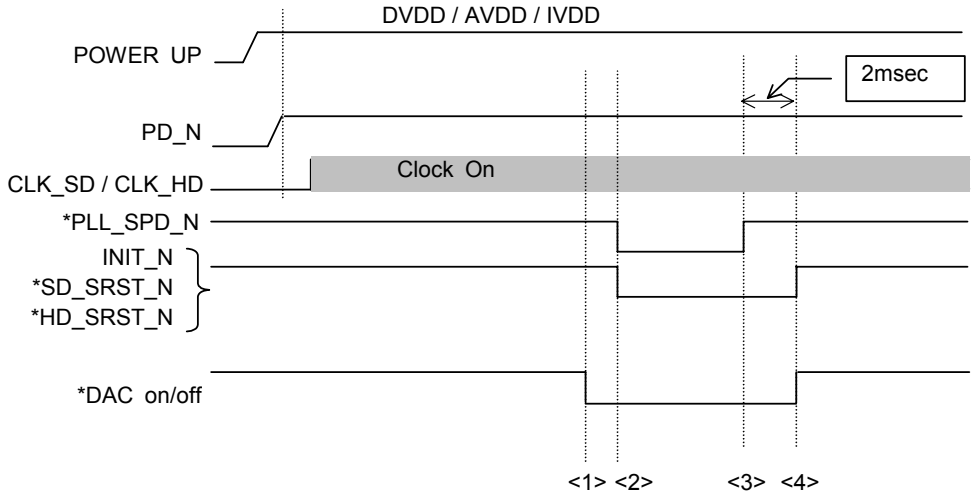


When to change mode by register setting

When a mode change is made, involving(accompanied with) PLL oscillator frequency change, following timing sequence should be met.
A longer than 2 msec transition time is required from sequence <3> to sequence <4> below.

<1> DAC off
<2> PLL operation off (PLL_SPD_N : 0) → initialization of internal filter (INIT_N pin " L " or SD_SRST_N / HD_SRST_N : 0) → mode change setting (D1 to D3 change, CLK_HD frequency is also changed during this period)
<3> start PLL operation (PLL_SPD_N : 1)
<4> release of internal filter initialization (INIT_N pin " H " or SD_SRST_N / HD_SRST_N : 1) → DAC on

When a Video Mute Circuit etc is externally equipped and used, DAC manipulation of sequences <1> and <4> above can be eliminated.
It is also true that its manipulation can be eliminated when the internal filter initialization register is always used in operating condition " 1 ".



Register setting via I2C interface (all other register change)

Access to the AK8823 registers is possible even when CLK_SD or CLK_HD clocks are not fed.
The AK8823 register manipulation can be made anytime, but care must be taken when the power is up or when the internal PLL oscillating frequency is changed or when the input clock is changed.
In Macrovision setting mode and VBID setting mode where changes of PLL oscillating frequency are not involved, target registers can be directly accessed.

15. HD Block

15-1. Video Interface Timing (HD)

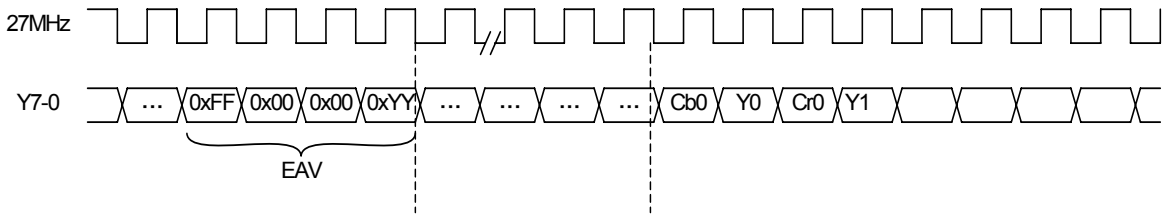
The AK8823 has 2 types of Video Interfaces, EAV Decode mode and Slave SYNC mode.

EAV SYNC mode
(HD) [Mode Register] (Sub Address 0x00) set by EAVDEC (bit 4)

Slave SYNC mode
The AK8823 can also synchronize with externally-fed HSYNC signal and VSYNC signal as Slave SYNC mode operation.
HSYNC becomes Pixel Counter Reference Point within a Line and VSYNC becomes Line Counter Reference Point within a Frame.
Polarities of HSYNC_HD, VSYNC_HD are pre-settable.
When an interlaced signal is input, the First and the Second Fields are recognized from HSYNC and VSYNC relation.

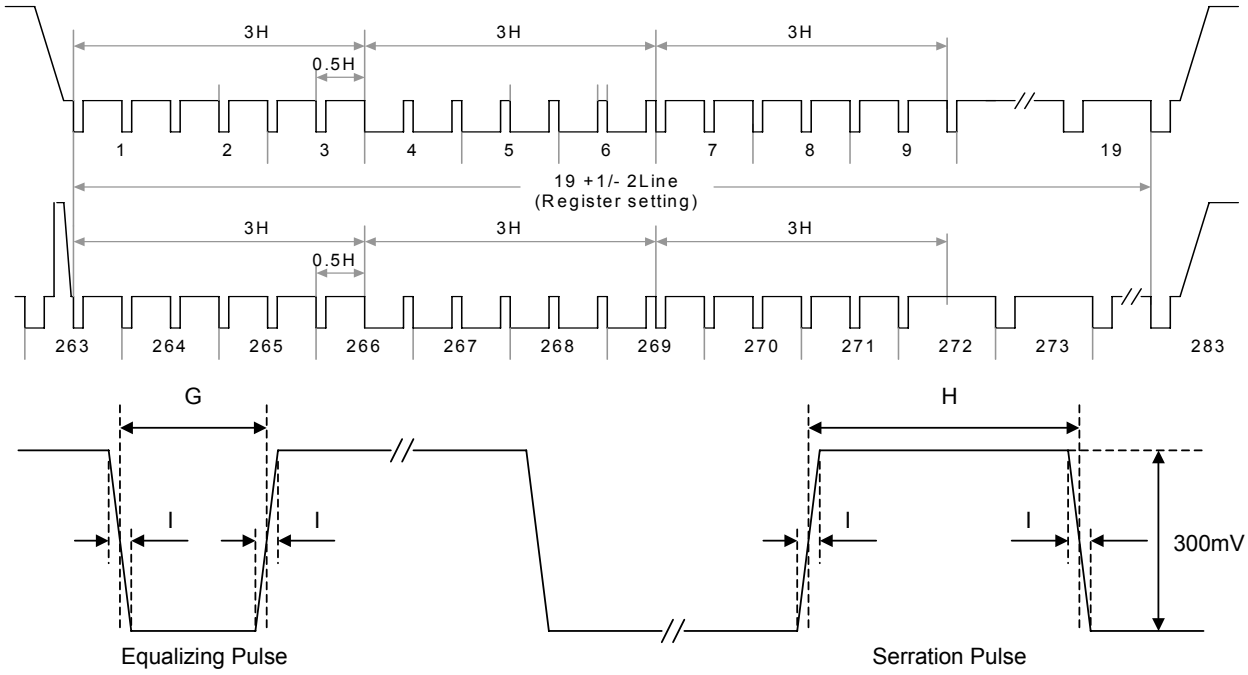
In this mode, the AK8823 also complies with EIA / CEA 861B compatible timing.
(HD) [Mode Register] (Sub Address 0x00) CEA 861B (bit 3)

(1) 525i (480i) / 60Hz (HD)
(1-1) Data Capture
(1-1-2) EAV Decode (Capture) : 525i (480i) / 60 Hz (HD)



(1-2) Analog Output : 525i (480i) / 60 Hz (HD)

(1-2-1) Frame Configuration : Vertical SYNC Signal Waveform Timing

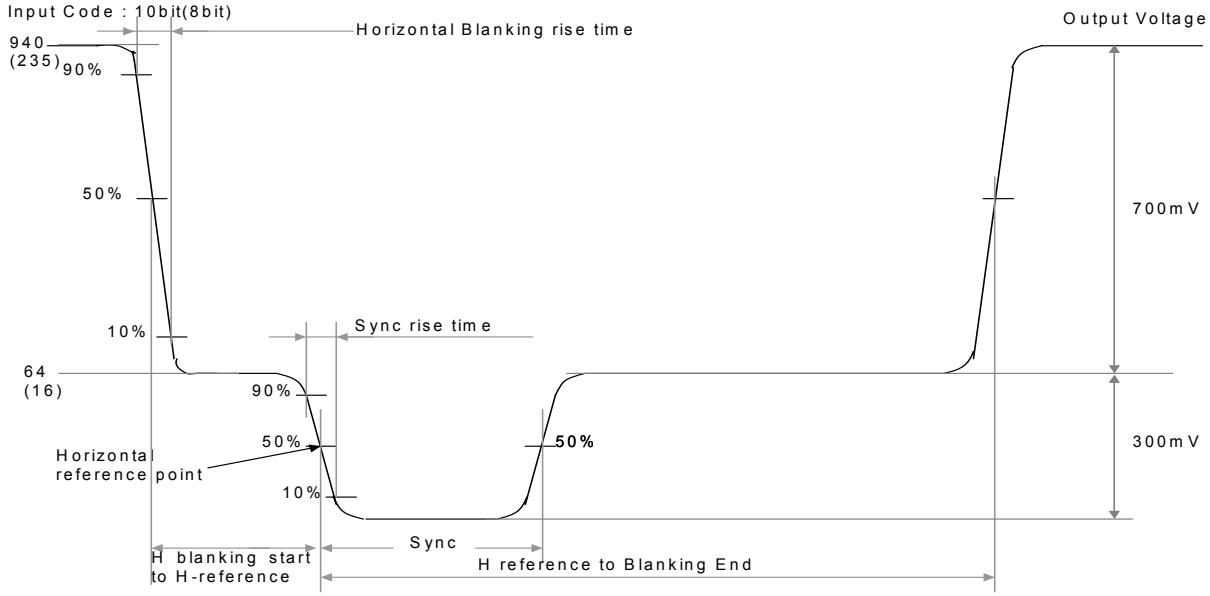


Equalizing Pulse and Serration Pulse

Symbol		Measurement point	Value	Recommended tolerance	units
	Field Period (derived)		16.6833		msec
	Frame period (derived)		33.3667		msec
	Vertical blanking start before first equalizing pulse	50%	1.5	+/- 0.1	usec
	Vertical blanking (63.556usec x 20lines + 1.5usec)		19* lines + 1.5 usec	0 +/- 0.1	lines usec
	Pre-equalizing duration		3		lines
G	Pre-equalizing pulse width	50%	2.3	+/- 0.1	usec
	Vertical sync duration		3		lines
H	Vertical serration pulse width	50%	4.7	+/- 0.1	usec
	Post-equalizing duration		3		lines
G	Post-equalizing pulse width	50%	2.3	+/- 0.1	usec
I	Sync rise time		140	+/- 20	nsec

* there is a case of V-Blank of 20 lines. This value is pre-settable by register.

(1-2-2) Waveform Levels (codes) : SYNC Signal Waveform : 525i (480i) / 60 Hz (HD)
SYNC signal is super-imposed on Luminance signal (Y).
Horizontal SYNC Signal Waveform Timing

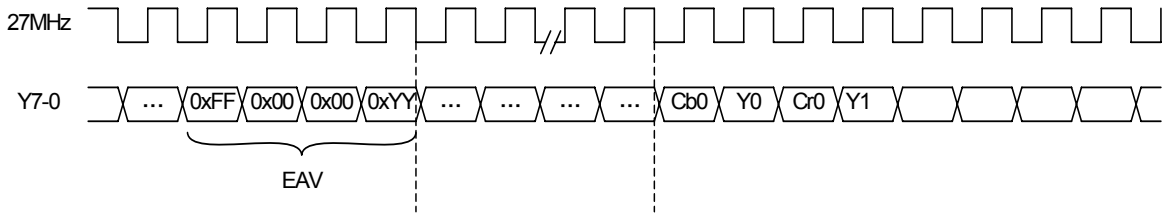


	measurement point	value	Recommended tolerance	units
Total line period(derived)		63.556		usec
Horizontal Blanking rise time	10% - 90%	140	+/- 20	nsec
Sync rise time	10% - 90%	140	+/- 20	nsec
H-Blanking start to H-reference	50%	1.5	+/- 0.1	usec
Horizontal Sync	50%	4.7	+/- 0.1	usec
H reference to H-blanking end	50%	9.2	+ 0.2 / - 0.1	usec

(2) 625i(576i) / 50Hz HD

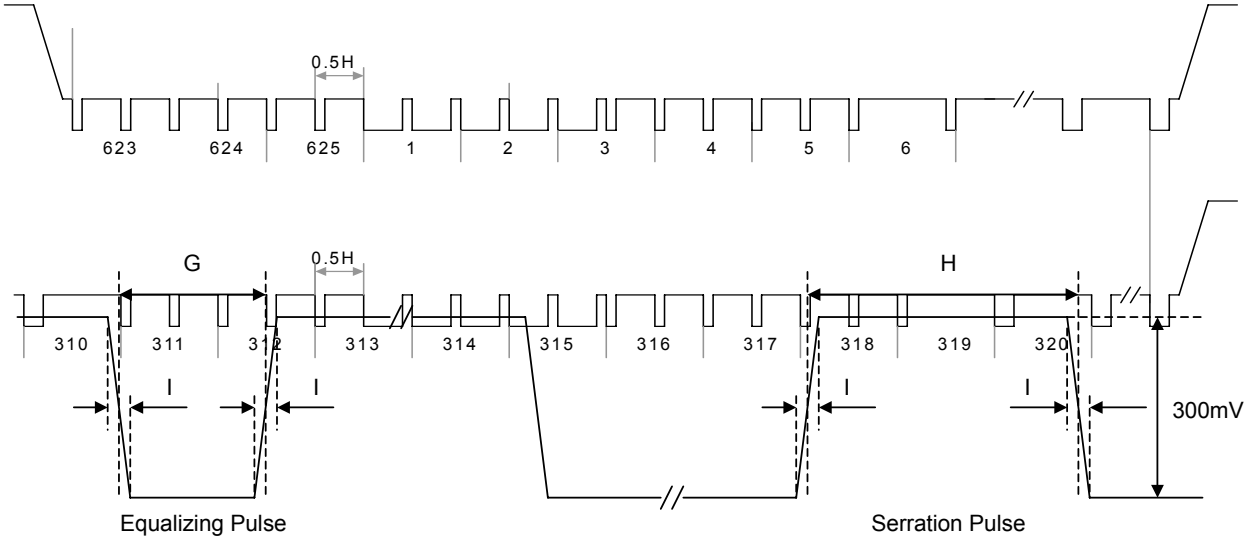
(2-1) Data Capture

(2-1-1) EAV Decode (Capture) : 625i (576i) / 50 Hz HD



(2-2) Analog Output : 625i (576i) / 50 Hz HD

(2-2-1) Frame Configuration : Vertical SYNC Signal Waveform Timing

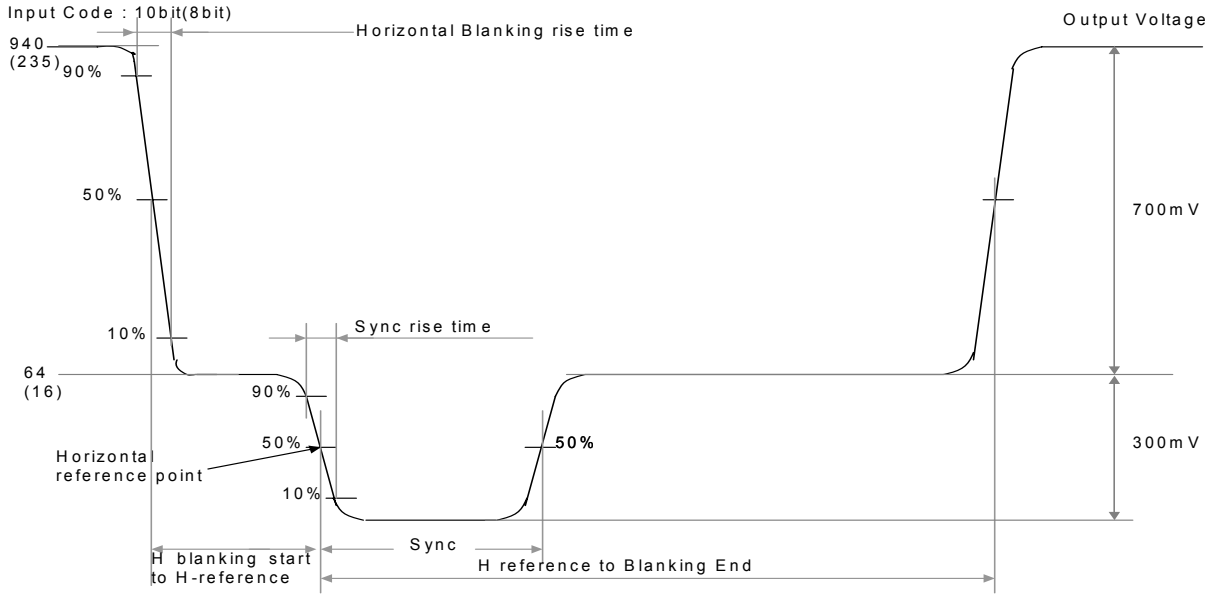


Equalizing Pulse and Serration Pulse

Symbol		Measurement point	Value	Recommended tolerance	units
G	Pre-equalizing pulse width	50%	2.35	+/- 0.1	usec
H	Vertical serration pulse width	50%	4.7	+/- 0.2	usec
G	Post-equalizing pulse width	50%	2.35	+/- 0.1	usec
I	Sync rise time		200	MAX300	nsec

* there is case where tolerance of Sync rise time is added to Pulse width tolerance.

(2-2-2) Waveform Levels (Codes) :
SYNC Signal Waveform : 625i (576i) / 50 Hz HD
SYNC signal is super-imposed on Luminance signal (Y).

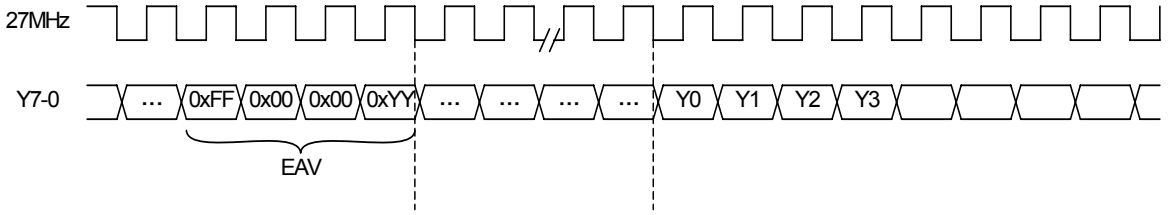


	measurement point	value	Recommended tolerance	units
Total line period(derived)		64.0		usec
Horizontal Blanking rise time	10% - 90%	0.3	+/- 0.1	usec
Sync rise time	10% - 90%	0.2	+/- 0.1	usec
H-Blanking start to H-reference	50%	1.5	+/- 0.3	usec
Horizontal Sync	50%	4.7	+/- 0.2	usec
H reference to H-blanking end	50%	10.5		usec

(3) 525p(480p) / 60Hz : HD

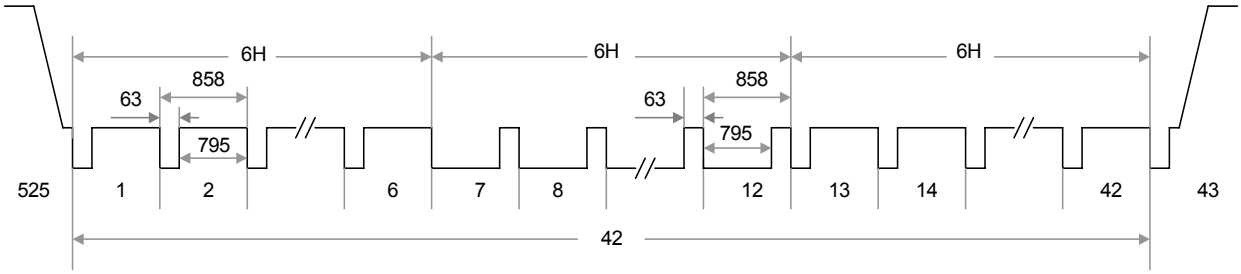
(3-1) Data Capture

(3-1-1) EAV Decode (Capture) 525p (480p) / 60 Hz HD



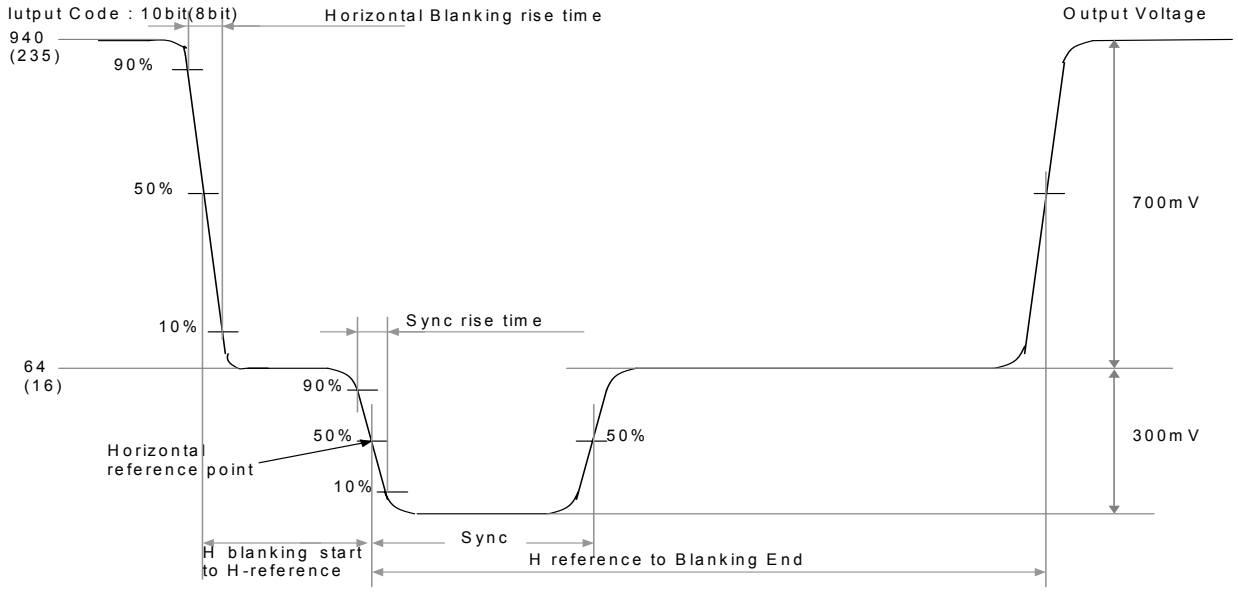
(3-2) Analog Output : 525p (480p) / 60 Hz HD

(3-2-1) Frame Configuration : Vertical SYNC Signal Waveform Timing



(3-2-2) Waveform Levels (Codes) : SYNC Signal Waveform : 525p (480p) / 60 Hz HD
SYNC signal is super-imposed on Luminance signal (Y).

Horizontal SYNC Signal Waveform Timing

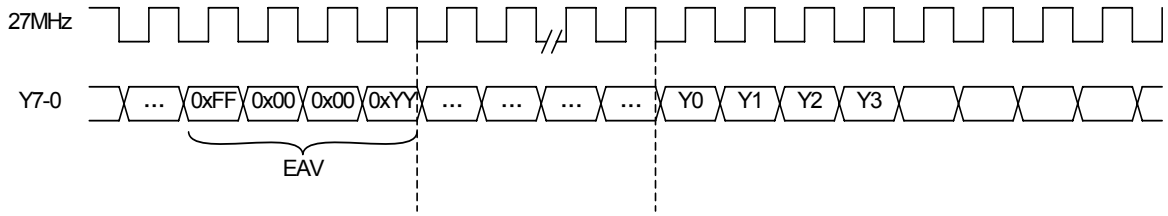


	measurement point	value	Recommended tolerance	units
Total line period(derived)		31.776		usec
Horizontal Blanking rise time	10% - 90%	70	+/- 10	nsec
Sync rise time	10% - 90%	70	+/- 10	nsec
H-Blanking start to H-reference	50%	0.59	+/- 0.05	usec
Horizontal Sync	50%	2.33	+/- 0.05	usec
H reference to H-blanking end	50%	4.52	+ 0.1 / - 0.05	usec

(4) 625p(576p) / 50Hz : HD

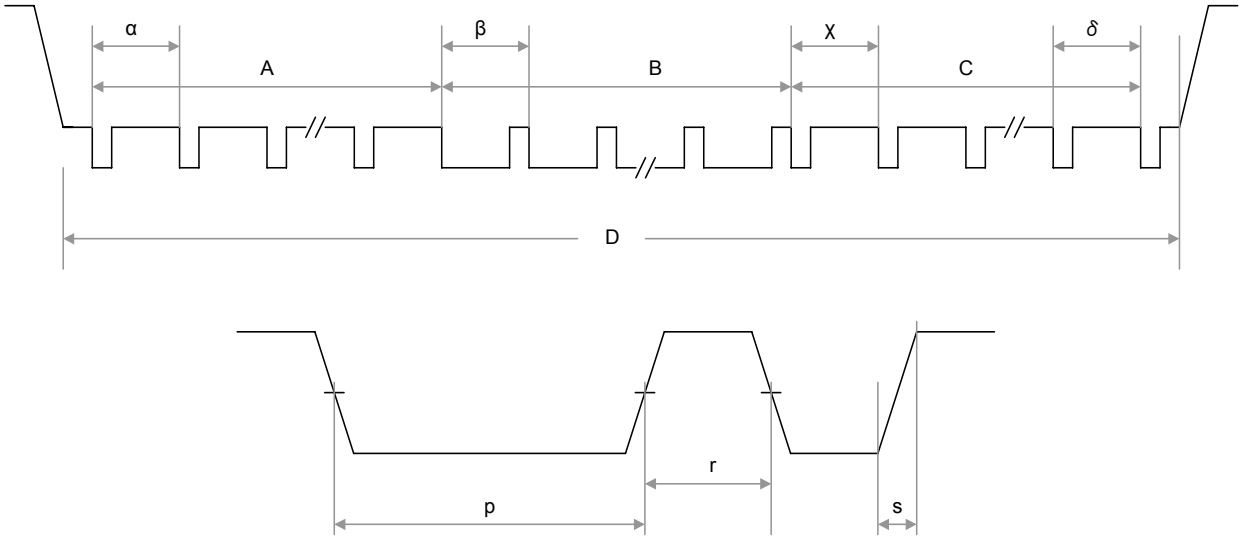
(4-1) Data Capture

(4-1-1) EAV Decode (Capture) : 625p (576p) / 50 Hz HD



(4-2) Analog Output : 625p (576p) / 50 Hz HD

(4-2-1) Frame Configuration : Vertical SYNC Signal Waveform Timing

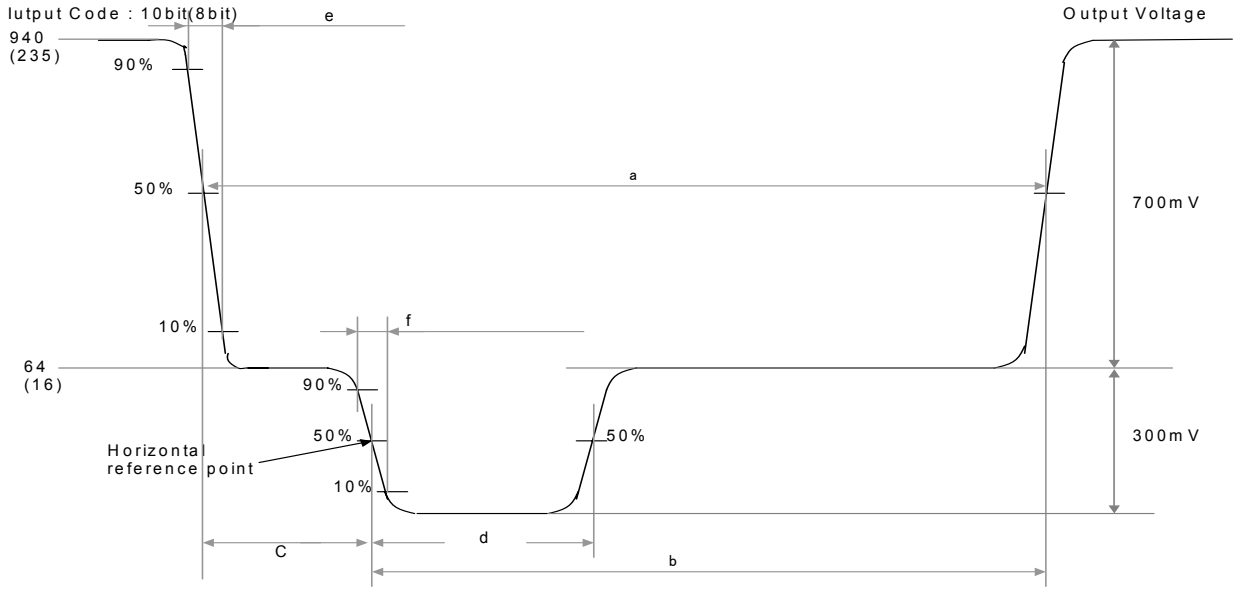


Symbol	Characteristics	625/50/1:1
V	Nominal frame period (ms)	20
D	Vertical blanking interval	49H+ α *
-	Build-up time (10 to 90%) of the edges of vertical blanking pulse (us)	0.15±0.05
A	Interval between front edges of vertical blanking interval and front edges of first vertical synchronizing pulse	5H*
C	Interval between back edges of last vertical synchronizing pulse and back edge of vertical blanking interval	39H*
B	Duration of sequence of vertical synchronizing pulses	5H*
p	Duration of vertical synchronizing pulse (us)	29.65±0.1
r	Interval between vertical synchronizing pulse(us)	2.35±0.1
s	Build-up time (10 to 90%) og the vertical synchronizing pulses (us)	0.1±0.05

* For H and a, see Table 1 (**ITU-R BT.1358**)

(4-2-2) Waveform Levels (Codes) : SYNC Signal Waveform (BT. 1368) : 625p (576p) / 50 Hz HD SYNC signal is super-imposed on Luminance signal (Y).

Horizontal SYNC Signal Waveform Timing

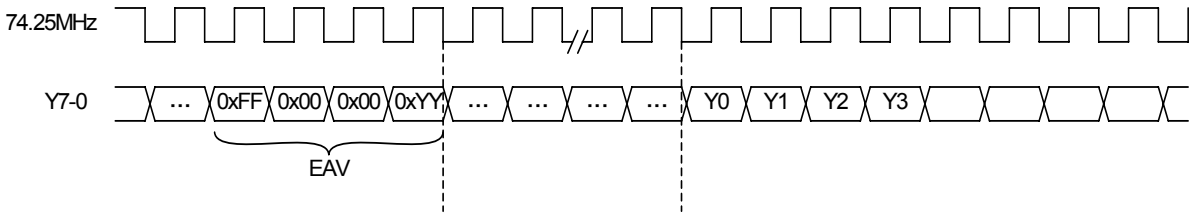


Symbol	Characteristics	625/50/1:1
H	Nominal line period (us)	32
a	Horizontal blanking interval(us)	6.0±1.5
b	Interval between time datum (0H) and back edge of horizontal blanking pulse (us)	5.25
c	Front porch (us)	0.75±0.15
d	Synchronizing pulse (us)	2.35±0.1
e	Build-up time (10 to 90%) of the edges of the horizontal blanking pulse (us)	0.15±0.05
f	Build-up time (10 to 90%) of the edges of the horizontal synchronizing pulses (us)	0.1±0.05

(5) 1080i / 60Hz : HD

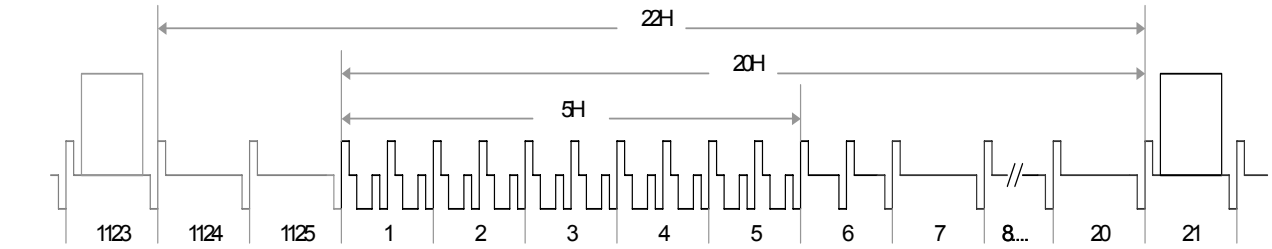
(5-1) Data Capture

(5-1-1) EAV Decode (Capture) : 1080i / 60 Hz HD

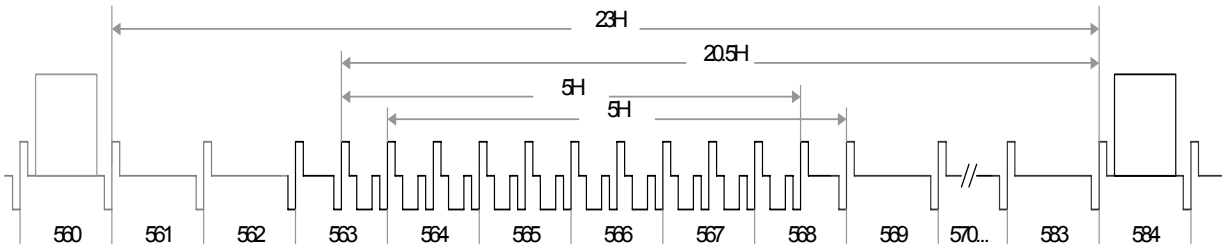


(5-2) Analog Output : 1080i / 60 Hz HD

(5-2-1) Frame Configuration : Vertical SYNC Timing

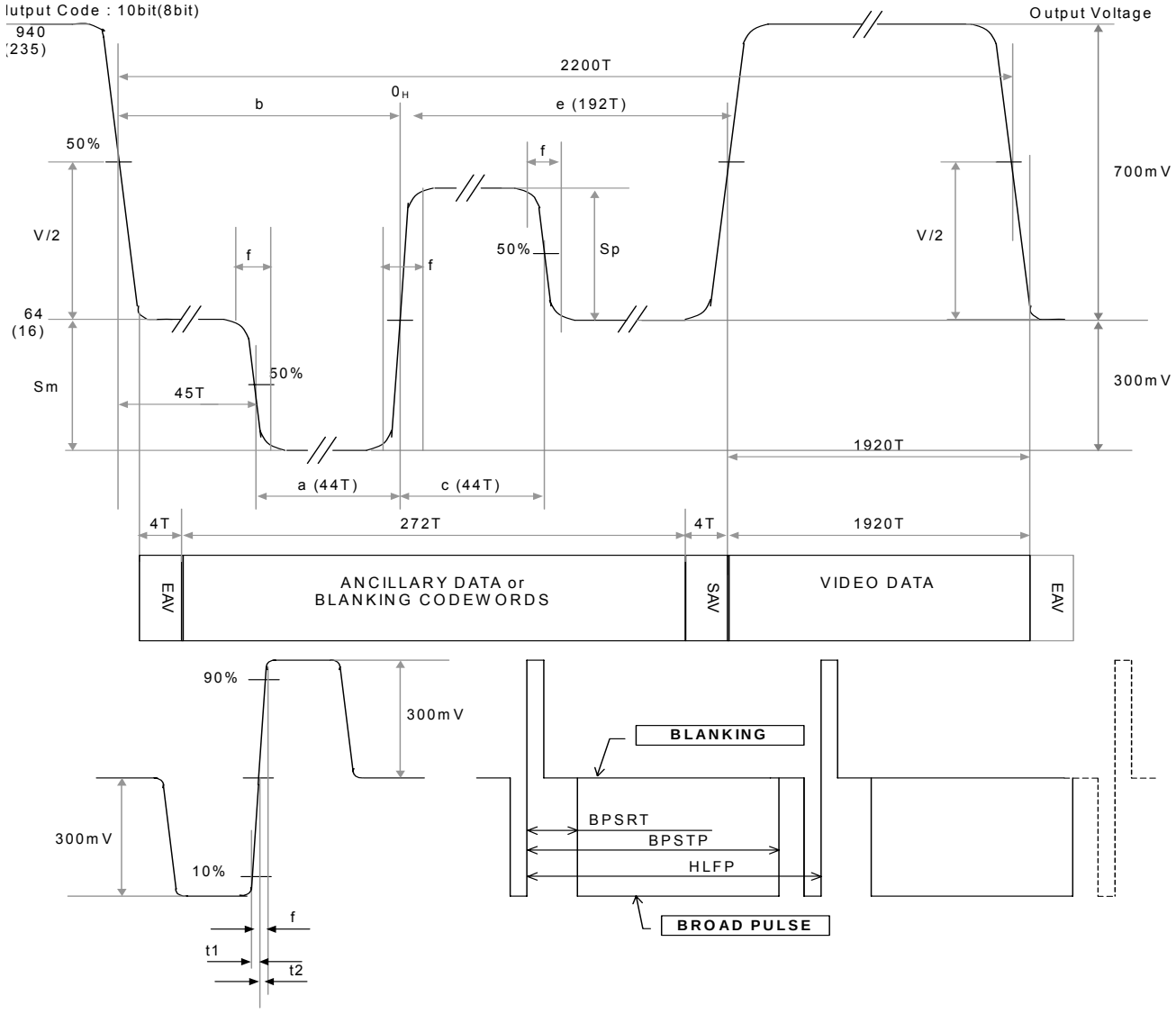


First Field



Second Field

(5-2-2) Waveform Levels (Codes) : SYNC Signal Waveform Timing : 1080i / 60 Hz HD
SYNC signal is super-imposed on Luminance signal (Y).

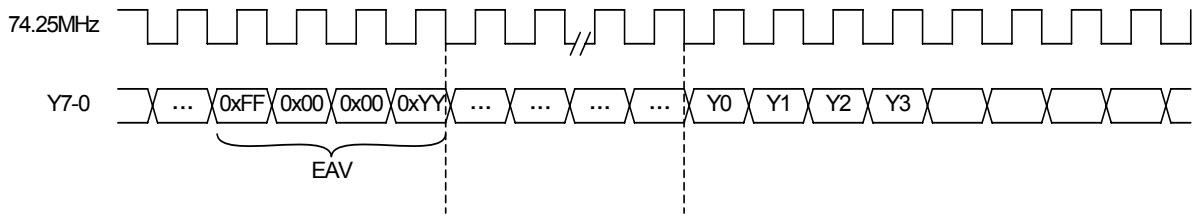


Symbol	Characteristics	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
b	End of active video	*1.120* [usec]	*89*		+0.080 [usec]
c	positive line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
e	Start of active video	2.589 [usec]	192	-0 / + 6	+0.080 [usec]
f	Rise/fall time	0.054 [usec]	4	+/- 1.5	+/- 0.020 [usec]
t2 - t1	Symmetry of rising edge	-	-		+/- 0.002 [usec]
Sm	Amplitude of negative pulse	300 [mV]	-		+/- 6mV
Sp	Amplitude of positive pulse	300 [mV]	-		+/- 6mV
V	Amplitude of video signal	700 [mV]	-		
-	Field-blanking interval	45 [H/field]	99000		
	H Total		2200		
	H Active		1920		
BPSRT	Broad pulse start pos		132		-3 ~ +3
BPSTP	Broad pulse stop pos		1012		-3 ~ +3
HLFP	H/2 pos		1100		-3 ~ +3

(6) 1080i / 50Hz : HD

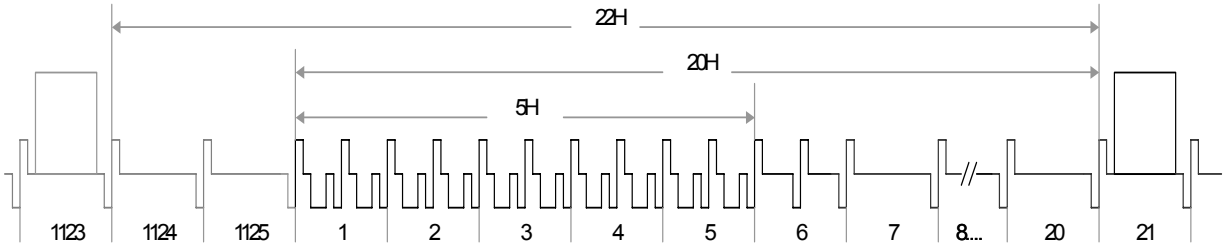
(6-1) Data Capture

(6-1-1) EAV Decode (Capture) : 1080i / 50 Hz HD

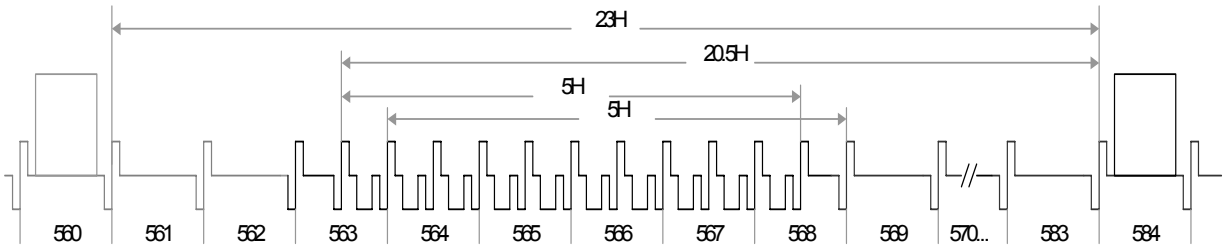


(6-2) Analog Output : 1080i / 50 Hz HD

(6-2-1) Frame Configuration : Vertical SYNC Timing

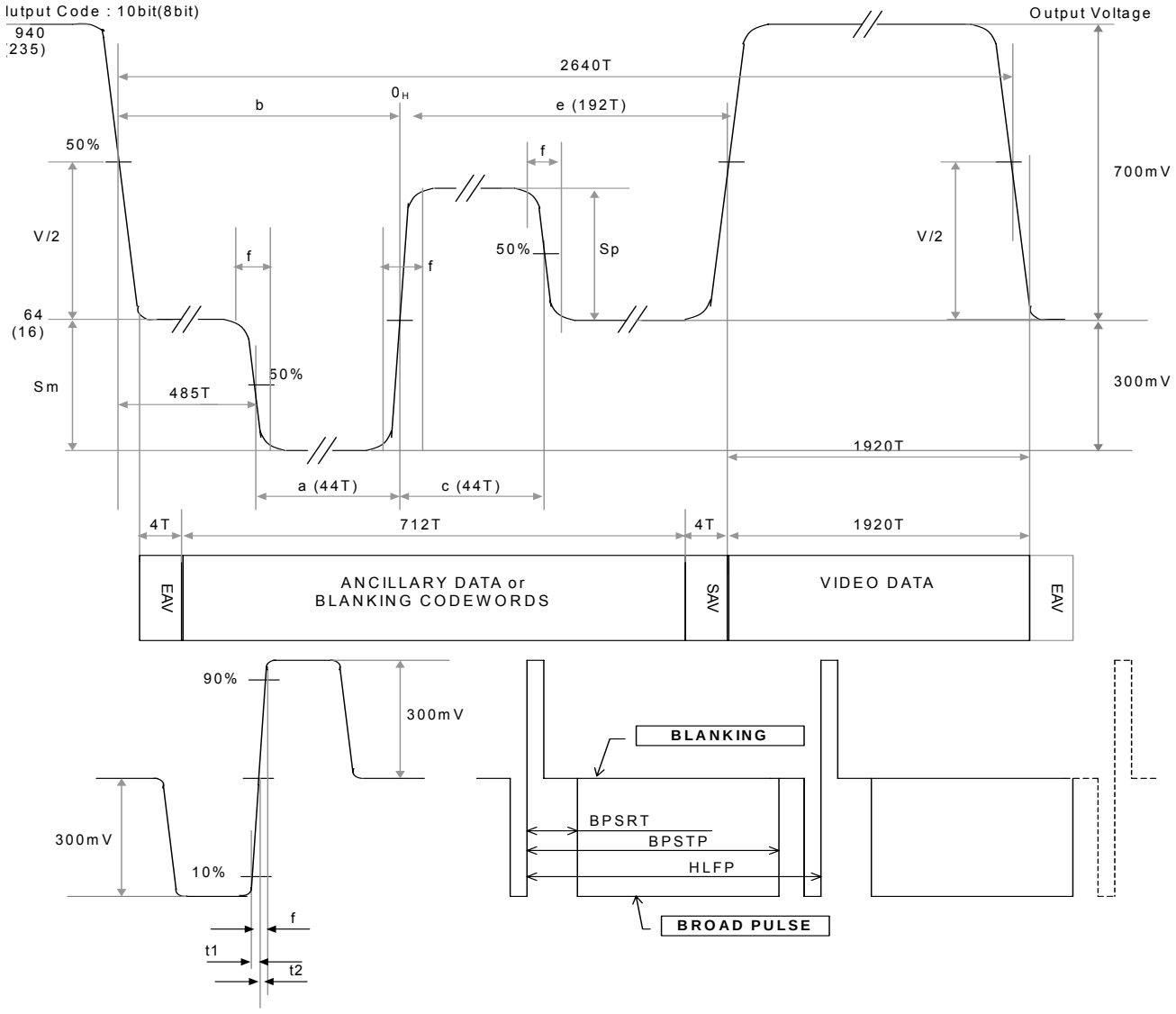


First Field



Second Field

(6-2-2) Waveform Levels (Codes) :SYNC Signal Waveform Timing : 1080i / 50 Hz HD
SYNC signal is super-imposed on Luminance signal (Y).

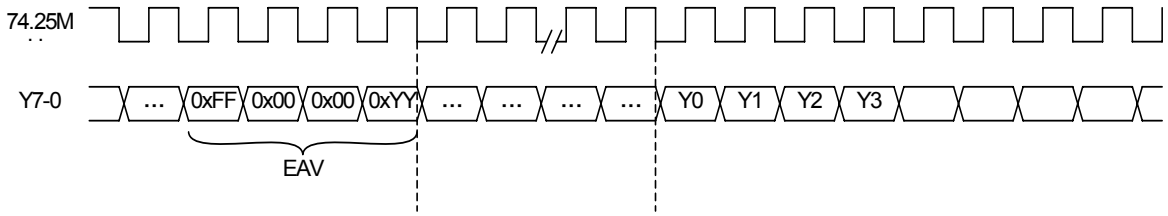


Symbol	Characteristics	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
b	End of active video	*1.120* [usec]	*529*		+0.080 [usec]
c	positive line sync width	0.593 [usec]	44	+/- 3	+/- 0.040 [usec]
e	Start of active video	2.589 [usec]	192	-0 / + 6	+0.080 [usec]
f	Rise/fall time	0.054 [usec]	4	+/- 1.5	+/- 0.020 [usec]
t2 - t1	Symmetry of rising edge	-	-		+/- 0.002 [usec]
Sm	Amplitude of negative pulse	300 [mV]	-		+/- 6mV
Sp	Amplitude of positive pulse	300 [mV]	-		+/- 6mV
V	Amplitude of video signal	700 [mV]	-		
-	Field-blanking interval	45 [H/field]	99000		
	H Total		2640		
	H Active		1920	-12, +0	
BPSRT	Broad pulse start pos		132		-3 ~ +3
BPSTP	Broad pulse stop pos		1012		-3 ~ +3
HLFP	H/2 pos		1320		-3 ~ +3

(7) 720p / 60Hz : HD

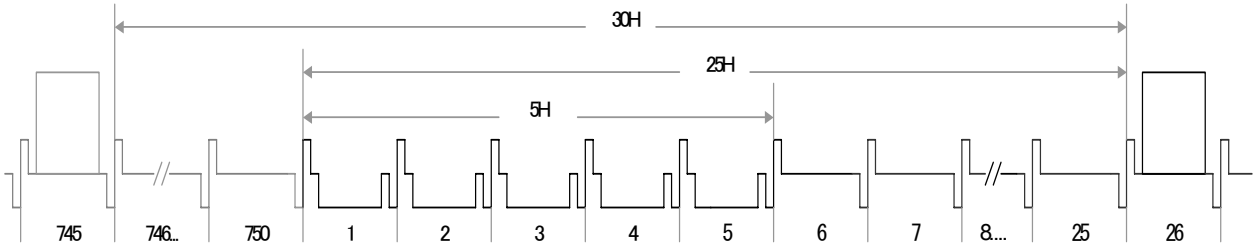
(7-1) Data Capture

(7-1-1) EAV Decode (Capture) : 750p (720p) / 60 Hz HD

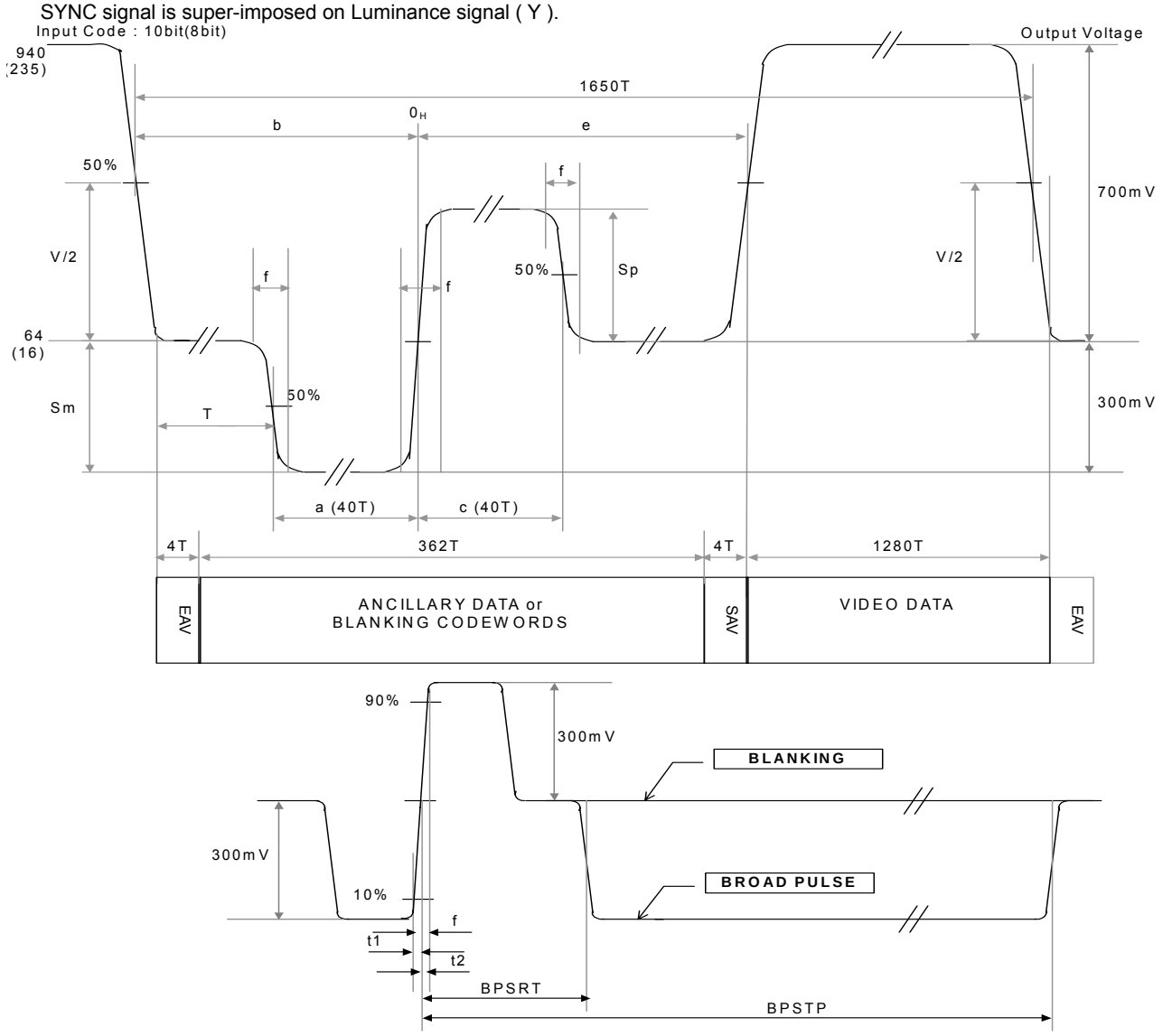


(7-2) Analog Output : 720p / 60 Hz HD

(7-2-1) Frame Configuration : Vertical SYNC Timing



(7-2-2) Waveform Levels (Codes) :SYNC Signal Waveform Timing : 720p / 60 Hz HD
SYNC signal is super-imposed on Luminance signal (Y).

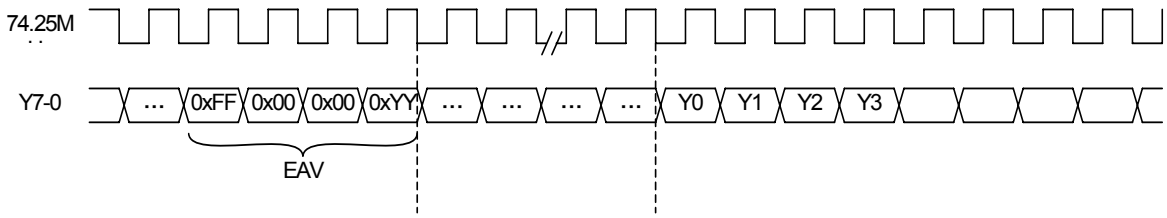


Symbol	Characteristics	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	[usec]	40		[usec]
b	End of active video	[usec]	*111*		[usec]
c	positive line sync width	[usec]	40		[usec]
e	Start of active video	[usec]	260		[usec]
f	Rise/fall time	[usec]	4		[usec]
t2 - t1	Symmetry of rising edge	-	-		[usec]
Sm	Amplitude of negative pulse	300 [mV]	-		+/- 6mV
Sp	Amplitude of positive pulse	300 [mV]	-		+/- 6mV
V	Amplitude of video signal	700 [mV]	-		
	H Total s		1650		
	H Active		1280		
BPSRT	Broad pulse start pos		260		0 ~ +6
BPSTP	Broad pulse stop pos		1540		-6 ~ 0

(8) 720p / 50Hz : HD

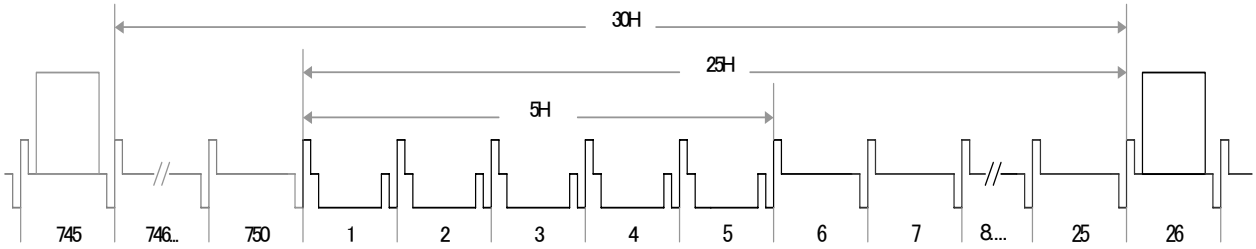
(8-1) Data Capture

(8-1-1) EAV Decode (Capture) : 720p / 50 Hz HD

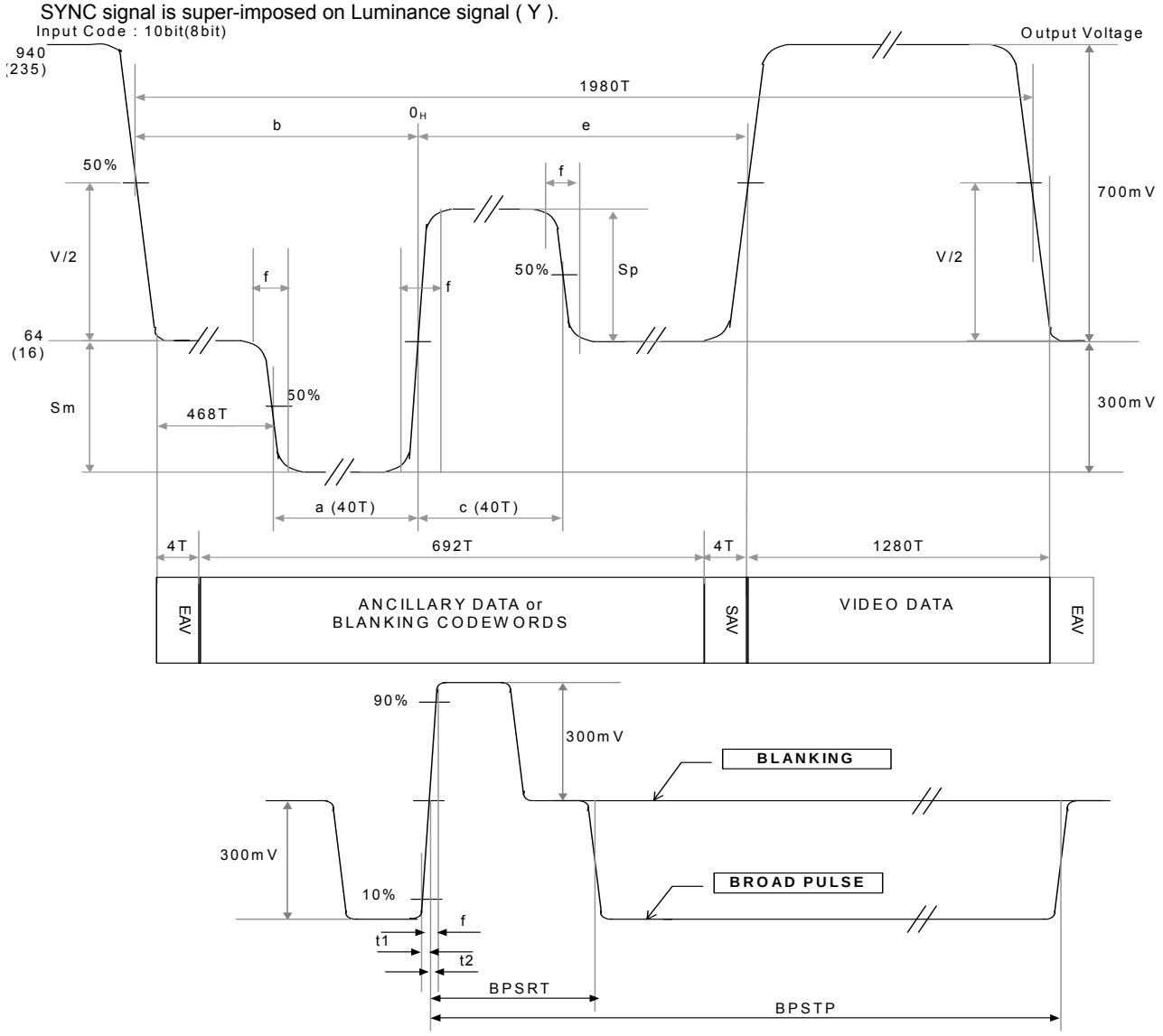


(8-2) Analog Output : 720p / 50 Hz HD

(8-2-1) Frame Configuration : Vertical SYNC Timing



(8-2-2) Waveform Levels (Codes) : SYNC Signal Waveform Timing : 720p / 50 Hz HD
SYNC signal is super-imposed on Luminance signal (Y).



Symbol	Characteristics	Nominal value	Reference clock Interval	Tolerance CLK	Tolerance
a	Negative line sync width	[usec]	40		[usec]
b	End of active video	[usec]			[usec]
c	positive line sync width	[usec]	40		[usec]
e	Start of active video	[usec]			[usec]
f	Rise/fall time	[usec]	4		[usec]
t2 - t1	Symmetry of rising edge	-	-		[usec]
Sm	Amplitude of negative pulse	300 [mV]	-		
Sp	Amplitude of positive pulse	300 [mV]	-		
V	Amplitude of video signal	700 [mV]	-		
	H Total		1980		
	H Active		1280		
BPSRT	Broad pulse start pos		260		0 ~ +6
BPSTP	Broad pulse stop pos		1540		-6 ~ 0

15-2. Signal Relations in EAV Decoding

(1) EAV Synchronization (HD)

EAV code which is encoded on input signal is decoded, and the device makes synchronization with its timing.
In 2 channel input case, synchronization is made with EAV of the Y7 ~ Y0 signal, and it is not referenced to the EAV / SAV which are contained in CBCR7 ~ 0 signal.

EAV / SAV Codes

Those codes succeeding 0xFF ~ 0x00 ~ 0x00 which are fed as input data become EAV / SAV codes.

EAV /SAV codes have following meanings, starting with MSB.

Bit Number		MSB							LSB
WORD	VALUE	7	6	5	4	3	2	1	0
0	0xFF	1	1	1	1	1	1	1	1
1	0x00	0	0	0	0	0	0	0	0
2	0x00	0	0	0	0	0	0	0	0
3	0xxx	1	F	V	H	P3	P2	P1	P0

Here, F = 0 : Field 1
F = 1 : Field 2

But, in Progressive Output Modes 525p (480p) / 720p, F-bit is always set to " zero ".

V = 0 : other than Field Blanking (V - Blanking)
V = 1 : Field Blanking (V - Blanking)

H = 0 : SAV
H = 1 : EAV

P3, P2, P1, P0 : Protection bits. Those bits are ignored in the AK8823.

In 525i (480i) / 625i (576i) input cases

Y port data	Cr359	Y719	0xFF	0x00	0x00	0xXX		0xFF	0x00	0x00	0xXX	Cb0	Y0	Cr0	Y1
Pixel No.(60Hz)	1438	1439	1440	1441	1442	1443	……	272	273	1714	1715	0	1	2	3
Pixel No.(50Hz)	1438	1439	1440	1441	1442	1443		284	285	1716	1727	0	1	2	3
			EAV					SAV							

In 525p (480p) / 625p (576p) input cases

Y port data	Y718	Y719	0xFF	0x00	0x00	0xXX		0xFF	0x00	0x00	0xXX	Y0	Y1	Y2	Y3
Pixel No.(60Hz)	718	719	720	721	722	723	……	854	855	856	857	0	1	2	3
Pixel No.(50Hz)	718	719	720	721	722	723		860	861	862	863	0	1	2	3
			EAV					SAV							

In 1080i input case

Y port data	Y	Y	0xFF	0x00	0x00	0xXX		0xFF	0x00	0x00	0xXX	Y0	Y1	Y2	Y3
Pixel No.(60Hz)	1918	1919	1920	1921	1922	1923	……	2196	2197	2198	2199	0	1	2	3
Pixel No.(50Hz)	1918	1919	1920	1921	1922	1923		2636	2637	2638	2639	0	1	2	3
TRS			EAV					SAV							

In 720pi input case

Y port data	Y	Y	0xFF	0x00	0x00	0xXX		0xFF	0x00	0x00	0xXX	Y0	Y 1	Y 2	Y 3
Pixel No.(60Hz)	1278	1279	1280	1281	1282	1283	……	1646	1647	1648	1649	0	1	2	3
Pixel No.(50Hz)	1278	1279	1280	1281	1282	1283		1976	1977	1978	1979	0	1	2	3
TRS			EAV					SAV							

(2) EAV / SAV Codes and Line Synchronization (HD)

The AK8823 makes Vertical Synchronization (Line Synchronization) with either F-bit or V-bit of EAV.
In the Interlaced input signal case, it is synchronized with F-bit.
In the Progressive input signal case, it is synchronized with V-bit.

F-bit of EAV / SAV and Line relation is as follows.

F-bit	525i(480i)	625i(576i)	525P/625P	1080i	720P
0	Line4 - Line265	Line1 - Line312	All lines F = 0	Line1 - Line563	All lines F = 0
1	Line266 - Line525 Line1 - Line3	Line313 - Line625		Line564 - Line1125	

V-bit of EAV / SAV and Line relation is as follows.

. 525i (480i) and 1080i cases

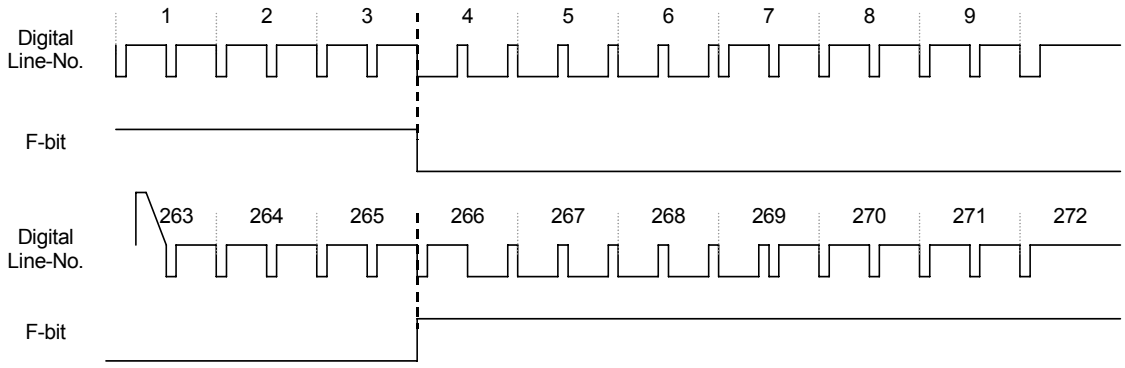
Field	V-bit	525i (480i)	625i (576i)	1080i(60/50Hz)
Field 1	Start (V=1)	Line1 - Line19	Line624 - Line22	Line1124 - Line1125 - Line20
	End (V=0)	Line20 - Line263	Line23 - Line310	Line21 - Line560
Field 2	Start (V=1)	Line264 - Line282	Line311 - Line335	Line561 - Line583
	End (V=0)	Line283 - Line525	Line336 - Line623	Line584 - Line1123

. 525p (480p) and 750p (720p) cases

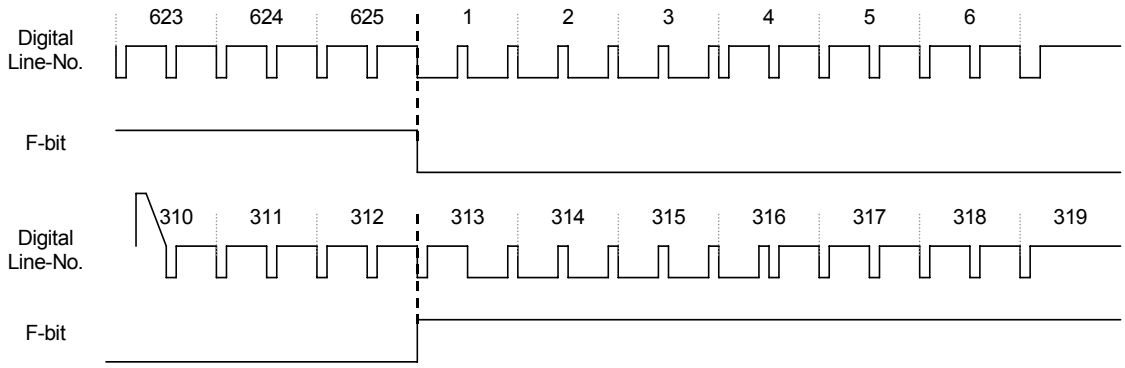
V-bit	525P (480P)	625P (576P)	750P (720P)
Start (V=1)	Line1 - Line42	*Line1 - Line44	Line746 - Line750 - Line25
End (V=0)	Line43 - Line525	Line45 - Line625	Line26 - Line745

(Caution*) EAV decode at 625P(576P) operation mode.
AK8823 considers the transition of V-bit in EAV “0”->”1” as line 1.
(Also refer to page 40 for 625p EAV synchronization.)

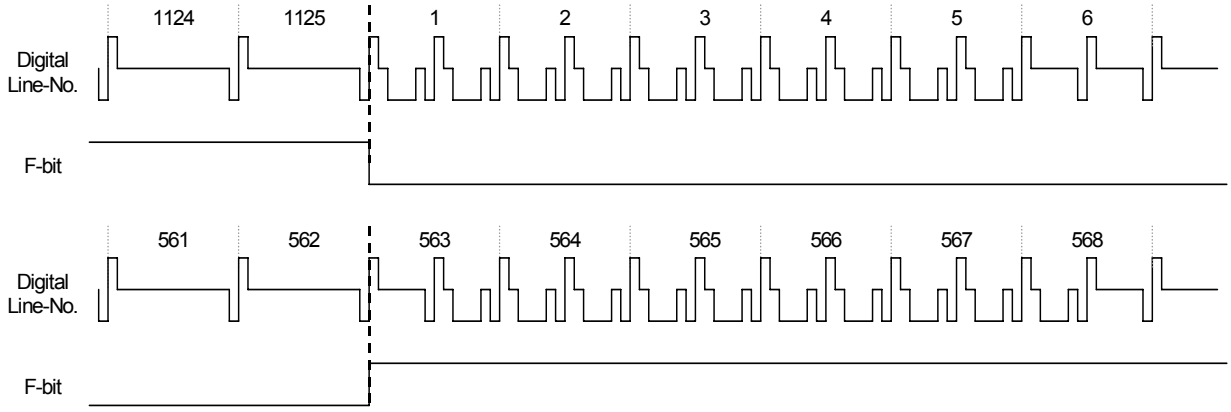
. When in the Interlaced input signal cases (525i (480i), 625i(576i) and 1080i modes),
Line Synchronization with input signal is made with F-bit of EAV.



Line Synchronization with EAV in 525i (480i) Input Mode

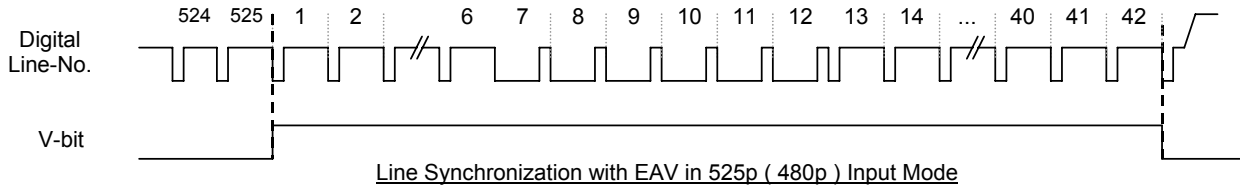


Line Synchronization with EAV in 625i (576i) Input Mode

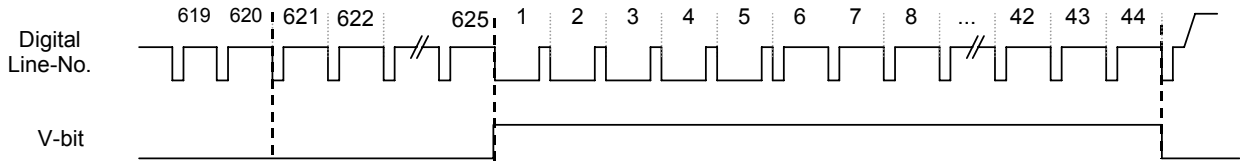


Line Synchronization (60 Hz / 50 Hz) with EAV in 1125i (1080i) Input Mode

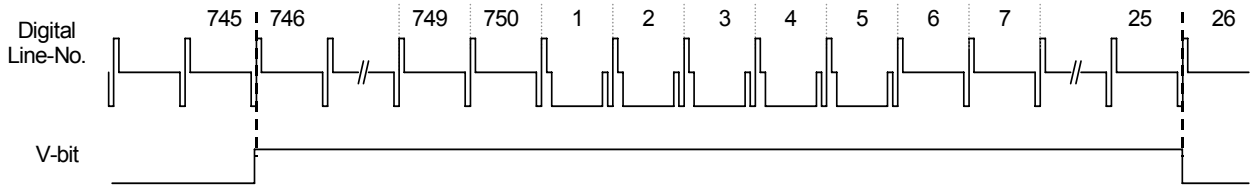
When in the Progressive signal input cases 525p (480p), 625P（576P） and 750p (720p)
Line Synchronization with input signal is made with V-bit of EAV.



Line Synchronization with EAV in 525p (480p) Input Mode



Line Synchronization with EAV in 625p (576p) Input Mode



Line Synchronization with EAV in 750p (720p) Input Mode

15-3. Setting Functions of V-Blank Interval and Output Mode (HD)

The AK8823 has functions to set V-Blank Interval and to control Output Mode during the V-Blank Interval.
V-Blank Interval is set by [Address : 0x01 VL1 : VL0] – bits of [VBI Length & Data Delay] register (see the following table below).
The Output Mode during V-Blank Interval is set by [Address : 0x01 VUNMASK]- bit2.

(note) pull the input signal to the Pedestal level. So when input signal level is equal to Pedestal level, difference is not detected.

mode / [VL1:VL0]	525i mode	625i mode	525P(625p) mode
01	Line1 – Line21 Line264 – Line284	Line623 – Line23 Line311 – Line336	Line1 – Line43 (Line621 – Line45)
00	Line1 – Line20 Line264 – Line283	Line623 – Line22 Line311 – Line335	Line1 – Line42 (Line621 – Line44)
11	Line1 – Line19 Line264 – Line282	Line623 – Line21 Line311 – Line334	Line1 – Line41 (Line621 – Line43)
10	Line1 – Line18 Line264 – Line281	Line623 – Line20 Line311 – Line333	Line1 – Line40 (Line621 – Line42)

V-Blank 期間設定

mode / [VL1:VL0]	1125i mode	750p mode
01	Line1124 – Line1125 Line1 – Line21 Line561 – Line584	Line746 – Line750 Line1 – Line26
00	Line1124 – Line1125 Line1 – Line20 Line561 – Line583	Line746 – Line750 Line1 – Line25
11	Line1124 – Line1125 Line1 – Line19 Line561 – Line582	Line746 – Line750 Line1 – Line24
10	Line1124 – Line1125 Line1 – Line18 Line561 – Line581	Line746 – Line750 Line1 – Line23

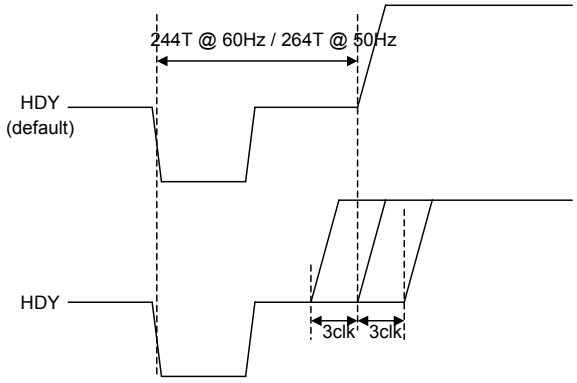
Output conditions during V-Blank Interval are set by Address : 0x01 VUNMASK-bit, as follows

mode / VUNMASK	525i/625i mode	525p/625p mode	1125i mode	750p mode
0	Black level output during V-Blank Interval	Black level output during V-Blank Interval	Black level output during V-Blank Interval	Black level output during V-Blank Interval
1	Input data is output even during V-Blank Interval (525i : Lines 1 ~9 & Lines 264 ~ 272 / 625i : Lines 624 ~ 5 & Lines 311 ~ 318 are excluded)	Input data is output even during V-Blank Interval (525p : Lines 1 ~ 12 / 625p : Lines 641 ~ 5 are excluded)	Input data is output even during V-Blank Interval (1125i : Lines 1124 ~ 1125 ~ 6 & Lines 561 ~ 568 are excluded)	Input data is output even during V-Blank Interval (750p : Lines 746 ~ 750 ~ 5 are excluded)

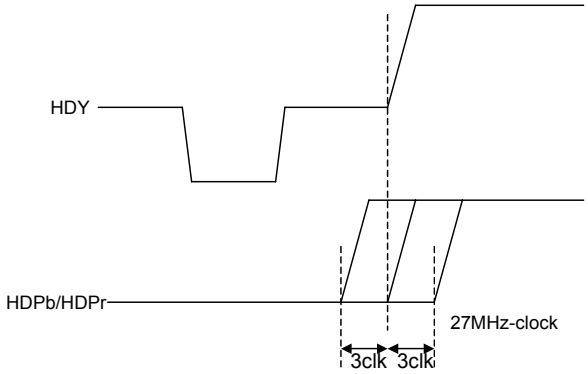
15-4. Adjustable Timing Function Between SYNC Signal and HDY Signal, and Between HDPB Signal and HDPR Signal (HD)

SYNC Timing and HDY signal output relation is adjustable in the AK8823.
Setting of adjustable amount is made by [HDYPBPR Delay Register].
Adjustable range between SYNC signal and HDY signal is + / _ 3 clocks.
Adjustable unit in 525i / p modes is based on 27MHz clock, and in 1080i / 720p modes, it is based on 74.25MHz clock.
By this bit manipulation, HDPb / HDPr are shifted similarly as in the case of HDY.

HDPb / HDPr signals with HDY signal relation are adjusted by Sub Address 0x02 [HDYPBPR Delay Register].
Adjustable range is +/- 3clocks.
Adjustable unit in 525i / p modes is based on 27MHz clock, and in 1080i / 720p modes, it is based on 74.25MHz.

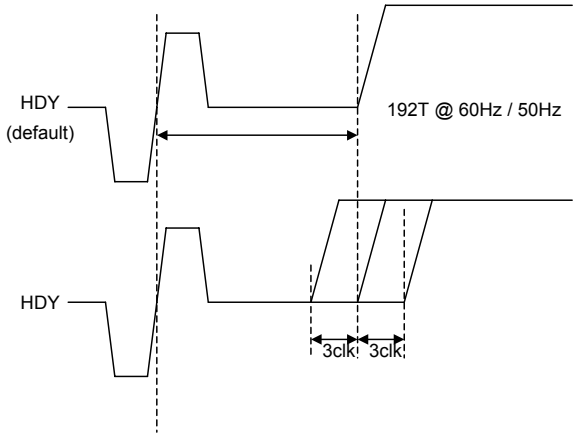


SYNC Signal and HDY Signal relation

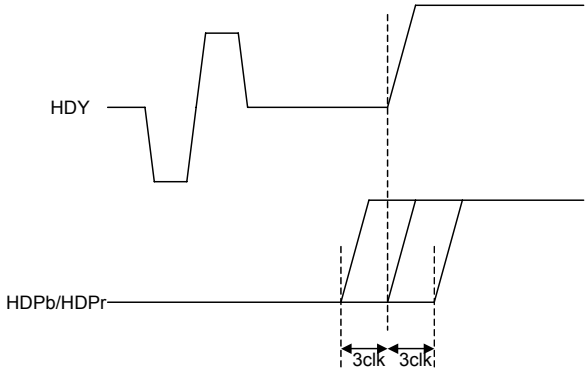


HDY Signal and HDPb / HDPr Signal relation

In 525i / 625i Input Mode T : 27 MHz

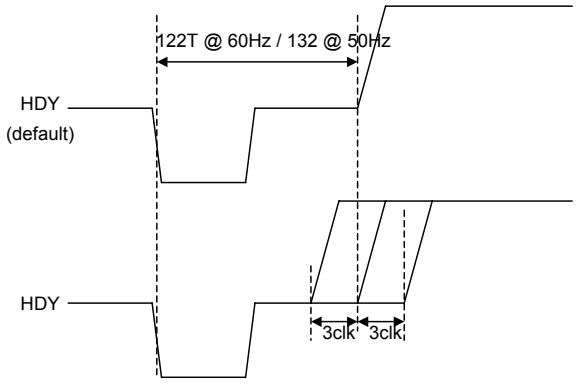


SYNC Signal and HDY Signal relation

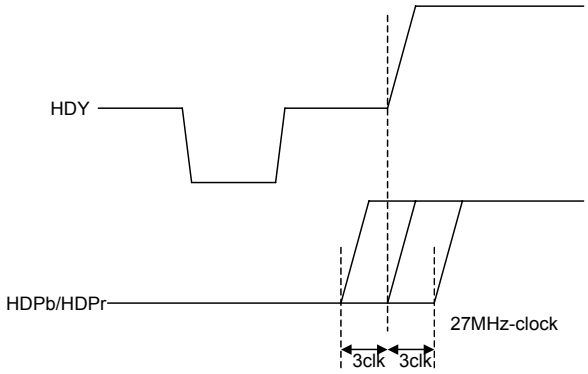


HDY Signal and HDPb / HDPr Signal relation

In 1080i @ 60 Hz / 50 Hz Input Mode T : 74.25 MHz

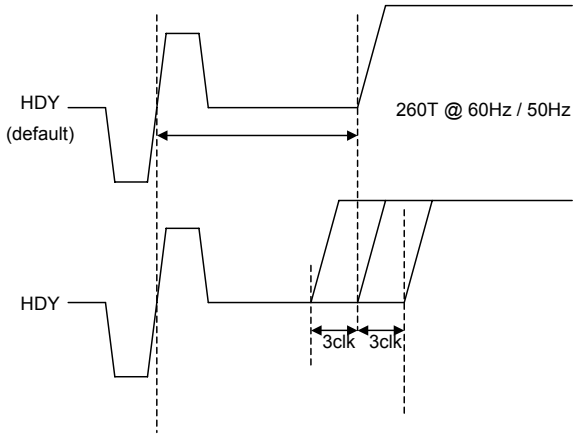


SYNC Signal and HDY Signal relation

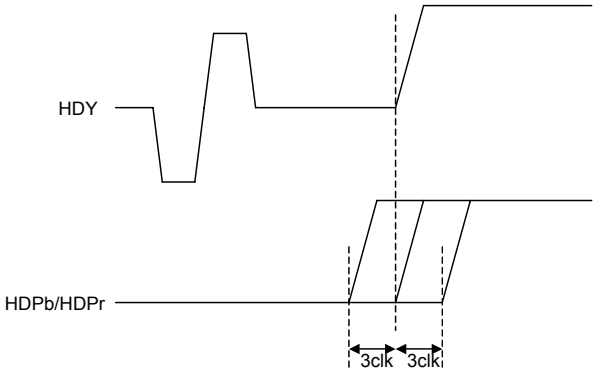


HDY Signal and HDPb / HDPr Signal relation

In 525p / 625p Input Mode T : 27 MHz



SYNC Signal and HDY Signal relation



HDY Signal and HDPb / HDPr Signal relation

In 720p @ 60 Hz / 50 Hz Input Mode T : 74.25 MHz

15-5. Set-Up Process Function (HD)

In the AK8823, a 7.5 % set-up can be added by [Mode Register] setting.
Set-Up process is done in the following manner.

Luminance Signal = 700 [mV] x 7.5 % + (Luminance signal without set-up) x 0.925
Chroma Signal = (Cb/Cr signals without set-up) x 0.925

15-6. On chip out-put Video Limiter (HD, SD Modes)

Limiter function is performed on signals which exceed Pedestal Level.
Limiter Levels are set at 0 IRE (no limiter), - 1.5 IRE and - 7 IRE.
These levels can be independently controlled for HD and SD Blocks.

15-7. Black Burst Signal Generator Function (HD)

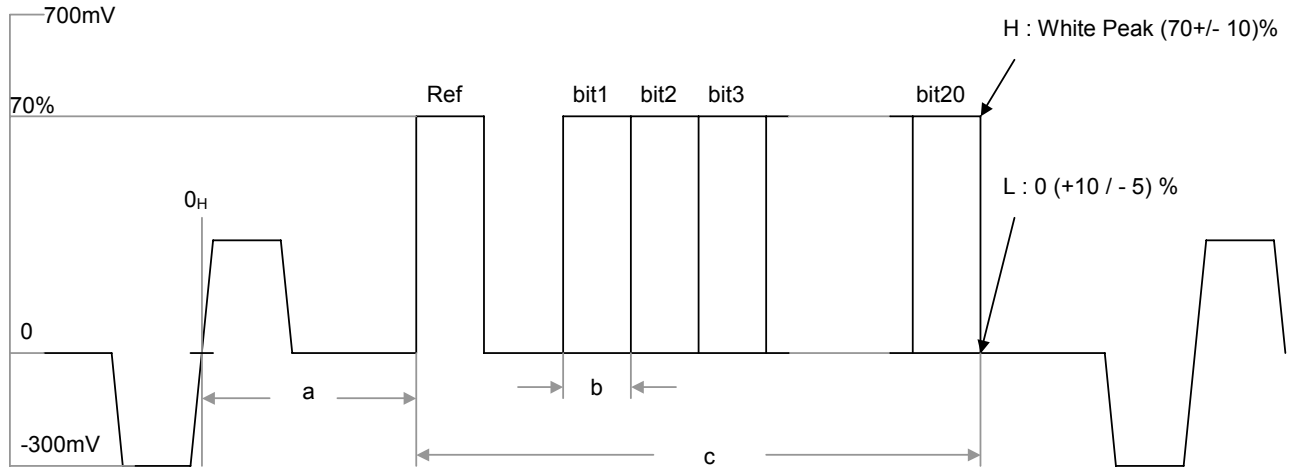
The AK8823 can output Black Burst Signal (Black Level Output).
When BB-bit of [Mode Register] is set to " 1 ", same operation is processed as in the case when the fixed-16 Luminance signal and the fixed-128 Cb / Cr signal outputs are input.
In this case, when set-up bit is " ON ", set-up process is done and when it is " OFF ", no set-up process is made.

15-8. Color Bar Signal Generator Function (HD)

The AK8823 can output Color Bar Signal in all output modes.
Color Bar Signal is output by setting CB-bit of [Mode Register] to " 1 ".
In this case, when set-up bit is " ON ", set-up process is done and when it is " OFF ", no set-up process is made.
When to output Color Bar Signal, required timing is automatically generated internally.
Namely, it is no need to input SYNC timing from outside of the chip.

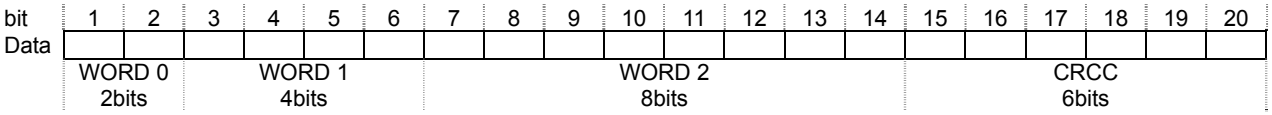
15-9. Video ID(HD)

The AK8823 has a function to super-impose a Copy Protect Information CGMS-A type-A on output signal.

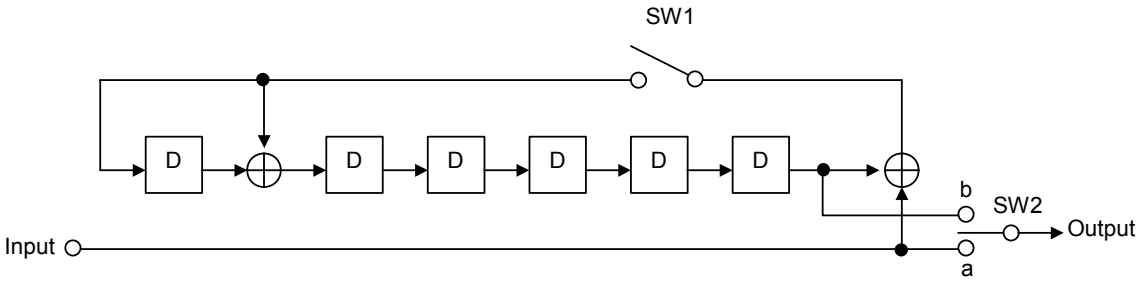


	a	b	c		Line
525i* (480i)	11.2 +/- 0.3usec (time from 0H)	2.235 +/- 50nsec	49.1 +/- 0.44usec		Line 20 Line 283
525P* (480P)	6T (5.8 +/- 0.15usec) (time from 0H)	T +/- 30nsec	22T (21.2 +/- 0.22usec)	T : 1/(f_H x 33) = 963nsec	Line 41
1080i	4T (4.15 +/- 0.16usec)	T +/- 30nsec	22T (22.84 +/- 0.21usec)	T : 1/(f_H x 2200/77) = 1.038usec	Line 19 Line 582
720P	4T (3.13 +/- 0.09usec)	T +/- 30nsec	22T (17.20+/- 0.16usec)	T : 1/(f_H x 1650/58) = 0.782usec	Line 24

* SYNC signal waveform of 525i / p (480i / p) signals differ from the above, but timing is defined based on 0H point as starting point.



20 Bit data is configured with WORD 0 : 2 bits / WORD 1 : 4 bits / WORD 2 : 8 bits / CRCC : 6 bits, as shown above.
When to set CGMS-A Data, set CGMS-bit of [Mode Register] (Address 0x03) to " 1 ", and write a setting value to [CGMS-A Data 1 / 2 Register].
CRCC is automatically calculated and added in the AK8823.
Default value of " CRCC Polynomial expression X6 + X + 1 " are all ones (see diagram below).



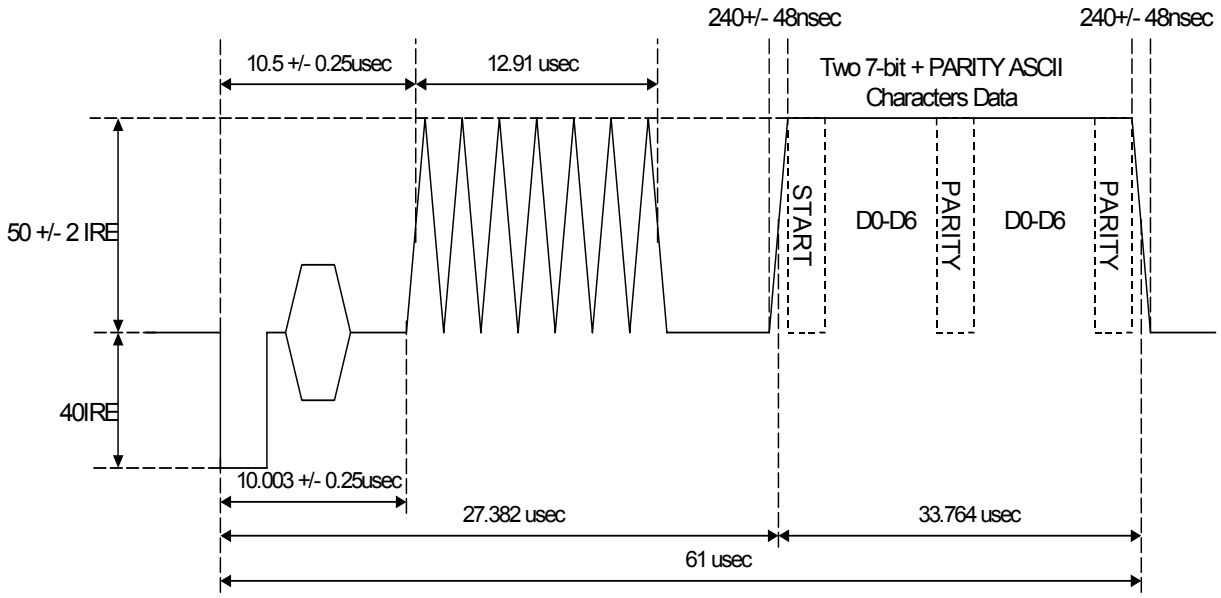
CRCC generation is made as follows –
Set default values to all ones and close SW1.
Set SW2 to " a " position and first 14 bit data is input, then at the 15th bit, open SW1 and set SW2 to " b " position, and CRCC is output.
When CGMS-A output and other signal waveforms coincide, CGMS-A precedes.

15-10. Closed Caption(HD)

The AK8823 has encoding functions of the Closed Captioning and Extended Data.
ON / OFF control of these functions and its data are in accordance with { Video Process 2 Register (12H) } setting for SD side.
As for the HD side, HD side Output can be disabled by setting Bit 3, CC_DIS at Address 0x01.
Since Closed Caption function is shared with SD side, it functions properly only when Video Data is received from SD port.
Each Data occupies a consecutive 2 Byte Register area { Closed Caption R (26H, 27H)}.
Data is written at 26H first, then 27H in this order.
Data is judged to be updated when data at 27H is written.
When data is updated, it is encoded on a coming thereafter, pre-scribed Line.
When no data updating is made, ASCII Null code is output.
Each data is assumed with ODD parity + 7 bit US ASCII code. Parity is processed at the Host side.。

* Closed Caption Data is encoded on the following Lines.

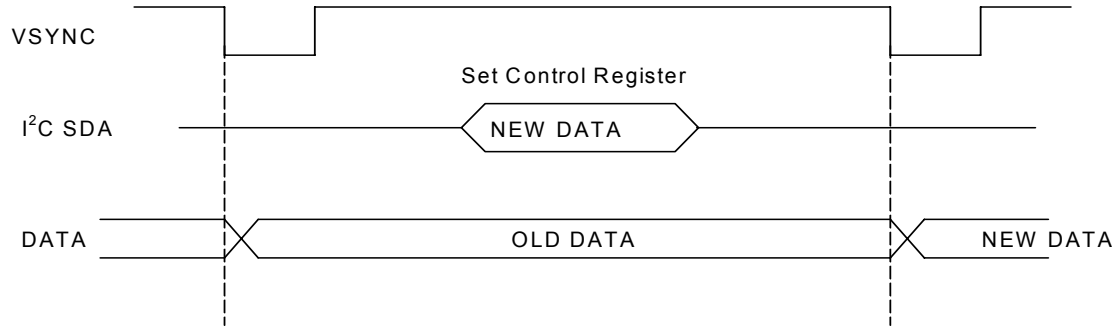
	D1/60 System (SMPTE)	625/50 System (ITU-R)
Closed Caption	21 Line default	22 Line default
Extended Data	284 Line default	335 Line default



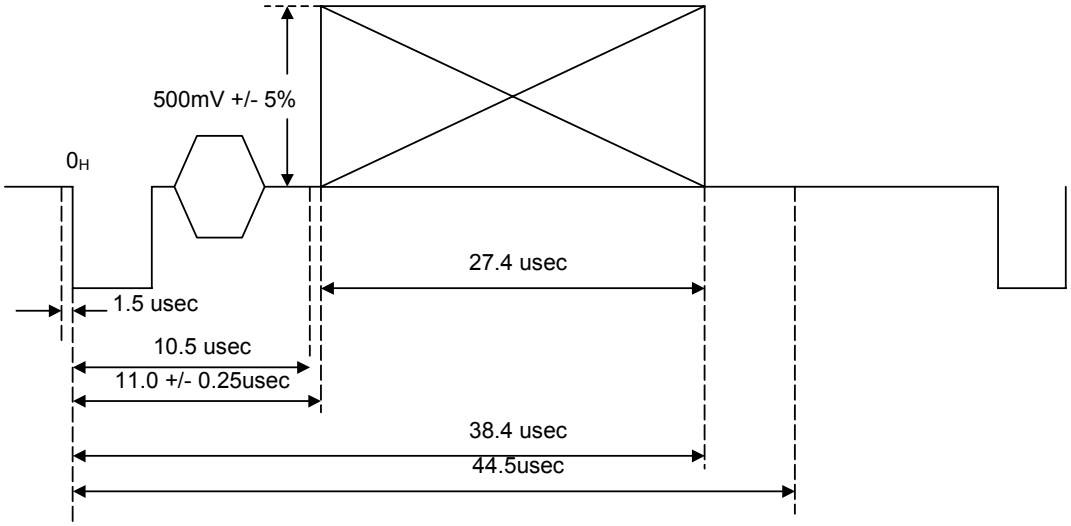
15-11. WSS Function (HD D1/50Hz)

The AK8823 supports to encode WSS (ITU-R BT.1119), IEC62375 which distinguish the Aspect Ratio etc..
Turning " ON / OFF " of this function is controlled by HDWSS bit of { Video Process HD Register (07H bit [7])}, and setting data is set at { WSS Data Register (0x08, 0x09)}.

WSS Data Up-date Timing



WSS Waveform



Encode Line : 625i / 50 former half of Line 23
(note) When to encode WSS in HD mode, video signal at the latter half line is not output.
Coding : Bi-Phase Modulation coding
Clock : 625i / 50 5 MHz (Ts = 200 ns)
Encoding details are listed in the follow table.

Run-in	Start code	Group 1 Aspect ratio	Group 2 Enhanced Services	Group 3 Subtitles	Group4 Reserved
29 elements	24 elements	24 elements	24 elements	18 elements	18 elements
		Bit numbering 0 1 2 3 LSB MSB 0 : 000111 1 : 111000	Bit numbering 4 5 6 7 LSB MSB 0 : 000111 1 : 111000	Bit numbering 8 9 10 LSB MSB 0 : 000111 1 : 111000	Bit numbering 11 12 13 LSB MSB 0 : 000111 1 : 111000
0x1F1C71C7	0x1E3C1F				

16. SD Block

16-1. Color Burst Signal (SD)

Color Burst signal is generated by a 32-Bit Digital Frequency Synthesizer.
Color Burst Sub-carrier frequency is set by VM0 ~ VM1 bits of { Video Process 1 Register (0x11)}.

spec	Subcarrier Freq (MHz)	Video Process 1 [VM1,VM0]
NTSC-M	3.57954545	[0,0]
PAL-M	3.57561188	[0,1]
PAL-B,D,G,H,I	4.43361875	[1,1]
PAL-N(Arg)	3.5820558	[1,0]
PAL-N(non-Arg)	4.43361875	[1,1]
PAL60	4.43361875	[1,1]
NTSC-4.43	4.43361875	[1,1]

Burst Signal Table

Sub-carrier frequency of 3.57561188 MHz is supported in PAL-M mode only.
Burst Frequency and Initial Phase Resolutions are as follows.

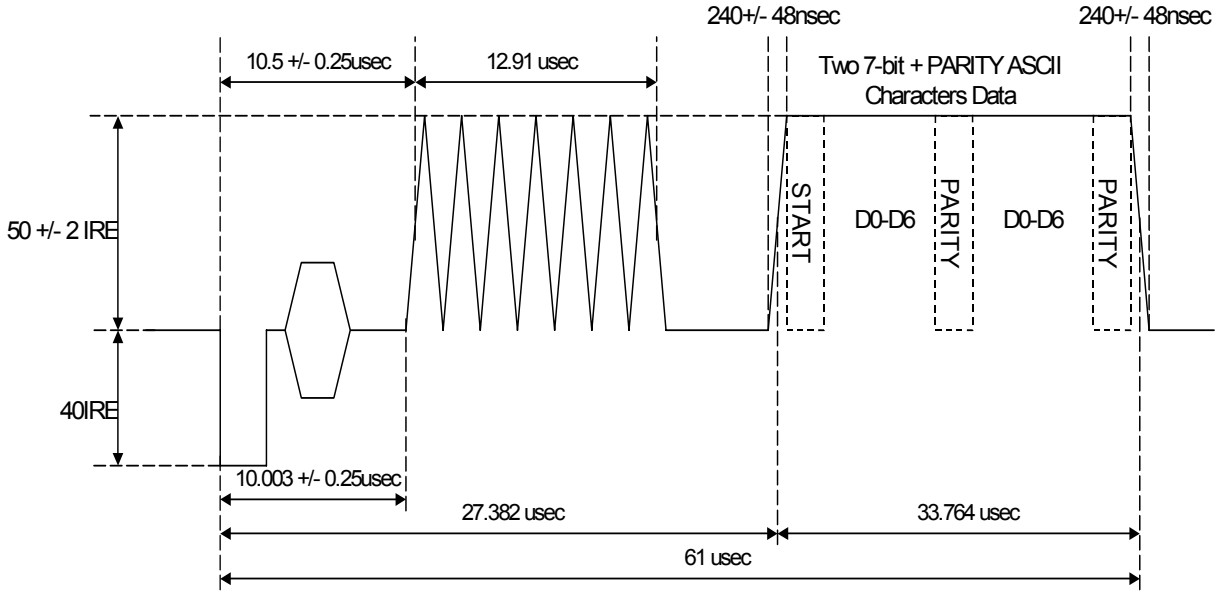
Pre-settable Frequency Resolution 0.8046 Hz
SCH Phase Resolution 360 / 256 degrees

16-2. Closed Caption(SD)

The AK8823 has encoding functions of the Closed Captioning and Extended Data.
ON / OFF control of these functions is in accordance with { Video Process 2 Register (12H) } setting.
Each Data occupies a consecutive 2 Byte Register area { Closed Caption R (26H, 27H)}.
Data is written at 26H first, then 27H in this order.
Data is judged to be updated when data at 27H is written.
When data is updated, it is encoded on a coming thereafter, pre-scribed Line.
When no data updating is made, ASCII Null code is output.
Each data is assumed with ODD parity + 7 bit US ASCII code. Parity is processed at the Host side.

* In PAL Encoding mode, output is also made in the same timing & format as in NTSC mode.
* Closed Caption Data is encoded on the following Lines.

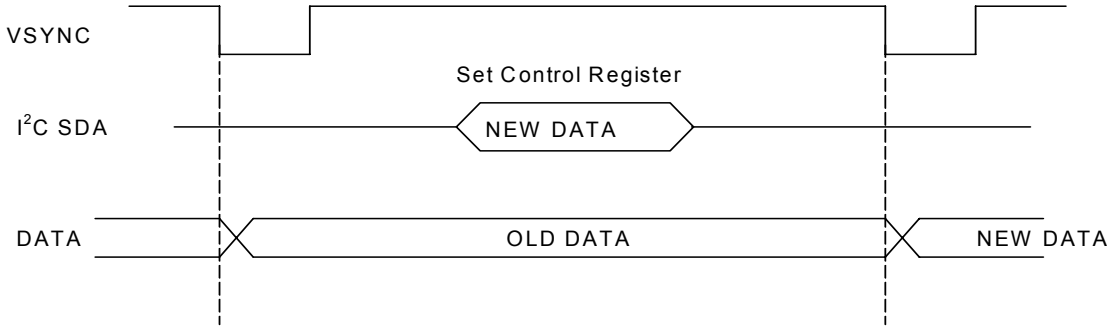
	525/60 System (SMPTE)	625/50 System (ITU-R)
Closed Caption	21 Line default	22 Line default
Extended Data	284 Line default	335 Line default



16-3. Video ID (SD)

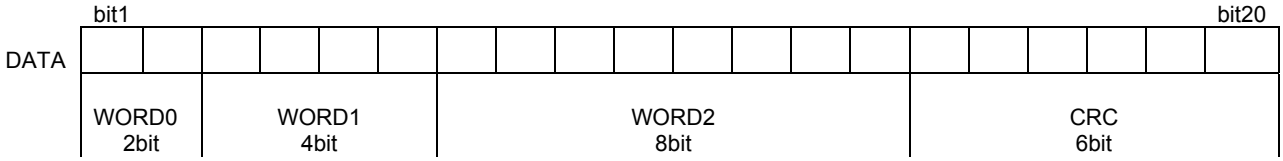
The AK8823 supports to encode the Video ID (EIAJ CPR-1204) which distinguishes the Aspect Ratio etc..
This is also used as CGMS (Copy Generation Management System).
Turning " ON / OFF " of this function is controlled by VBID bit of { Video Process 2 Register (12H)} and setting data is set at { Video ID Data Register (2AH, 2BH)}.
Video ID information has the highest order of priority among VBI information (when simultaneous output with Macrovision signaling occurs, only the VBI information is super-imposed on this line).

VBID Data Up-date Timing

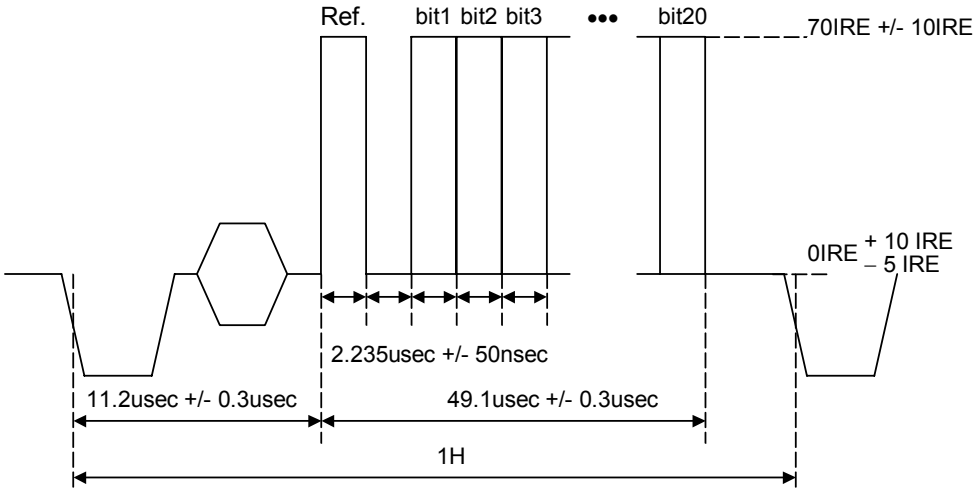


VBID Data Code Assignment

20 bit data is configured with WORD0 = 2 bits, WORD1 = 4 bits, WORD2 = 8 bits, CRC = 6 bits.
CRC is automatically calculated and added in the AK8823.
Default values of "CRC Polynomial Expression X6 + X + 1" are all ones.



VBID Signal Waveform

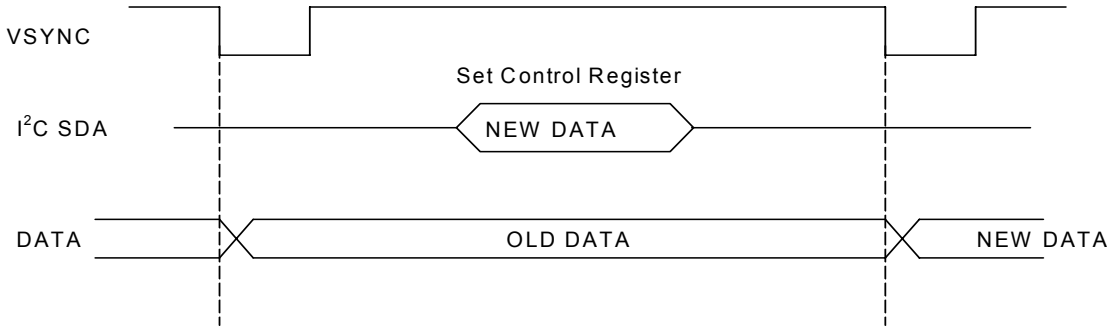


	525/60 System	625/50 System
Amplitude	70IRE	490mV
Decode line	20/283	20/333

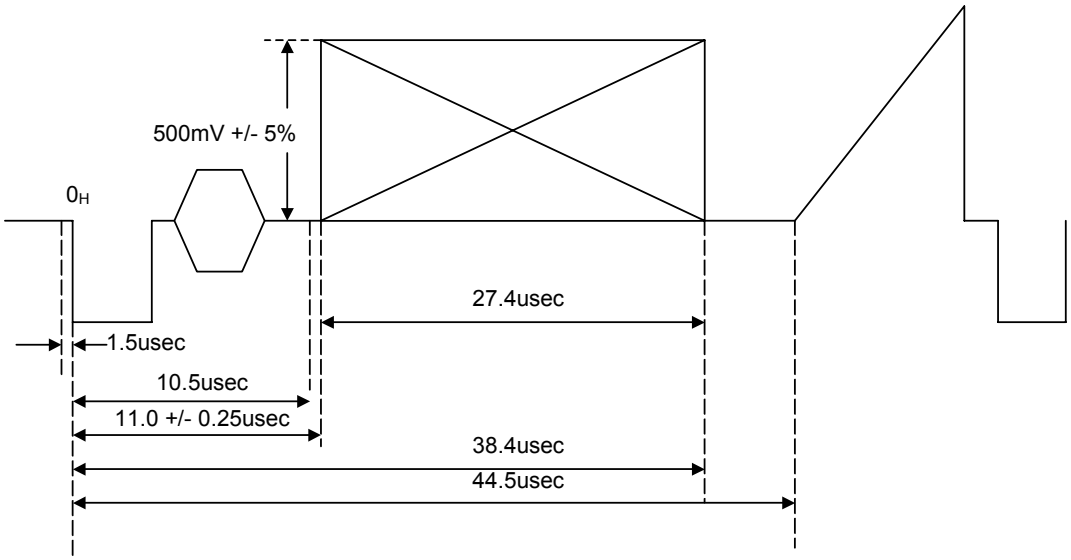
16-4. WSS Function (SD)

The AK8823 supports to encode the WSS (ITU-R BT.1119) which distinguishes the Aspect Ratio etc..
Turning " ON / OFF " of this function is controlled by WSS bit of { Video Process 2 Register (12H)}, and setting data is set at { WSS Data Register (0x18, 0x19)}.

WSS Data Up-date Timing



WSS Waveform



Encode Line : former half of Line 23
(note) When to stop Video output at the latter half line, Blanking should be made at Line23.
Coding : Bi-Phase Modulation coding
Clock : 5 MHz (Ts = 200 ns)
Encoding details are listed in the follow table.

Run-in	Start code	Group 1 Aspect ratio	Group 2 Enhanced Services	Group 3 Subtitles	Group4 Reserved
29 elements	24 elements	24 elements	24 elements	18 elements	18 elements
		Bit numbering 0 1 2 3 LSB MSB 0 : 000111 1 : 111000	Bit numbering 4 5 6 7 LSB MSB 0 : 000111 1 : 111000	Bit numbering 8 9 10 LSB MSB 0 : 000111 1 : 111000	Bit numbering 11 12 13 LSB MSB 0 : 000111 1 : 111000
0x1F1C71C7	0x1E3C1F				

16-5. Slave Mode (SD)

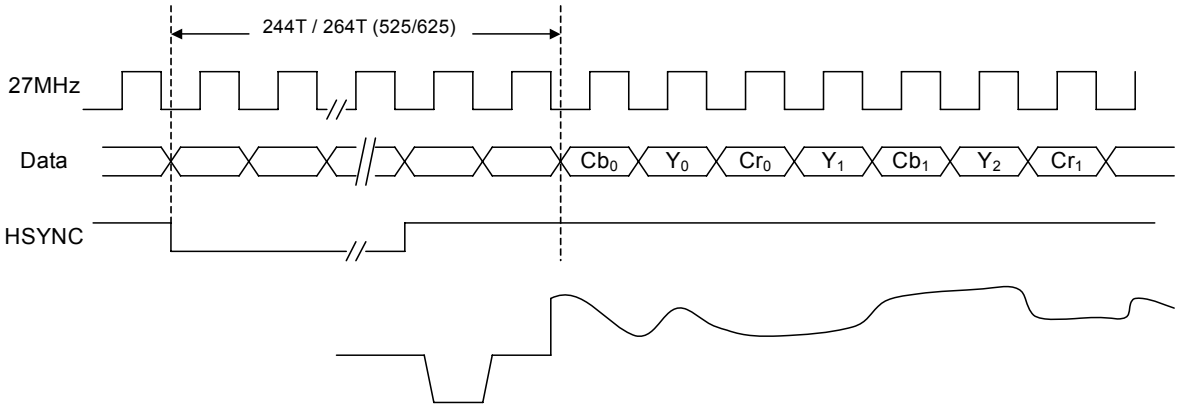
HSYNC and FID or VSYNC (selectable by register setting) timing signals are input when the AK8823 is in Slave mode operation.

In Slave mode, the AK8823 checks transition change of HSYNC at the rise timing of SYSCLK (refer to AC Characteristics).

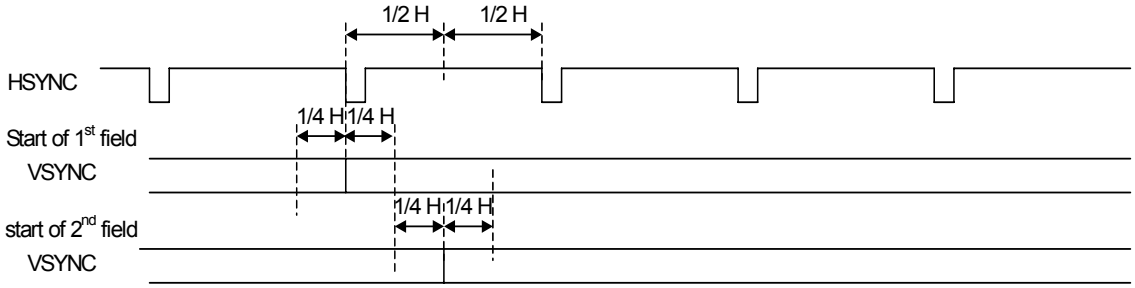
Rise timing of SYSCLK right after HSYNC changes to low, is recognized to be the 32nd (24th) data in Video Stream, and the 276th (288th) Data is captured as Cb Data.

Video Field is recognized with FID / VSYNC relation with HSYNC (refer to Video Field Recognition diagram below).

As shown in the diagram, its relation allows +/_ 1/4 H time margin respectively.



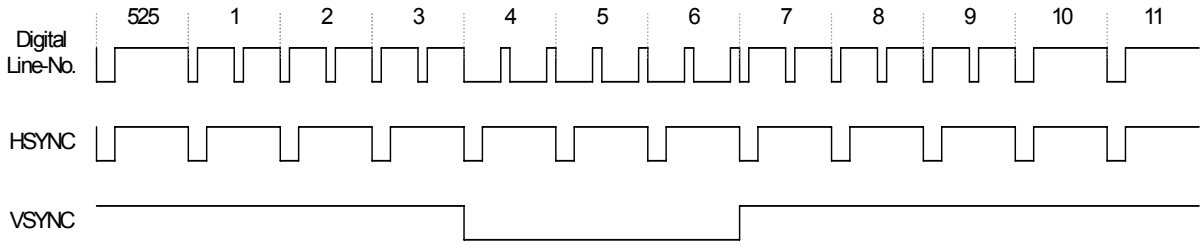
Field Recognition is made in the following timing.

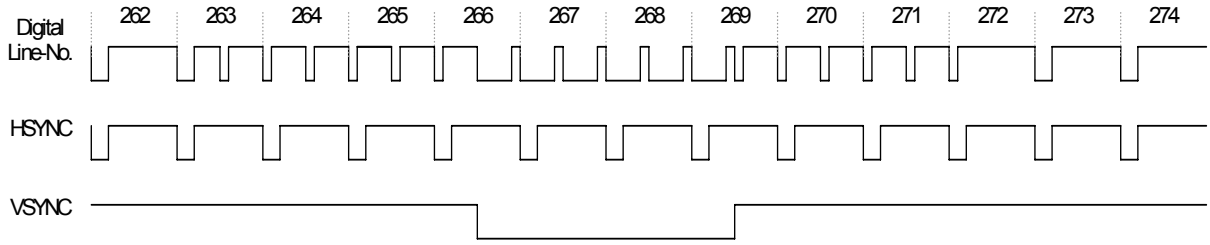


Field Recognition

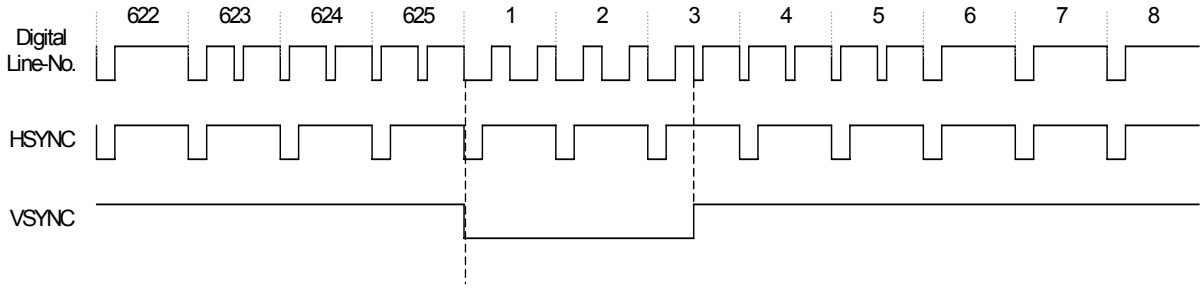
Line and VSYNC input relation is as follows.

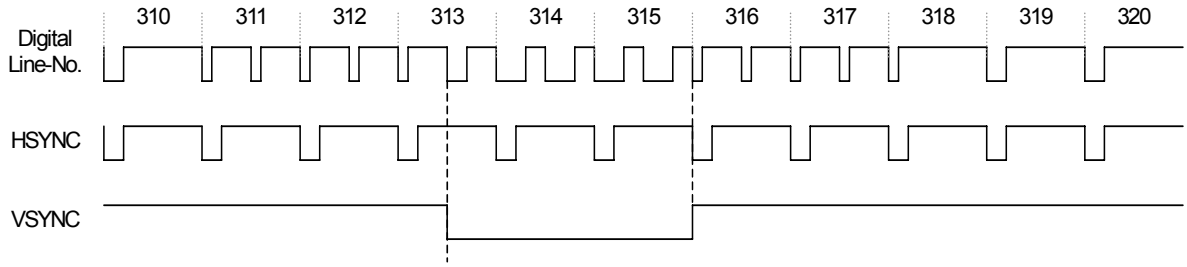
525 System





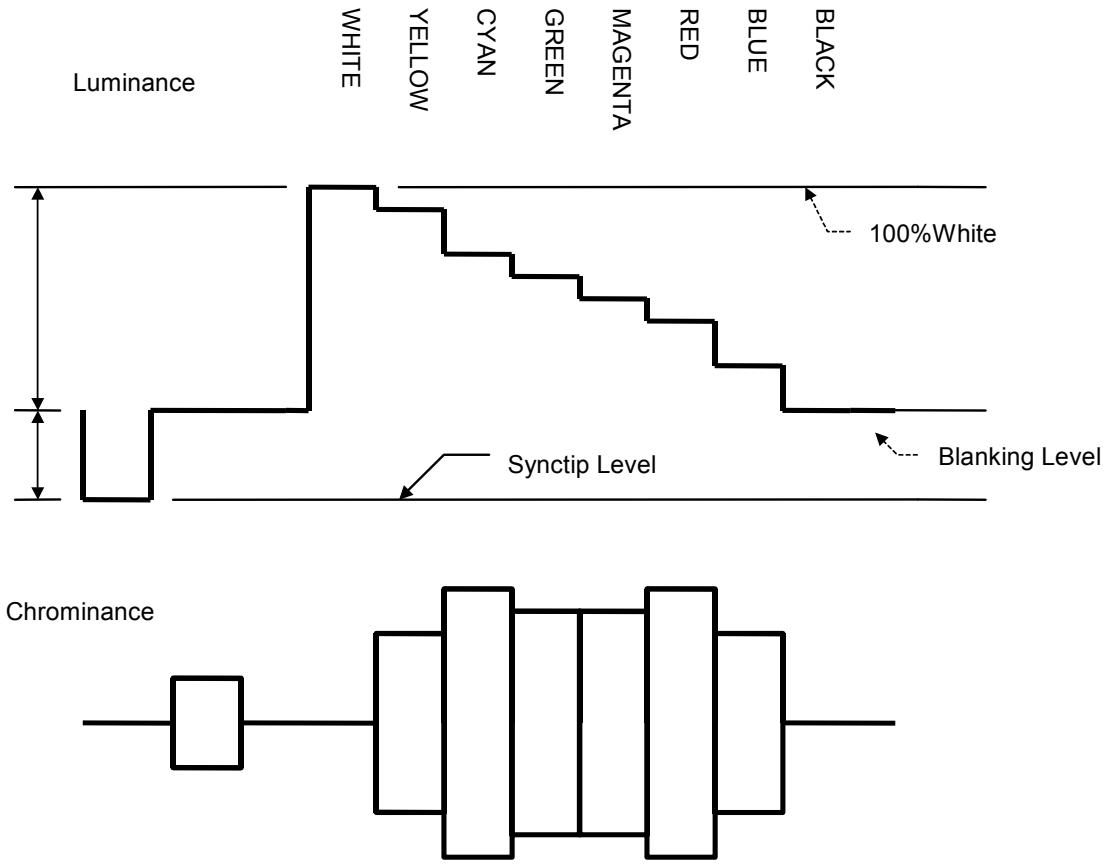
625 System





16-6. On-chip Color Bar (SD)

The AK8823 can output Color Bar Signal. Color Bar Signal to be generated has 100 % Amplitude and 100% Saturation Levels.
Color Bar Signal is output by setting CBG-bit of [Video Process 1 Register] to " 1 ".
In this case, Set-up process is performed when Set-up bit is " ON " and no set-up process is done when Set-up bit is " OFF ".
When to output Color Bar Signal, required timing is automatically generated internally.
Namely, it is no need to input SYNC timing from outside of the chip.
The AK8823 outputs Black Level when BBG-bit is set, and no Color Bar output is made.



codes are expressed in ITU-R BT. 601 Format

	WHITE	YELLOW	CYAN	GREEN	MAGENTA	RED	BLUE	BLACK
Cb	128	16	166	54	202	90	240	128
Y	235	210	170	145	106	81	41	16
Cr	128	146	16	34	222	240	110	128

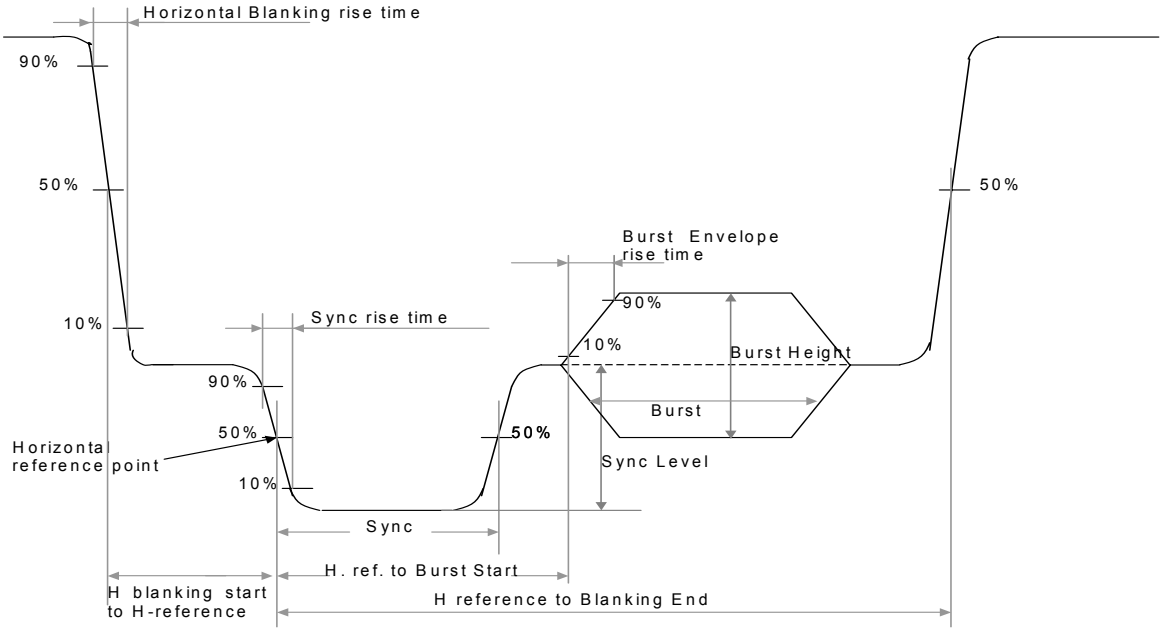
note) transition of each color is in accordance with ITU-R Rec.601.

16-7. Black Burst Signal Generator Function (SD)

The AK8823 can output Black Burst signal (Black Level Output).
When BBG-bit of [Video Process 1 Register] is set to " 1 ", same operation is processed as in the case when the fixed-16 Luminance signal and the fixed-128 Cb / Cr signal outputs are input.
In this case, Set-up process is done when Set-up bit is " ON ", and no set-up process is done when it is " OFF ". If CBG-bit is set, it is ignored.

16-8. SYNC Signal Waveform . Burst Waveform (SD)

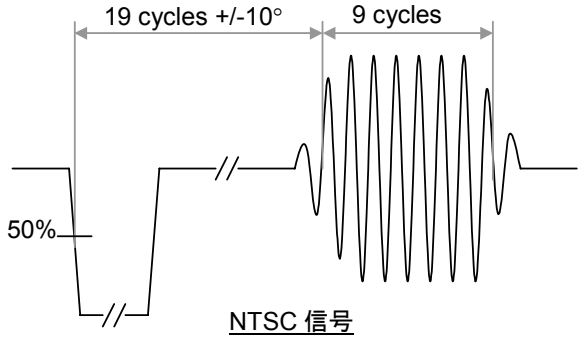
(1-1) NTSC /NTSC-4.43 / PAL-M (in case of Video Process 1 Register [VM3 : VM2]-bit = 00 / 01) (SMPTE-170M)



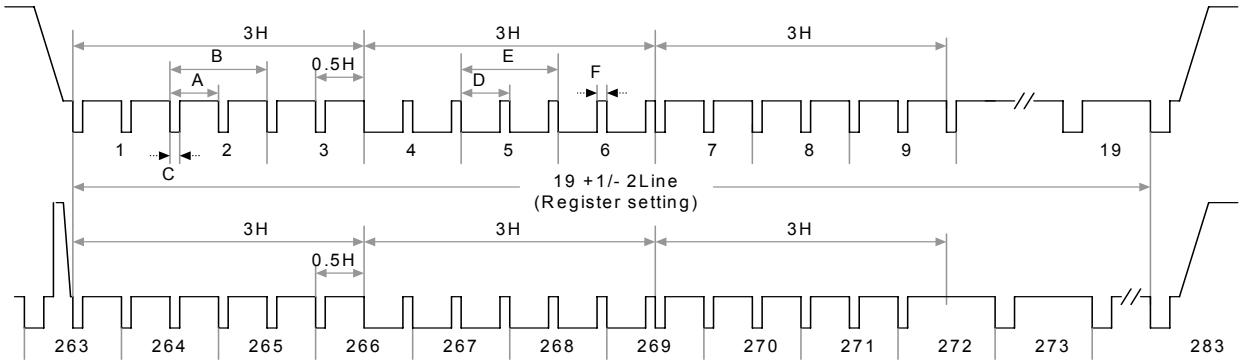
	measurement point	value	Recommended tolerance	units
Total line period(derived)		63.556		usec
Sync Level		40	+/- 1	IRE
Horizontal Blanking rise time	10% - 90%	140	+/- 20	nsec
Sync rise time	10% - 90%	140	+/- 20	nsec
Burst envelope rise time	10% - 90%	300	+200 -100	nsec
H-Blanking start to H-reference	50%	1.5	+/- 0.1	usec
Horizontal Sync	50%	4.7	+/- 0.1	usec
Horizontal reference point to burst start	50%	19	defined by SC/H	cycles
H reference to H-blanking end	50%	9.2	+ 0.2 - 0.1	usec
Burst *	50%	9	+/- 1	cycles
Burst Height **		40	+/- 1	IRE

* Measurement of Burst Timing Length is made between the Burst Start Point which is defined as the zero-cross point, preceding the first-half cycle of the sub-carrier where Burst Amplitude becomes higher than 50 % level and the Burst End Point, defined in the same manner.
Burst Time Length (period) is 10 cycles in NTSC-4.43 mode.

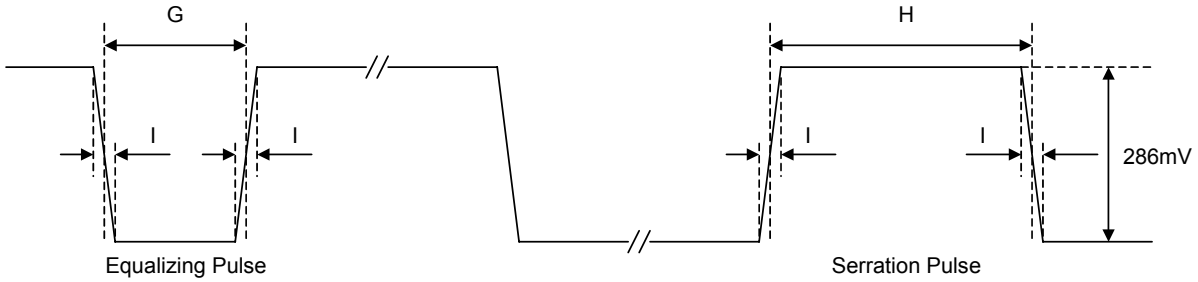
** Burst Height of PAL-M mode is 306 mV.



(1-2-1) Vertical SYNC Signal Timing (NTSC / NTSC-4.43)



Symbol	Duration	Measurement point	Reference
A	429T	50%	13.5MHz Clock
B	858T		
C	31T		
D	429T		
E	858T		
F	63T		

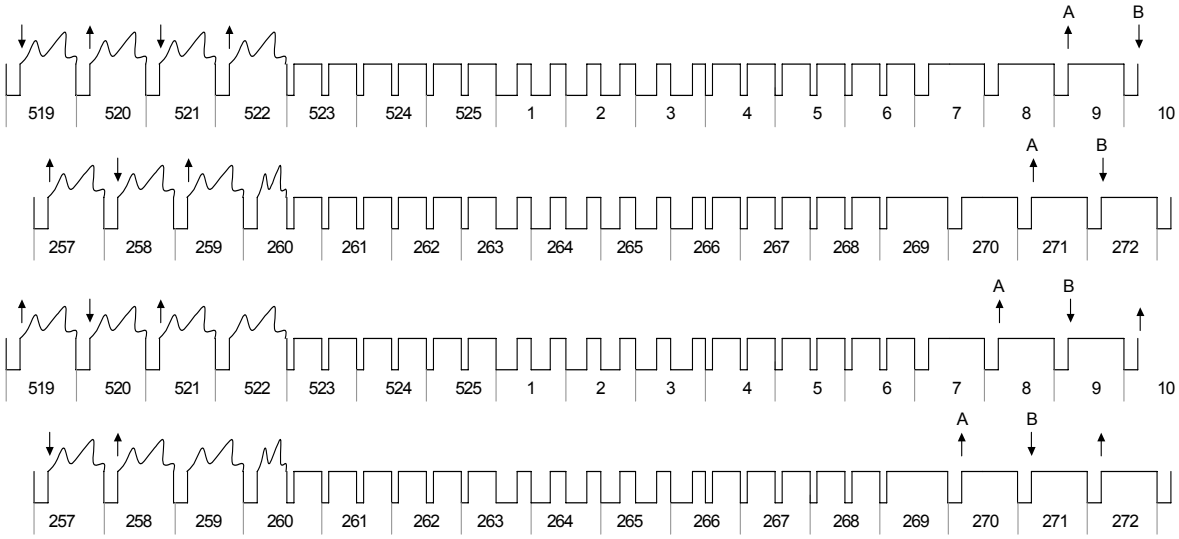


Equalizing Pulse and Serration Pulse

Symbol		Measurement point	Value	Recommended tolerance	units
	Field Period (derived)		16.6833		msec
	Frame period (derived)		33.3667		msec
	Vertical blanking start before first equalizing pulse	50%	1.5	+/- 0.1	usec
	Vertical blanking (63.556usec x 20lines + 1.5usec)		19* lines + 1.5 usec	0 +/- 0.1	lines usec
	Pre-equalizing duration		3		lines
G	Pre-equalizing pulse width	50%	2.3	+/- 0.1	usec
	Vertical sync duration		3		lines
H	Vertical serration pulse width	50%	4.7	+/- 0.1	usec
	Post-equalizing duration		3		lines
G	Post-equalizing pulse width	50%	2.3	+/- 0.1	usec
I	Sync rise time		140	+/- 20	nsec

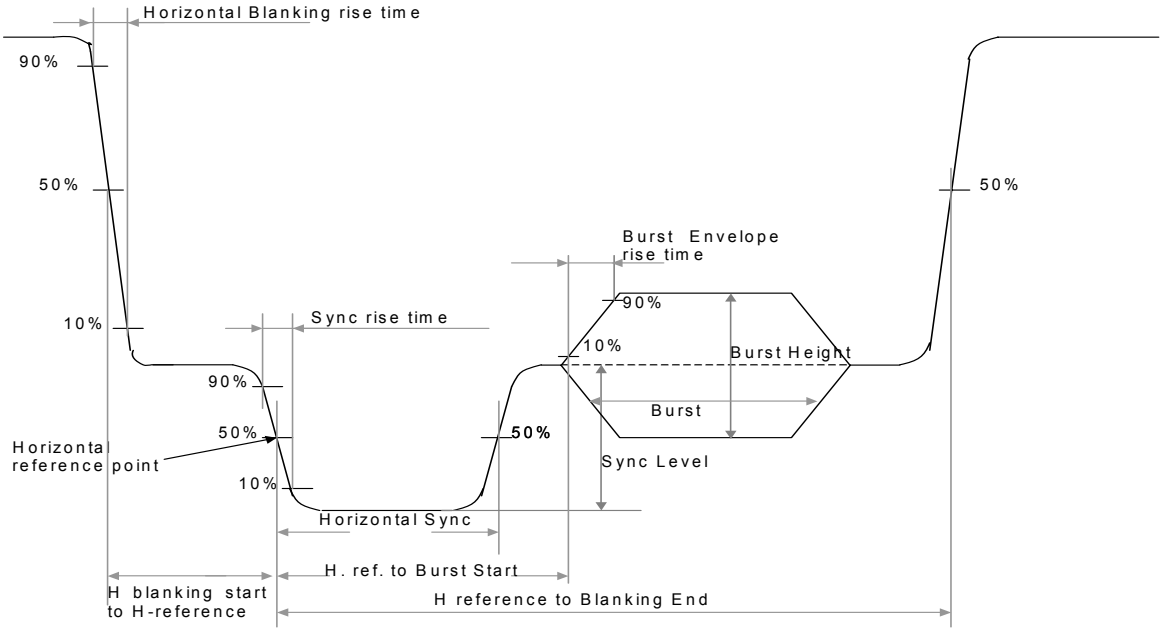
* there is a case with V-Blank of 20 Lines. This value is pre-settable by register.

(1-2-2) Vertical SYNC Signal Timing and Burst Phases (PAL-M)



A : Phase of Burst : nominal Value + 135°
B : Phase of Burst : nominal Value - 135°

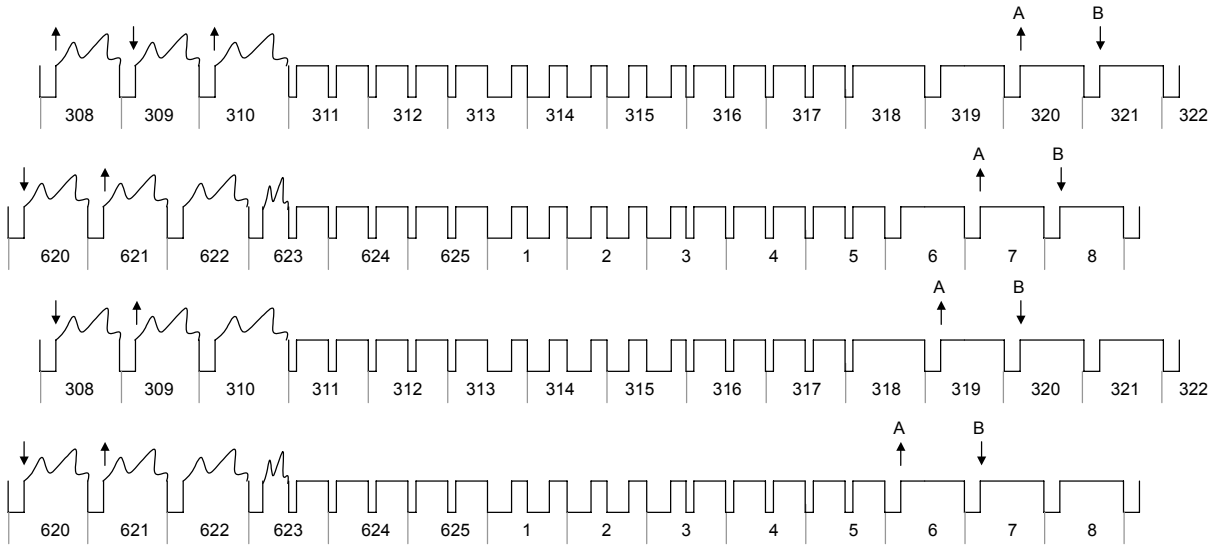
(2-1) PAL-B, D, G, H, I, N / PAL-60 (in case of Video Process 1 Register [VM3 : VM2] –bit = 11)



	measurement point	value	Recommended tolerance	units
Total line period(derived)		64.0		usec
Sync Level		300		mV
Horizontal Blanking rise time	10% - 90%	0.3	+/- 0.1	usec
Sync rise time	10% - 90%	0.2	+/- 0.1	usec
Burst envelope rise time	10% - 90%			nsec
H-Blanking start to H-reference	50%	1.5	+/- 0.3	usec
Horizontal Sync	50%	4.7	+/- 0.2	usec
Horizontal reference point to burst start	50%	19	defined by SC/H	cycles
H reference to H-blanking end	50%	10.5		usec
Burst *	50%	10	+/- 1	cycles
Burst Height **		300		mV

(2-2) Vertical SYNC Signal Timing and Burst Phases

PAL-B, D, G, H, I, N / PAL-60 (in case of Video Process 1 Register [VM3 : VM2]-bit = 11)



A : Phase of Burst : nominal Value + 135°

B : Phase of Burst : nominal Value - 135°

17. Device Control Interface

The AK8823 is controlled via I2C Bus Control Interface.

[I2C Bus Slave Address]
I2C Slave Address is selectable to be either 0x40 or 0x42 by SELA pin setting.

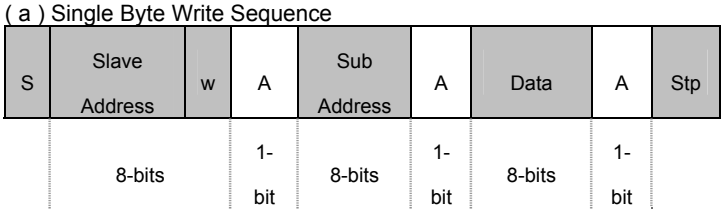
SELA pin state	SLAVE Address (*)
pull-down [low]	0x40
pull-up [high]	0x42

(*) SLAVE Address is depicted in 8-bits, LSB is reserved for W/R bit.

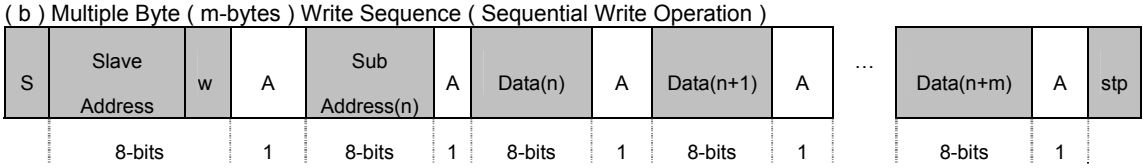
[I2C Control Sequence]
(1) Write Sequence
When the Slave Address of the AK8823 Write mode is received at the first byte, Sub-Address at the second byte and Data at the third & succeeding bytes are received.
There are 2 operations in Write sequence—

A sequence to write at every single byte and a sequential write operation that to write multiple bytes successively.

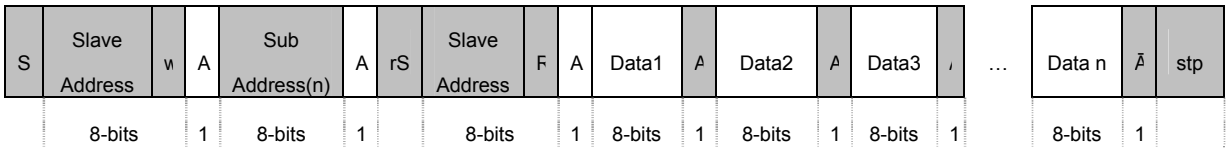
(a) Single Byte Write Sequence



(b) Multiple Byte (m-bytes) Write Sequence (Sequential Write Operation)



(2) Read Sequence
When the Slave Address of the AK8823 Read Mode is received at the first byte, data at the second and succeeding bytes are transmitted from the AK8823.



Abbreviated Terms listed above mean :

S, rS : Start Condition
A : Acknowledge (SDA low)
Ā : Not Acknowledged (SDA high)
stp : Stop Condition
R / W : 1 : Read 0 : Write

: to be controlled by the Master Device. To be output by micro-computer normally.

: to be controlled by the Slave Device. To be output by the AK8823.

18. Register Map

Address	Register	Default	R/W	Function
0x00	Mode Register	0x00	R/W	to define input-output modes and SYNC mode.
0x01	VBI Control	0x04	R/W	to set VBI and Output clipping values
0x02	HDYPBPR Delay Register	0x00	R/W	delay amounts of HDY / HDPb / HDPr are set.
0x03	VBID (CGMS-A) Data 1 Register	0x00	R/W	CGMS-A value is set.
0x04	VBID (CGMS-A) Data 2 Register	0x00	R/W	CGMS-A value is set.
0x05	HD DAC Control Register	0x00	R/W	on / off of DACs is set.
0x06	Power down Mode Control Register	0x00	R/W	Power-down and operation modes are set.
0x07	Video Process HD Register	0x00	R/W	HD Filter setting and on / off setting of WSS.
0x08	HD WSS Data 1 Register	0x00	R/W	HD WSS Data Write register
0x09	HD WSS Data 2 Register	0x00	R/W	HD WSS Data Write register
0x0A 0x0B 0x0C 0x0D 0x0E 0x0F				
Address	Register	Default	R/W	Function
0x10	Interface Mode Register	0xa1	R/W	Video Interface mode is set.
0x11	Video Process 1 Register	0x30	R/W	specification to be displayed etc. are set.
0x12	Video Process 2 Register	0x00	R/W	Closed Caption / Extended Data / VBID setting are made.
0x13	Video Process 3 Register	0x00	R/W	Fine adjustment of SDC / SDY signal delays are set.
0x14	Video Process 4 Register	0x00	R/W	SDC / SDY Filters are set
0x15	SD DAC Control Register	0x00	R/W	on / off of DACs is set.
0x16	Reserved	0x00	R/W	write 0x00 (note)
0x17	Sub Carrier Phase Resister	0x00	R/W	Sub-carrier phase adjustment is set.
0x18	WSS Data 1 Register	0x00	R/W	SD WSS Data Write register
0x19	WSS Data 2 Register	0x00	R/W	SD WSS Data Write register
0x1A 0x1B 0x1C 0x1D 0x1E 0x1F 0x20 0x21 0x22 0x23 0x24	Reserved		R/W	Reserved
0x25	Reserved	0xA5	R/W	write 0x00 (note)
0x26	Closed Caption 1 Register	0x00	R/W	Closed Caption Data Write register
0x27	Closed Caption 2 Register	0x00	R/W	Closed Caption Data Write register
0x28	Closed Caption Extended 1 Register	0x00	R/W	Extended Data Write register
0x29	Closed Caption Extended 2 Register	0x00	R/W	Extended Data Write register
0x2A	Video ID 1 Register	0x00	R/W	Video ID Data Write register
0x2B	Video ID 2 Register	0x00	R/W	Video ID Data Write register
0x2C	Reserved	0x5A	R/W	write 0x00 (note)
0x2D 0x2E 0x2F 0x30 0x31 0x32 0x33	Reserved		R/W	Reserved
0x34	Status Register	-	R	Status Register
0x35	Device ID Register	0x23	R	Device ID Register
0x36	Device Revision Register	0x00	R	Device Revision Register

(note) when to write data , do not write other than " 0 "s.

Mode Register (R/W) [Address 0x00]

Register to set the AK8823 mode

Sub Address 0x00 < HD Block > Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDCB	HDBB	SETUP	EAVDEC	CEA861B	MODE1	MODE0	RFRSH
Default Value							
0	0	0	0	0	0	0	0

Mode Register Definition

BIT	Register Name		R/W	Definition
bit 0	RFRSH	Refresh Rate bit	R/W	to select refresh rate 0 : 60Hz 1 : 50Hz
bit1 - bit2	MODE0,1	Mode Set bit	R/W	to select input / output signals [MODE1:MODE0] 00 : 525i/625i 01 : 525p/625p 10 : 1080i 11 : 720p
bit3	CEA861B	H/V timing std	R/W	to appoint relation when to synchronize with HSYNC / VSYNC 0 : Data capture is done by the AK8823 timing. 1 : it is done by the compatible timing specified in CEA 861B. When EAVDEC is " 1 ", set CEA861B to " 0 ".
bit 4	EAVDEC	EAV decode	R/W	to select the AK8823 Sync mode 0 : to be synchronized with HSYNC / VSYNC signals 1 : to be synchronized with EAV
bit 5	HDSETUP	Setup bit	R/W	to set on / off of 7.5 % set-up 0 : no set-up process is done. 1 : set-up process is done.
bit 6	HDBB	Black Burst output bit	R/W	to output Black Burst Signal (SYNC Signal Output only) 0 : normal output 1 : Black Burst Signal Output is enabled.
bit 7	HDCB	Color Bar output bit	R/W	to output Color Bar Signal 0 : normal output 1 : Color Bar Signal is output. When HDBB bit is set, HDBB is prioritized.

Reserved Register (R/W) [Address 0x01]

Register to set VBI and Output Clipping values.

Sub Address 0x01 < HD Block > Default Value 0x04

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLPLVL_HD1	CLPLVL_HD0	Reserved	Reserved	CC_DIS	VUNMASK	VL1	VL0
Default Value							
0	0	0	0	0	1	0	0

BIT	Register Name		R/W	Definition
bit 0 ~ bit 1	VL0 - VL1	VB setting		to set Vertical Blanking Interval. The last Line during the Vertical blanking Interval can be changed, which is referenced to the initial value (20 Lines). [VL1 : VL0] – bits 01 : one line longer 00 : initial value 11 : one line shorter 10 : two lines shorter
bit 2	VUNMSK	V-Blank Un Mask bit	R/W	to set whether input data during V-Blank interval is masked or not. 0 : masked during V-Blank Interval (Black level is output). 1 : un-masked during V-Blank Interval (input data is output even during V-Blank Interval). Un-masked interval is set as follows, depending on the selected mode. 525i : 10 ~ 20 (+/_ VL [1 : 0]) Lines & 273 ~ 283 (+/- VL [1 : 0]) Lines 525p : 13 ~ 42 (+/_ VL [1 : 0]) Lines 1080i : 7 ~ 20 (+/_ VL [1 : 0]) Lines & 569 ~ 583 (+/- VL [1 : 0]) Lines 750p : 6 ~ 24 (+/_ VL [1 : 0]) Lines
bit 3	CC_DIS	Closed Caption Disable	R/W	Closed Caption Data Encoding is forced to stop. 0 : in 525i / 625i mode operation, data which is set at SD side is encoded. 1 : in 525i / 625i mode operation, data is not encoded on the Component outputs even if data encoding is set at SD side.
bit 4 ~ bit 5	Reserved	Reserved	R/W	write " 0 "
bit 6 ~ bit 7	CLPLVL_HD0 ~ CLPLVL_HD1	Clip Level bit	R/W	The under-shoot part of the Over-Sampling Filter Output is clipped to a pre-set value. 00 : no clipping 01 : to be clipped at approximately – 7.0 IRE 10 : to be clipped at approximately – 1.5 IRE 11 : reserved

HDYPBPR Delay Control Register (R/W) [Address 0x02]

Delay amounts of HDY signal and HDPb / HDPr signals are set.

Address 0x02 < HD Block > Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	HDPBPRDELAY2	HDPBPRDELAY1	HDPBPRDELAY0	Reserved	HDYDELAY2	HDYDEALY1	HDYDELAY0
Default Value							
0	0	0	0	0	0	0	0

HDY/HDPBPR Delay Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	HDYDELAY0 ~ HDYDELAY2	HDY Delay Set bits	R/W	Luminance signal delay amount is set. It is a delay from SYNC signal. Delay amount is set, based on 27 MHz clock in 480i / p modes, and 74.25 MHz clock in 1080i / 720p modes. HDPb / HDPr are handled in the same way as HDY by these bit manipulation. [HDYDELAY2 : HDYDELAY0] - bit 000 : delay amount 0 001 : 1 CLK time is delayed. 010 : 2 CLK time is delayed. 011 : 3 CLK time is delayed. 111 : 1 CLK time is advanced to output. 110 : 2 CLK time is advanced to output. 101 : 3 CLK time is advanced to output. 100 : reserved
bit 3	Reserved	Reserved bit	R/W	write " 0 ".
bit 4 ~ bit 6	HDPBPRDELAY0 ~ HDPBPRDELAY2	C Delay Set bits	R/W	Chroma signal delay amount is set. It is a delay from Luminance signal. Delay amount is set, based on 27 MHz clock in 480i/p modes, and 74.25 MHz clock in 1080i / 720p modes. Both PB/PR are delayed by the same amount, by setting Delay Amount. [HDPBPRDELAY2 : HDPBPRDELAY0] – bit 000 : delay amount 0 001 : 1 CLK time is delayed. 010 : 2 CLK time is delayed. 011 : 3 CLK time is delayed. 111 : 1 CLK time is advanced to output. 110 : 2 CLK time is advanced to output. 101 : 3 CLK time is advanced to output. 100 : reserved
bit 7	Reserved	Reserved bit	R/W	write " 0 ".

CGMS Data 1 Register (R/W) [Address 0x03]
CGMS Data 2 Register (R/W) [Address 0x04]

Registers to set VBID (CGMS-A) Data

Address 0x03 < HD Block > Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID_HD	Reserved	CGMS1	CGMS2	CGMS3	CGMS4	CGMS5	CGMS6
Default Value							
0	0	0	0	0	0	0	0

Address 0x04 < HD Block > Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CGMS7	CGMS8	CGMS9	CGMS10	CGMS11	CGMS12	CGMS13	CGMS14
Default Value							
0	0	0	0	0	0	0	0

CGMS-A Data is set. CRCC Data is automatically generated and added.

CGMS Data 1 Register Definition (Address 0x03)

BIT	Register Name		R/W	Definition
bit 0 ~ bit 5	CGMS6 ~ CGMS1	CGMS Data bit	R/W	CGMS-A Data is set which is super-imposed on Y output of HD signal. Data to be set are CGMS1 ~ CGMS6. CGMS7 ~ CGMS14 should be set at CGMS Data 2 Register
bit 6	Reserved	Reserved bit	R/W	write " 0 ".
bit 7	VBID_HD	VBID Set bit	R/W	This bit is set when CGMS-A signal is to be super-imposed on Y output of HD signal. Target Line to be super-imposed with, is automatically decided by setting [MODE1 : MODE0]-bits. 0 : CGMS-A function is " OFF ". 1 : CGMS-A signal is super-imposed.

CGMS Data 2 Register Definition (Address 0x04)

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	CGMS14 ~ CGMS7	CGMS Data bit	R/W	CGMS-A Data is set which is super-imposed on Y output of HD signal. Data to be set are CGMS7 ~ CGMS14. CGMS1 ~ CGMS6 should be set at CGMS Data 1 Register.

- About Outputting CGMS Data

Write Operation of CGMS Data via I2C interface must be completed by the time when the preceding 2 Lines are completed, from a target output Line. Each Line starts at EAV.

DAC Control Register (R/W) [Address 0x05]

Register to set on / off of DACs

Address 0x05 < HD Block > Default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HD_SINIT_N	HVINV	VPRT	Reserved	Reserved	HDPR	HDPB	HDY
Default Value							
0	0	0	0	0	0	0	0

HD DAC Control Register Definition

BIT	Register Name		R/W	Definition
bit 0	HDY	Y On/Off bit	R/W	on / off of HDY signal is set. 0 : OFF 1 : ON
bit 1	HDPB	HDPB On/Off bit	R/W	on / off of HDPB signal is set 0 : OFF 1 : ON
bit 2	HDPR	PR On/Off bit	R/W	on / off of HDPR signal is set 0 : OFF 1 : ON
bit 3 ～ bit 4	Reserved	Reserved bit	R/W	do not write other than “ 0 “s.
bit 5	VPRT	Video Input Port	R/W	Digital Video signals to be fed on HD block are set. Proper clock is automatically selected in link with this operation. 0 : HD Port 1 : SD Port
bit 6	HVINV	H/V pol select	R/W	Polarity of H / V SYNC input signals is selected. This operates on HD Block only. 0 : active low 1 : active hi
bit 7	HD_SINIT_N	HD Block soft init	R/W	to set Soft initialization of Filter in HD Block 0 : initialize 1 : release

Powerdown Mode Control Register(R/W) [Address 0x06]
Register to sets Power-Down and Operation modes of the AK8823.

Sub Address 0x06 < SD Block / HD Block > default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	PLL_SPD_N	BLKCNT1	BLKCNT0
Default Value							
0	0	0	0	0	0	0	0

Power Down Mode Control Register

BIT	Register Name		R/W	Definition
Bit0 ー Bit1	BLKCNT1,0	SD/HD BLOCK CNT	R/W	to control operation of SD / HD Blocks (digital portion) [BLKCNT1 : BLKCNT0]-bit 00 : both SD /HD Blocks are enabled. 01 : HD Block only is enabled. 10 : SD Block only is enabled. In this mode of operation, it is required to power-down DACs and PLL in the HD Block. (note 1) Refer to register setting to disable HD Block below. 11 : entire device is put into Power-Down mode (note 2).
bit2	PLL_SPD_N	PLL Power Down	R/W	to control Power-Down of PLL 0 : Power-Down 1 : release from Power-Down
bit3 ～ bit7	Reserved	Reserved bit	R/W	do not write other than “ 0 “s.

(note 1) Register setting to disable HD Block
DAC off : address 0x05 bits 2 ~ 0 [000]
PLL off : address 0x06 bit 2 [0]

(note 2) SD Port and HD Port in the Video Input block are powered-down by this setting.

Address 0x07 < HD Block >

default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
HDWSS	HDPBPRFLT1	HDPBPRFLT0	HDYFLT1	HDYFLT0	HDDFMT	Reserved	VRATIO
Default Value							
0	0	0	0	0	0	0	0

Video Process HD Register

BIT	Register Name		R/W	Definition
bit 0	VRATIO	Video ratio bit	R/W	286 / 714 Ratio Video Signal is output at D1 / 60 Hz operation. 0 : 300 / 700 Ratio Video Signal is output (770. 2-A) 1 : 286 / 714 Ratio Video Signal is output (770. 1-A)
Bit1	Reserved	Reserved bit	R/W	do not write other than “ 0 “s.
bit 2	HDDFMT	HD Data Format	R/W	HD Block Input Data Format. Available only in D1 mode. 0 : Y-Port only 1 : Y and CbCr ports (2 ports) In Either case, EAV is multiplexed in Y-Port.
Bit3 - bit4	HDYFLT0,1	HDY Filter select	R/W	to select HDY Video Signal Band Limit Filter. [HDYFLT 1 : HDYFLT 0] 00 : Normal 01 : Mild 10 : Soft 11 : inhibited
Bit5 - bit6	HDPBPRFLT0,1	HDPBPR Filter select	R/W	to select HDPBPR Video Signal Band Limit Filter [HDPBPFLT 1 : HDPBPFLT 0] 00 : Normal 01 : Mild 10 : Soft 11 : inhibited
bit 7	HDWSS	WSS set bit	R/W	to encode WSS signal It is turned on only when D1 / 50 Hz is output. 0 : WSS off 1 : WSS on

WSS Data 1 Register (R/W) [Address 0x08]
WSS Data 2 Register (R/W) [Address 0x09]

Register to set WSS Data

Sub Address 0x08 < HD Block > default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x09 default Value 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G412	G4-11	G3-10	G3-9	G3-8
Default Value							
0	0	0	0	0	0	0	0

note) WSS Data is written in order of 0x08 and then 0x09.
When the second byte (0x09) of WSS Data is written, the AK8823 interprets that Data has been up-dated and it encodes the WSS signal on the next Video Line (Line 23).
Data is retained till it is up-dated with a new one

Interface Mode Register (R/W) [Address 0x10]

Register to set the AK8823 modes

Sub Address 0x10 < SD Block > Default Value 0xa1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBLN4	SDBLN3	SDBLN2	SDBLN1	SDBLN0	Reserved	Reserved	REC656
Default Value							
1	0	1	0	0	0	0	1

Interface Mode Register Definition

BIT	Register Name		R/W	Definition
bit 0	REC656	REC656 I/F mode bit	R/W	set this bit when to synchronize with ITU-R. BT.656 (compatible) EAV. 0 : EVA is not decoded (synchronization with HSYNC / VSYNC) 1 : EVA is decoded and the timing is synchronized with it.
bit 1 ~ bit 2	Reserved	Reserved bit	R/W	do not write other than " 0 "s.
bit 3 ~ bit 7	SDBLN0 ~ SDBLN4	SD Blanking Line No.	R/W	to set Line Blanking #. At the default condition, it is set that Blanking output is made up to 20 Lines. VBID and CC settings are prioritized, though.

Video Process 1 Register (R/W) [Address 0x11]

Register to set Output signals

Sub Address 0x11 < SD Block > Default Value 0x30

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SDBBG	SDCBG	SDSETUP	SCR	VM3	VM2	VM1	VM0
Default Value							
0	0	1	1	0	0	0	0

Video Process 1 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 3	VM0 ~ VM3	Video Mode 0 Register ~ Video Mode 3 Register	R/W	[VM1:VM0]-bit 00 : 3.57954545 MHz 01 : 3.57561188 MHz 10 : 3.5820558 MHz 11 : 4.43361875 MHz [VM3:VM2]-bit 00 : 525/60 01 : 525/60 PAL (PAL-M etc.) 10 : Reserved 11 : 625/50 PAL (PAL-B,D,G,H,I,N)
bit 4	SCR	Sub Carrier Reset bit	R/W	to enable / disable Sub-carrier reset for each color sequence 0 : no sub-carrier reset is done. 1 : sub-carrier reset is enabled. NTSC : reset at every 2 Frames. PAL : reset at every 4 Frames.
bit 5	SDSETUP	Setup bit	R/W	to set the Set-Up 0 : no set-up 1 : 7.5 % set-up is added. Even when the set-up is turned on, set-up (Pedestal) is not added while Blanking Line is being output.
bit 6	SDCBG	Color Bar Generator bit	R/W	setting bit of On-Chip Color Bar 0 : input data is encoded. 1 : On-Chip Color Bar is output. When SDBBG bit is set, SDBBG is prioritized.
bit 7	SDBBG	Black Burst Generator	R/W	to output Black Burst signal 0 : input data is encoded. 1 : Black Burst signal is output. Even when SDCBG bit is set, SDBBG is prioritized.。

VM3 – VM0 settings for each Standard are as follows.

	VM3:VM0
NTSC	0000
PAL-B,D,G,H,I	1111
PAL-M	0101
PAL-60	0111
NTSC-4.43	0011

Video Process 2 Register (R/W) [Address 0x12]

Register to set output signals

Sub Address 0x12 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	WSS	CC284	CC21	VBID
Default Value							
0	0	0	0	0	0	0	0

Video Process 2 Register Definition

BIT	Register Name		R/W	Definition
bit 0	VBID	Video ID bit	R/W	to set Video ID on CVBS / Y output at SD Block 0 : Video ID off 1 : Video ID on
bit 1	CC21	Closed Caption bit	R/W	to control encoding of Closed Caption data on CVBS / Y output at SD Block When to encode it on HD Block, set " 1 " : on.。 0 : Closed caption off 1 : Closed Caption on
bit 2	CC284	Closed Caption Extended Data bit	R/W	to control encoding of Closed Caption Extended data on CVBS / Y output at SD Block When to encode it on HD Block, set " 1 " : on 0 : Extended Data off 1 : Extended data on
bit 3	WSS	WSS set bit	R/W	to control encoding of WSS signal 0 : WSS off 1 : WSS on
bit 4 ~ bit 7	Reserved	Reserved bit	R/W	do not write other than " 0 "s.

Video Process 3 Register (R/W) [Address 0x13]

Register to adjust YC Delay amount of output signals

Sub Address 0x13 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLPLVL_SD1	CLPLVL_SD0	SYD2	SYD1	SYD0	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

Video Process 3 Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 2	Reserved	Reserved bit	R/W	do not write other than “0 “ s.
bit 3 ~ bit 5	SYD0 ~ SYD2	S-video Y Delay bit	R/W	SDY and SDC signals can be output in up to +/- 3 system clock time (27 MHz) [SYD2 : SYD0] – bit 101 : SDY component output advances 3 clock time to SDC component. 110 : SDY component output advances 2 clock time to SDC component. 111 : SDY component output advances 1 clock time to SDC component. 000 : no delay between SDY component and SDC component 001 : SDY component output is delayed by 1 clock time to SDC component. 010 : SDY component output is delayed by 2 clock time to SDC component. 011 :SDY component output is delayed by 3 clock time to SDC component.
bit 6 ~ bit 7	CLPLVL_SD0 ~ CLPLVL_SD1	Clip Level bit	R/W	to clip the under-shoot of the Over-Sampling Filter Outputs to a pre-set value. 00 : no clipping 01 : to be clipped at approximately – 7.0 IRE 10 : to be clipped at approximately – 1.5 IRE 11 : reserved

Reserved Register (R/W) [Address 0x14]

Register to set SDC / SDY Filters

Address 0x14 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VPRTSD	Reserved	Reserved	SDYFLT1	SDYFLT0	Reserved	Reserved	Reserved
Default Value							
0	0	0	0	0	0	0	0

Video Process 4 Register

BIT	Register Name		R/W	Definition
bit 0 - bit 2	Reserved	Reserved bit	R/W	do not write other than " 0 "s
Bit3 - bit4	SDYFLT0,1	SDY Filter select	R/W	to set SDY Video Signal Band Limit Filter [SDYFLT 1 : SDYFLT 0] 00 : Normal 01 : Mild 10 : Soft 11 : inhibited
Bit5 - bit6	Reserved	Reserved bit	R/W	do not write other than " 0 "s
Bit 7	VPRTSD (Note)	Video Input Port SD	R/W	to set Digital Video signal which is fed to SD Block clock operation is also linked. 0 : SD Port 1 : HD Port

(Note) In case "1 : HD Port" is set, the clock in CLK_HD pin must be fed to CLK_SD pin.

DAC Control Register (R/W) [Address 0x15]

Register to control ON / OFF of Output DACs

Sub Address 0x15 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	SD_SINIT_N	Reserved	Reserved	SDC	SDY
Default Value							
0	0	0	0	0	0	0	0

SD DAC Control Register Definition

BIT	Register Name		R/W	Definition
bit 0	SDY	SDY Out bit	R/W	to control ON / OFF of SDY 0 : Off 1 : On
bit 1	SDC	SDC Out bit	R/W	to control ON / OFF of SDC 0 : Off 1 : On
bit 2 - bit 3	Reserved	Reserved bit	R/W	do not write other than " 0 "s.
bit 4	SD_SINIT_N	SD Block soft Init	R/W	to set Soft initialization of Filter in SD Block 0 : initialization 1 : release of initialization
bit 5 - bit 7	Reserved	Reserved bit	R/W	do not write other than " 0 "s.

Sub Carrier Phase Control Register (R/W) [Address 0x17]

Register to set Sub-Carrier Phase

Sub Address 0x17 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SUBP7	SUBP6	SUBP5	SUBP4	SUBP3	SUBP2	SUBP1	SUBP0
Default Value							
0	0	0	0	0	0	0	0

Sub Carrier Frequency Control Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	SUBP0 ~ SUBP7	Sub Carrier Phase control bit	R/W	to set default value of sub-carrier phase Adjustable step : 360 / 255 [deg.] Sub-Carrier Phase is set at - 180 degrees at default condition. Phase rotates counter-clockwise to the set value.

WSS Data 1 Register (R/W) [Address 0x18]
WSS Data 2 Register (R/W) [Address 0x19]

Register to set WSS Data

Sub Address 0x18 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
G2-7	G2-6	G2-5	G2-4	G1-3	G1-2	G1-1	G1-0
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x19 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	G4-13	G412	G4-11	G3-10	G3-9	G3-8
Default Value							
0	0	0	0	0	0	0	0

note) WSS Data is written in order of 0x18 and then 0x19.
When the second byte (0x19) of WSS Data is written, the AK8823 interprets that Data has been up-dated and it encodes the Data on the next Video Line (Line 23).
Data is retained till it is up-dated with a new one.

Closed Caption Data 1 Register (R/W) [Address 0x26]
Closed Caption Data 2 Register (R/W) [Address 0x27]

Register to set Closed Caption Data (SD). It is also possible to output same data on HD side.

Sub Address 0x26 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x27 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8
Default Value							
0	0	0	0	0	0	0	0

note) Closed Caption Data is written in order of 0x26 and then 0x27.
When the second byte (0x27) of Closed Caption Data is written, the AK8823 interprets that Data has been up-dated and it encodes the Data on the next Video Line.
Null Codes are automatically output on those, not-data-updated lines.
It is assumed that Parity bit of each Byte Data is added by the Host side.

Closed Caption Extended Data 1 Register (R/W) [Address 0x28]
Closed Caption Extended Data 2 Register (R/W) [Address 0x29]

Register to set Closed Caption Extended Data (SD). It is also possible to output same data on HD side.

Sub Address 0x28 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	EXT0
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x29 < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EXT15	EXT14	EXT13	EXT12	EXT11	EXT10	EXT9	EXT8
Default Value							
0	0	0	0	0	0	0	0

note) Closed Caption Extended Data is written in order of 0x28 and then 0x29.
When the second byte (0x29) of Closed Caption Extended Data is written, the AK8823 interprets that Data has been up-dated and it encodes the Data on the next Video Line.
Null Codes are automatically output on those, not-data-updated lines.
It is assumed that parity bit of each Byte Data is added by the Host side.

Video ID 1 Register (R/W) [Address 0x2A] < SD Block >
Video ID 2 Register (R/W) [Address 0x2B] < SD Block >

Register to set VIDEO ID Data. Data can be super-imposed on CVBS / Y signal of SD Block.

Sub Address 0x2A < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	VBID1	VBID2	VBID3	VBID4	VBID5	VBID6
Default Value							
0	0	0	0	0	0	0	0

Sub Address 0x2B < SD Block > **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VBID7	VBID8	VBID9	VBID10	VBID11	VBID12	VBID13	VBID14
Default Value							
0	0	0	0	0	0	0	0

note) write " 0 "s to reserved bits.
VBID1 ---- VBID14 correspond to bit 1 ---- bit 14 which are described at { VBID Data Code Assignment } diagram at item { 16-3. Video ID }.
A 6 Bit CRC Code from bit 15 ~ bit 20 is automatically added by the AK8823.
Data is retained till it is up-dated with a new one.

Status Register (R) [Address 0x34]

Register to show Status of the AK8823

Sub Address 0x34 < SD Block >

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN284	EN21

Status Register Definition

BIT	Register Name		R/W	Definition
bit 0	EN21	Encode 21 bit	R	to indicate up-date timing of the Closed-Caption Data When EN21 bit is " 1 ", the AK8823 waits for data input coming. This bit becomes " 0 " after data is written at the second byte (0x27).
bit 1	EN284	Encode 284 bit	R	to indicate up-date timing of the Closed-Caption Extended Data When EN284 bit is " 1 ", the AK8823 waits for data input coming. This bit becomes " 0 " after data is written at the second byte (0x29).
bit 2 ~ bit 7	Reserved	Reserved bit	R	do not write other than " 0 "s.

Device ID Register (R) [Address 0x35]

Register to indicate the AK8823 Device ID

Sub Address 0x35 **default Value 0x23**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0
0	0	1	0	0	0	1	1

Device ID Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	DEV0 ~ DEV7	Device ID bit	R	to indicate Device ID 0x23 is assigned to the AK8823.

Revision ID Register (R) [Address 0x36]

Register to indicate the AK8823 Revision ID

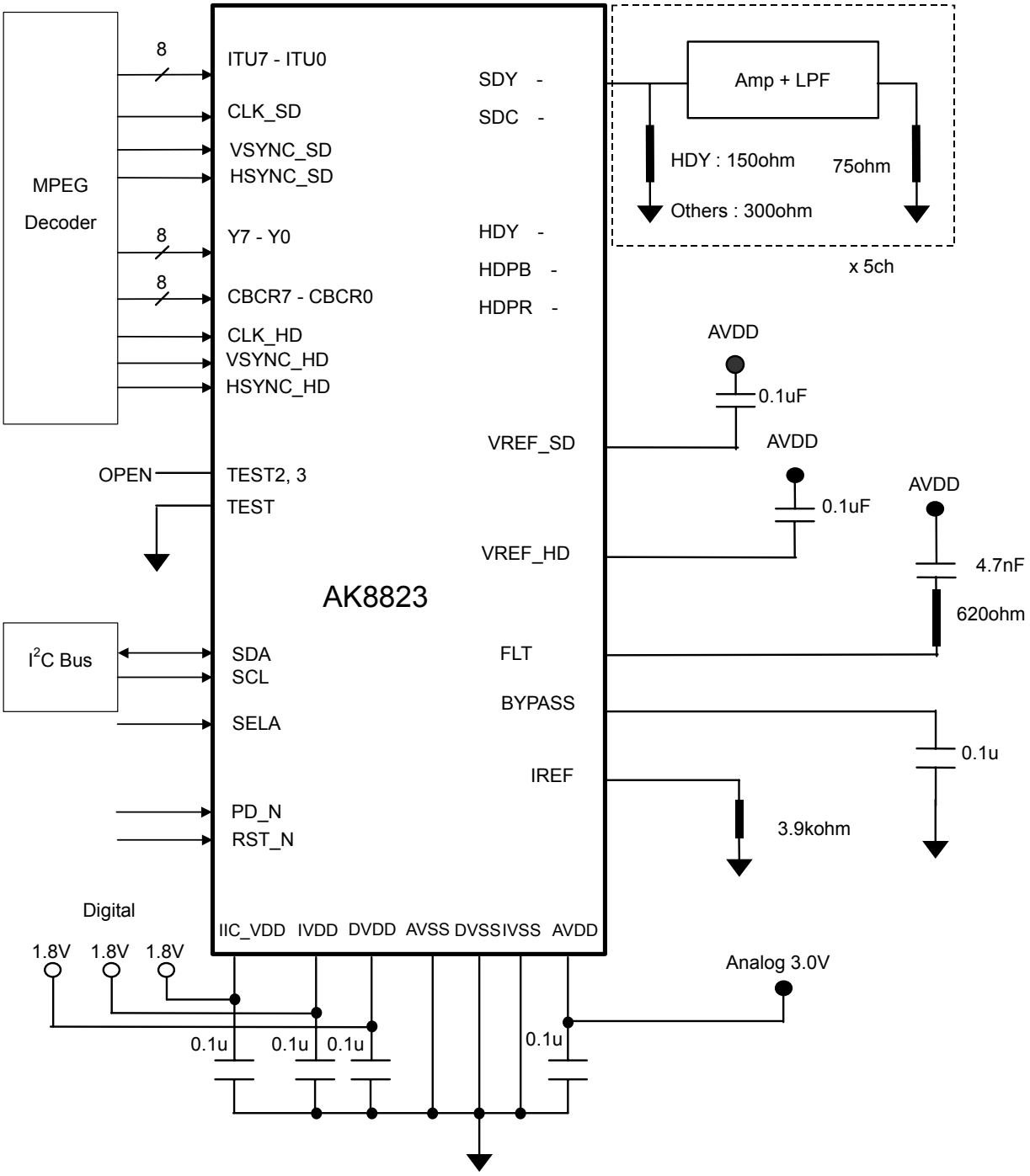
Sub Address 0x36 **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
0	0	0	0	0	0	0	0

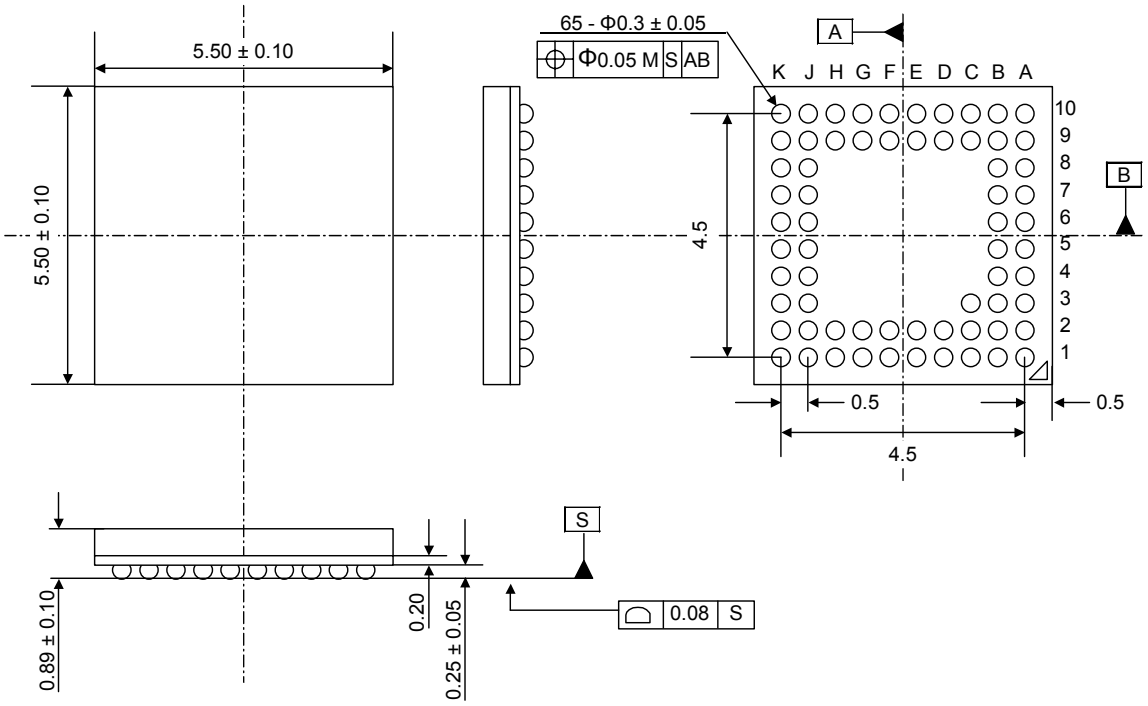
Revision ID Register Definition

BIT	Register Name		R/W	Definition
bit 0 ~ bit 7	REV0 ~ REV2	Revision ID bit	R	to indicate Revision ID. Revision ID is up-dated when a possible software modification is made. It starts at 0x00.

19. System Connection Example

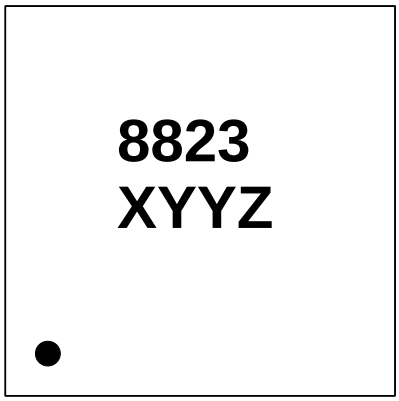


20. Package Outline Dimensions



21. Package Marking

(1) Pin Type : BGA
(2) Pin Count : 65 pins
(3) Product Number : 8823
(4) Control Code : XYYZ (4 digits)
X : Year Number (lowest, single digit)
YY : Week Number
Z : Lot Number in a same week



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