

PLL0305A

Serial Input PLL Frequency Synthesizer

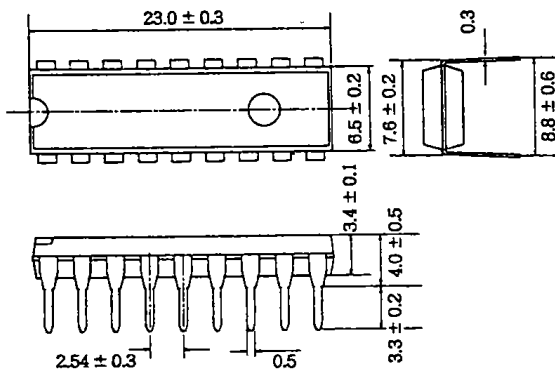
VIEW

PLL0305A is a PLL synthesizer LSI fabricated using NPC's original molybdenum-gate CMOS technology. The input frequency divider ratio can be set by externally inputting serial data. The output frequency divider ratio can be selected from 8 choices stored in the built-in ROM.

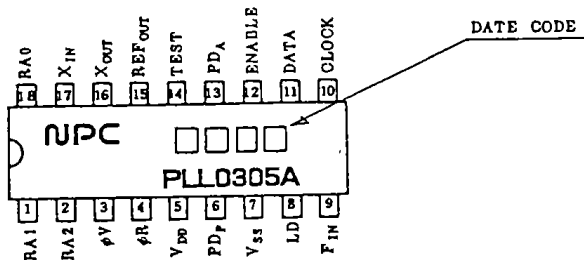
FEATURES

- 100 MHz (5 V, F_{IN})
- 100 MHz (5 V, X_{IN})
- Reference frequency
- Divider ratios: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Output frequency divider ratios: 5 to 16383
- Lock detector pin
- Can be used with active or passive filters

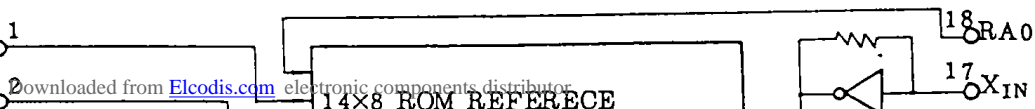
PACKAGE DIMENSIONS Unit: mm



PINOUT TOP VIEW



BLOCK DIAGRAM



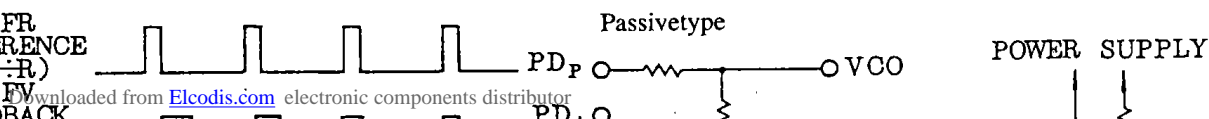
PLL0305A

FUNCTION DESCRIPTION

NAME (No.)	DESCRIPTION																																				
<table border="1"> <thead> <tr> <th>RA2</th> <th>RA1</th> <th>RA0</th> <th>Divider ratio</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>16</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>512</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1024</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>2048</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>3668</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>4096</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>6144</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>8192</td> </tr> </tbody> </table>	RA2	RA1	RA0	Divider ratio	0	0	0	16	0	0	1	512	0	1	0	1024	0	1	1	2048	1	0	0	3668	1	0	1	4096	1	1	0	6144	1	1	1	8192	<p>Input pins used to select the reference frequency divider ratio from the table.</p>
RA2	RA1	RA0	Divider ratio																																		
0	0	0	16																																		
0	0	1	512																																		
0	1	0	1024																																		
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<p>CLOCK (10)</p> <p>DATA (11)</p>	<p>Shift register data and clock input. Data shifts by 1 bit when CLOCK changes from "L" to "H".</p> <p>The shift register configuration is shown below.</p> <p>Make the input data format coincide with the shift register configuration.</p>																																				
<p>ENABLE (12)</p>	<p>Latch write signal. When "H", writing is enabled. Internal pull-up resistor.</p>																																				
<p>TEST (14)</p>	<p>Test pin. Should be left open during normal operation. Internal pull-down resistor.</p>																																				
<p>REF_{OUT} (15)</p>	<p>Buffered reference oscillator (X_{IN}, X_{OUT}) output. Recommend to connect a load to this pin for stable oscillation.</p>																																				
<p>X_{OUT} (16)</p> <p>X_{IN} (17)</p>	<p>Pin for a quartz crystal oscillator. Internal feedback resistor is provided for AC coupling. Input an external clock to the X_{IN} pin via a capacitor.</p>																																				
<p>Power supply 4.5 to 5.5 V</p>																																					
<p>Ground</p>																																					
<p>Unlock detection. When unlocked, it is "L." When locked, it is "H."</p>																																					
<p>Input frequency divider (N COUNTER) input. Internal feedback resistor for AC coupling.</p>																																					

PHASE DETECTOR TIMING CHART

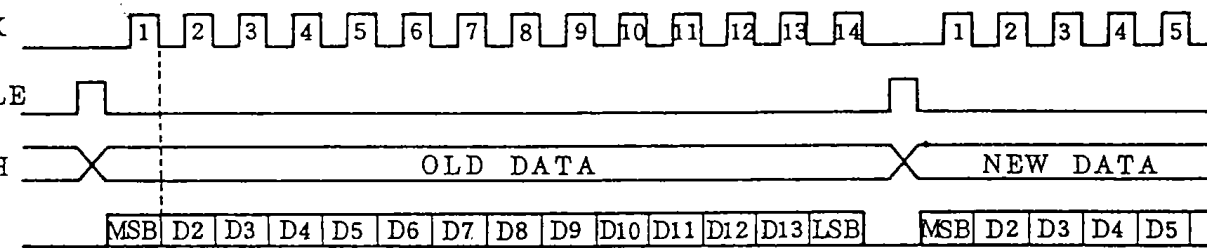
■ LOWPASS FILTER



PLL0305A

TIMING CHART

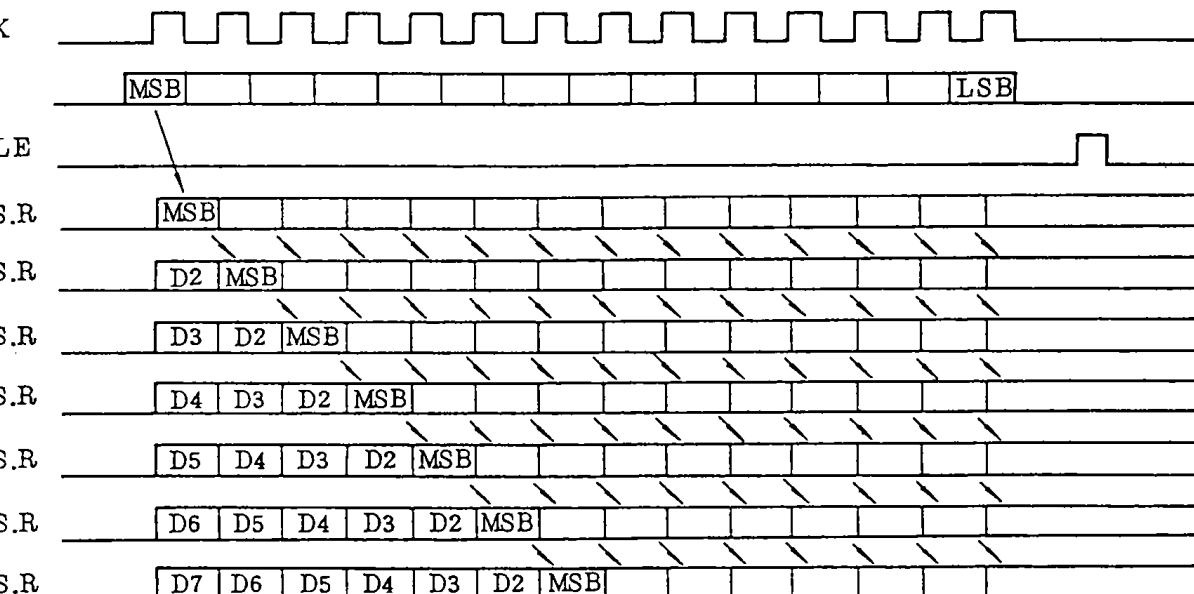
Input frequency divider data setting



Input data MSB first.

Data is input on the rising edge of CLOCK, so it is necessary to change data on the falling edge of CLOCK.

While the ENABLE signal is "H", data is transferred from the shift register to the input frequency divider's latch. Therefore, ENABLE must go "L" while data is being written into the shift register.



PLL0305A

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply voltage	$V_{DD}-V_{SS}$	-0.3 to +7.0	V
Input voltage	V_{IN}	$V_{SS}-3.0$ to $V_{DD}+0.3$	V
Operating temperature	T_{OPR}	-30 to +80	°C
Storage temperature	T_{STG}	-40 to +125	°C
Soldering temperature	T_{SLD}	260±5	°C
Soldering time	t_{SLD}	10	Sec

Setup time, hold time

ELECTRICAL CHARACTERISTICS

$V_{SS} = 0V, V_{DD} = 4.5$ to $5.5V, T_a = -30$ to $+80\text{ °C}$

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT	REMARKS
			MIN	TYP	MAX		
Supply voltage	V_{DD}		4.5		5.5	V	
Current consumption	I_{DD}	F_{IN} =sine wave 30MHz 500mV _{p-p} X_{IN} =sine wave 15MHz 1V _{p-p}		4.0	8.0	mA	* Output pin open
Maximum operating frequency 1	F_{MAX1}	F_{IN} =sine wave 500mV _{p-p}	30	50		MHz	F_{IN}
Maximum operating frequency 2	F_{MAX2}	X_{IN} =sine wave 1V _{p-p}	15	50		MHz	X_{IN}
Input voltage	V_{INAC}	F_{IN} =AC coupling X_{IN} =AC coupling	0.5 1.0		$V_{DD}-0.5$ $V_{DD}-0.5$	V	F_{IN} X_{IN}
Input voltage	V_{IH} V_{IL}		$V_{DD}-0.3$ 0		V_{DD} 0.5	V	RA0 to RA2DAT, CLK, LE
Input current 1	I_{IH1} I_{IL1}	$V_{IH1}=V_{DD}$ $V_{IL1}=0V$			15 15	µA	F_{IN}, X_{IN}
Input current 2	I_{IL2}	$V_{IL2}=0V$			30	µA	ENABLE
Input current 3	I_{IH3} I_{IL3}	$V_{IH3}=V_{DD} \quad T_a=25\text{ °C}$ $V_{IL3}=0V \quad T_a=25\text{ °C}$		0.001	0.1 0.1	µA	RA0 to RA2DAT, CLK
Output current	I_{OH} I_{OL}	$V_{OH}=V_{DD}-0.4V$ $V_{OL}=0.4V$	0.4 0.4			µA	øV, øR, PDP PDA, REFOUT
Output leak current	I_{LH} I_{LL}	$V_{LH}=V_{DD} \quad T_a=25\text{ °C}$ $V_{LL}=0V \quad T_a=25\text{ °C}$		0.001	0.1 0.1	µA	PDP PDA