National Semiconductor

PRELIMINARY
September 2006

DS90UR241/DS90UR124
5-43 MHz DC-Balanced 24-Bit LVDS Serializer and Deserializer

General Description

The DS90UR241/124 Chipset translates a 24-bit parallel bus into a fully transparent data/control LVDS serial stream with embedded clock information. This single serial stream simplifies transferring a 24-bit bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

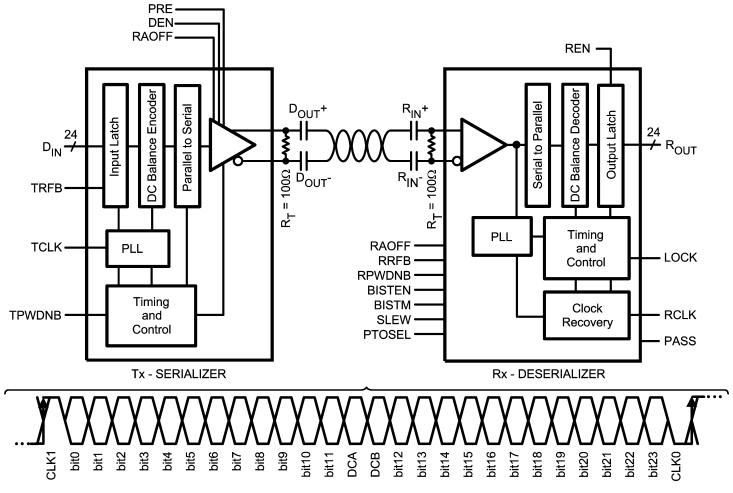
The DS90UR241/124 incorporates LVDS signaling on the high-speed I/O. LVDS provides a low power and low noise environment for reliably transferring data over a serial transmission path. By optimizing the Serializer output edge rate for the operating frequency range EMI is further reduced.

In addition the device features pre-emphasis to boost signals over longer distances using lossy cables. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects. Using National Semiconductor's proprietary random lock, the Serializer's parallel data are randomized to the Deserializer without the need of REFCLK.

Features

- 5 MHz–43 MHz embedded clock and DC-Balanced 24:1 and 1:24 data transmission
- User defined pre-emphasis driving ability through external resistor on LVDS outputs and capable to drive up to 10 meters shielded twisted-pair cable
- User selectable clock edge for parallel data on both Transmitter and Receiver
- Supports AC-coupling data transmission
- Individual power-down controls for both Transmitter and Receiver
- 1.8V V_{CM} at LVDS input side
- Embedded clock CDR (clock and data recovery) on Receiver and no source of reference clock needed
- All codes RDL (random data lock) to support hot-pluggable applications
- LOCK output flag to ensure data integrity at Receiver side
- Balanced T_{SETUP}/T_{HOLD} between RCLK and RDATA on Receiver side
- Adjustable PTO (progressive turn-on) LVCMOS outputs on Receiver to minimize EMI and SSO effects
- @Speed BIST to validate link integrity
- All LVCMOS inputs and control pins have internal pulldown
- On-chip filters for PLLs on Transmitter and Receiver
- 48-pin TQFP package for Transmitter and 64-pin TQFP package for Receiver
- Pure CMOS .35 µm process
- Power supply range 3.3V ± 10%
- Temperature range −40˚C to +105˚C
- Greater than 8 kV HBM ESD structure
- Meets ISO 10605 ESD compliance
- Backwards compatible with DS90C241/DS90C124

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage	−0.3V to (V_{DD} +0.3V)
LVCMOS/LVTTL Output Voltage	−0.3V to (V_{DD} +0.3V)
LVDS Receiver Input Voltage	−0.3V to +3.9V
LVDS Driver Output Voltage	−0.3V to +3.9V
LVDS Output Short Circuit Duration	10 ms
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 seconds)	+260˚C
Maximum Package Power Dissipation Capacity	
Package De-rating:	$1/\theta_{JA}$ ˚C/W above +25˚C
DS90UR241 – 48L TQFP	
θ_{JA}	45.8 (4L*); 75.4 (2L*) ˚C/W
θ_{JC}	21.0˚C/W
DS90UR124 – 64L TQFP	
θ_{JA}	42.8 (4L*); 67.2 (2L*)˚C/W
θ_{JC}	14.6˚C/W
	**JEDEC*
ESD Rating (HBM)	>8 kV
ESD Rating (ISO10605)	
R_D = 2 kΩ, C_S = 330 pF	DS90UR241 meets ISO 10605
Contact Discharge (D_{OUT+}, D_{OUT-}) to GND	±10 kV
Air Discharge (D_{OUT+}, D_{OUT-}) to GND	±30 kV
R_D = 2 kΩ, C_S = 330 pF	DS90UR124 meets ISO 10605
Contact Discharge (R_{IN+}, R_{IN-}) to GND	±10 kV
Air Discharge (R_{IN+}, R_{IN-}) to GND	±30 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DD})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+105	˚C
Clock Rate	5		43	MHz
Supply Noise			±100	mV_{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage		**Tx:** D_{IN}[0:23], TCLK, TPWDNB, DEN, TRFB, RAOFF, RESVRD. **Rx:** RPWDNB, RRFB, REN, PTOSEL, BISTEN, BISTM, SLEW, RESVRD.	2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.8	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V	**Tx:** D_{IN}[0:23], TCLK, TPWDNB, DEN, TRFB, RAOFF, RESVRD. **Rx:** RRFB, REN, PTOSEL, BISTEN, BISTM, SLEW, RESVRD.	−10	±2	+10	µA
			Rx: RPWDNB	−20	±5	+20	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA	**Rx:** R_{OUT}[0:23], RCLK, LOCK, PASS.	2.3	3.0	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +2 mA, SLEW = L I_{OL} = +4 mA, SLEW = H		GND	0.33	0.5	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−40	−70	−110	mA
I_{OZ}	TRI-STATE® Output Current	RPWDNB, REN = 0V, V_{OUT} = 0V or V_{DD}	**Rx:** R_{OUT}[0:23], RCLK, LOCK, PASS.	−30	±0.4	+30	µA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVDS DC SPECIFICATIONS							
V_{TH}	Differential Threshold High Voltage	V_{CM} = +1.8V	**Rx:** R_{IN+}, R_{IN-}			+100	mV
V_{TL}	Differential Threshold Low Voltage			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{DD} = 3.6V or 0V			±100	±250	µA
		V_{IN} = 0V, V_{DD} = 3.6V or 0V			±100	±250	µA
V_{OD}	Output Differential Voltage (D_{OUT+})−(D_{OUT-})	R_L = 100Ω, w/o pre-emphasis	**Tx:** D_{OUT+}, D_{OUT-}	300	500	700	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω, w/o pre-emphasis			1	50	mV
V_{OS}	Offset Voltage	R_L = 100Ω, w/o pre-emphasis		1.00	1.25	1.50	V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω, w/o pre-emphasis			3	50	mV
I_{OS}	Output Short Circuit Current	D_{OUT} = 0V, D_{IN} = H, TPWDNB = 2.4V		−2.0		−8.0	mA
I_{OZ}	TRI-STATE Output Current	TPWDNB = 0V, D_{OUT} = 0V OR V_{DD}		−15	±1	15	µA
		TPWDNB = 2.4V, DEN = 0V D_{OUT} = 0V OR V_{DD}		−15	±1	15	µA
		TPWDNB = 2.4V, DEN = 2.4V, D_{OUT} = 0V OR V_{DD} NO LOCK (NO TCLK)		−15	±1	15	µA
SER/DES SUPPLY CURRENT (DVDD*, PVDD* AND AVDD* PINS) *DIGITAL, PLL, AND ANALOG VDDS*							
I_{DDT}	Serializer Total Supply Current (includes load current)	R_L = 100Ω, PRE = OFF, RAOFF = H	f = 43 MHz, CHECKER BOARD Pattern *(Figure 1)*		60	85	mA
		R_L = 100Ω, PRE = 12 kΩ, RAOFF = H			65	90	mA
I_{DDTZ}	Serializer Supply Current Power-down	TPWDNB = 0V			200	800	µA
I_{DDR}	Deserializer Total Supply Current (includes load current)	C_L = 4 pF, SLEW = H/L	f = 43 MHz, CHECKER BOARD Pattern LVCMOS/LVTTL Output *(Figure 2)*			95	mA
		C_L = 4 pF, SLEW = H/L	f = 43 MHz, RANDOM pattern LVTTL Output			90	mA
I_{DDRZ}	Deserializer Supply Current Power-down	RPWDNB = 0V			200	800	µA

Serializer Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	*(Figure 6)*	23.25	T	200	ns
t_{TCIH}	Transmit Clock High Time		0.3T	0.5T	0.7T	ns
t_{TCIL}	Transmit Clock Low Time		0.3T	0.5T	0.7T	ns
t_{CLKT}	TCLK Input Transition Time	*(Figure 5)*		2.5		ns
t_{JIT}	TCLK Input Jitter	(Note 8)			±100	ps

Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LLHT}	LVDS Low-to-High Transition Time	R_L = 100Ω, C_L = 10 pF to GND, *(Figure 3)*		245	550	ps
t_{LHLT}	LVDS High-to-Low Transition Time			264	550	ps
t_{DIS}	D_{IN} (0:23) Setup to TCLK	R_L = 100Ω, C_L = 10 pF to GND, (Note 7), *(Figure 6)*	4			ns
t_{DIH}	D_{IN} (0:23) Hold from TCLK		4			ns
t_{HZD}	D_{OUT} ± HIGH to TRI-STATE Delay	R_L = 100Ω, C_L = 10 pF to GND, (Note 4), *(Figure 7)*		10	15	ns
t_{LZD}	D_{OUT} ± LOW to TRI-STATE Delay			10	15	ns
t_{ZHD}	D_{OUT} ± TRI-STATE to HIGH Delay			75	150	ns
t_{ZLD}	D_{OUT} ± TRI-STATE to LOW Delay			75	150	ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω			10	ms
t_{SD}	Serializer Delay	R_L = 100Ω, PRE = OFF, RAOFF = L, TRFB = H, *(Figure 9)*	3.5T+2		3.5T+10	ns
		R_L = 100Ω, PRE = OFF, RAOFF = L, TRFB = L, *(Figure 9)*	3.5T+2		3.5T+10	ns
TxOUT_E_O	**TxOUT_E**ye_**O**pening. TxOUT_E_O centered on (tBIT/)2	5 MHz–43 MHz, (Notes 8, 9, 12), *(Figure 15)*		0.80		UI

Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	**R**eceiver out **C**lock **P**eriod	t_{RCP} = t_{TCP}, PTOSEL = H *(Figure 11)*	RCLK	23.25		200	ns
t_{RDC}	**R**CLK **D**uty **C**ycle	PTOSEL = H *(Figure 11)*	RCLK	45	50	55	%
t_{CLH}	LV**C**MOS/LVTTL **L**ow-to-**H**igh Transition Time	C_L = 4 pF (lumped load), SLEW = H	R_{OUT} [0:23], RCLK, LOCK			2.5	ns
t_{CHL}	LV**C**MOS/LVTTL **H**igh-to-**L**ow Transition Time					2.5	ns
t_{CLH}	LV**C**MOS/LVTTL **L**ow-to-**H**igh Transition Time	C_L = 4 pF (lumped load), SLEW = L	R_{OUT} [0:23], RCLK, LOCK			3.5	ns
t_{CHL}	LV**C**MOS/LVTTL **H**igh-to-**L**ow Transition Time					3.5	ns

Deserializer Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{ROS}	**R**$_{OUT}$ (0:7) **S**etup Data to RCLK (Group 1)	PTOSEL = L, *(Figure 12)*	R_{OUT}[0:7]	(0.35)* t_{RCP}	(0.5*t_{RCP})–3 UI		ns
t_{ROH}	**R**$_{OUT}$ (0:7) **H**old Data to RCLK (Group 1)			(0.35)* t_{RCP}	(0.5*t_{RCP})–3 UI		ns
t_{ROS}	**R**$_{OUT}$ (8:15) **S**etup Data to RCLK (Group 2)		R_{OUT} [8:15], LOCK	(0.35)* t_{RCP}	(0.5*t_{RCP})–3 UI		ns
t_{ROH}	**R**$_{OUT}$ (8:15) **H**old Data to RCLK (Group 2)			(0.35)* t_{RCP}	(0.5*t_{RCP})–3 UI		ns
t_{ROS}	**R**$_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)		R_{OUT} [16:23]	(0.35)* t_{RCP}	(0.5*t_{RCP})–3 UI		ns
t_{ROH}	**R**$_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)			(0.35)* t_{RCP}	(0.5*t_{RCP})–3 UI		ns
t_{ROS}	**R**$_{OUT}$ (0:7) **S**etup Data to RCLK (Group 1)	PTOSEL = H, *(Figure 11)*	R_{OUT}[0:7]	(0.35)* t_{RCP}	(0.5*t_{RCP})–2 UI		ns
t_{ROH}	**R**$_{OUT}$ (0:7) **H**old Data to RCLK (Group 1)			(0.35)* t_{RCP}	(0.5*t_{RCP})+2 UI		ns
t_{ROS}	**R**$_{OUT}$ (8:15) **S**etup Data to RCLK (Group 2)		R_{OUT} [8:15], LOCK	(0.35)* t_{RCP}	(0.5*t_{RCP})–1 UI		ns
t_{ROH}	**R**$_{OUT}$ (8:15) **H**old Data to RCLK (Group 2)			(0.35)* t_{RCP}	(0.5*t_{RCP})+1 UI		ns
t_{ROS}	**R**$_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)		R_{OUT} [16:23]	(0.35)* t_{RCP}	(0.5*t_{RCP})+1 UI		ns
t_{ROH}	**R**$_{OUT}$ (16:23) **S**etup Data to RCLK (Group 3)			(0.35)* t_{RCP}	(0.5*t_{RCP})–1 UI		ns
t_{HZR}	**H**IGH to TRI-STATE Delay	PTOSEL = H, *(Figure 13)*	R_{OUT} [0:23], RCLK, LOCK		3	10	ns
t_{LZR}	**L**OW to TRI-STATE Delay				3	10	ns
t_{ZHR}	TRI-STATE to **H**IGH Delay				3	10	ns
t_{ZLR}	TRI-STATE to **L**OW Delay				3	10	ns
t_{DD}	**D**eserializer **D**elay	PTOSEL = H, *(Figure 10)*	RCLK		[5+(5/56)]T+3.7	[5+(5/56)]T +8	ns
t_{DSR}	Deserializer PLL Lock Time from Powerdown	(Notes 5, 7)	5 MHz			128k*T	ms
			43 MHz			128k*T	ms
RxIN_TOL-L	**R**eceiver **IN**put **TOL**erance **L**eft	(Notes 6, 9), *(Figure 16)*	5 MHz–43 MHz	0.25			UI
RxIN_TOL-R	**R**eceiver **IN**put **TOL**erance **R**ight	(Notes 6, 9), *(Figure 16)*	5 MHz–43 MHz	0.25			UI

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Typical values are given for V_{DD} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.

Note 4: When the Serializer output is tri-stated, the Deserializer will lose PLL lock. Resynchronization MUST occur before data transfer.

Note 5: t_{DSR} is the time required by the Deserializer to obtain lock when exiting powerdown mode.

Note 6: RxIN_TOL is a measure of how much phase noise (jitter) the Deserializer can tolerate in the incoming data stream before bit errors occur. It is a measurement in reference with the ideal bit position, please see National's AN-1217 for detail.

Note 7: Guaranteed by Design (GBD) using statistical analysis.

Note 8: t_{JIT} (@BER of 10e-9) specifies the allowable jitter on TCLK. t_{JIT} not included in TxOUT_E_O parameter.

Note 9: UI – Unit Interval, equivalent to one ideal serialized data bit width. The UI scales with frequency.

Note 10: *Figures 1, 2, 9, 10, 14* show a falling edge data strobe (TCLK IN/RCLK OUT).

Note 11: *Figures 6, 11, 12* show a rising edge data strobe (TCLK IN/RCLK OUT).

Note 12: TxOUT_E_O is affected by pre-emphasis value.

AC Timing Diagrams and Test Circuits

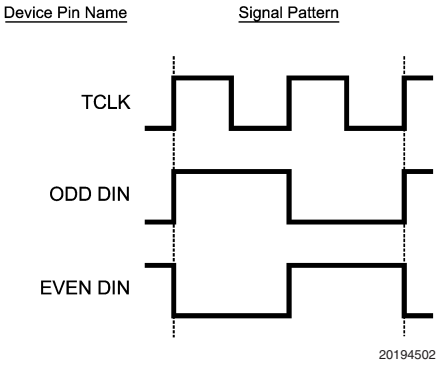


FIGURE 1. Serializer Input Checkerboard Pattern

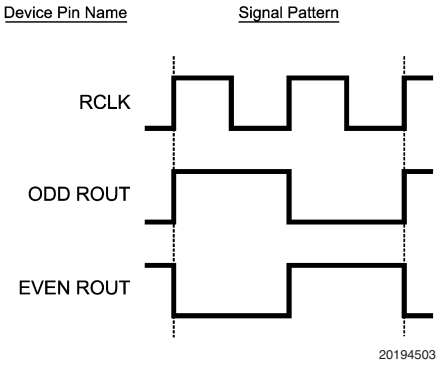


FIGURE 2. Deserializer Output Checkerboard Pattern

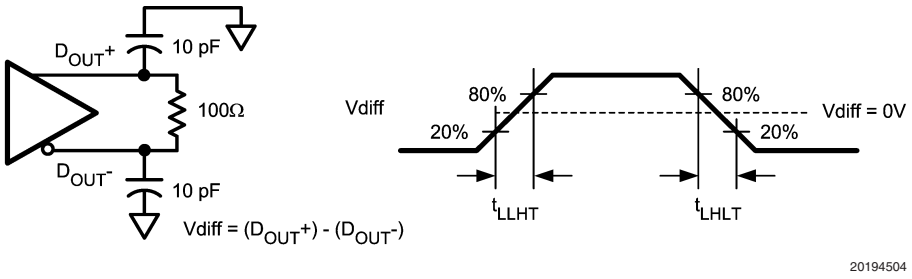


FIGURE 3. Serializer LVDS Output Load and Transition Times

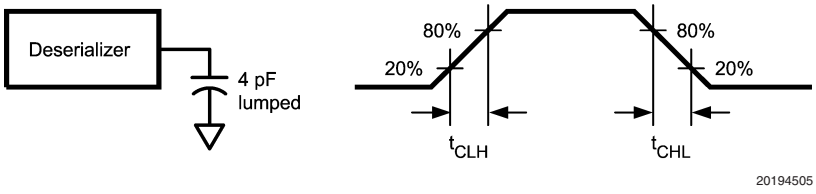


FIGURE 4. Deserializer LVCMOS/LVTTL Output Load and Transition Times

AC Timing Diagrams and Test Circuits (Continued)

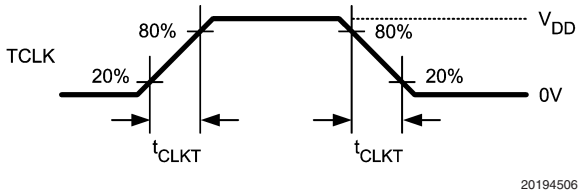


FIGURE 5. Serializer Input Clock Transition Times

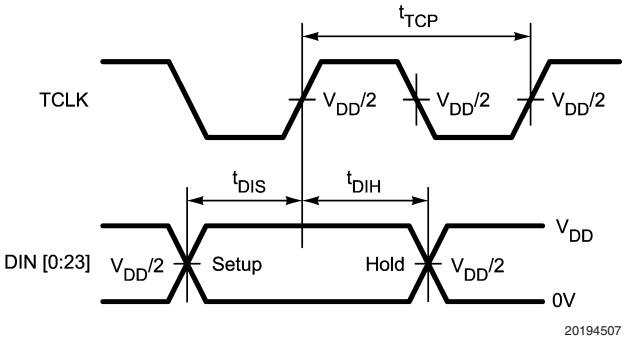


FIGURE 6. Serializer Setup/Hold Times

AC Timing Diagrams and Test Circuits (Continued)

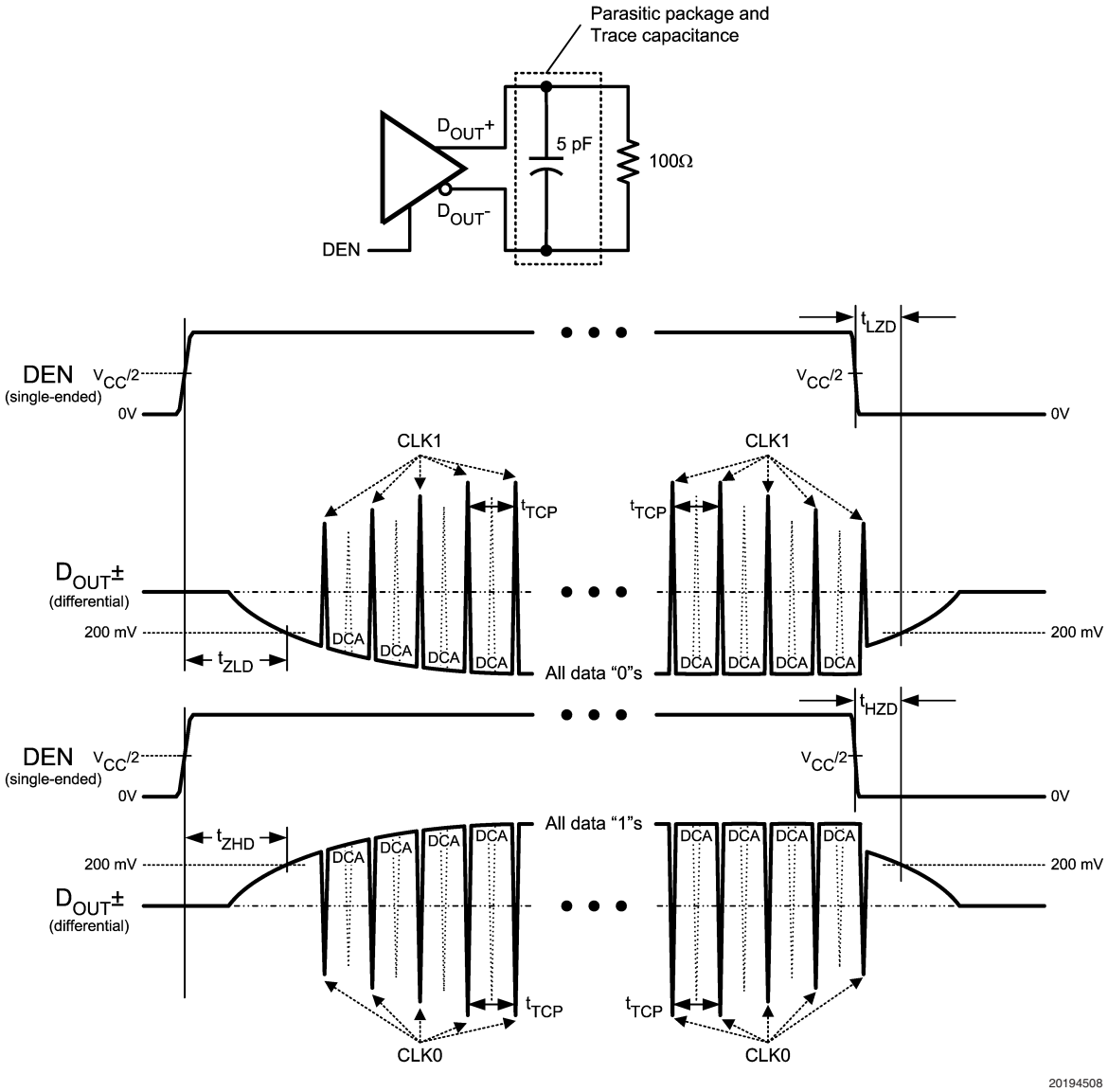


FIGURE 7. Serializer TRI-STATE Test Circuit and Delay

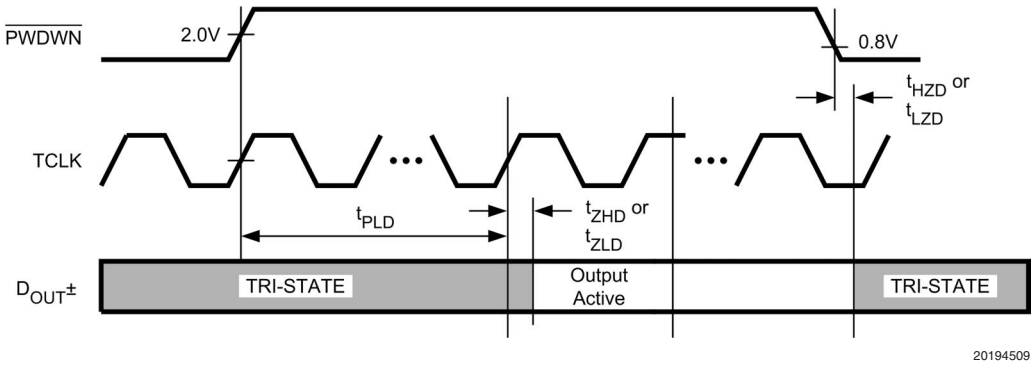


FIGURE 8. Serializer PLL Lock Time, and TPWDNB TRI-STATE Delays

AC Timing Diagrams and Test Circuits (Continued)

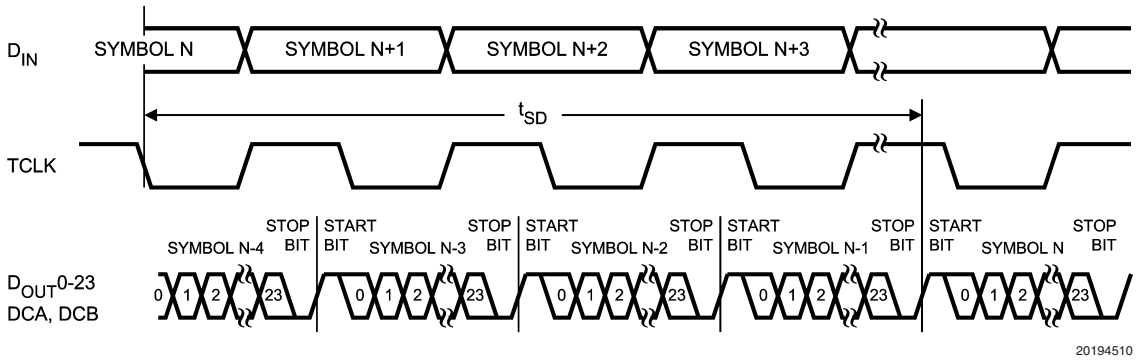


FIGURE 9. Serializer Delay

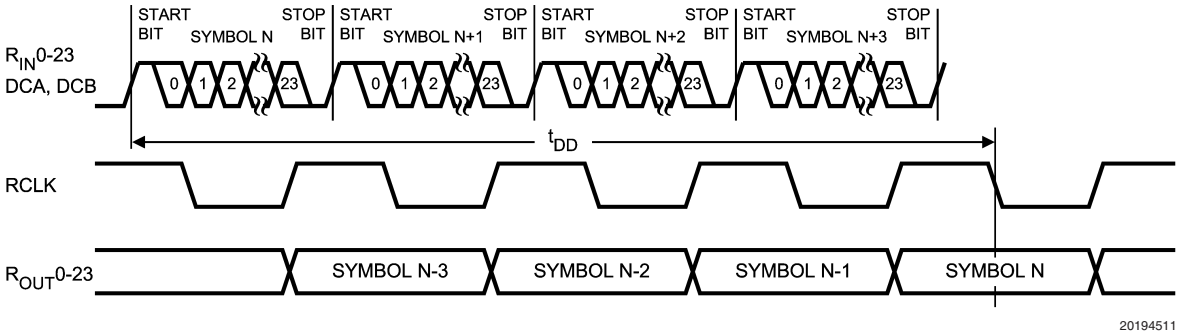


FIGURE 10. Deserializer Delay

AC Timing Diagrams and Test Circuits (Continued)

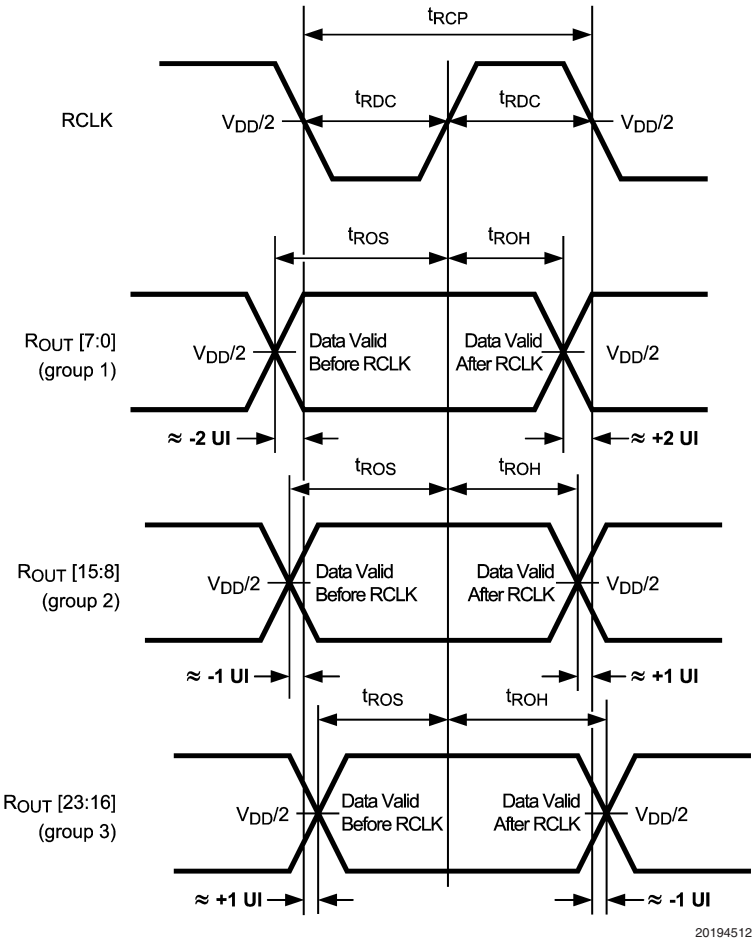
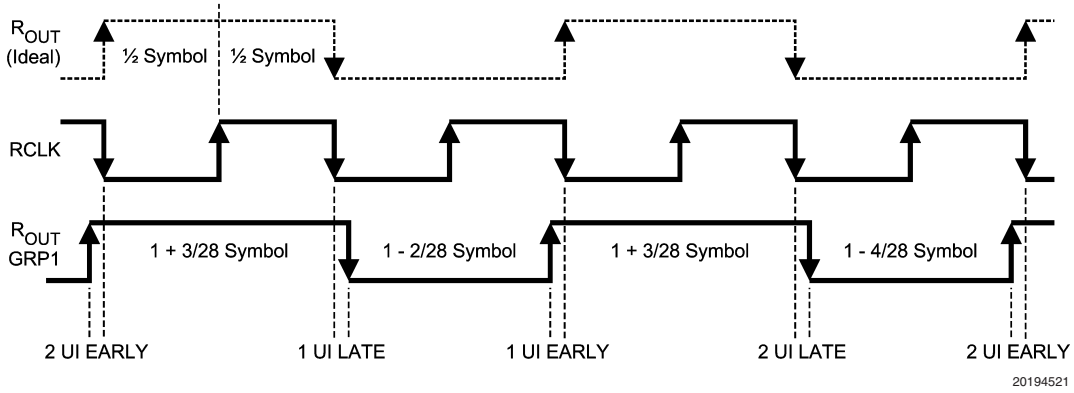


FIGURE 11. Deserializer Setup and Hold Times and PTO, PTOSEL = H



Group 1 will be latched internally by sequence of (early 2UI, late 1UI, early 1UI, late 2UI)
Group 2 will be latched internally by sequence of (late 1UI, early 1UI, late 2UI, early 2UI)
Group 3 will be latched internally by sequence of (early 1UI, late 2UI, early 2UI, late 1UI)

FIGURE 12. Deserializer Setup and Hold Times and PTO Spread, PTOSEL = L

AC Timing Diagrams and Test Circuits (Continued)

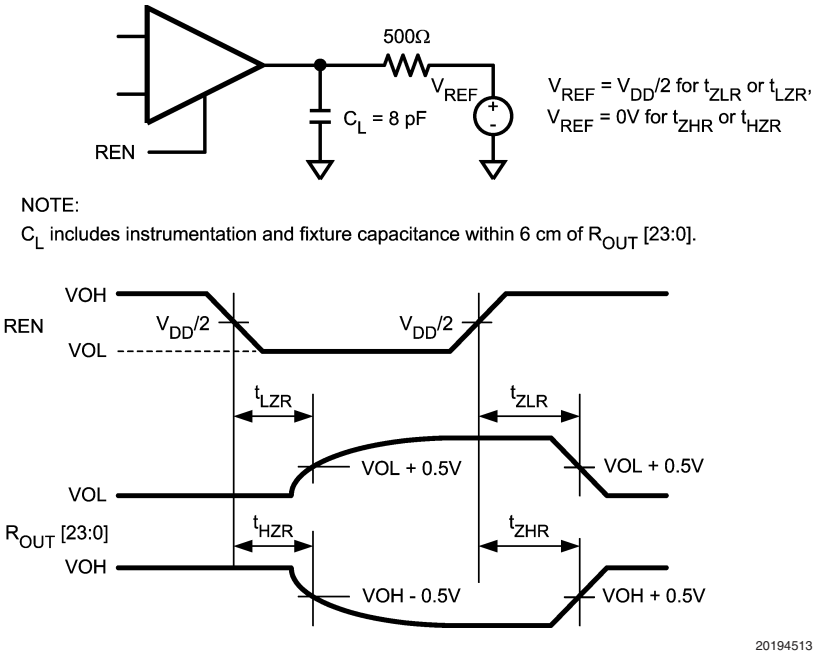


FIGURE 13. Deserializer TRI-STATE Test Circuit and Timing

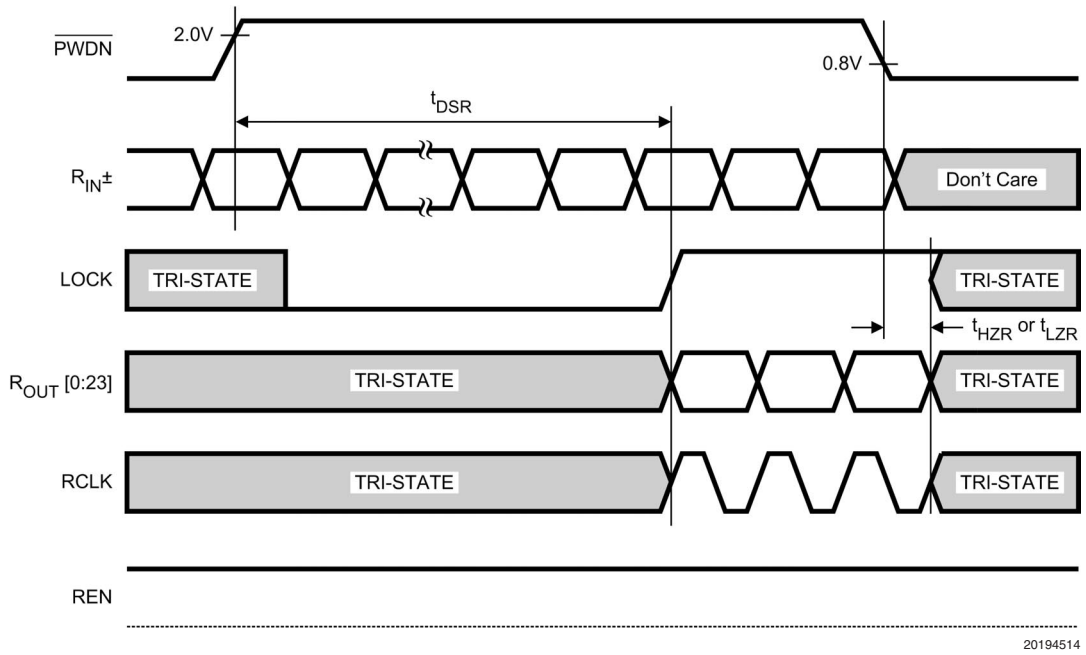


FIGURE 14. Deserializer PLL Lock Times and RPWDNB TRI-STATE Delay

AC Timing Diagrams and Test Circuits (Continued)

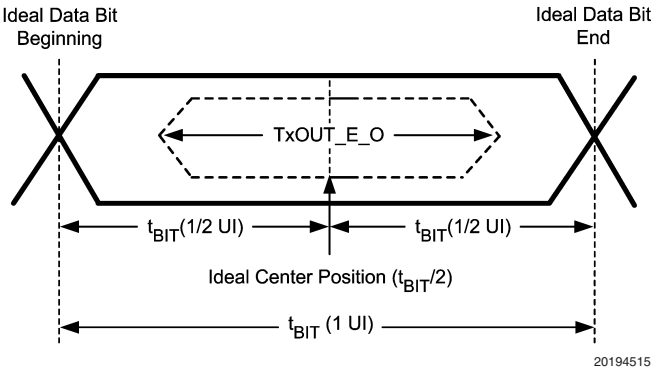


FIGURE 15. Transmitter Output Eye Opening (TxOUT_E_O)

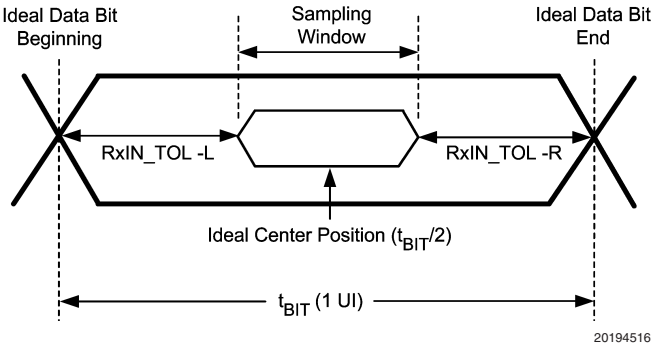
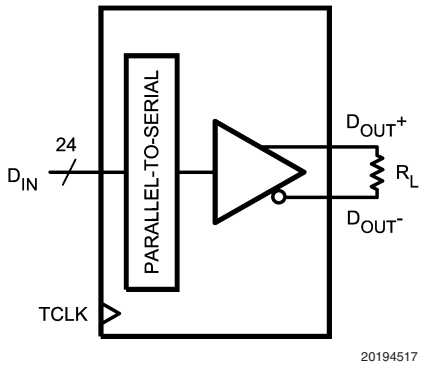


FIGURE 16. Receiver Input Tolerance (RxIN_TOL) and Sampling Window



VOD = (D_{OUT+}) − (D_{OUT-})

Differential output signal is shown as (D_{OUT+}) − (D_{OUT-}), device in Data Transfer mode.

FIGURE 17. Serializer V_{OD} Diagram

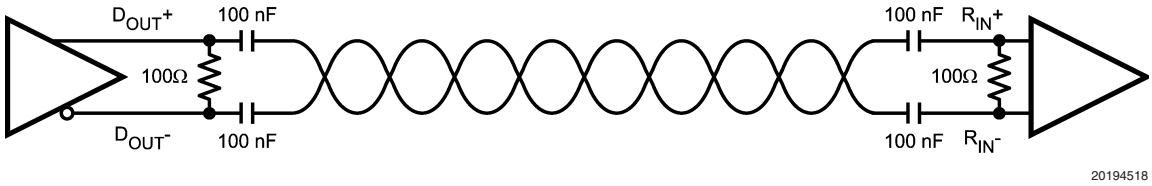


FIGURE 18. AC Coupled Application

Pin Descriptions

Pin #	Pin Name	I/O/PWR	Description
DS90UR241 SERIALIZER PIN DESCRIPTIONS			
22	VDDDR	VDD	Analog **V**oltage supply, LVDS Output POWER
21	VSSDR	GND	Analog Ground, LVDS Output **GROUND**
16	VDDPT0	VDD	Analog **V**oltage supply, VCO POWER
17	VSSPT0	GND	Analog Ground, VCO **GROUND**
14	VDDPT1	VDD	Analog **V**oltage supply, **P**LL POWER
15	VSSPT1	GND	Analog Ground, **P**LL **GROUND**
30	VDDT	VDD	Digital **V**oltage supply, **T**x serializer POWER
31	VSST	GND	Digital Ground, **T**x serializer **GROUND**
7	VDDL	VDD	Digital **V**oltage supply, **T**x **L**ogic POWER
6	VSSL	GND	Digital Ground, Tx Logic **GROUND**
42	VDDIT	VDD	Digital **V**oltage supply, **T**x **I**NPUT POWER
43	VSSIT	GND	Digital Ground, Tx Input **GROUND**
24	RESVRD	CMOS_I	**RES**e**RV**e**D** MUST tie LOW
4-1, 48-44, 41-32, 29-25	D_{IN}[23:0]	CMOS_I	Transmitter **D**ata **IN**puts
10	TCLK	CMOS_I	**T**ransmitter reference **CL**oc**K**. Used to strobe data at the D_{IN} inputs and to drive the transmitter PLL
9	TPWDNB	CMOS_I	**T**ransmitter **P**o**W**er **D**ow**N** **B**ar (ACTIVE L). TPWDNB = L; Disabled, D_{OUT} (+/-) are TRI-STATED stand-by mode, PLL is shutdown TPWDNB = H; **E**nabled
18	DEN	CMOS_I	**D**ata **EN**able (ACTIVE H) DEN = L; Disabled, D_{OUT} (+/-) are TRI-STATED, PLL still operational DEN = H; **E**nabled
13	RESRVD	CMOS_I	**RES**e**RV**e**D** - MUST tie Low
23	PRE	CMOS_I	**PRE**-emphasis select pin. PRE = ($R_{PRE} \geq 6\ k\Omega$); I_{max} = [(1.2/R) x 20 x 2], R_{min} = 6 kΩ PRE = H or floating; pre-emphasis is disabled
11	TRFB	CMOS_I	**T**ransmitter **R**ising/**F**alling **B**at Clock Edge Select TRFB = L; falling edge TRFB = H; rising edge
12	RAOFF	CMOS_I	Additional **RA**ndomizer **OFF.** (ACTIVE H) RAOFF = L; (default) Additional randomization ON RAOFF = H; backwards compatible with DS90**C**124
5	RESVRD	CMOS_I	**RES**e**RV**e**D** MUST tie LOW
8	RESVRD	CMOS_I	**RES**e**RV**e**D** MUST tie LOW
20	D_{OUT+}	LVDS_O	Transmitter LVDS true **(+) OUT**put
19	D_{OUT-}	LVDS_O	Transmitter LVDS inverted **(-) OUT**put
DS90UR124 DESERIALIZER PIN DESCRIPTIONS			
51	VDDIR	VDD	Analog LVDS **V**oltage supply, POWER
52	VSSIR	GND	Analog LVDS **G**rou**ND**
59	VDDPR0	VDD	Analog **V**oltage supply, **P**LL POWER
58	VSSPR0	GND	Analog Ground, **P**LL **GROUND**
57	VDDPR1	VDD	Analog **V**oltage supply, **P**LL VCO POWER
56	VSSPR1	GND	Analog Ground, **P**LL VCO **GROUND**
32	VDDR1	VDD	Digital **V**oltage supply, LOGIC POWER
31	VSSR1	GND	Digital Ground, Logic **GROUND**

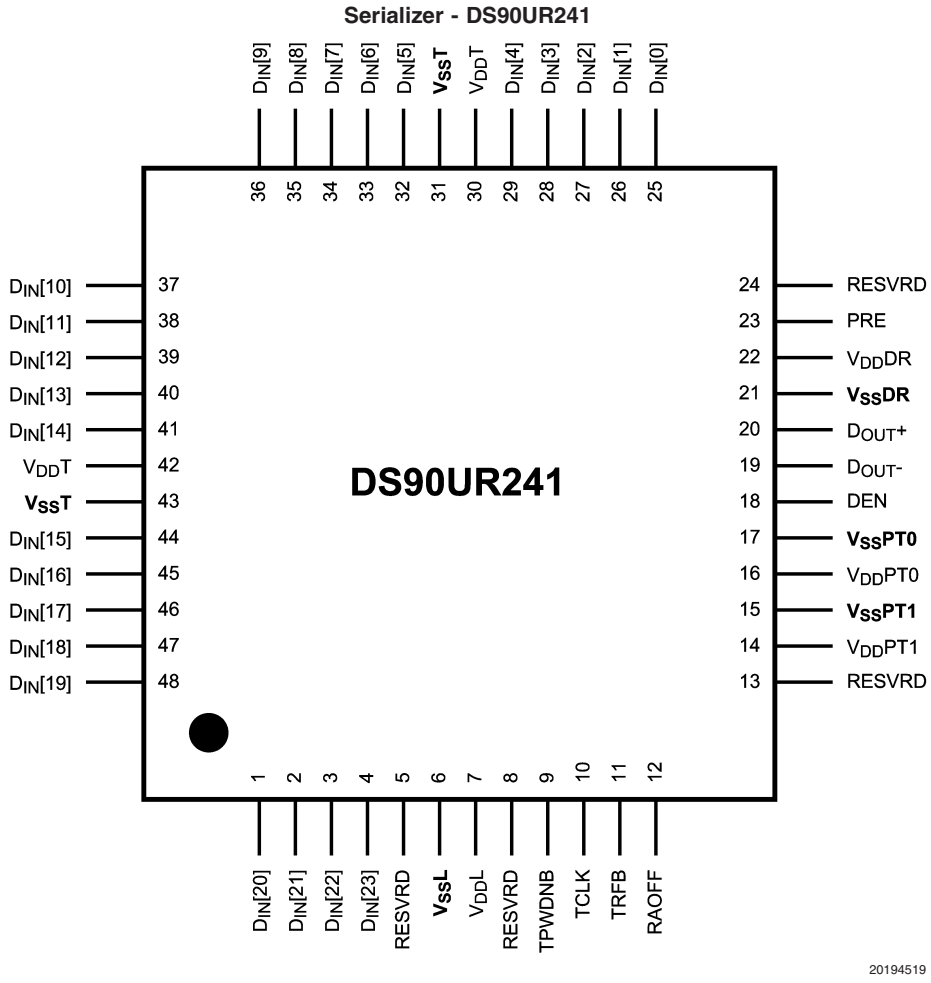
Pin Descriptions (Continued)

Pin #	Pin Name	I/O/PWR	Description
DS90UR124 DESERIALIZER PIN DESCRIPTIONS			
46	VDDR0	VDD	Digital **V**oltage supply, LOGIC POWER
47	VSSR0	GND	Digital Ground, LOGIC **GROUND**
40	VDDOR1	VDD	Digital **V**oltage supply, LVCMOS/LVTTL Output POWER
39	VSSOR1	GND	Digital Ground, LVCMOS/LVTTL Output **GROUND**
26	VDDOR2	VDD	Digital **V**oltage supply, LVCMOS/LVTTL Output POWER
25	VSSOR2	GND	Digital Ground, LVCMOS/LVTTL Output **GROUND**
11	VDDOR3	VDD	Digital **V**oltage supply, LVCMOS/LVTTL Output POWER
12	VSSOR3	GND	Digital Ground, LVCMOS/LVTTL Output **GROUND**
53	R_{IN+}	LVDS_I	**R**eceiver **LVDS** true (+) **IN**put
54	R_{IN-}	LVDS_I	**R**eceiver **LVDS** inverted **(–) IN**put
50	RESRVD	CMOS_I	**RES**e**RV**e**D** - MUST tie Low
55	RRFB	CMOS_I	**R**eceiver **R**ising **F**alling **B**ar clock Edge Select RRFB = H; R_{OUT} LVCMOS/LVTTL Output clocked on **R**ising CLK RRFB = L; R_{OUT} LVCMOS/LVTTL Output clocked on **F**alling CLK
60	REN	CMOS_I	**R**eceiver **EN**able, (ACTIVE H) REN = L; Disabled, R_{OUT}[23-0] and RCLK TRI-STATED, PLL still operational REN = H; **EN**abled
48	RPWDNB	CMOS_I	**R**eceiver **P**o**W**er **D**ow**N** **B**ar (ACTIVE L) RPWDNB = L; Disabled, R_{OUT}[23-0], RCLK, and LOCK are TRI-STATED in stand-by mode, PLL is shutdown RPWDNB = H; **EN**abled
49	PTOSEL	CMOS_I	**P**rogressive **T**urn **O**n **SEL**ect PTO = L (default); PTO = H; PTO Spread *(Figure 12*)
61	BISTEN	COMS_I	@speed_**BIST ENable** (ACTIVE H) BISTEN = L; (default), OFF BISTEN = H; BIST enabled. Set DS90UR241 D_{IN}[23-0] all LOW or floating. Check PASS condition.
62	BISTM	CMOS_I	**BIST** error reporting **M**ode selection BISTM = L; (default), Status of all R_{OUT} with respective bit error on cycle-by-cycle basis BISTM = H; Total accumulated bit error counter on R[7:0] (up to 255)
63	RAOFF	CMOS_I	Additional Randomizer OFF (ACTIVE H) RAOFF = L; (default) Additional randomization ON RAOFF = H; additional randomization OFF (backwards compatible with DS90C124)
64	SLEW	CMOS_I	LVCMOS/LVTTL Output **SLEW** rate control. SLEW = 0; (default) SLEW = 1; 2X drive/edge rate
23	LOCK	CMOS_O	**LOCK** indicates the status of the receiver PLL LOCK = L; receiver PLL is unlocked, R_{OUT}[23-0] and RCLK are TRI-STATED LOCK = H; receiver PLL is locked
35-38, 41-44	R_{OUT}[7:0]	CMOS_O	**R**eceiver **O**utputs – Group 1
19-22, 27-30	R_{OUT}[15:8]	CMOS_O	**R**eceiver **O**utputs – Group 2
7-10, 13-16	R_{OUT}[23:16]	CMOS_O	**R**eceiver **O**utputs – Group 3
24	RCLK	CMOS_O	**R**ecovered **CL**oc**K**. Parallel data rate clock recovered from the embedded clock.
45	PASS	CMOS_O	PASS = L; BIST failure PASS = H; LOCK = H before BIST can be enabled, then $1x10^{-9}$ error rate achieved across link

Pin Descriptions (Continued)

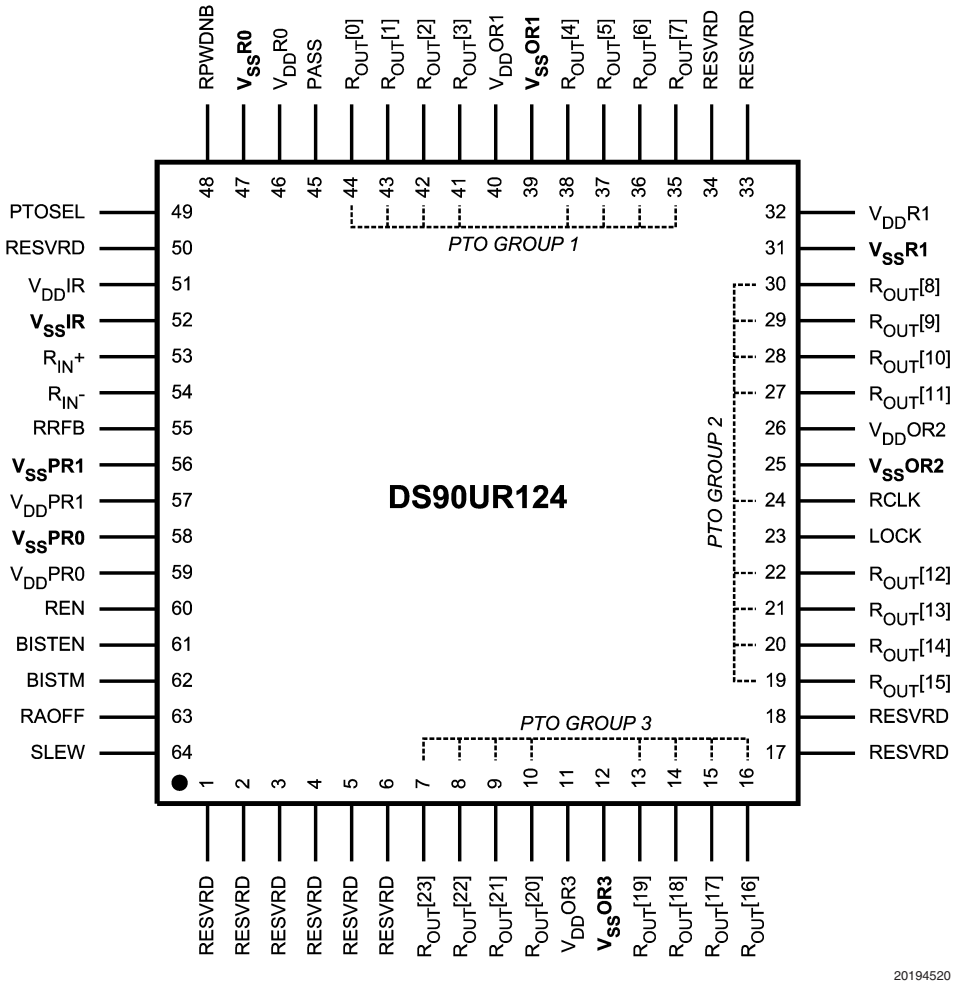
Pin #	Pin Name	I/O/PWR	Description
DS90UR124 DESERIALIZER PIN DESCRIPTIONS			
1-6, 17, 18, 33, 34	RESRVD	NC	**RESeRVeD** - no connect (n/c)

Pin Diagram



Pin Diagram (Continued)

Deserializer - DS90UR124



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Functional Description

The DS90UR241 Serializer and DS90UR124 Deserializer chipset is an easy-to-use transmitter and receiver pair that sends 24-bits of parallel LVCMOS data over a single serial LVDS link from 120 Mbps to 1.032 Gbps throughput. The DS90UR241 transforms a 24-bit wide parallel LVCMOS data into a single high speed LVDS serial data stream with embedded clock. The DS90UR124 receives the LVDS serial data stream and converts it back into a 24-bit wide parallel data and recovered clock. The 24-bit Serializer/Deserializer chipset is designed to transmit data up to 10 meters over shielded twisted pair (STP) at clock speeds from 5 MHz to 43MHz.

The Deserializer can attain lock to a data stream without the use of a separate reference clock source. The Deserializer synchronizes to the Serializer regardless of data pattern, delivering true automatic “plug and lock” performance. The Deserializer recovers the clock and data by extracting the embedded clock information and validating data integrity from the incoming data stream and then deserializes the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the LOCK output high when lock occurs. Each has a power down control to enable efficient operation in various applications.

INITIALIZATION AND LOCKING MECHANISM

Initialization of the DS90UR241 and DS90UR124 must be established before each device sends or receives data. Initialization refers to synchronizing the Serializer’s and Deserializer’s PLL’s together. After the Serializers locks to the input clock source, the Deserializer synchronizes to the Serializers as the second and final initialization step.

Step 1: When V_{DD} is applied to both Serializer and/or Deserializer, the respective outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When V_{DD} reaches V_{DD} OK (2.2V) the PLL in Serializer begins locking to a clock input. For the Serializer, the local clock is the transmit clock, TCLK. The Serializer outputs are held in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer block is now ready to send data patterns. The Deserializer output will remain in TRI-STATE while its PLL locks to the embedded clock information in serial data stream. Also, the Deserializer LOCK output will remain low until its PLL locks to incoming data and sync-pattern on the RIN± pins.

Step 2: The Deserializer PLL acquires lock to a data stream without requiring the Serializer to send special patterns. The Serializer that is generating the stream to the Deserializer will automatically send random (non-repetitive) data patterns during this step of the Initialization State. The Deserializer will lock onto embedded clock within the specified amount of time. An embedded clock and data recovery (CDR) circuit locks to the incoming bit stream to recover the high-speed receive bit clock and re-time incoming data. The CDR circuit expects a coded input bit stream. In order for the Deserializer to lock to a random data stream from the Serializer, it performs a series of operations to identify the rising clock edge and validates data integrity, then locks to it. Because this locking procedure is independent on the data pattern, total random locking duration may vary. At the point when the Deserializer’s CDR locks to the embedded clock, the LOCK pin goes high and valid RCLK/data appears on the outputs. Note that the LOCK signal is synchronous to valid data appearing on the outputs. The Deserializer’s LOCK pin is a convenient way to ensure data integrity is achieved on receiver side.

DATA TRANSFER

After lock is established, the Serializer inputs DIN0–DIN23 may be used to input data to the Serializer. Data is clocked into the Serializer by the TCLK input. The edge of TCLK used to strobe the data is selectable via the TRFB pin. TRFB high selects the rising edge for clocking data and low selects the falling edge. The Serializer outputs (DOUT±) are intended to drive point-to-point connections or limited multipoint applications.

CLK1, CLK0, DCA, DCB are four overhead bits transmitted along the single LVDS serial data stream. The CLK1 bit is always high and the CLK0 bit is always low. The CLK1 and CLK0 bits function as the embedded clock bits in the serial stream. DCB functions as the DC Balance control bit. It does not require any pre-coding of data on transmit side. The DC Balance bit is used to minimize the short and long-term DC bias on the signal lines. This bit operates by selectively sending the data either unmodified or inverted. The DCA bit is used to validate data integrity in the embedded data stream. Both DCA and DCB coding schemes are integrated and automatically performed within Serializer and Deserializer.

Serialized data and clock/control bits (24+4 bits) are transmitted from the serial data output (DOUT±) at 28 times the TCLK frequency. For example, if TCLK is 43 MHz, the serial rate is 43 x 28 = 1.20 Giga bits per second. Since only 24 bits are from input data, the serial “payload” rate is 24 times the TCLK frequency. For instance, if TCLK = 43 MHz, the payload data rate is 43 x 24 = 1.03 Gbps. TCLK is provided by the data source and must be in the range of 5 MHz to 43 MHz nominal. The Serializer outputs (DOUT±) can drive a point-to-point connection. The outputs transmit data when the enable pin (DEN) is high, TPWDNB is high. The DEN pin may be used to TRI-STATE the outputs when driven low.

When the Deserializer channel attains lock to the input from a Serializer, it drives its LOCK pin high and synchronously delivers valid data and recovered clock on the output. The Deserializer locks onto the embedded clock, uses it to generate multiple internal data strobes, and then drives the recovered clock to the RCLK pin. The recovered clock (RCLK output pin) is synchronous to the data on the ROUT[23:0] pins. While LOCK is high, data on ROUT[23:0] is valid. Otherwise, ROUT[23:0] is invalid. The polarity of the RCLK edge is controlled by the RRFB input. ROUT(0-23), LOCK and RCLK outputs will each drive a maximum of 4 pF load with a 43 MHz clock. REN controls TRI-STATE for ROUTn and the RCLK pin on the Deserializer.

RESYNCHRONIZATION

If the Deserializer loses lock, it will automatically try to re-establish lock. For example, if the embedded clock edge is not detected one time in succession, the PLL loses lock and the LOCK pin is driven low. The Deserializer then enters the operating mode where it tries to lock to a random data stream. It looks for the embedded clock edge, identifies it and then proceeds through the locking process.

The logic state of the LOCK signal indicates whether the data on ROUT is valid; when it is high, the data is valid. The system must monitor the LOCK pin to determine whether data on the ROUT is valid.

POWERDOWN

The Powerdown state is a low power sleep mode that the Serializer and Deserializer may use to reduce power when no data is being transferred. The TPWDNB and RPWDNB are used to set each device into power down mode, which

Functional Description (Continued)

reduces supply current to the µA range. The Serializer enters powerdown when the TPWDNB pin is driven low. In powerdown, the PLL stops and the outputs go into TRI-STATE, disabling load current and reducing supply. To exit Powerdown, TPWDNB must be driven high. When the Serializer exits Powerdown, its PLL must lock to TCLK before it is ready for the Initialization state. The system must then allow time for Initialization before data transfer can begin. The Deserializer enters powerdown mode when RPWDNB is driven low. In powerdown mode, the PLL stops and the outputs enter TRI-STATE. To bring the Deserializer block out of the powerdown state, the system drives RPWDNB high.

Both the Serializer and Deserializer must reinitialize and relock before data can be transferred. The Deserializer will initialize and assert LOCK high until it is locked to the input clock.

TRI-STATE

For the Serializer, TRI-STATE is entered when the DEN or TPWDNB pin is driven low. This will TRI-STATE both driver output pins (DOUT+ and DOUT–). When DEN is driven high, the serializer will return to the previous state as long as all other control pins remain static (TPWDNB, TRFB).

When you drive the REN or RPWDNB pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT23) and RCLK will enter TRI-STATE. The LOCK output remains active, reflecting the state of the PLL. The Deserializer input pins are high impedance during receiver powerdown (RPWDNB low) and power-off (V_{DD} = 0V).

PRE-EMPHASIS

The DS90UR241 features a Pre-Emphasis function used to compensate for long or lossy transmission media. Cable drive is enhanced with a user selectable Pre-Emphasis feature that provides additional output current during transitions to counteract cable loading effects. The transmission distance will be limited by the loss characteristics and quality of the media. Pre-Emphasis adds extra current during LVDS logic transition to reduce the cable loading effects and increase driving distance. In addition, Pre-Emphasis helps provide faster transitions, increased eye openings, and improved signal integrity. To enable the Pre-Emphasis function, the “PRE” pin requires one external resistor (Rpre) to Vss in order to set the additional current level. Pre-Emphasis strength is set via an external resistor (Rpre) applied from min to max (floating to 6kΩ) at the “PRE” pin. A lower input resistor value on the ”PRE” pin increases the magnitude of dynamic current during data transition. There is an internal current source based on the following formula: PRE = (Rpre ≥ 6kΩ); I_{MAX} = [(1.2/Rpre) x 20 x 2]. The ability of the DS90UR241 to use the Pre-Emphasis feature will extend the transmission distance up to 10 meters in most cases.

AC-COUPLING AND TERMINATION

The DS90UR241 and DS90UR124 supports AC-coupled interconnects through integrated DC balanced encoding/decoding scheme. To use AC coupled connection between the Serializer and Deserializer, insert external AC coupling capacitors in series in the LVDS signal path as illustrated in *Figure 18*. The Deserializer input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal V_{CM} to +1.8V. With AC signal coupling, capacitors provide the ac-coupling path to the signal input.

For the high-speed LVDS transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The most common used capacitor value for the interface is 100 nF (0.1 uF) capacitor.

A termination resistor across DOUT± and RIN± is also required for proper operation to be obtained. The termination resistor should be equal to the differential impedance of the media being driven. This should be in the range of 90 to 132 Ohms. 100 Ohms is a typical value common used with standard 100 Ohm transmission media. This resistor is required for control of reflections and also to complete the current loop. It should be placed as close to the Serializer DOUT± outputs and Deserializer RIN± inputs to minimize the stub length from the pins. To match with the deferential impedance on the transmission line, the LVDS I/O are terminated with 100 ohm resistors on Serializer DOUT± outputs pins and Deserializer RIN± input pins.

PROGRESSIVE TURN–ON (PTO)

The DS90UR124 Deserializer offers two types of Progressive Turn-On modes (Fixed-PTO and PTO Frequency Spread) to help reduce EMI, simultaneous switching noise, and system ground bounce. For Fixed-PTO mode, the Deserializer ROUT[23:0] outputs are grouped into three groups of eight, with each group switching about 2 or 1 UI apart in phase from RCLK for Group 1 and Groups 2, 3 respectively. In the PTO Frequency Spread mode, ROUT[23:0] are also grouped into three groups of eight, with each group is separated out of phase with the adjacent groups (see *Figure 12*). Note that in the PTO Frequency Spread operating mode RCLK is also spreading and separated by 1 UI.

@SPEED-BIST TEST FEATURE

To assist vendors with test verification, the DS90UR241/DS90UR124 is equipped with built-in self-test (BIST) capability to support both system manufacturing and field diagnostics. BIST mode is intended to check the entire high-speed serial link at full link-speed, without the use of specialized and expensive test equipment. This feature provides a simple method for a system host to perform diagnostic testing of both Serializer and Deserializer. The BIST function is easily configured through the 2 control pins on the DS90UR124. When the BIST mode is activated, the Serializer has the ability to transfer an internally generated PRBS data pattern. This pattern traverses across interconnecting links to the Deserializer. The DS90UR124 includes an on-chip PRBS pattern verification circuit that checks the data pattern for bit errors and reports any errors on the data output pins on the Deserializer.

The @SPEED-BIST feature uses 2 signal pins (BISTEN and BISTM) on the DS90UR124 Deserializer. The BISTEN and BISTM pins together determine the functions of the BIST mode. The BISTEN signal (HIGH) activates the test feature on the Deserializer. After the BIST mode is enabled, all the data input channels DIN[23:0] on the DS90UR241 Serializer must be set logic LOW or floating in order for Deserializer to start accepting data. An input clock signal (TCLK) for the Serializer must also be applied during the entire BIST operation. The BISTM pin selects error reporting status mode of the BIST function. When BIST is configured in the error status mode (BISTM = LOW), each of the ROUT[23:0] outputs will correspond to bit errors on a cycle-by-cycle basis. The result of bit mismatches are indicated on the respective parallel inputs on the ROUT[23:0] data output pins. In the BIST error-count accumulator mode (BISTM = HIGH), an

Functional Description (Continued)

8-bit counter on ROUT[7:0] is used to represent the number of errors detected (0 to 255 max). The successful completion of the BIST test is reported on the PASS pin on the Deserializer. The Deserializer's PLL must first be locked to ensure the PASS status is valid. The PASS status pin will stay LOW and then transition to HIGH once a BER of $1x10^{-9}$ is achieved across the transmission link.

Applications Information

USING THE DS90UR241 AND DS90UR124

The DS90UR241/DS90UR124 Serializer/Deserializer (SERDES) pair sends 24 bits of parallel LVCMOS data over a serial LVDS link up to 1.03 Gbps. Serialization of the input data is accomplished using an on-board PLL at the Serializer which embeds clock with the data. The Deserializer extracts the clock/control information from the incoming data stream and deserializes the data. The Deserializer monitors the incoming clockl information to determine lock status and will indicate lock by asserting the LOCK output high.

POWER CONSIDERATIONS

An all CMOS design of the Serializer and Deserializer makes them inherently low power devices. Additionally, the constant current source nature of the LVDS outputs minimize the slope of the speed vs. I_{DD} curve of CMOS designs.

NOISE MARGIN

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably recover data. Various environmental and systematic factors include:

Serializer: TCLK jitter, V_{DD} noise (noise bandwidth and out-of-band noise)

Media: ISI, V_{CM} noise

Deserializer: V_{DD} noise

For a graphical representation of noise margin, please see *Figure 16*.

TRANSMISSION MEDIA

The Serializer and Deserializer can be used in point-to-point configuration, through a PCB trace, or through twisted pair cable. In a point-to-point configuration, the transmission media needs be terminated at both ends of the transmitter and receiver pair. Interconnect for LVDS typically has a differential impedance of 100 Ohms. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. In most applications that involve cables, the transmission distance will be determined on data rates involved, acceptable bit error rate and transmission medium.

HOT PLUG INSERTION

The Serializer and Deserializer devices support hot pluggable applications. The "Hot Inserted" operation on the serial interface does not disrupt communication data on the active data lines. The automatic receiver lock to random data "plug & go" hot insertion capability allows the DS90UR124 to attain lock to the active data stream during a live insertion event.

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS SERDES devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz range. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS (LVTTL) signals away from the LVDS lines to prevent coupling from the CMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Termination of the LVDS interconnect is required. For point-to-point applications, termination should be located at both ends of the devices. Nominal value is 100 Ohms to match the line's differential impedance. Place the resistor as close to the transmitter DOUT± outputs and receiver RIN± inputs as possible to minimize the resulting stub between the termination resistor and device.

Applications Information (Continued)

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - —S = space between the pair
  - —2S = space between pairs
  - —3S = space to LVCMOS/LVTTL signal
- Minimize the number of VIA
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the National web site at: **www.national.com/lvds**

Truth Tables

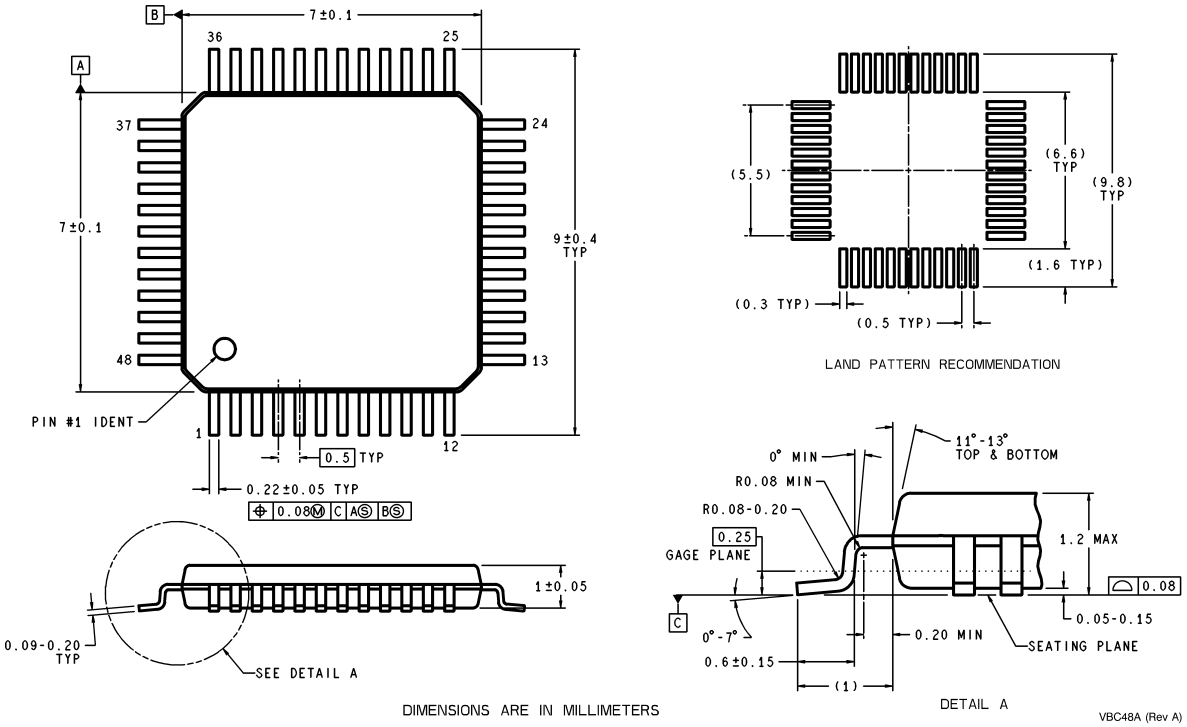
TABLE 1. DS90UR241 Serializer Truth Table

Pin 9	Pin 18	Pin 12	(Internal)	Pins 19 and 20
TPWDNB	DEN	RAOFF	Tx PLL Status	LVDS Outputs
L	X	X	X	Hi Z
H	L	X	X	Hi Z
H	H	X	Not Locked	Hi Z
H	H	L	Locked	Serialized Data with Embedded Clock (DS90**UR**124 compatible)
H	H	H	Locked	Serialized Data with Embedded Clock (DS90**C**124 compatible)

TABLE 2. DS90UR124 Deserializer Truth Table

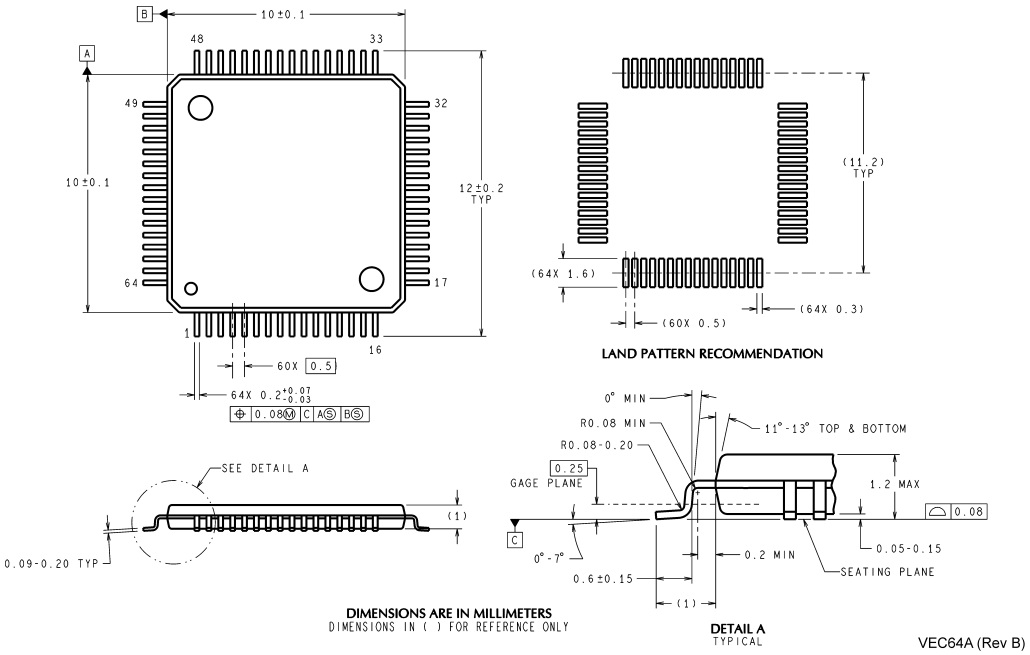
Pin 48	Pin 60	Pin 63	(Internal)	(See Pin Diagram)	Pin 23
RPWDNB	REN	RAOFF	Rx PLL Status	ROUTn and RCLK	LOCK
L	X	X	X	Hi Z	Hi Z
H	L	X	X	Hi Z	L = PLL Unocked; H = PLL Locked
H	H	X	Not Locked	Hi Z	L
H	H	L	Locked	Data and RCLK Active (DS90**UR**241 compatible)	H
H	H	H	Locked	Data and RCLK Active (DS90**C**241 compatible)	H

Physical Dimensions inches (millimeters) unless otherwise noted



Dimensions show in millimeters only
Order Number DS90UR241IVS
NS Package Number VBC48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dimensions show in millimeters only
Order Number DS90UR124IVS
NS Package Number VEC64A

Ordering Information

NSID	Package Type	Package ID
DS90UR241	48-Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch, DS90UR241IVS	VBC48A
DS90UR241	48-Lead TQFP style, 7.0 X 7.0 X 1.0 mm, 0.5 mm pitch, 1000 std reel, DS90UR241IVSX	VBC48A
DS90UR124	64-Lead TQFP style, 10.0 X 10.0 X 1.0 mm, 0.5 mm pitch, DS90UR124IVS	VEC64A
DS90UR124	64-Lead TQFP style, 10.0 X 10.0 X 1.0 mm, 0.5 mm pitch, 1000 std reel, DS90UR124IVSX	VEC64A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

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Lead free products are RoHS compliant.

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