

NT7107

Copyright: NEOTEC (C) 2002
<http://www.neotec.com.tw>

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electric or mechanical, by photocopying, recording, or otherwise, without the prior written consent of NEOTEC

INTRODUCTION

The NT7107 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the NT7108.

The NT7107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the NT7108 (64 channel segment driver).

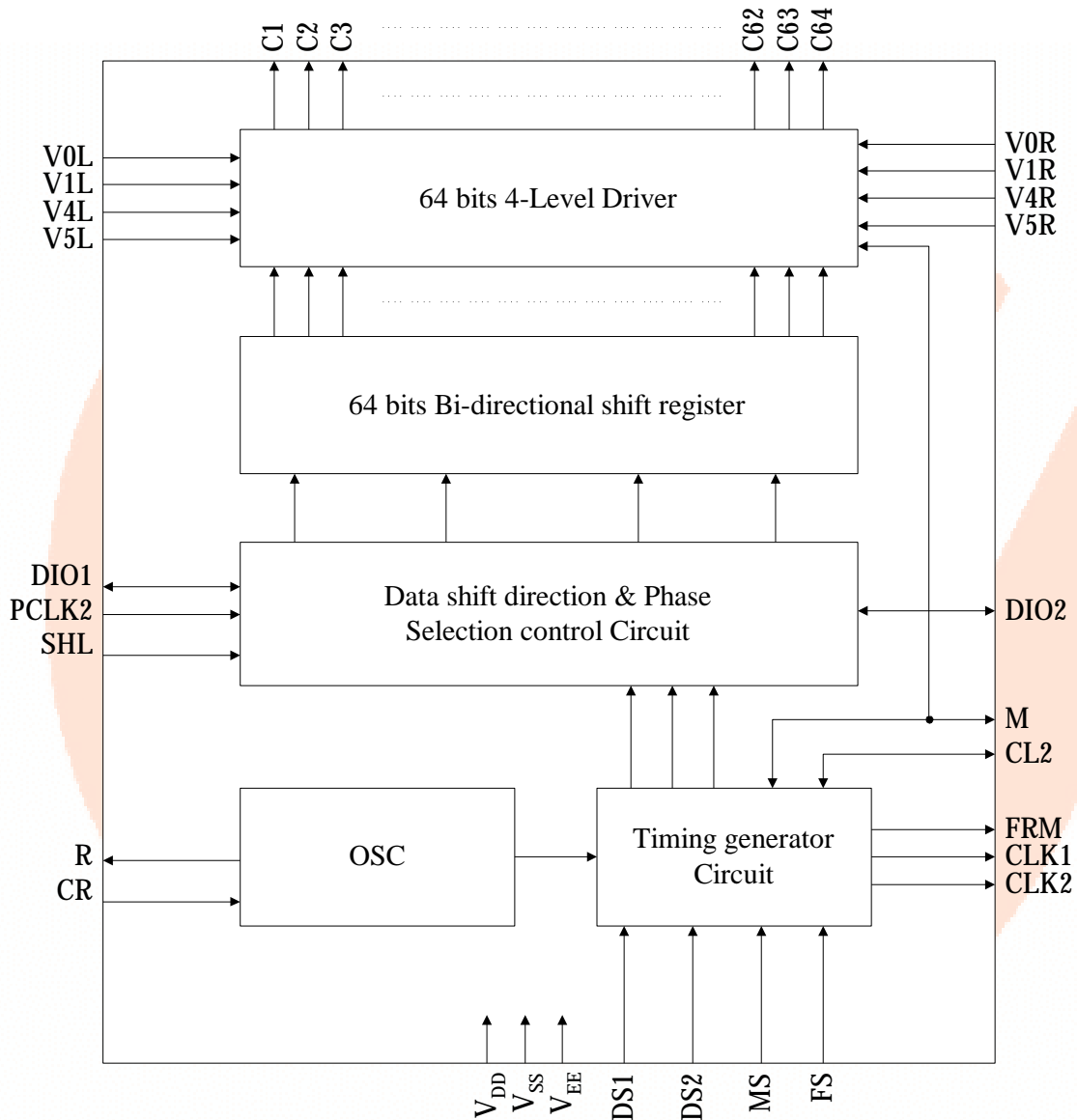
FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage: +2.7~+5.5V
- LCD driving voltage: 8V~17V (VDD-VEE)
- Interface

Driver		Controller
COMMON	SEGMENT	
Other NT7107	Other NT7108	MPU

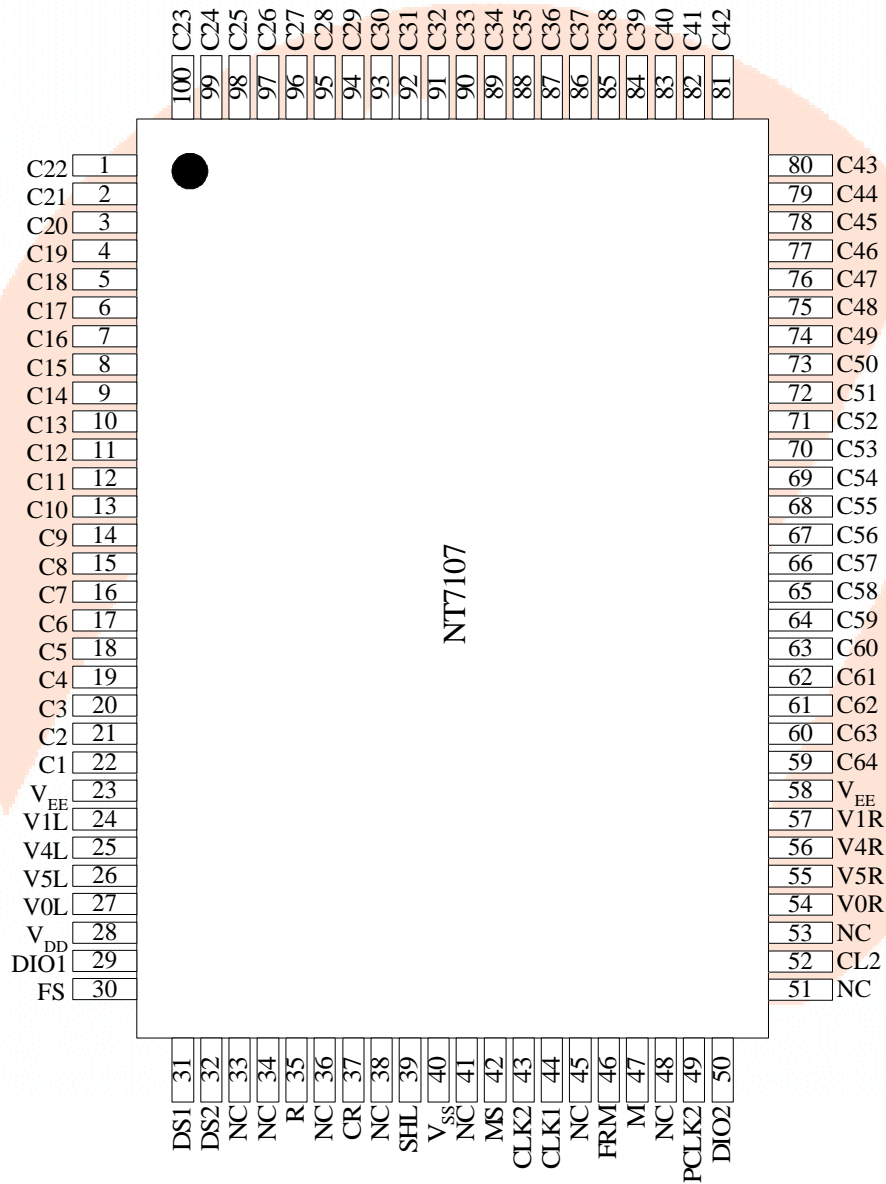
- High voltage CMOS process
- 100QFP or bare chip available

BLOCK DIAGRAM

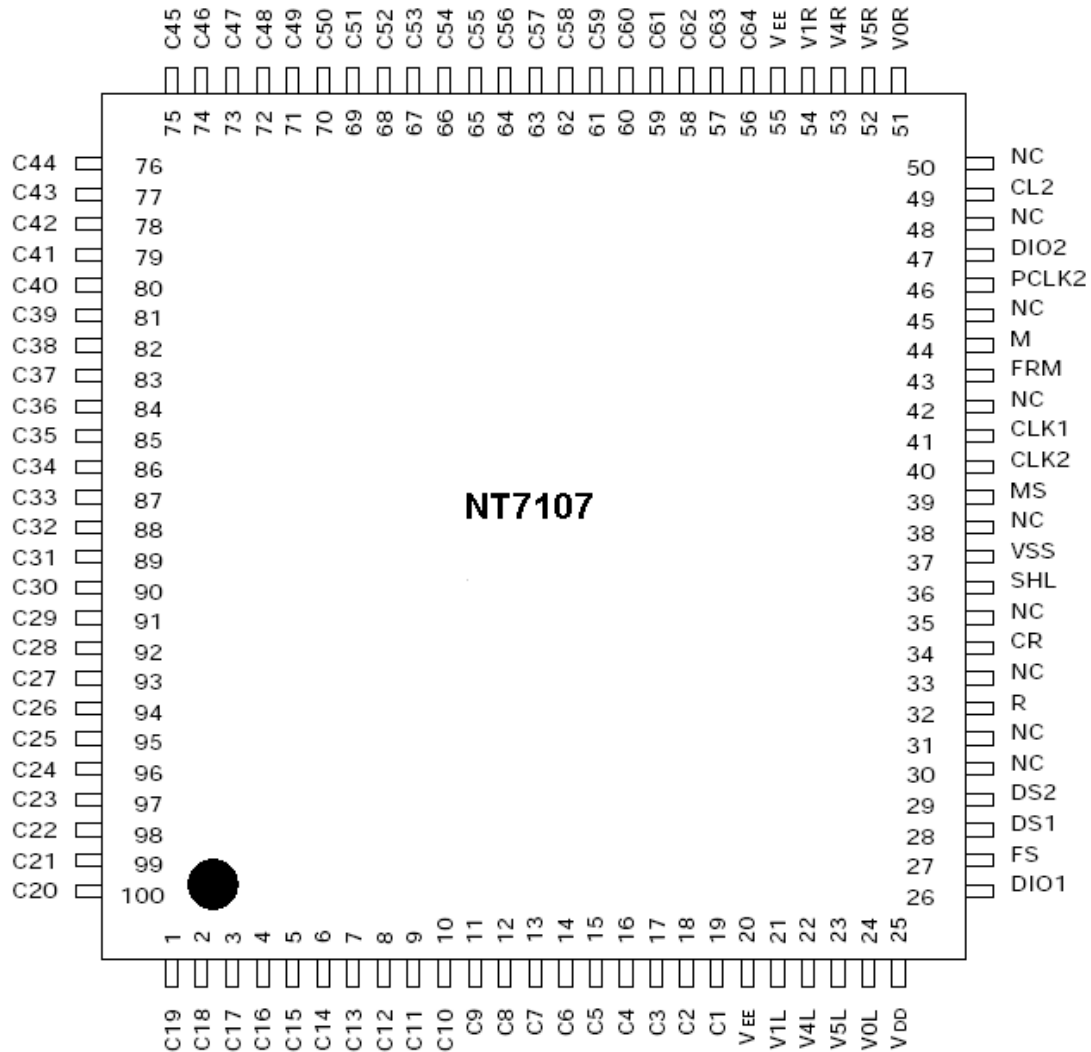


PIN CONFIGURATION

100 PQFP PACKAGE



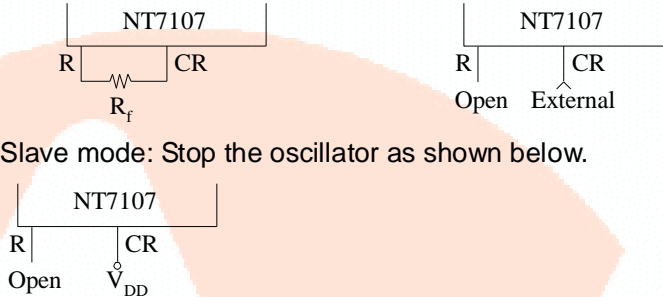
100 PQ PACKAGE



PIN DESCRIPTION

Table 1. Pin Description

Pin Number QFP	Symbol	I/O	Description													
28	V _{DD}	Power	For internal logic circuit (+2.7~+5.5V)													
40	V _{SS}		GND (=0V)													
23,58	V _{EE}		For LCD driver circuit													
27,54	V0L,V0R	Power	Bias supply voltage terminals to drive LCD. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Select Level</th> <th>Non-Select Level</th> </tr> </thead> <tbody> <tr> <td>V0L (R), V5L (R)</td> <td>V1L (R), V4L (R)</td> </tr> </tbody> </table> <p>The same voltage should connect V0L and V0R (V1L & V1R, V4L & V4R, V5L & V5R).</p>	Select Level	Non-Select Level	V0L (R), V5L (R)	V1L (R), V4L (R)									
Select Level	Non-Select Level															
V0L (R), V5L (R)	V1L (R), V4L (R)															
24,57	V1L,V1R															
25,56	V4L,V4R															
26,55	V5L,V5R															
42	MS	Input	Section of master/slave mode <ul style="list-style-type: none"> · Master mode (MS=1) DIO1, DIO2, CL2 and M is output state. · Slave mode (MS=0) SHL=1 DIO1 is input state (DIO2 is output state) SHL=0 DIO2 is input state (DIO1 is output state) CL2 and M are input state. 													
39	SHL	Input	Selection of data shift direction. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SHL</th> <th>Data Shift Direction</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>DIO1 C1....C64 DIO2</td> </tr> <tr> <td>L</td> <td>DIO2 C64....C1 DIO1</td> </tr> </tbody> </table>	SHL	Data Shift Direction	H	DIO1 C1....C64 DIO2	L	DIO2 C64....C1 DIO1							
SHL	Data Shift Direction															
H	DIO1 C1....C64 DIO2															
L	DIO2 C64....C1 DIO1															
49	PCLK2	Input	Selection of shift clock (CL2) phase. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>PCLK2</th> <th>Data Clock (CL2) Phase</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Data shift at the rising edge of CL2</td> </tr> <tr> <td>L</td> <td>Data shift at the falling edge of CL2</td> </tr> </tbody> </table>	PCLK2	Data Clock (CL2) Phase	H	Data shift at the rising edge of CL2	L	Data shift at the falling edge of CL2							
PCLK2	Data Clock (CL2) Phase															
H	Data shift at the rising edge of CL2															
L	Data shift at the falling edge of CL2															
30	FS	Input	Selection of oscillation frequency. <ul style="list-style-type: none"> · Master mode when the frame frequency is 70 Hz, the oscillation frequency should be fosc=430kHz at FS=1(V_{DD}) fosc=215kHz at FS=0(V_{SS}) · Slave mode Connect to V_{DD} 													
31 32	DS1 DS2	Input	Selection of display duty. <ul style="list-style-type: none"> · Master mode <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DS1</th> <th>DS2</th> <th>Duty</th> </tr> </thead> <tbody> <tr> <td rowspan="2">L</td> <td>L</td> <td>1/48</td> </tr> <tr> <td>H</td> <td>1/64</td> </tr> <tr> <td rowspan="2">H</td> <td>L</td> <td>1/96</td> </tr> <tr> <td>H</td> <td>1/128</td> </tr> </tbody> </table> · Slave mode Connect to V_{DD} 	DS1	DS2	Duty	L	L	1/48	H	1/64	H	L	1/96	H	1/128
DS1	DS2	Duty														
L	L	1/48														
	H	1/64														
H	L	1/96														
	H	1/128														

Pin Number QFP	Symbol	I/O	Description																		
35 37	R CR		<p>RC Oscillator (Built-in capacitor)</p> <ul style="list-style-type: none"> Master mode: Use these terminals as shown below.  <ul style="list-style-type: none"> Slave mode: Stop the oscillator as shown below. 																		
44 43	CLK1 CLK2	Output	<p>Operating clock output for the NT7108</p> <ul style="list-style-type: none"> Master mode: connection to CLK1 and CLK2 of the NT7108 Slave mode: open 																		
46	FRM	Output	<p>Synchronous frame signal.</p> <ul style="list-style-type: none"> Master mode: connection to FRM of the NT7108 Slave mode: open 																		
47	M	Input/ Output	<p>Alternating signal input for LCD driving.</p> <ul style="list-style-type: none"> Master mode: output state Connection to M of the NT7108 Slave mode: input state Connection to the controller 																		
52	CL2	Input/ Output	<p>Data shift clock</p> <ul style="list-style-type: none"> Master mode: output state Connection to CL of the NT7108 Slave mode: input state connection to shift clock terminal of the controller. 																		
29 50	DIO1 DIO2	Input/ Output	<p>Data input/output pins of internal shift register.</p> <table border="1" data-bbox="649 1249 1291 1417"> <thead> <tr> <th>MS</th> <th>SHL</th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Output</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>	MS	SHL	DIO1	DIO2	H	H	Output	Output	L	Output	Output	L	H	Input	Output	L	Output	Input
MS	SHL	DIO1	DIO2																		
H	H	Output	Output																		
	L	Output	Output																		
L	H	Input	Output																		
	L	Output	Input																		
22-1 100-59	C1-C64	Output	<p>Common signal output for LCD driving.</p> <table border="1" data-bbox="649 1480 1209 1648"> <thead> <tr> <th>Data</th> <th>M</th> <th>Out</th> </tr> </thead> <tbody> <tr> <td rowspan="2">L</td> <td>L</td> <td>V1</td> </tr> <tr> <td>H</td> <td>V4</td> </tr> <tr> <td rowspan="2">H</td> <td>L</td> <td>V5</td> </tr> <tr> <td>H</td> <td>V0</td> </tr> </tbody> </table>	Data	M	Out	L	L	V1	H	V4	H	L	V5	H	V0					
Data	M	Out																			
L	L	V1																			
	H	V4																			
H	L	V5																			
	H	V0																			
33 34,36 38,41 45,48 51,53	NC		No connection																		

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	V_{DD}	-0.3 to +7.0	V	(1)
Supply voltage	V_{EE}	$V_{DD}-19.0$ to $V_{DD}+0.3$		(4)
Driver supply voltage	V_B	-0.3 to $V_{DD}+0.3$		(1),(2)
	V_{LCD}	$V_{EE}-0.3$ to $V_{DD}+0.3$		(3),(4)
Operating temperature	T_{OPR}	-30 to +85	°C	-
Storage temperature	T_{STG}	-55 to +125		-

NOTES:

1. Based on $V_{SS}=0V$
2. Applies to input terminals and I/O terminals at high impedance. (Except $V_{0L(R)}$, $V_{1L(R)}$, $V_{4L(R)}$ and $V_{5L(R)}$)
3. Applies to $V_{0L(R)}$, $V_{1L(R)}$, $V_{4L(R)}$ and $V_{5L(R)}$.
4. Voltage level: $V_{DD} \geq V_{0L} = V_{0R} \geq V_{1L} = V_{1R} \geq V_{4L} = V_{4R} \geq V_{5L} = V_{5R} \geq V_{EE}$.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS ($V_{DD}=+5.0V$, $V_{SS}=0V$, $|V_{DD}-V_{EE}|=8\sim 17V$, $T_A=-30 \sim +85^\circ C$)

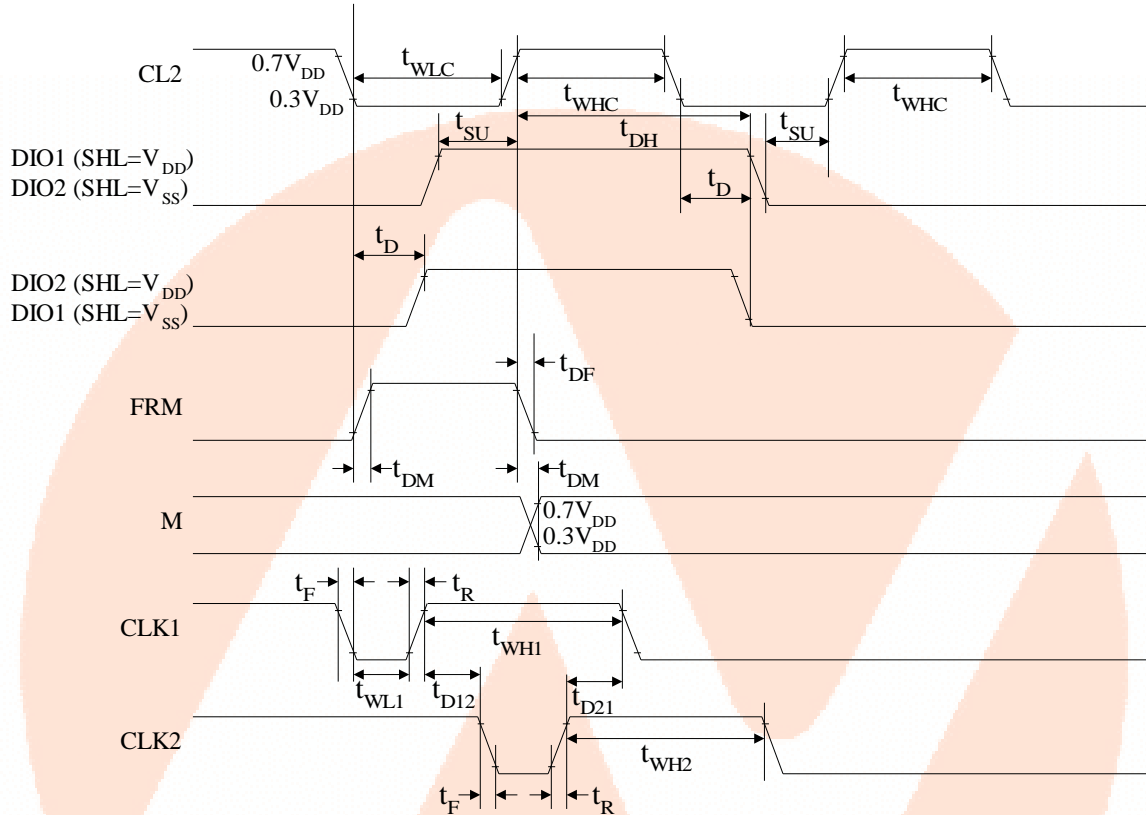
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	V_{DD}	-	2.7	-	5.5	V	(1)
Input Voltage	High	V_{IH}	$0.7V_{DD}$	-	V_{DD}		
	Low	V_{IL}	V_{SS}	-	$0.3V_{DD}$		
Output Voltage	High	V_{OH}	$I_{OH}=-0.4mA$	$V_{DD}-0.4$	-		
	Low	V_{OL}	$I_{OL}=0.4mA$	-	0.4		
Input leakage current	I_{LKG}	$V_{IN}=V_{DD}-V_{SS}$	-1.0	-	1.0	μA	(1)
OSC frequency	f_{OSC}	$R_f=47K\Omega \pm 2\%$	315	450	585	kHz	
On resistance ($V_{DIV} - C_i$)	R_{ON}	$V_{DD}-V_{EE}=17V$ Load current = $\pm 150 \mu A$	-	-	1.5	$K\Omega$	
Operating current	I_{DD1}	Master mode; 1/128duty	-	-	1.0	mA	
	I_{DD2}	Slave mode; 1/128 duty	-	-	200	μA	(4)
Supply current	I_{EE}	Master mode; 1/128 duty	-	-	100	μA	(5)
Operating Frequency	f_{OP1}	Master mode; External clock	50	-	600	kHz	
	f_{OP2}	Slave mode	0.5	-	1500		

NOTES:

1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the Output State.
3. This value is specified at about the current flowing through V_{SS} . Internal oscillation circuit: $R_f = 47k\Omega$, Each terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
4. This value is specified at about the current flowing through V_{SS} . Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD} , and MS is connected to V_{SS} . CL2, M, DIO1 is external clock.
5. This value is specified at the current flowing through V_{EE} . Don connect to V_{LCD} (V1-V5).

AC CHARACTERISTICS ($V_{DD}=5V\pm 10\%$, $T_A=-30 \sim +85^{\circ}C$)

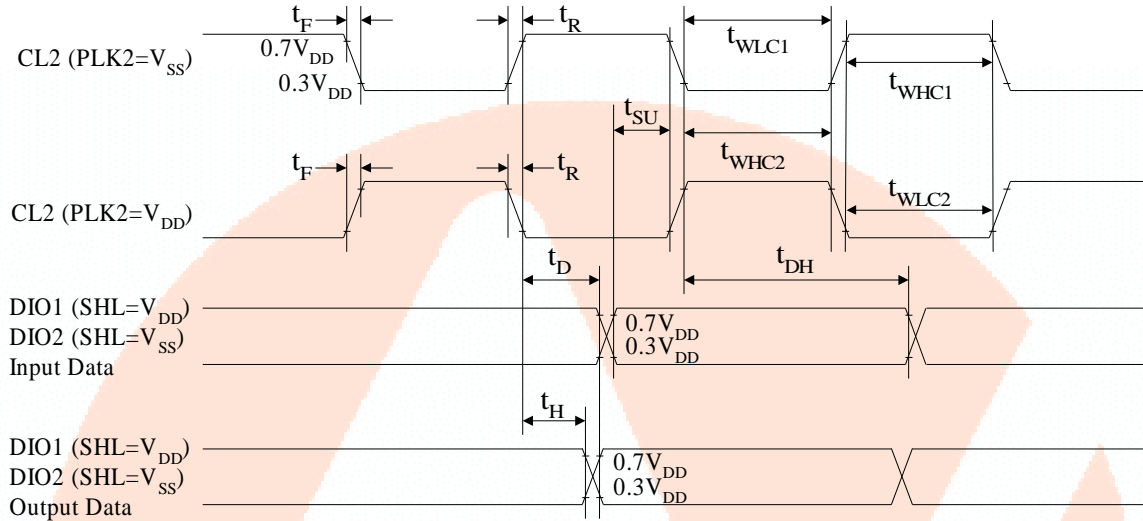
Master Mode (MS= V_{DD} , PCLK2= V_{DD})



Master Mode

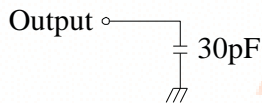
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Data setup time	t_{SU}	20	-	-	μs
Data hold time	t_{DH}	40	-	-	
Data delay time	t_D	5	-	-	
FRM delay time	t_{DF}	-2	-	2	
M delay time	t_{DM}	-2	-	2	
CL2 low level width	t_{WLC}	35	-	-	ns
CL2 high level width	t_{WHC}	35	-	-	
CLK1 low level width	t_{WL1}	700	-	-	
CLK2 low level width	t_{WL2}	700	-	-	
CLK1 high level width	t_{WH1}	2100	-	-	
CLK2 high level width	t_{WH2}	2100	-	-	
CLK1-CLK2 phase difference	t_{D12}	700	-	-	
CLK2-CLK1 phase difference	t_{D21}	700	-	-	
CLK1,CLK2 rise/fall time	t_R/t_F	-	-	150	

Slave Mode (MS=V_{SS})



Characteristic	Symbol	Min.	Typ.	Max.	Unit	Note
CL2 low level width	t _{WLC1}	450	-	-	ns	PCLK2=V _{SS}
CL2 high level width	t _{WHC1}	150	-	-		PCLK2=V _{SS}
CL2 low level width	t _{WLC2}	150	-	-		PCLK2=V _{DD}
CL2 high level width	t _{WHC2}	450	-	-		PCLK2=V _{DD}
Data setup time	t _{SU}	100	-	-		
Date hold time	t _{DH}	100	-	-		
Data delay time	t _D	-	-	200		(NOTE)
Output data hold time	t _H	10	-	-		
CL2 rise/fall time	t _R / t _F	-	-	30		

NOTE: Connect load CL = 30pF



FUNCTIONAL DESCRIPTION

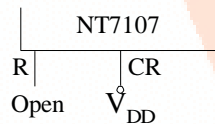
RC Oscillator

The RC Oscillator generates CL2, M, FRM of the NT7107, and CLK1 and CLK1 of the NT7108 by the oscillation resistor R and internal capacitor C. When selecting the master/slave mode, the oscillation circuit is as following:

Master Mode: In the master mode, use these terminals as shown below.



Slave Mode: In the slave mode, stop the oscillator as shown below.



Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

Selection of Master/Slave (M/S) Mode

When MS is H, it generates CL2, M, FRM, CLK1 and CLK2 internally.

When MS is L, it operates by receiving M and CL2 from the master device.

Frequency Selection (FS)

To adjust FRM frequency by 70Hz, the oscillation frequency should be as follows:

FS	Oscillation Frequency
H	$f_{OSC}=430kHz$
L	$f_{OSC}=215kHz$

In the slave mode, it is connected to V_{DD} .

Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	Duty
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

Data Shift & Phase Select Control

Phase Selection

It is a circuit to shift data on synchronization of rising edge, or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

Data shift Direction Selection

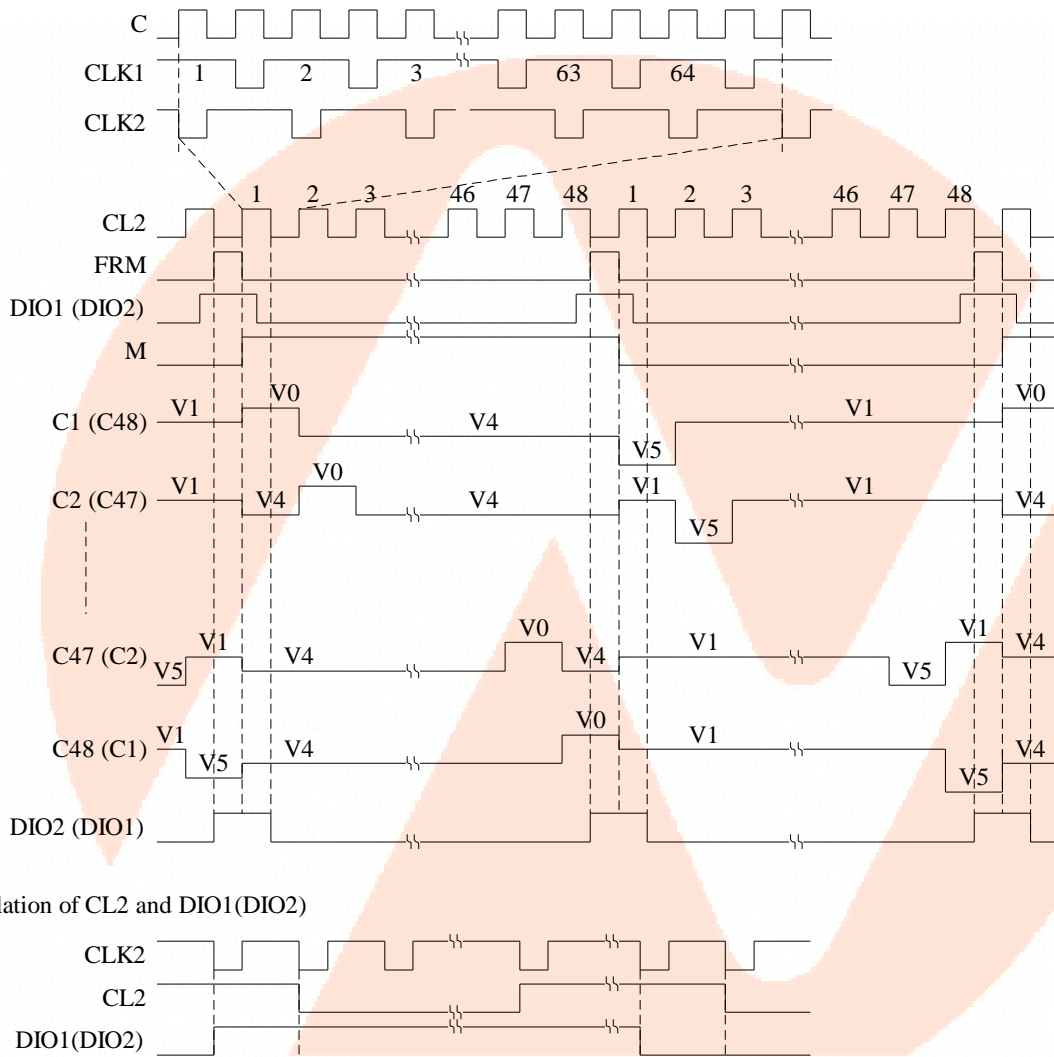
When MS is connected to VDD, DIO1 and DIO2 terminal is only output.

When MS is connected to Vss, it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1 à C64
	L	Output	Output	C64 à C1
L	H	Input	Output	DIO1 à C1 à C64 à DIO2
	L	Output	Input	DIO2 à C64 à C1 à DIO1

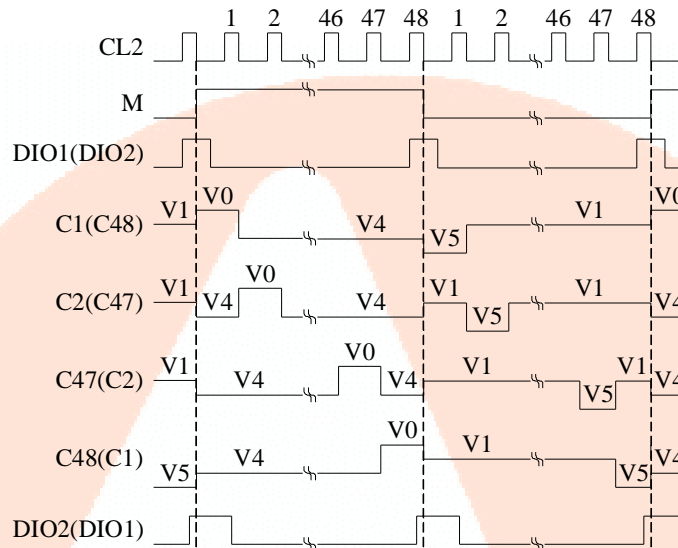
TIMING DIAGRAM
1/48 DUTY TIMING (MASTER MODE)

Condition: DS1=L, DS2=L, SHL=H (L), PCLK2=H

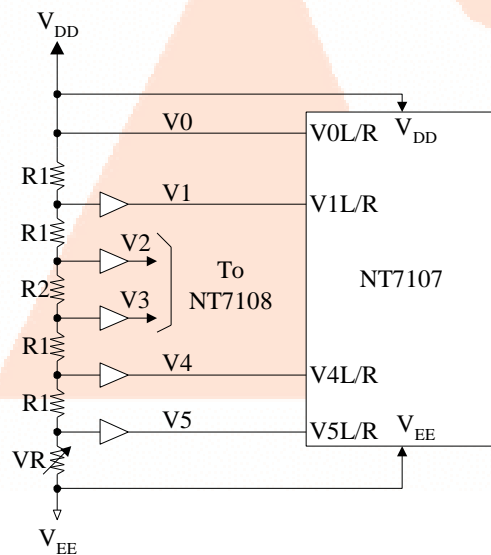


1/48 DUTY TIMING (SLAVE MODE)

Condition: SHL=H (L), PCLK2=L



POWER DRIVER CIRCUIT



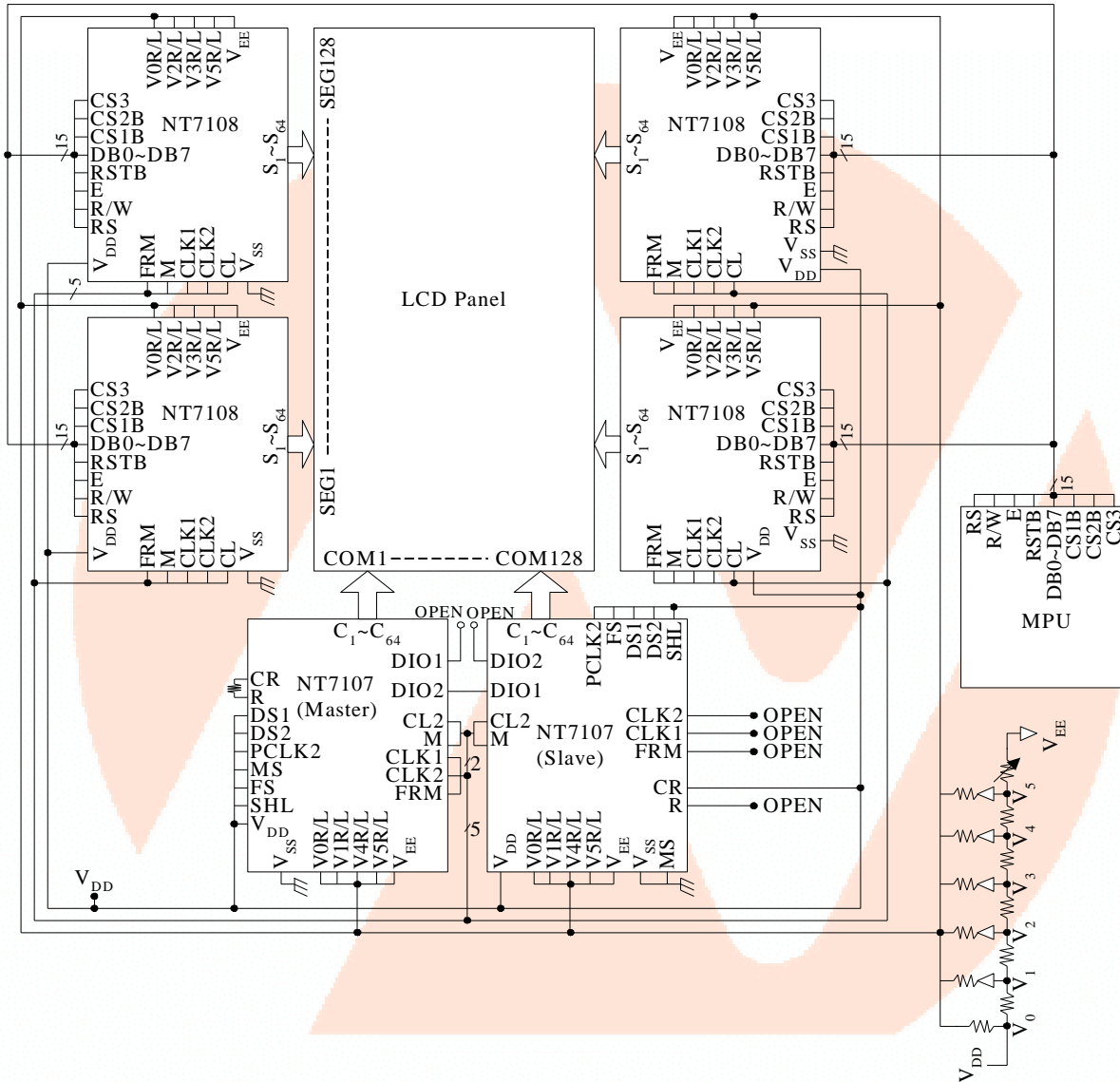
Relation of Duty & Bias

Duty	Bias	RDIV
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

When duty factor is 1/48, the value of R1 & R2 should satisfy.
 $R1/(4R1 + R2) = 1/8$;
 $R1 = 3k\Omega$, $R2 = 12k\Omega$

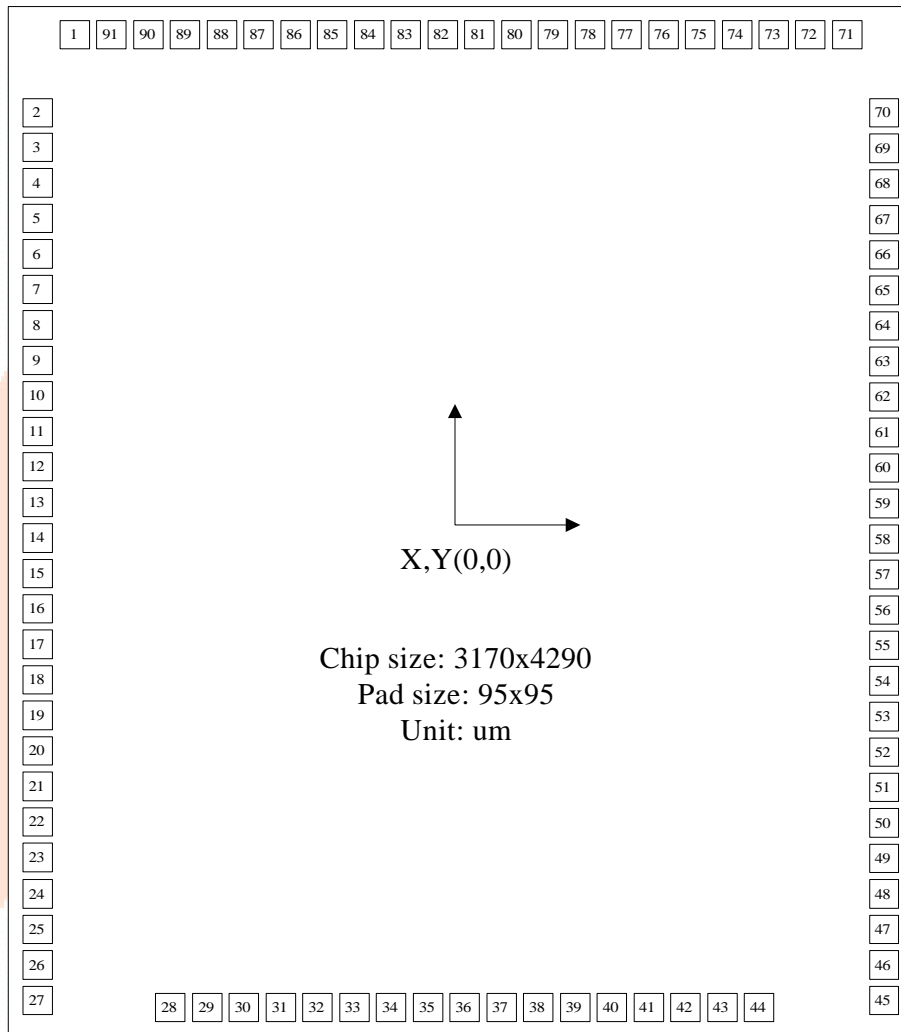
APPLICATION CIRCUIT

1/128 duty Segment driver (NT7108) interface circuit



PAD DIAGRAM

Note: Please connects the substrate to V_{DD} or floating.



PAD DIAGRAM

Pad No.	Pad name	X(μm)	Y(μm)	Pad No.	Pad name	X(μm)	Y(μm)
1	C22	-1312.5	2019	47	V4R	1461.3	-1743.5
2	C21	-1461.4	1131.5	48	V1R		-1618.5
3	C20		1006.5	49	VEE		-1493.5
4	C19		881.5	50	C64		-1368.5
5	C18		756.5	51	C63		-1243.5
6	C17		631.5	52	C62		-1118.5
7	C16		506.5	53	C61		-993.5
8	C15		381.5	54	C60		-868.5
9	C14		256.5	55	C59		-743.5
10	C13		131.5	56	C58		-618.5
11	C12		6.5	57	C57		-493.5
12	C11		-118.5	58	C56		-368.5
13	C10		-243.5	59	C55		-243.5
14	C9		-368.5	60	C54		-118.5
15	C8		-493.5	61	C53		6.5
16	C7		-618.5	62	C52		131.5
17	C6		-743.5	63	C51		256.5
18	C5		-868.5	64	C50		381.5
19	C4		-993.5	65	C49		506.5
20	C3		-1118.5	66	C48		631.5
21	C2		-1243.5	67	C47		756.5
22	C1		-1368.5	68	C46		881.5
23	VEE		-1493.5	69	C45		1006.5
24	V1L		-1618.5	70	C44		1131.5
25	V4L		-1743.5	71	C43	1312.5	2019.9
26	V5L		-1868.5	72	C42	1187.5	
27	V0L		-1993.5	73	C41	1062.5	
28	VDD	-1029.598	-2019.8	74	C40	937.5	
29	DIO1	-904.598		75	C39	812.5	
30	FS	-773.200		76	C38	687.5	
31	DS1	-648.198		77	C37	562.5	
32	DS2	-523.198		78	C36	437.5	
33	R	-398.198		79	C35	312.5	
34	CR	-273.198		80	C34	187.5	
35	SHL	-148.198		81	C33	62.5	
36	GND	-8.198		82	C32	-62.5	
37	MS	131.800		83	C31	-187.5	
38	CLK2	262.600		84	C30	-312.5	
39	CLK1	392.600		85	C29	-437.5	
40	FRM	522.800		86	C28	-562.5	
41	M	655.600		87	C27	-687.5	
42	PCLK2	785.800		88	C26	-812.5	
43	DIO2	916.000		89	C25	-937.5	
44	CL2	1046.000		90	C24	-1062.5	
45	V0R	1461.300	-1993.5	91	C23	-1187.5	
46	V5R	1461.300	-1868.5	-	-	-	-

VERSION HISTORY

Date	Description
6/5/2002	Add the notice of substrate connection.
12/11/2002	To correct some mistakes at page 6,8,10,11,15
12/18/2002	To correct some mistakes at page 4,5,6,8,9,14,15
03/15/2006	Add 100LQFP pin configuration



溫度監控系統U2.52a

新德科技

無鉛製程 IR Reflow Profile

