Advanced Communication Devices

INTRODUCTORY

Data Sheet: ACD82124

24 Ports 10/100 Fast Ethernet Switch Controller

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INTRODUCTORY

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1. GENERAL DESCRIPTION

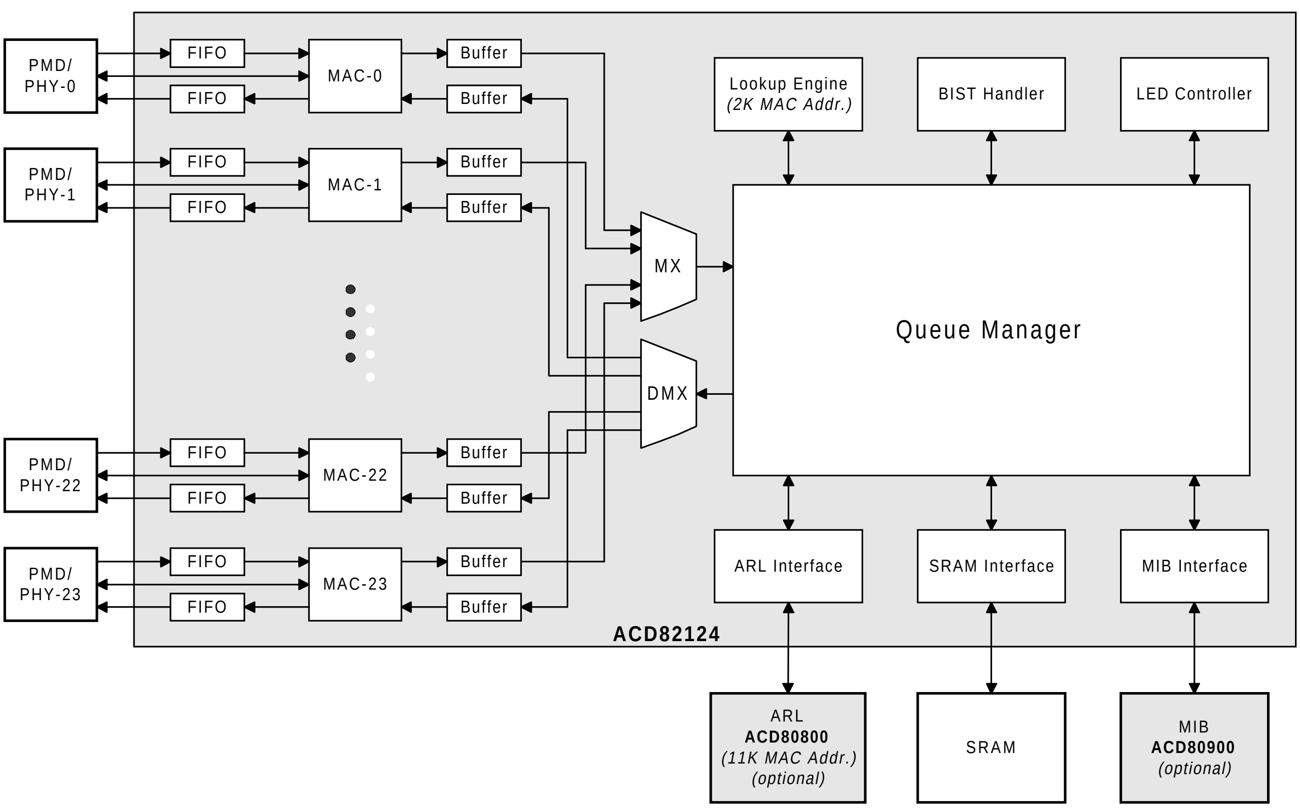
The ACD82124 is a single chip implementation of a 24 port 10/100 Ethernet switch system intended for IEEE 802.3 and 802.3u compatible networks. The device includes 24 independent 10/100 MACs. Each MAC interfaces with an external PMD/PHY device through a standard MII interface. Speed can be automatically configured through the MDIO port. Each port can operate at either 10Mbps or 100Mbps. The core logic of the ACD82124, implemented with patent pending BASIQ (Bandwidth Assured Switching with Intelligent Queuing) technology, can simultaneously process 24 asynchronous 10/100Mbps port traffic. The Queue Manager inside the ACD82124 provides the capability of routing traffic with the same order of sequence, without any packet loss.

A complete 24 port 10/100 switch can be built with the use of the ACD82124, 10/100 PHY and ASRAM. The MAC addresses can be expanded from the built-in 2K to 11K by the use of ACD's external ARL chip (ACD80800 Address Resolution Logic). Advanced network management features can be supported with the use of ACD's MIB (ACD80900 Management Information Base) chip.

2. FEATURES

- 24 ports 10/100 auto-sensing with MII interface
- Half-duplex operation, with optional full-duplex configuration by combining 2 adjacent ports
- 2.4 Gbps aggregated throughput
- True non-blocking switch architecture
- Flexible port configuration (up to 12 full duplex 10/100 ports, up to 24 half duplex 10/100 ports)
- Built-in storage of 2,000 MAC address
- Automatic source address learning
- Zero-Packet Loss back-pressure flow control
- Store-and-forward switch mode
- Port based V-LAN support
- UART type CPU management interface
- Supports up to 11K MAC addresses with the ACD80800
- RMON and SNMP support with ACD80900
- Status LEDs: Link, Speed, Full Duplex, Transmit, Receive, Collision and Frame Error
- Reversible MII option for CPU and expansion port interface
- Wire speed forwarding rate
- 576 pin BGA package
- 3.3V power supply, 3.3V I/O with 5V tolerance

3. SYSTEM BLOCK DIAGRAM



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4. SYSTEM DESCRIPTION

The ACD82124 is a single chip implementation of a 24-port Fast Ethernet switch. Together with external ASRAM and transceiver devices, it can be used to build a complete desktop class Fast Ethernet switch. Each individual port can be either auto-sensed or manually selected to run at 10 Mbps or 100 Mbps speed rate, under Half Duplex mode.

The ACD82124 Ethernet switch contains three major functional blocks: the Media Access Controller (MAC), the Queue Manager, and the Lookup Engine.

There are 24 independent MACs within the ACD82124. The MAC controls the receiving, transmitting, and deferring process of each individual port, in accordance to IEEE 802.3 and 802.3u standard. The MAC logic also provides framing, FCS checking, error handling, status indication and back-pressure flow control functions. Each MAC interfaces with an external transceiver through standard MII interface.

The device utilizes ACD's proprietary BASIQ (Bandwidth Assured Switching with Intelligent Queuing) technology. It is a technology to enforce the first-in-first-out rule of Ethernet Bridge-type devices in a very efficient way. The technology enables a true non-blocking frame switching operation at wire speed for a high throughput and high port density Ethernet switch.

The on-chip 2,000 MAC addresses Lookup Engine maps each destination address into a destination port. Each port's MAC address is automatically learned by the Lookup Engine when it receives a frame with no error. Therefore, the ACD82124 alone can be used to build a desktop class Fast Ethernet switch without any additional switching devices.

The MAC address space can be expanded from 2,000 to 8,000 per system by using the ACD80800. The ACD82124 has a proprietary ARL interface that allows direct connection with ACD80800. System designers can also use this ARL interface to implement a vendor-specific address resolution algorithm.

The ACD82124 provides management support through its MIB (Management Information Base) interface. The MIB interface can be used to monitor all traffic activities of the switch system. ACD's supporting chip (the ACD80900) provides a full set of statistical counters to support both SNMP and RMON network management. The MIB interface can also be used by system designers to implement vendor-specific network management functionality.

Among the 24 MII interfaces, 10 of them can be configured as reversed MII, to connect directly with standalone MAC controller devices. A MAC in the ACD82124 can be viewed logically as a PHY device if it is configured as a reversed MII interface. The reversed MII is intended for a CPU network interface, or expansion port interface.

A system CPU can access various registers inside the ACD82124 through a serial CPU management interface. The CPU can configure the switch by writing into the appropriate registers, or retrieve the status of the switch by reading the corresponding registers. The CPU can also access the registers of external transceiver (PHY) devices through the CPU management interface.

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5. FUNCTIONAL DESCRIPTION

The MAC controller performs transmit, receive, and defer functions, in accordance to IEEE 802.3 and 802.3u standard specification. The MAC logic also handles frame detection, frame generation, error detection, error handling, status indication and flow control functions.

Frame Format

The ACD82124 assumes that the received data packet will have the following format:

Preamble	SFD	DA	SA	Type/Len	Data	FCS

Where,

- *Preamble* is a repetitive pattern of '1010….' of any length with nibble alignment.
- *SFD* (Start Frame Delimiter) is defined as an octet pattern of 10101011.
- *DA* (Destination Address) is a 48-bit field that specifies the MAC address of the destined DTE. If the first bit of DA is 1, the ACD82124 will treat the frame as a broadcast/multicast frame and will forward the frame to all ports within the source port's VLAN except the source port itself or BPDU address.
- *SA* (Source Address) is a 48-bit field that contains the MAC address of the source DTE that is transmitting the frame to the ACD82124. After a frame is received with no error, the SA is learned as the port's MAC address.
- *Type/Len* field is a 2-byte field that specifies the type (DIX Ethernet frame) or length (IEEE 802.3 frame) of the frame. The ACD82124 does not process this information.
- *Data* is the encapsulated information within the Ethernet Packet. The ACD82124 does not process any of the data information in this field.
- *FCS* (Frame Check Sequence) is a 32-bit field of a CRC (Cyclic Redundancy Check) value based on the destination address, the source address, the type/length and the data field. The ACD82124 will verify the FCS field for each frame. The procedure of computing FCS is described in section of "FCS Calculation."

Start of Frame Detection

When a port's MAC is idle, assertion of the RXDV in the MII interface will cause the port to go into the receive state. The MII presents the received data in 4-bit nibbles that are synchronous to the receive clock (25Mhz or 2.5MHz). The ACD82124 will convert this data into a serial bit stream, and attempt to detect the occurrence of the SFD (10101011) pattern. All data prior to the detection of SFD are discarded. Once SFD is detected, the following frame data are forwarded and stored in the buffer of the switch.

Frame Reception

Under normal operating conditions, the ACD82124 expects a received frame to have a minimum inter frame gap (IFG). The minimum IFG required by the device is 80 BT (Bit Time).

In the event the ACD82124 receives a packet with IFG less than 80BT, the ACD82124 does not guarantee to be able to receive the frame. The packet will be dropped if the ACD82124 cannot receive the frame.

The device will check all received frames for errors such as symbol error, FCS error, short event, runt, long event, jabber etc. Frames with any kind of error will not be forwarded to any port.

Preamble Bit Processing

The preamble bit in the header of each frame will be used to synchronize the MAC logic with the incoming bit stream. The minimum length of the preamble is 0 bits and there is no limitation on the maximum length of preamble. After the receive data valid signal RXDV is asserted by the external PHY device, the port will wait for the occurrence of the SFD pattern (10101011) and then start a frame receiving process.

Source Address and Destination Address

After a frame is received by the ACD82124, the embedded destination address and source address are retrieved. The destination address is passed to the lookup table to find the destination port. The source address is automatically stored into the address lookup table. For applications that use an external ARL, the ACD82124 will disable the internal lookup table and pass the DA and SA to the external ARL for address lookup and learning.

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A port's MAC address register is cleared on power-up, hardware reset, or when the port enters into Link Fail state. If the SA aging option is enabled *(Register-16 bit 4)*, the learned SA will be cleared if it does not reappear within five minutes.

During the receive process, the Lookup Engine will attempt to match the destination address with the addresses stored in the address table. If a match is found, a link between the source port and the destination port is established. If an external ARL is used, the ACD82124 indicates the presence of a 48-bit DA through the status line of the ARL interface. The external ARL will use the value of DA for address comparison and return a result of the lookup to the ACD82124.

Frame Data

Frame data are transparent to the ACD82124. The ACD82124 will forward the data to the destination port(s) without interpreting the content of the frame data field.

FCS Calculation

Each port of the ACD82124 has CRC checking logic to verify if the received frame has a correct FCS value. A wrong FCS value is an indication of a fragmented frame or a frame with frame bit error. The method of calculating the CRC value is using the following polynomial,

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1$$

as a divider to divide the bit sequence of the incoming frame, beginning with the first bit of the destination address field, to the end of the data field. The result of the calculation, which is the residue after the polynomial division, is the value of the frame check sequence. This value should be equal to the FCS field appended at the end of the frame. If the value does not match the FCS field of the frame, the Frame Bit Error LED of the port will be turned on once and the packet will be dropped.

Frame Length

During the receiving process, the MAC will monitor the length of the received frame. Legal Ethernet frames should have a length of not less than 64 bytes and no more than 1518 bytes. If the carrier sense signal of a frame is asserted for less than 76 BT, the frame is flagged with short event error. If the length of a frame is less then 64 bytes, the frame is flagged with runt error.

In order to support an application where extra byte length is required, an Extra-Long-Frame option is provided. When the Extra long frame option is enabled *(Table 12: CFG7)*, only frames longer than 1530 bytes are marked with a long event error. Frame length is measured from the first byte of DA to the last byte of FCS.

Frame Filtering

Frames with any kind of error will be filtered. Types of error include code error (indicated by assertion of RXER signal), FCS error, alignment error, short event, runt, and long event.

Any frame heading to its own source port will be filtered. If external ARL is used, the ACD82124 will filter the frame as directed by the external ARL.

If the *Spanning Tree Support* option is enabled, frames containing DA equal to any reserved Bridge Management Group Address specified in Table 3.5 of IEEE 802.1d will not be forwarded to any ports, except the Port-23, which may receive BPDU frames. If spanning tree support is not enabled, frames with DA equal to the reserved Group Address for PBDU will be broadcasted to all ports in the same VLAN of the source port.

Jabber Lockup Protection

If a receiving port is active continuously for more than 50,000 BT, the port is considered to be jabbering. A jabbering port will automatically be partitioned from the switch system in order to prevent it from impairing the performance of the network. The partitioned port will be re-activated as soon as the offending signal discontinues.

Excessive Collision

In the event that there are more than 16 consecutive collision, the ACD82124 will reset the counter to zero and retransmit the packet. This implementation insures there is no packet loss even under channel capture situation. However, ACD82124 has an option to drop the packet on excessive collision. When this option is enabled *(Table 12: CG11)*, the frame will be dropped after 16 consecutive collisions.

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False Carrier Events

If the RXER signal in the MII interface is asserted when the receive data valid (RXDV) signal is not asserted, the port is considered to have a false carrier event. If a port has more than two consecutive false carrier events, the port will automatically be partitioned from the switch system. The partitioned port will be re-activated if it has been idling for 33,000 BT or it has received a valid frame.

Frame Forwarding

If the first bit of the destination address is 0, the frame is handled as a unicast frame. The destination address is passed to the Address Resolution Logic, which returns a destination port number to identify which port the frame should be forwarded to. If Address Resolution Logic cannot find any match for the destination address, the frame will be treated as a frame with unknown DA. The frame will be processed in one of two ways. If the option flood-to-all-port is enabled, the switch will forward the frame to all ports within the same VLAN of the source port, except the source port itself. If the option is not enabled, the frame will be forwarded to the 'dumping port' of the source port VLAN only. The dumping port is determined by the VLAN ID of the source port. If the source port belongs to multiple VLANs, a frame with unknown DA will then be forwarded to multiple dumping ports of the VLANs.

If the first bit of the destination address is a 1, the frame is handled as a multicast or broadcast frame. The ACD82124 does not differentiate a multicast packet from a broadcast packet except the reserved bridge management group address, as specified in table 3.5 of the IEEE 802.1d standard. The destination ports of the broadcast frame is all ports within the same VLAN except the source port itself.

The order of all broadcast frames with respect to the unicast frames is strictly enforced by the ACD82124.

Frame Transmission

The ACD82124 transmits all frames in accordance to IEEE 802.3 standard. The ACD82124 will send the frames with a guaranteed minimum interframe gap of 96 BT, even if the received frames have an IFG less than the minimum requirement. Before the transmit process is started, the MAC logic will check if the channel has been silent for more than 64 BT. Within the 64 BT silent window, the transmission process will defer on any receiving process. If the channel has been silent for more than 64 BT, the MAC will wait an additional 32 BT before starting the transmit process. In the event that the carrier sense signal is asserted by the MII during the wait period, the MAC logic will generate a JAM signal to cause a forced collision.

The MAC logic will abort the transmit process if a collision is detected through the assertion of the Col signal of the MII. Re-transmission of the frame is scheduled in accordance to IEEE 802.3's truncated binary exponential backoff algorithm. If the transmit process has encountered 16 consecutive collisions, an excessive collision error is reported, and the ACD82124 will try to re-transmit the frame, unless the drop-on-excessive-collision option of the port is enabled. It will first reset the number of collisions to zero and then start the transmission after 96 BT of interframe gap. If drop-on-excessive-collision is enabled, the ACD82124 will not try to re-transmit the frame after 16 consecutive collisions. If a collision is detected after 512 BT of the transmission, a late collision error will be reported, but the frame will still be retransmitted after proper backoff time.

Frame Generation

During a transmit process, frame data is read out from the memory buffer and is forwarded to the destination port's PHY device in nibbles. 7 bytes of preamble signal (10101010) will be generated first followed by the SFD (10101011), and then the frame data and 4 bytes of FCS are sent out last.

Frame Buffer

All ports of the ACD82124 work in Store-And-Forward mode so that all ports can support both 10Mbps and 100Mbps data speed. The ACD82124 utilizes a global memory buffer pool, which is shared by all ports. The device has a unique architecture that inherits the advantage of both output buffer-based and input buffer-based switches. An output buffer-based switch stores the received data only once into the memory, and hence has a short latency. Whereas an input buffer-based switch typically has more efficient flow control.

Flow Control

Under half duplex mode of operation, when the switch cannot handle the receiving of an incoming frame, a collision is generated by sending a jam pattern to the sending party to force it to back off and re-transmit the frame later. Back pressure flow control is applied to a port when its reserved-buffer is full and no more shared buffer is available, or when starvation control is active.

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This process is used to ensure that there are no dropped frames. *Backpressure flow control* can be disabled by setting the corresponding bit of the *register-21.*

VLAN Support *(register 23 & 24)*

The ACD82124 can support up to 4 port-based security VLANs. Each port of the ACD82124 can be assigned up to four VLAN. On power up, every port is assigned to VLAN-0 as default VLAN. Frames from the source port will only be forwarded to destination ports within the same VLAN domain. A broadcast/multicast frame will be forwarded to all ports within the VLAN(s) of the source port. A unicast frame will be forwarded to the destination port only if the destination port is in the same VLAN as the source port. Otherwise, the frame will be treated as a frame with unknown DA. Each VLAN can be assigned with a dedicated dumping port. Multiple VLANs can also share a dumping port. Unicast frames with unknown destination addresses will be forwarded to the dumping port of the source port VLAN.

Security VLAN can be disabled by setting the corresponding bit in the system configuration register (bit 8 of *Register 16*). When security VLAN is disabled, each VLAN becomes a leaky VLAN and is equivalent to a broadcast domain. Four dumping ports of four different virtual VLAN can be grouped together to form a fat pipe uplink (For example, if port 0&1, port 2&3, port 3&4, port 5&6 are combined to form 4 full duplex ports with 200Mbps per port throughput, these 4 full duplex ports can be grouped to form an 800 Mbps uplink port). When multiple dumping ports are grouped as a single pipe, each port has to be assigned to one and only one VLAN. A unicast frame with a matched DA will be forwarded to any destination, even if the VLAN ID is different. All unmatched DA packets will be forwarded to the designated dumping port of the source port VLAN. The broadcast and multicast packets will only be forwarded to the ports in the same VLAN of the source port. Therefore, a 200 to 800 Mbps pipe can be established by carefully grouping the dumping ports, and connects directly with the segmentation switches.

Dumping Port

Each VLAN can be assigned with a dedicated dumping port. Multiple VLANs can share a dumping port. Each dumping port can be used for up-link connection or for DTE connection. That is, the dumping port can be used to connect the switch with a computer repeater hub, a workgroup switch, a router, or any type of interconnecting device compliant with the IEEE 802.3 standard. The ACD82124 will direct the following frames to the dumping port:

- frame with unicast destination address that does not match with any port's source address within the VLAN of the source port
- frame with broadcast/multicast destination address*

* See *Spanning Tree Support*

If the device is configured to work under Flood-to-All-Port mode *(Register 25, bit 8)*, frames listed above will be forwarded to all the ports in the VLAN(s) of the source port except the source port itself.

Mode of Operation

By default, all ports of the ACD82124 work in half duplex mode. A full-duplex port can be configured by combining two half-duplex ports. In this case, the operation mode of the port is determined by the port's PHY device through auto-negotiation. The mode of a port can also be assigned by the duplex mode indication/assignment register *(Register 27)*.

Spanning Tree Support

The ACD82124 supports Spanning Tree protocol. When Spanning Tree Support is enabled *(Register 16 bit 1)*, frames from the CPU port (port 23) having a DA equal to the reserved Bridge Management Group Address for BPDU will be forwarded to the port specified by the CPU. Frames from all other ports with a DA equal to the Reserved Group Address for BPDU will be forwarded to the CPU port if the port is in the same VLAN of the CPU port. Port 23 is designed as the default CPU port. When Spanning Tree Support is disabled, all reserved group addresses for Bridge Management is treated as broadcast address.

Every port of the ACD82124 can be set to block-and-listen mode through the CPU interface. In this mode, incoming frames with DA equal to the reserved Group Address for BPDU will be forwarded to the CPU port. Incoming frames with all other DA value will be dropped. Outgoing frames with DA value equal to the Group Address for BPDU will be forwarded to the attached PHY device; all other outgoing frames will be filtered.

Queue Management

Each port of the ACD82124 has its own individual transmission queue. All frames coming into the ACD82124 are stored into the shared memory buffer,

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and are lined up in the transmission queues of the corresponding destination port. The order of all frames, unicast or broadcast, is strictly enforced by the ACD82124. The ACD82124 is designed with a non-blocking switching architecture. It is capable of achieving wire-speed frame forwarding rate and handling maximum traffic load.

MII Interface

The MAC of each port of the ACD82124 interfaces with the port's PHY device through the standard MII interface. For reception, the received data (RXD) can be sampled by the rising edge (default) or the falling edge of the receive clock (RXCLK). Assertion of the receive data valid (RXDV) signal will cause the MAC to look for start of Frame Delimiter (SFD). For transmission, the transmit data enable (TXEN) signal is asserted when the first preamble nibble is sent on the transmit data (TXD) lines. The transmit data are clocked out by the falling edge of the transmit clock (TXCLK).

The ACD82124 supports PHY device management through the serial MDIO and MDC signal lines. The ACD82124 can continuously poll the status of the PHY devices through the serial management interface, without CPU intervention. The ACD82124 will also configures the PHY capability field to ensure proper operation of the link. The ACD82124 also enables the CPU to access any registers in the PHY devices through the CPU interface.

Reversed MII Interface

Ten ports of the ACD82124 can be configured as reversed MII interface. Reversed MII behaves as a PHY MII, that the TXCLK, COL, RXD<3:0>, RXCLK, RXDV, CRS signals (names specified by IEEE 802.3u) become output signals of the ACD82124, and the TXER, TXD<3:0>, TXEN, RXER, signals (names specified by IEEE 802.3u) become input signals of the ACD82124. Reversed MII interface enables an external MAC device to be connected directly with the ACD82124.

ASRAM Interface

The ACD82124 requires the use of asynchronous SRAM as a memory buffer. Each read or write cycle takes up to 20 ns. An ASRAM chip with access speed at 12 ns or faster should be used. The ASRAM interface contains a 52-bit data bus, a 17-bit address bus and 4 chip-select signals.

CPU Interface

The ACD82124 does not require a microprocessor for operation. Initialization and most configurations can be done with the use of external hardware pins. However, the ACD82124 provides a CPU interface for a microprocessor to access some of its control registers and status registers. The microprocessor can send a read command to retrieve the status of the switch, or send a write command to configure the switch through a serial interface. This interface is a commonly used UART type interface. The CPU interface can also be used to access the registers inside each PHY device connected with the ACD82124.

ARL Interface

The ACD82124 has a built-in ARL that can store up to 2,000 MAC addresses. It is actually a subset of the full ACD80800 ARL IC. For detailed description, please refer to the ACD80800 Data Sheet. The UARTID for this built-in ARL is shared with the ACD82124 (CFG16 & 17).

The ACD82124 also provides an ARL interface *(Table 12: CFG9)* for supporting additional MAC addresses. Through the ARL interface, the external ARL (ACD80800) device can tap the value of DA out from the data bus in the ASRAM interface, and execute a lookup process to map the value of DA into a port number. The external ARL device also learns the SA values embedded in the received frames via the ARL interface. The value of SA is used to build up the address lookup table.

MIB Interface

Traffic activities on all ports of the ACD82124 can be monitored through the MIB interface. Through the MIB interface, a MIB device can view what the source port is receiving, or what the destination port is transmitting. Therefore, the MIB device can maintain a record of traffic statistics for each port to support network management. Since all received data are stored into the memory buffer, and all transmitted data are retrieved from the memory buffer, the data of the activities can also be captured from the data bus of ASRAM interface. The status of each data transaction between the ACD82124 and the ASRAM is displayed by some dedicated status signal pins of the ACD82124.

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LED Interface

The ACD82124 provides a wide variety of LED indicators for simple system management. The update of the LED is completely autonomous and merely requires low speed TTL or CMOS devices as LED drivers. The status display is designed to be flexible to allow the system designer to choose those indicators appropriate for the specification of the equipment.

There are two LED control signals, LEDVLD0 and LEDVLD1, used to indicate the start and end of the LED data signal. LEDCLK signal is a 2.5MHz clock signal. The rising edge of LEDCLK should be used to latch the LED data signal into the LED driver circuitry.

The LED data signals contain Lnk, Xmt, Rcv, Col, Err, Adr, Fdx and Spd, which represent Link status, Transmit status, Receive status, Collision indication, Frame error indication, Port Address learning status, Full duplex operation and Operational Speed status respectively. These status signals are sent out sequentially from port 23 to port 0, once every 50ms. For details about the timing diagrams of the LED signals, refer to the chapter of “Timing Description ”

Life Pulse

The ACD82124 continuously sends out life pulses to the WCHDOG pin when it is operating properly. In a catastrophic event, the ACD82124 will not send the life pulse to cause the external watchdog circuitry to time-up and reset the switch system.

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6. INTERFACE DESCRIPTION

MII Interface (MII)

The ACD82124 communicates with the external 10/ 100 Ethernet transceivers through standard MII interface. The signals of MII interface are described in *table-6.1*:

Table-6.1: MII Interface Signals

Name	Type	Description
PxCRS	I	Carrier sense
PxRXDV	I	Receive data valid
PxRXCLK	I	Receive clock (25/2.5 MHz)
PxRXERR	I	Receive error
PxRXD0	I	Receive data bit 0
PxRXD1	I	Receive data bit 1
PxRXD2	I	Receive data bit 2
PxRXD3	I	Receive data bit 3
PxCOL	I	Collision indication
PxTXEN	O	Transmit data valid
PxTXCLK	I	Transmit clock (25/2.5 MHz)
PxTXD0	O	Transmit data bit 0
PxTXD1	O	Transmit data bit 1
PxTXD2	O	Transmit data bit 2
PxTXD3	O	Transmit data bit 3

For MII interface, signal PxRXDV, PxRXER and PxRXD0 through PxRXD3 are sampled by the rising edge of PxRXCLK. Signal PxTXEN, and PxTXD0 through PxTXD3 are clocked out by the falling edge of PxTXCLK. The detailed timing requirement is described in the chapter of "Timing Description"

Ports 0,1, 2, 3, 4, 5, 6, 7, 22 and 23 can be configured as reversed MII ports (*Register 28*, the Reversed MII Enable register). These ports, when configured as "normal" MII, have the same characteristics as all other MII ports. However, when configured as reversed MII interface, they will behave logically like a PHY device, and can interface directly with a MAC device. The signal of reversed MII interface are described by *table-6.2*:

Note: * *Collision Indication* for half-duplex mode. *Not-Ready (output)* for full duplex mode.

Table-6.2: Reversed MII Interface Signals

Name	Type	Description
PxCRSR	O	Carrier sense
PxRXDVR	I	Transmit data valid
PxRXCLKR	O	Transmit clock (25/2.5 MHz)
PxRXERR	I	Not-Ready (Input)
PxRXD0R	I	Transmit data bit 0
PxRXD1R	I	Transmit data bit 1
PxRXD2R	I	Transmit data bit 2
PxRXD3R	I	Transmit data bit 3
PxCOLR	O	Collision Indication/ Not-Ready (Output)
PxTXENR	O	Receive data valid
PxTXCLKR	O	Receive clock (25/2.5 MHz)
PxTXD0R	O	Receive data bit 0
PxTXD1R	O	Receive data bit 1
PxTXD2R	O	Receive data bit 2
PxTXD3R	O	Receive data bit 3

For reversed MII interface, signal PxRXDVR, and PxRXD0R through PxRXD3R are clocked out by the falling edge of PxRXCLKR. Signal PxTXENR, and PxTXD0R through PxTXD3R can be sampled by the falling edge or rising edge of PxTXCLKR, depends on the setting of bit 9 of *Register 16*. The timing behavior is described in the chapter of "Timing Description."

PHY Management Interface

All control and status registers of the PHY devices are accessible through the PHY management interface. The interface consists of two signals: MDC and MDIO, which are described in *Table-6.3*.

Table-6.3: PHY Management Interface Signals

Name	Type	Description
MDC	O	PHY management clock (1.25MHz)
MDIO	I/O	PHY management data

Frames transmitted on MDIO has the following format (*Table-6.4*):

Table-6.4: MDIO Format

Operation	PRE	ST	OP	PHY-ID	REG-AD	TA	DATA	IDLE
Write	1…1	01	01	aaaaa	rrrrr	10	d…d	Z
Read	1…1	01	10	aaaaa	rrrrr	Z0	d…d	Z

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Prior to any transaction, the ACD82124 will output thirty-two bits of '1' as a preamble signal. After the preamble, a '01' signal is used to indicate the start of the frame.

For a write operation, the device will send a '01' to signal a write operation. Following the '01' write signal will be the 5 bit ID address of the PHY device and the 5 bit register address. A '10' turn around signal is then followed. After the turn around, the 16 bit of data will be written into the register. After the completion of the write transaction, the line will be left in a high impedance state.

For a read operation, the ACD82124 will output a '10' to indicate read operation after the start of frame indicator. Following the '10' read signal will be the 5-bit ID address of the PHY device and the 5-bit register address. Then, the ACD82124 will cease driving the MDIO line, and wait for one BT. During this time, the MDIO should be in a high impedance state. The ACD82124 will then synchronize with the next bit of '0' driven by the PHY device, and continue on to read 16 bits of data from the PHY device.

The system designer should set the ID of the PHY devices as '1' for port-0, '2' for port-1, … and '24' for port-23. The detail timing requirement on PHY management signals are described in the chapter of "Timing Description."

CPU Interface

The ACD82124 includes a CPU interface to enable an external CPU to access the internal registers of the ACD82124. The protocol used in the CPU is the asynchronous serial signal (UART). The baud rate can be from 1200 bps to 76800 bps. The ACD82124 automatically detects the baud rate for each command, and returns the result at the same baud rate. The signals in CPU interface are described in *Table-6.5*.

Table-6.5: CPU Interface Signals

Name	Type	Description
CPUDI	I	CPU data input
CPUDO	O	CPU data output
CPUIRQ	O	CPU interrupt request

A command sent by CPU comes through the CPUDI line. The command consists of 9 octets. Command frames transmitted on CPUDI have the following format (*Table-6.6*):

Table-6.6: CPU Command Format

Operation	Command	Register	Index	Data	Checksum
Write	0010XX11	8-bit	8-bit	24-bit	8-bit
Read	0010XX01	8-bit	8-bit	24-bit	8-bit

The byte order of data in all fields follows the big-endian convention, i.e. most significant octet first. The bit order is least significant order first. The Command octet specifies the type of the operation. Bit 2 and bit 3 of the command octet is used to specify the device ID of the chip. They are set by bit 16 and bit 17 of the *Register 25* at power on strobing. The address octet specifies the type of the register. The index octet specifies the ID of the register in a register array. For write operation, the Data field is a 4-octet value to specify what to write into the register. For read operation, the Data field is a 4-octet 0 as padded data. The checksum value is an 8-bit value of exclusive-OR of all octets in the frame, starting from the Command octet.

The ACD82124 will respond to each valid command received by sending a response frame through the CPUDO line. The response frames have the following format (*Table-6.7*):

Table-6.7: Response Format

Response	Command	Result	Data	Checksum
Write	00100011	8-bit	24-bit	8-bit
Read	00100001	8-bit	24-bit	8-bit

The command octet specifies the type of the response. The result octet specifies the result of the execution.

The Result field in a response frame is defined as:

- 00 for no error
- 01 for Checksum
- 10 for address incorrect
- 11 for MDIO waiting time-out

For response to a read operation, the Data field is a 3-octet value to indicate the content of the register. For response to a write operation, the Data field is 24 bits of 0. The checksum value is an 8-bit value of exclusive-OR of all octets in the response frame, starting from the Command octet.

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CPUIRQ is used to inform the CPU of some special status has been encountered by the ACD82124, like port partition, fatal system error, etc. By clearing the appropriate bit in the interrupt mask register, one can stop the specific source from generating an interrupt request. Reading the interrupt source register retrieves the source of the interrupt and clears the interrupt source register.

ASRAM Interface

All received frames are stored into the shared memory buffer through the ASRAM interface. When the destination port is ready to transmit the frame, data is read from the shared memory buffer through the ASRAM interface. The signals in ASRAM interface are described in *Table-6.8*.

Table-6.8: ASRAM Interface

Name	Type	Description
DATA0-DATA51	I/O	memory data bus
ADDR0-ADDR16	O	memory address bus
nOE	O	output enable, low active
nWE	O	write enable, low active
nCS0 - nCS3	O	chip select signals, low active.

Data is written into the ASRAM or read from the ASRAM in 52-bit wide words. The data is a 48-bit wide value and the control is a 4 bit-wide value. ADDR specifies the address of the word, and DATA contains the content of the word. Bit 0 ~ 47 of DATA bus are used to pass 48-bit frame data. Bit 48 are used to indicate the start and end of a frame. Bit 49 ~ 51 are used to indicate the length of actual data presented on DATA0 ~ DATA47.

nOE and nWE are used to control the timing of read or write operation respectively. nCSx selects the ASRAM chip corresponding to the word address. The timing requirement on ASRAM access is described in the chapter-9 “Timing Description”.

ARL Interface

ARL interface provides a communication path between the ACD82124 and an ARL device, which can provide up to 8K of additional address lookup function. As the ACD82124 receives a frame, the destination address and source address of the frame are displayed on the ARLDO data lines for the external ARL device. After the external ARL finds the corresponding destination port, it returns the result through the ARLDIx lines to the ACD82124. The timing requirement on ARL signals is described in *Chapter-9* “Timing Description.” *Table-6.9* shows the associated signals in ARL interface.

Table-6.9: ARL Interface Signals

Name	Type	Description
ARLDO0-RLDO51	O	ARL data output, shared with DATA 0 - DATA 51
ARLDIR1-ARLDIR0	O	ARL data direction indicator 00 for idle 01 for receive 10 for transmit 11 for control
ARLSYNC	O	ARL port synchronization
ARLSTAT0-ARLSTAT3	O	ARL data state indicator
ARLCLK	O	ARL clock
ARLDI0 - ARLDI3	I	ARL data input
ARLDIV	I	ARL input data valid

The data signal is tapped from the DATA bus of ASRAM interface. Since all data of the received frames will be written into the shared memory through the DATA bus, the bus can be used to monitor occurrences of DA and SA values, indicated by the status signal of ARLSTAT. Therefore, ARLD0 through ARLD51 are the same signals of DATA0 through DATA47.

ARLDIR1 and ARLDIR0 are used to indicate the direction of data on the ARLDO bus:

- 00: Idle
- 01: for receiving data
- 10: for transmitting data
- 11: Header

ARLSYNC is used to indicate port 0 is driving the DATA bus. Since the bus is pre-allocated in time division multiplexing manner, the ARL device can determine which port is driving the DATA bus.

ARLSTAT are used to indicate the status of the data shown on the first 48 bits of DATA bus. The 4-bit status is defined as:

- 0000 - Idle
- 0001 - First word (DA)
- 0010 - Second word (SA)
- 0011 - Third through last word
- 0100 - Filter Event
- 0101 - Drop Event
- 0110 - Jabber
- 0111 - False Carrier/Deferred Transmission*
- 1000 - Alignment error/Single Collision*

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Table-11: LED Interface Signals

Name	Type	Description	Signal Group 1	Signal Group 2
LEDVLD0	O	LED signal valid #0	1	0
LEDVLD1	O	LED signal valid #1	0	1
nLEDCLK	O	2.5 MHz LED clock	-	-
nLED0	O	Dual purpose indicator	address learning status	frame error indicator
nLED1	O	Dual purpose indicator	full duplex indication	collision indication
nLED2	O	Dual purpose indicator	port speed (1=10Mbps,0=100Mbps)	receiving activity
nLED3	O	Dual purpose indicator	Link status	transmit activity

- 1001 - Flow Control/Multiple Collision*
- 1010 - Short Event/Excessive Collision*
- 1011 - Runt/Late Collision*
- 1100 - Symbol Error
- 1101 - FCS Error
- 1110 - Long Event
- 1111 - Reserved

**Note: error type depends on whether the port is receiving or transmitting.*

ARLDIx is used to receive the lookup result from the external ARL. Result is returned by external ARL device through the ARLDIx lines. Returned data is sampled by the rising edge of ARLCLK. The ARL result has the following format:

SID	RSLT	DID

Where
- SID is a 5-bit ID of the source port (0 - 23)
- RSLT is a 2-bit result, defined as:
  - 00 - reserved
  - 01 - matched
  - 10 - not matched
  - 11 - forced discard
- DID is a 5-bit ID of the destination port (0 - 23)

The start of each ARL result is indicated by assertion of ARLDIV signal.

<u>LED Interface</u>

The signals in the LED interface is described in *table-6.10*:

The status of each port is displayed on the LED interface for every 50ms. LEDVLD0 and LEDVLD1 are used to indicate the start and end of the LED data. LED data is clocked out by the falling edge of LEDCLK, and should be sampled by the rising edge of LEDCLK. LED data of port 23 are clocked out first, followed by port 22 down to port 0. All LED signals are low active.

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Configuration Interface

There are 20 pins whose pull-up or pull-down state will be used as Power-On-Strobing configuration data *(Register 25, & CFG0 - CFG19)* to specify various working modes of the ACD82124. The CFG pins are shared with other functional pins of the ACD82124. The pull-high or pull-low status of the CFG pins are used to indicate specific configuration settings, described in *Table-6.11*. The register description section will provide more details about the *POS Configuration register*.

Table-6.11: Configuration Interface

<table>
<tr><th>Pin Name</th><th>Register #</th><th>Bit #</th><th>Setting</th></tr>
<tr><td>P7TXD0</td><td rowspan="19">25</td><td>0</td><td rowspan="19">See Table-7.25</td></tr>
<tr><td>P7TXD1</td><td>1</td></tr>
<tr><td>P7TXD2</td><td>2</td></tr>
<tr><td>P7TXD3</td><td>3</td></tr>
<tr><td>P6TXD0</td><td>4</td></tr>
<tr><td>P6TXD1</td><td>5</td></tr>
<tr><td>P6TXD2</td><td>6</td></tr>
<tr><td>P6TXD3</td><td>7</td></tr>
<tr><td>LEDCLK</td><td>8</td></tr>
<tr><td>LEDVLD0</td><td>9</td></tr>
<tr><td>LEDVLD1</td><td>10</td></tr>
<tr><td>nLED3</td><td>11</td></tr>
<tr><td>nLED2</td><td>12</td></tr>
<tr><td>nLED1</td><td>13</td></tr>
<tr><td>nLED0</td><td>14</td></tr>
<tr><td>P5TXD0</td><td>15</td></tr>
<tr><td>P5TXD1</td><td>16</td></tr>
<tr><td>P5TXD2</td><td>17</td></tr>
<tr><td>P5TXD3</td><td>18</td></tr>
<tr><td>P2TxD0</td><td rowspan="12">26</td><td>0</td><td rowspan="12">See Table-7.26</td></tr>
<tr><td>P2TxD1</td><td>1</td></tr>
<tr><td>P2TxD2</td><td>2</td></tr>
<tr><td>P2TxD3</td><td>3</td></tr>
<tr><td>P3TxD0</td><td>4</td></tr>
<tr><td>P3TxD1</td><td>5</td></tr>
<tr><td>P3TxD2</td><td>6</td></tr>
<tr><td>P3TxD3</td><td>7</td></tr>
<tr><td>P4TxD0</td><td>8</td></tr>
<tr><td>P4TxD1</td><td>9</td></tr>
<tr><td>P4TxD2</td><td>10</td></tr>
<tr><td>P4TxD3</td><td>11</td></tr>
<tr><td>P0TXD0</td><td rowspan="8">30</td><td>0</td><td rowspan="8">See Table-7.30</td></tr>
<tr><td>P0TXD1</td><td>1</td></tr>
<tr><td>P0TXD2</td><td>2</td></tr>
<tr><td>P0TXD3</td><td>3</td></tr>
<tr><td>P1TXD0</td><td>4</td></tr>
<tr><td>P1TXD1</td><td>5</td></tr>
<tr><td>P1TXD2</td><td>6</td></tr>
<tr><td>P1TXD3</td><td>7</td></tr>
<tr><td>P23TXD0R</td><td rowspan="4">20, inside the Internal ARL</td><td>0</td><td rowspan="2">See Appendix-A1</td></tr>
<tr><td>P23TXD1R</td><td>1</td></tr>
<tr><td>P23TXD2R</td><td>2</td><td rowspan="2">0</td></tr>
<tr><td>P23TXD3R</td><td>3</td></tr>
</table>

Other Interface (*Table-6.12*)

Table-6.12: Other Interface

Name	Type	Description
CLK50	I	50 MHz clock input
nRESET	I	hardware reset
WCHDOG	O	watch dog life pulse signal
VDD	-	3.3 V power
VSS	-	ground

CLK50 should come from a clock oscillator, with 0.01% (100 ppm) accuracy.

Assertion of the nRESET pin will cause the ACD82124 to go through the power-up initialization process. All registers are set to their default value after reset.

When the ACD82124 is working properly, it will generate pulses from the WCHDOG pin continuously. It is used as a safeguard, so that in case something unexpected happens, the external watchdog circuit will reset the switch system.

VDD is 3.3V power supply. VSS is power ground.

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7. REGISTER DESCRIPTION

Registers in the ACD82124 are used to define the operation mode of various function modules of the switch controller and the peripheral devices. Default values at power-on are defined by the factory. The management CPU (optional) can read the content of all registers and modify some of the registers to change the operation mode. Table-7.0 lists all the registers inside the switch controller.

INTSRC register (register 1)

The INTSRC register indicates the source of the interrupt request. Before the CPU starts to respond to an interrupt request, it should read this register to find out the interrupt source. This register is automatically cleared after each read. Table-7.1 lists all the bits of this register.

SYSERR register (register 2)

The SYSERR register indicates the presence of system errors. It is automatically cleared after each read. Table-7.2 lists all kind of system error.

Table-7.1: INTSRC Register

Bit	Description	Default
0	System initialization completed	0
1	System error occurred	0
2	Port partition occurred	0
3	ARL Interrupt	0
4	Reserved	0
5	Reserved	0
6	Reserved	0
7	Reserved	0

Table-7.2: SYSERR Register

Bit	Description	Default
0	BIST failure indication	0
1	Reserved	0
2	Reserved	0
3	Reserved	0
4	Reserved	0
5	Reserved	0
6	Reserved	0
7	Reserved	0
8	Reserved	0

Table-7.0: Register List

Address	Name	Type	Size	Depth	Description
0	Reserved				
1	INTSRC	R	8 Bit	1	Interrupt Source
2	SYSERR	R	24 Bit	1	System Error
3	PAR	R	24 Bit	1	Port Partition Indication
4	PMERR	R	24 Bit	1	PHY Management Error
5	ACT	R	24 Bit	1	Port Avtivity
6-15	Reserved				
16	SYSCFG	R/W	16 Bit	1	System Configuration
17	INTMSK	R/W	8 Bit	1	Interrupt Mask
18	SPEED	R/W	24 Bit	1	Port Speed
19	LINK	R/W	24 Bit	1	Port Link
20	nFWD	R/W	24 Bit	1	Port Forward Disable
21	nBP	R/W	24 Bit	1	Port Back Pressure Disable
22	nPORT	R/W	24 Bit	1	Port Disable
23	PVID	R/W	4 Bit	24	Port VLAN ID
24	VPID	R/W	5 Bit	4	VLAN Dumping Port
25	POSCFG	R/W	19 Bit	1	Power-On-Strobe Configuration
26	nPAUSE	R/W	24 Bit	1	Port Pause Frame Disable
27	DPLX	R/W	24 Bit	1	Port Duplex Mode
28	RVSMII	R/W	5 Bit	1	Reversed MII Selection
29	nPM	R/W	24 Bit	1	Port PHY Management Disable
30	ERRMSK	R/W	8 Bit	1	Error Mask
31	CLKADJ	R/W	4 Bit	1	ARL Clock Delay Adjustment
32-63	PHYREG	R/W	16 Bit	24	Registers in PHY device, (REG# - 32)

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PAR register (register 3)

The PAR register indicates the presence of the partitioned ports and the port ID. A port can be automatically partitioned if there is a consecutive false carrier event, an excessive collision or a jabber. This register is automatically cleared after each read. Table-7.3 lists all the bits of this register.

Table-7.3: PAR Register

Bit	Description	Default
0	0 - Port 0 not partitioned. 1 - Port 0 partitioned.	
1	0 - Port 1 not partitioned. 1 - Port 1 partitioned.	
2	0 - Port 2 not partitioned. 1 - Port 2 partitioned.	
3	0 - Port 3 not partitioned. 1 - Port 3 partitioned.	
4	0 - Port 4 not partitioned. 1 - Port 4 partitioned.	
5	0 - Port 5 not partitioned. 1 - Port 5 partitioned.	
6	0 - Port 6 not partitioned. 1 - Port 6 partitioned.	
7	0 - Port 7 not partitioned. 1 - Port 7 partitioned.	
8	0 - Port 8 not partitioned. 1 - Port 8 partitioned.	
9	0 - Port 9 not partitioned. 1 - Port 9 partitioned.	
10	0 - Port 10 not partitioned. 1 - Port 10 partitioned.	
11	0 - Port 11 not partitioned. 1 - Port 11 partitioned.	0
12	0 - Port 12 not partitioned. 1 - Port 12 partitioned.	
13	0 - Port 13 not partitioned. 1 - Port 13 partitioned.	
14	0 - Port 14 not partitioned. 1 - Port 14 partitioned.	
15	0 - Port 15 not partitioned. 1 - Port 15 partitioned.	
16	0 - Port 16 not partitioned. 1 - Port 16 partitioned.	
17	0 - Port 17 not partitioned. 1 - Port 17 partitioned.	
18	0 - Port 18 not partitioned. 1 - Port 18 partitioned.	
19	0 - Port 19 not partitioned. 1 - Port 19 partitioned.	
20	0 - Port 20 not partitioned. 1 - Port 20 partitioned.	
21	0 - Port 21 not partitioned. 1 - Port 21 partitioned.	
22	0 - Port 22 not partitioned. 1 - Port 22 partitioned.	
23	0 - Port 23 not partitioned. 1 - Port 23 partitioned.	

PMERR register (register 4)

The PMERR register indicates the presence of PHYs that have failed to respond to the PHY Management command issued through the MDIO line. This register is automatically cleared after each read. Table-7.4 describes all the bit of this register.

Table-7.4: PMERR Register

Bit	Description	Default
0	0 - Port 0 PHY responded 1 - Port 0 PHY failed to respond	
1	0 - Port 1 PHY responded 1 - Port 1 PHY failed to respond	
2	0 - Port 2 PHY responded 1 - Port 2 PHY failed to respond	
3	0 - Port 3 PHY responded 1 - Port 3 PHY failed to respond	
4	0 - Port 4 PHY responded 1 - Port 4 PHY failed to respond	
5	0 - Port 5 PHY responded 1 - Port 5 PHY failed to respond	
6	0 - Port 6 PHY responded 1 - Port 6 PHY failed to respond	
7	0 - Port 7 PHY responded 1 - Port 7 PHY failed to respond	
8	0 - Port 8 PHY responded 1 - Port 8 PHY failed to respond	
9	0 - Port 9 PHY responded 1 - Port 9 PHY failed to respond	
10	0 - Port 10 PHY responded 1 - Port 10 PHY failed to respond	
11	0 - Port 11 PHY responded 1 - Port 11 PHY failed to respond	0
12	0 - Port 12 PHY responded 1 - Port 12 PHY failed to respond	
13	0 - Port 13 PHY responded 1 - Port 13 PHY failed to respond	
14	0 - Port 14 PHY responded 1 - Port 14 PHY failed to respond	
15	0 - Port 15 PHY responded 1 - Port 15 PHY failed to respond	
16	0 - Port 16 PHY responded 1 - Port 16 PHY failed to respond	
17	0 - Port 17 PHY responded 1 - Port 17 PHY failed to respond	
18	0 - Port 18 PHY responded 1 - Port 18 PHY failed to respond	
19	0 - Port 19 PHY responded 1 - Port 19 PHY failed to respond	
20	0 - Port 20 PHY responded 1 - Port 20 PHY failed to respond	
21	0 - Port 21 PHY responded 1 - Port 21 PHY failed to respond	
22	0 - Port 22 PHY responded 1 - Port 22 PHY failed to respond	
23	0 - Port 23 PHY responded 1 - Port 23 PHY failed to respond	

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ACT register (register 5)

The ACT register indicates the presence of transmit or receive activities of each port since the register was last read. This register is automatically cleared after each read. Table-7.5 describes all the bits of this register.

Table-7.5: ACT Register

Bit	Description	Default
0	0 - Port 0 no activity 1 - Port 0 has activity	0
1	0 - Port 1 no activity 1 - Port 1 has activity	
2	0 - Port 2 no activity 1 - Port 2 has activity	
3	0 - Port 3 no activity 1 - Port 3 has activity	
4	0 - Port 4 no activity 1 - Port 4 has activity	
5	0 - Port 5 no activity 1 - Port 5 has activity	
6	0 - Port 6 no activity 1 - Port 6 has activity	
7	0 - Port 7 no activity 1 - Port 7 has activity	
8	0 - Port 8 no activity 1 - Port 8 has activity	
9	0 - Port 9 no activity 1 - Port 9 has activity	
10	0 - Port 10 no activity 1 - Port 10 has activity	
11	0 - Port 11 no activity 1 - Port 11 has activity	
12	0 - Port 12 no activity 1 - Port 12 has activity	
13	0 - Port 13 no activity 1 - Port 13 has activity	
14	0 - Port 14 no activity 1 - Port 14 has activity	
15	0 - Port 15 no activity 1 - Port 15 has activity	
16	0 - Port 16 no activity 1 - Port 16 has activity	
17	0 - Port 17 no activity 1 - Port 17 has activity	
18	0 - Port 18 no activity 1 - Port 18 has activity	
19	0 - Port 19 no activity 1 - Port 19 has activity	
20	0 - Port 20 no activity 1 - Port 20 has activity	
21	0 - Port 21 no activity 1 - Port 21 has activity	
22	0 - Port 22 no activity 1 - Port 22 has activity	
23	0 - Port 23 no activity 1 - Port 23 has activity	

SYSCFG register (register 16)

The SYSCFG register specifies certain system configurations. The system options are described in the chapter of "Function Description." Table-7.16 describes all the bit of this register.

Table-7.16: SYSCFG Register

Bit	Description	Default
0	0 - BIST enabled; 1 - BIST disabled.	0
1	0 - Spanning Tree support disabled; 1 - Spanning Tree support enabled	0
2	Reserved.	0
3	Reserved.	0
4	Reserved.	0
5	0 - wait for CPU. 1 - system ready to start **This bit is used by the CPU when bit-15 of register-25 is set as "0" (for system with control CPU). The system will wait for CPU to set this bit.*	0
6	0 - PHY Management not completed 1 - PHY Management completed. **This bit is used by the CPU when bit-15 of register-25 is set as "0" (for system with a control CPU). The MAC will not start until this bit is set sy the CPU.*	0
7	0 - Watchdog function enabled. 1 - Watchdog function disabled.	0
8	0 - Secure VLAN checking rule enforced. 1 - Leaky VLAN checking rule enforced.	0
9	0 - Rising edge of RXCLK to latch data. 1 - Falling edge of RXCLK to latch data. **For Reversed MII port only.*	0
10	0 - Late Back-Pressure scheme disabled 1 - Late Back-Pressure scheme enabled **When enabled, the MAC will generate back-pressure only after reading the first bit of DA*	0
11	0 - special handling of broadcast frames disabled 1 - special handling of broadcast frames enabled **When enabled, all broadcast frames from non-CPU port are forwarded to the CPU port only, and all broadcast frames from the CPU port are forwarded to all other ports.*	0
12	Software Reset: "1" to start a system reset to innitialize all state machines.	0
13	Hardware Reset: "1" to stop the life pulse on the watchdog pin, which in turn will trigger the external watchdog circuitry to reset the whole system.	
14	Reserved	0
15	Reserved	0

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INTMSK register (register 17)

The INTMSK register defines the valid interrupt sources allowed to assert interrupt request pin. Table-7.17 lists all the bits of this register.

Table-7.17: INTMSK Register

Bit	Description	Default
0	Enable "system initialization completion" to interrupt	1
1	Enable "internal system error" to interrupt	1
2	Enable "port partition event" to interrupt	1
3	Reserved	1
4	Reserved	1
5	Reserved	1
6	Reserved	1
7	Reserved	1

SPEED register (register 18)

The SPEED register specifies or indicates the speed rate of each port. It is read-only, unless the bit-12 of register-25 is set (through POS to disable automatic PHY management). At read-only mode, it indicates the speed achieved through PHY management. At the write-able mode, the control CPU will be able to assign speed rate for each port. Table-7.18 describes all the bit of this register.

LINK register (register 19)

The LINK register specifies or indicates the link status of each port. It is read-only, unless bit-12 of register-25 is set (through POS, to disable automatic PHY management). At read-only mode, it indicates the result achieved by PHY management. At write-able mode,

Table-7.18: SPEED Register

Bit	Description	Default
0	0 - Port 0 at 10 Mbps 1 - Port 0 at 100 Mbps	0
1	0 - Port 1 at 10 Mbps 1 - Port 1 at 100 Mbps	
2	0 - Port 2 at 10 Mbps 1 - Port 2 at 100 Mbps	
3	0 - Port 3 at 10 Mbps 1 - Port 3 at 100 Mbps	
4	0 - Port 4 at 10 Mbps 1 - Port 4 at 100 Mbps	
5	0 - Port 5 at 10 Mbps 1 - Port 5 at 100 Mbps	
6	0 - Port 6 at 10 Mbps 1 - Port 6 at 100 Mbps	
7	0 - Port 7 at 10 Mbps 1 - Port 7 at 100 Mbps	
8	0 - Port 8 at 10 Mbps 1 - Port 8 at 100 Mbps	
9	0 - Port 9 at 10 Mbps 1 - Port 9 at 100 Mbps	
10	0 - Port 10 at 10 Mbps 1 - Port 10 at 100 Mbps	
11	0 - Port 11 at 10 Mbps 1 - Port 11 at 100 Mbps	
12	0 - Port 12 at 10 Mbps 1 - Port 12 at 100 Mbps	
13	0 - Port 13 at 10 Mbps 1 - Port 13 at 100 Mbps	
14	0 - Port 14 at 10 Mbps 1 - Port 14 at 100 Mbps	
15	0 - Port 15 at 10 Mbps 1 - Port 15 at 100 Mbps	
16	0 - Port 16 at 10 Mbps 1 - Port 16 at 100 Mbps	
17	0 - Port 17 at 10 Mbps 1 - Port 17 at 100 Mbps	
18	0 - Port 18 at 10 Mbps 1 - Port 18 at 100 Mbps	
19	0 - Port 19 at 10 Mbps 1 - Port 19 at 100 Mbps	
20	0 - Port 20 at 10 Mbps 1 - Port 20 at 100 Mbps	
21	0 - Port 21 at 10 Mbps 1 - Port 21 at 100 Mbps	
22	0 - Port 22 at 10 Mbps 1 - Port 22 at 100 Mbps	
23	0 - Port 23 at 10 Mbps 1 - Port 23 at 100 Mbps	

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the control CPU can assign link status for each port. Table-7.19 describes all the bit of this register.

nFWD register (register 20)

The nFWD register defines the forwarding mode of each port. Under *forwarding* mode, a port can forward all frames. Under *block-and-listen* mode, a port will not forward regular frames, except BPDU frames. If the spanning tree algorithm discovers redundant links, the control CPU will allow only one link remaining in *forwarding* mode and force all other links into *block-and-listen* mode. Setting the associated bit in this register will put the port into *block-and-listen* mode. Table-7.20 describes all the bit of this register.

Table-7.19: LINK Register

Bit	Description	Default
0	0 - Port 0 link not established 1 - Port 0 link established	0
1	0 - Port 1 link not established 1 - Port 1 link established	
2	0 - Port 2 link not established 1 - Port 2 link established	
3	0 - Port 3 link not established 1 - Port 3 link established	
4	0 - Port 4 link not established 1 - Port 4 link established	
5	0 - Port 5 link not established 1 - Port 5 link established	
6	0 - Port 6 link not established 1 - Port 6 link established	
7	0 - Port 7 link not established 1 - Port 7 link established	
8	0 - Port 8 link not established 1 - Port 8 link established	
9	0 - Port 9 link not established 1 - Port 9 link established	
10	0 - Port 10 link not established 1 - Port 10 link established	
11	0 - Port 11 link not established 1 - Port 11 link established	
12	0 - Port 12 link not established 1 - Port 12 link established	
13	0 - Port 13 link not established 1 - Port 13 link established	
14	0 - Port 14 link not established 1 - Port 14 link established	
15	0 - Port 15 link not established 1 - Port 15 link established	
16	0 - Port 16 link not established 1 - Port 16 link established	
17	0 - Port 17 link not established 1 - Port 17 link established	
18	0 - Port 18 link not established 1 - Port 18 link established	
19	0 - Port 19 link not established 1 - Port 19 link established	
20	0 - Port 20 link not established 1 - Port 20 link established	
21	0 - Port 21 link not established 1 - Port 21 link established	
22	0 - Port 22 link not established 1 - Port 22 link established	
23	0 - Port 23 link not established 1 - Port 23 link established	

Table-7.20: nFWD Register

Bit	Description	Default
0	0 - Port 0 in forwarding state 1 - Port 0 in block-and-listen state	0
1	0 - Port 1 in forwarding state 1 - Port 1 in block-and-listen state	
2	0 - Port 2 in forwarding state 1 - Port 2 in block-and-listen state	
3	0 - Port 3 in forwarding state 1 - Port 3 in block-and-listen state	
4	0 - Port 4 in forwarding state 1 - Port 4 in block-and-listen state	
5	0 - Port 5 in forwarding state 1 - Port 5 in block-and-listen state	
6	0 - Port 6 in forwarding state 1 - Port 6 in block-and-listen state	
7	0 - Port 7 in forwarding state 1 - Port 7 in block-and-listen state	
8	0 - Port 8 in forwarding state 1 - Port 8 in block-and-listen state	
9	0 - Port 9 in forwarding state 1 - Port 9 in block-and-listen state	
10	0 - Port 10 in forwarding state 1 - Port 10 in block-and-listen state	
11	0 - Port 11 in forwarding state 1 - Port 11 in block-and-listen state	
12	0 - Port 12 in forwarding state 1 - Port 12 in block-and-listen state	
13	0 - Port 13 in forwarding state 1 - Port 13 in block-and-listen state	
14	0 - Port 14 in forwarding state 1 - Port 14 in block-and-listen state	
15	0 - Port 15 in forwarding state 1 - Port 15 in block-and-listen state	
16	0 - Port 16 in forwarding state 1 - Port 16 in block-and-listen state	
17	0 - Port 17 in forwarding state 1 - Port 17 in block-and-listen state	
18	0 - Port 18 in forwarding state 1 - Port 18 in block-and-listen state	
19	0 - Port 19 in forwarding state 1 - Port 19 in block-and-listen state	
20	0 - Port 20 in forwarding state 1 - Port 20 in block-and-listen state	
21	0 - Port 21 in forwarding state 1 - Port 21 in block-and-listen state	
22	0 - Port 22 in forwarding state 1 - Port 22 in block-and-listen state	
23	0 - Port 23 in forwarding state 1 - Port 23 in block-and-listen state	

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nBP register (register 21)

The nBP register defines back-pressure flow control capability for each port. Table-7.21 describes all the bit of this register.

Table-7.21: nBP Register

Bit	Description	Default
0	0 - Port 0 back-pressure scheme enabled 1 - Port 0 back-pressure scheme disabled	0
1	0 - Port 1 back-pressure scheme enabled 1 - Port 1 back-pressure scheme disabled	
2	0 - Port 2 back-pressure scheme enabled 1 - Port 2 back-pressure scheme disabled	
3	0 - Port 3 back-pressure scheme enabled 1 - Port 3 back-pressure scheme disabled	
4	0 - Port 4 back-pressure scheme enabled 1 - Port 4 back-pressure scheme disabled	
5	0 - Port 5 back-pressure scheme enabled 1 - Port 5 back-pressure scheme disabled	
6	0 - Port 6 back-pressure scheme enabled 1 - Port 6 back-pressure scheme disabled	
7	0 - Port 7 back-pressure scheme enabled 1 - Port 7 back-pressure scheme disabled	
8	0 - Port 8 back-pressure scheme enabled 1 - Port 8 back-pressure scheme disabled	
9	0 - Port 9 back-pressure scheme enabled 1 - Port 9 back-pressure scheme disabled	
10	0 - Port 10 back-pressure scheme enabled 1 - Port 10 back-pressure scheme disabled	
11	0 - Port 11 back-pressure scheme enabled 1 - Port 11 back-pressure scheme disabled	
12	0 - Port 12 back-pressure scheme enabled 1 - Port 12 back-pressure scheme disabled	
13	0 - Port 13 back-pressure scheme enabled 1 - Port 13 back-pressure scheme disabled	
14	0 - Port 14 back-pressure scheme enabled 1 - Port 14 back-pressure scheme disabled	
15	0 - Port 15 back-pressure scheme enabled 1 - Port 15 back-pressure scheme disabled	
16	0 - Port 16 back-pressure scheme enabled 1 - Port 16 back-pressure scheme disabled	
17	0 - Port 17 back-pressure scheme enabled 1 - Port 17 back-pressure scheme disabled	
18	0 - Port 18 back-pressure scheme enabled 1 - Port 18 back-pressure scheme disabled	
19	0 - Port 19 back-pressure scheme enabled 1 - Port 19 back-pressure scheme disabled	
20	0 - Port 20 back-pressure scheme enabled 1 - Port 20 back-pressure scheme disabled	
21	0 - Port 21 back-pressure scheme enabled 1 - Port 21 back-pressure scheme disabled	
22	0 - Port 22 back-pressure scheme enabled 1 - Port 22 back-pressure scheme disabled	
23	0 - Port 23 back-pressure scheme enabled 1 - Port 23 back-pressure scheme disabled	

nPORT register (register 22)

The nPORT register is used to isolate ports from the network. Setting the associated bit in this register will stop a port from receiving or transmitting any frame. Table-7.22 describes all the bits of this register.

Table-7.22: nPort Register

Bit	Description	Default
0	0 - Port 0 enabled 1 - Port 0 disabled	0
1	0 - Port 1 enabled 1 - Port 1 disabled	
2	0 - Port 2 enabled 1 - Port 2 disabled	
3	0 - Port 3 enabled 1 - Port 3 disabled	
4	0 - Port 4 enabled 1 - Port 4 disabled	
5	0 - Port 5 enabled 1 - Port 5 disabled	
6	0 - Port 6 enabled 1 - Port 6 disabled	
7	0 - Port 7 enabled 1 - Port 7 disabled	
8	0 - Port 8 enabled 1 - Port 8 disabled	
9	0 - Port 9 enabled 1 - Port 9 disabled	
10	0 - Port 10 enabled 1 - Port 10 disabled	
11	0 - Port 11 enabled 1 - Port 11 disabled	
12	0 - Port 12 enabled 1 - Port 12 disabled	
13	0 - Port 13 enabled 1 - Port 13 disabled	
14	0 - Port 14 enabled 1 - Port 14 disabled	
15	0 - Port 15 enabled 1 - Port 15 disabled	
16	0 - Port 16 enabled 1 - Port 16 disabled	
17	0 - Port 17 enabled 1 - Port 17 disabled	
18	0 - Port 18 enabled 1 - Port 18 disabled	
19	0 - Port 19 enabled 1 - Port 19 disabled	
20	0 - Port 20 enabled 1 - Port 20 disabled	
21	0 - Port 21 enabled 1 - Port 21 disabled	
22	0 - Port 22 enabled 1 - Port 22 disabled	
23	0 - Port 23 enabled 1 - Port 23 disabled	

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PVID registers (register 23)

The PVID registers assign VLAN IDs for each port. There are 24 PVID registers, one for each port. A PVID consists of 4 bits, each corresponding to one of the 4 VLANs. A port can belong to more than one VLAN at the same time. Table-7.23 describes the bits of one of the registers.

Table-7.23: PVID Registers *(24 registers)*

Bit	Description	Default
0	0 - port not in VLAN-I. 1 - port in VLAN-I.	1
1	0 - port not in VLAN-II. 1 - port in VLAN-II.	0
2	0 - port not in VLAN-III. 1 - port in VLAN-III.	0
3	0 - port not in VLAN-IV. 1 - port in VLAN-IV.	0

VPID registers (register 24)

The VPID registers specify the dumping port for each VLAN. There are 4 VPID 5-bit registers, one for each VLAN. A valid VPID are “0” through “23” (other values are reserved and should not used). Table-7.24 describes the bits one of the registers.

Table-7.24: VPID Registers *(4 registers)*

Bit	Description	Default
4:0	Dumping port ID for VLAN-1	"00000"
4:0	Dumping port ID for VLAN-2	"11111" dumping port not defined
4:0	Dumping port ID for VLAN-3	
4:0	Dumping port ID for VLAN-4	

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Table-7.25: POSCFG Register

Bit	Description	Default
3:0	8 timing adjustment levels for SRAM Read data latching: 0000 - no delay 0001 - level 1 delay 0011 - level 2 delay 0101 - level 3 delay 0111 - level 4 delay 1001 - level 5 delay 1011 - level 6 delay 1101 - level 7 delay 1111 - level 8 delay	0000
4	0 - Absolute address mode: 1 row of 512K words, nCS2=ADDR17, nCS3=ADDR18 1 - Chip-Select address mode: 4 rows of 128K words, nCS[3:0] to select 4 rows of memory	0
6:5	SRAM size selection: 00 - 64K words 01 - 128K words 10 - 256k words 11 - 512K words	000
7	0 - Long Event defined as frame longer than 1518 byte. 1 - Long Event defined as frame longer than 1530 byte.	0
8	0 - Frames with unknown DA forwarded to the dumping port. 1 - Frames with unknown DA forwarded to all ports.	0
9	0 - Internal ARL selected (2K MAC address entry). 1 - External ARL selected (11K MAC address entry).	0
10	0 - PHY IDs start from 1, range from 1 to 24. 1 - PHY IDs start from 4, range from 4 to 27.	0
11	0 - Re-transmit after excessive collision. 1 - Drop after excessive collision.	0
12	0 - Automatic PHY Management enabled 1 - Automatic PHY Management disabled: the control CPU need to update the SPEED, LINK, DPLX and nPAUSE registers	0
13	0 - Rising edge of RxClk triggering for regular MII ports 0 - Falling edge of RxClk triggering for regular MII ports	0
14	0 - Sysem errors will trigger software reset 1 - Sysem errors will trigger hardware reset	0
15	0 - System start itself without a control CPU 1 - System start after system-ready bit in register-16 is set by the control CPU	0
17:16	2-bit device ID for UART communication. The device responses only to UART commands with matching ID	00
18	0 - Rising edge of ARLCLK to latch ARLDI. 1 - Falling edge of ARLCLK to latch ARLDI.	0

POSCFG register (register 25)

The POSCFG register specifies a certain configuration setting for the switch system. The default values of this register can be changed through pull-up/pull-down of specific pins, as described in the “Configuration Interface” section of the “Interface Description” chapter. Table-7.25 describes all the bit of this register.

FdEn register (*register 26*)

FdEn register is used to specify if an even numbered port has been connected as a full duplex port. The default value of FdCfg is determined by Pull-High or Pull-Low status of the hardware pins shown in Table-26.

DPLX register (register 27)

The DPLX register specifies or indicates the half/full-duplex mode of each of the 12 even-numbered ports (*port 0, 2, 4, .. 20 and 22*). It is read-only, unless bit-12 of register-25 is set (through POS, to disable automatic PHY management). At read-only mode, it indicates the result achieved by the PHY management. At write-able mode, the control CPU can assign a half-duplex or full-duplex mode for each of the 12 even-

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Table-7.26: FdEn Register

Bit	Description	Default
0	0 - Port 0 & 1 each in Half-Duplex mode 1 - Port 0 & 1 paired into ONE Full-Duplex-Capable port	0
1	0 - Port 2 & 3 each in Half-Duplex mode 1 - Port 2 & 3 paired into ONE Full-Duplex-Capable port	
2	0 - Port 4 & 5 each in Half-Duplex mode 1 - Port 4 & 5 paired into ONE Full-Duplex-Capable port	
3	0 - Port 6 & 7 each in Half-Duplex mode 1 - Port 6 & 7 paired into ONE Full-Duplex-Capable port	
4	0 - Port 8 & 9 each in Half-Duplex mode 1 - Port 8 & 9 paired into ONE Full-Duplex-Capable port	
5	0 - Port 10 & 11 each in Half-Duplex mode 1 - Port 10 & 11 paired into ONE Full-Duplex-Capable port	
6	0 - Port 12 & 13 each in Half-Duplex mode 1 - Port 12 & 13 paired into ONE Full-Duplex-Capable port	
7	0 - Port 14 & 15 each in Half-Duplex mode 1 - Port 14 & 15 paired into ONE Full-Duplex-Capable port	
8	0 - Port 16 & 17 each in Half-Duplex mode 1 - Port 16 & 17 paired into ONE Full-Duplex-Capable port	
9	0 - Port 18 & 19 each in Half-Duplex mode 1 - Port 18 & 19 paired into ONE Full-Duplex-Capable port	
10	0 - Port 20 & 21 each in Half-Duplex mode 1 - Port 20 & 21 paired into ONE Full-Duplex-Capable port	
11	0 - Port 22 & 23 each in Half-Duplex mode 1 - Port 22 & 23 paired into ONE Full-Duplex-Capable port	

Table-7.27: DPLX Register

Bit	Description	Default
0	0 - Port 0 & 1 run as TWO independant Half-Duplex ports 1 - Port 0 & 1 pair run as ONE Full-Duplex port	0
1	0 - Port 2 & 3 run as TWO independant Half-Duplex ports 1 - Port 2 & 3 pair run as ONE Full-Duplex port	
2	0 - Port 4 & 5 run as TWO independant Half-Duplex ports 1 - Port 4 & 5 pair run as ONE Full-Duplex port	
3	0 - Port 6 & 7 run as TWO independant Half-Duplex ports 1 - Port 6 & 7 pair run as ONE Full-Duplex port	
4	0 - Port 8 & 9 run as TWO independant Half-Duplex ports 1 - Port 8 & 9 pair run as ONE Full-Duplex port	
5	0 - Port 10 & 11 run as TWO independant Half-Duplex ports 1 - Port 10 & 11 pair run as ONE Full-Duplex port	
6	0 - Port 12 & 13 run as TWO independant Half-Duplex ports 1 - Port 12 & 13 pair run as ONE Full-Duplex port	
7	0 - Port 14 & 15 run as TWO independant Half-Duplex ports 1 - Port 14 & 15 pair run as ONE Full-Duplex port	
8	0 - Port 16 & 17 run as TWO independant Half-Duplex ports 1 - Port 16 & 17 pair run as ONE Full-Duplex port	
9	0 - Port 18 & 19 run as TWO independant Half-Duplex ports 1 - Port 18 & 19 pair run as ONE Full-Duplex port	
10	0 - Port 20 & 21 run as TWO independant Half-Duplex ports 1 - Port 20 & 21 pair run as ONE Full-Duplex port	
11	0 - Port 22 & 23 run as TWO independant Half-Duplex ports 1 - Port 22 & 23 pair run as ONE Full-Duplex port	

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number ports. Table-7.27 describes all the bits of this register.

RVSMII register (register 28)

The RVSMII register defines the *reversed MII* mode for each port. Table-7.28 describes all the bits of this register.

Table-7.28: RVSMII register

Bit	Description	Default
0	0 - Port 0 under normal MII mode 1 - Port 0 under reversed MII mode	0
1	0 - Port 1under normal MII mode 1 - Port 1 under reversed MII mode	0
2	0 - Port 2 under normal MII mode 1 - Port 2under reversed MII mode	0
3	0 - Port 3 under normal MII mode 1 - Port 3 under reversed MII mode	0
4	0 - Port 4 under normal MII mode 1 - Port 4 under reversed MII mode	0
5	1 - Port 5 under normal MII mode 2 - Port 5 under reversed MII mode	0
6	1 - Port 6 under normal MII mode 2 - Port 6 under reversed MII mode	0
7	1 - Port 7 under normal MII mode 2 - Port 7 under reversed MII mode	0
8	1 - Port 22 under normal MII mode 2 - Port 22 under reversed MII mode	0
9	1 - Port 23 under normal MII mode 2 - Port 23 under reversed MII mode	0

nPM register (register 29)

The nPM register indicates the automatic PHY management capability of each port. If a bit is set in this register, the corresponding SPEED, LINK, DPLX, and nPAUSE status registers of a port will remain unchanged. Table-7.29 describes all the bits of this register.

Table-7.29: nPM Register

Bit	Description	Default
0	0 - Port 0 status update enabled 1 - Port 0 status update disabled	0
1	0 - Port 1 status update enabled 1 - Port 1 status update disabled	
2	0 - Port 2 status update enabled 1 - Port 2 status update disabled	
3	0 - Port 3 status update enabled 1 - Port 3 status update disabled	
4	0 - Port 4 status update enabled 1 - Port 4 status update disabled	
5	0 - Port 5 status update enabled 1 - Port 5 status update disabled	
6	0 - Port 6 status update enabled 1 - Port 6 status update disabled	
7	0 - Port 7 status update enabled 1 - Port 7 status update disabled	
8	0 - Port 8 status update enabled 1 - Port 8 status update disabled	
9	0 - Port 9 status update enabled 1 - Port 9 status update disabled	
10	0 - Port 10 status update enabled 1 - Port 10 status update disabled	
11	0 - Port 11 status update enabled 1 - Port 11 status update disabled	
12	0 - Port 12 status update enabled 1 - Port 12 status update disabled	
13	0 - Port 13 status update enabled 1 - Port 13 status update disabled	
14	0 - Port 14 status update enabled 1 - Port 14 status update disabled	
15	0 - Port 15 status update enabled 1 - Port 15 status update disabled	
16	0 - Port 16 status update enabled 1 - Port 16 status update disabled	
17	0 - Port 17 status update enabled 1 - Port 17 status update disabled	
18	0 - Port 18 status update enabled 1 - Port 18 status update disabled	
19	0 - Port 19 status update enabled 1 - Port 19 status update disabled	
20	0 - Port 20 status update enabled 1 - Port 20 status update disabled	
21	0 - Port 21 status update enabled 1 - Port 21 status update disabled	
22	0 - Port 22 status update enabled 1 - Port 22 status update disabled	
23	0 - Port 23 status update enabled 1 - Port 23 status update disabled	

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ERRMSK register (register 30)

The ERRMSK register defines certain errors as *system errors*. It is reserved for factory use only. Table-7.30 lists all the error masks specified by this register.

Table-7.30: ERRMSK register

Bit	Description	Setting
0	Reserved	All "1", unless otherwise advised, to ensure proper operation.
1	Reserved	
2	Reserved	
3	Reserved	
4	Reserved	
5	Reserved	
6	Reserved	
7	Reserved	0

CLKADJ register (register 31)

The CLKADJ register defines the delay time of the ARLCLK relative to the transition edge of the data signals. The ARLCLK provides reference timing for supporting chips, such as the ACD80800 and the ACD80900, which need to snoop the data bus for certain activities. Table-7.31 describes all the bits of this register.

Table-7.31: CLKADJ Register

Bit	Description	Default
0	0 - ARLCLK not inverted 1 - ARLCLK inverted	0
3:1	ARLCLK delay levels: 000 - level 0 delay 001 - level 1 delay 010 - level 2 delay 011 - level 3 delay 100 - level 4 delay 101 - level 5 delay 110 - level 6 delay 111 - level 7 delay	000

PHYREG registers (register 32-63)

The PHYREG refers to the registers residing on the PHY devices. There are 24 sets of these registers. Each port has its own corresponding set of register 32-63. The ACD82124 merely provides an access path for the control CPU to access the registers on the PHYs. For detailed information about these registers, please refer to the PHY data sheet.

Since the native registers ID "0" through "31" on the PHYs have been used by the internal registers of the ACD82124, they need to be re-mapped into "32" through "63" by adding "32" to each original register ID. An index is used by the ACD82124 to specify the PHY ID. For example, register-32 with index-4 would refer to the control register (register-0) in the PHY-4.

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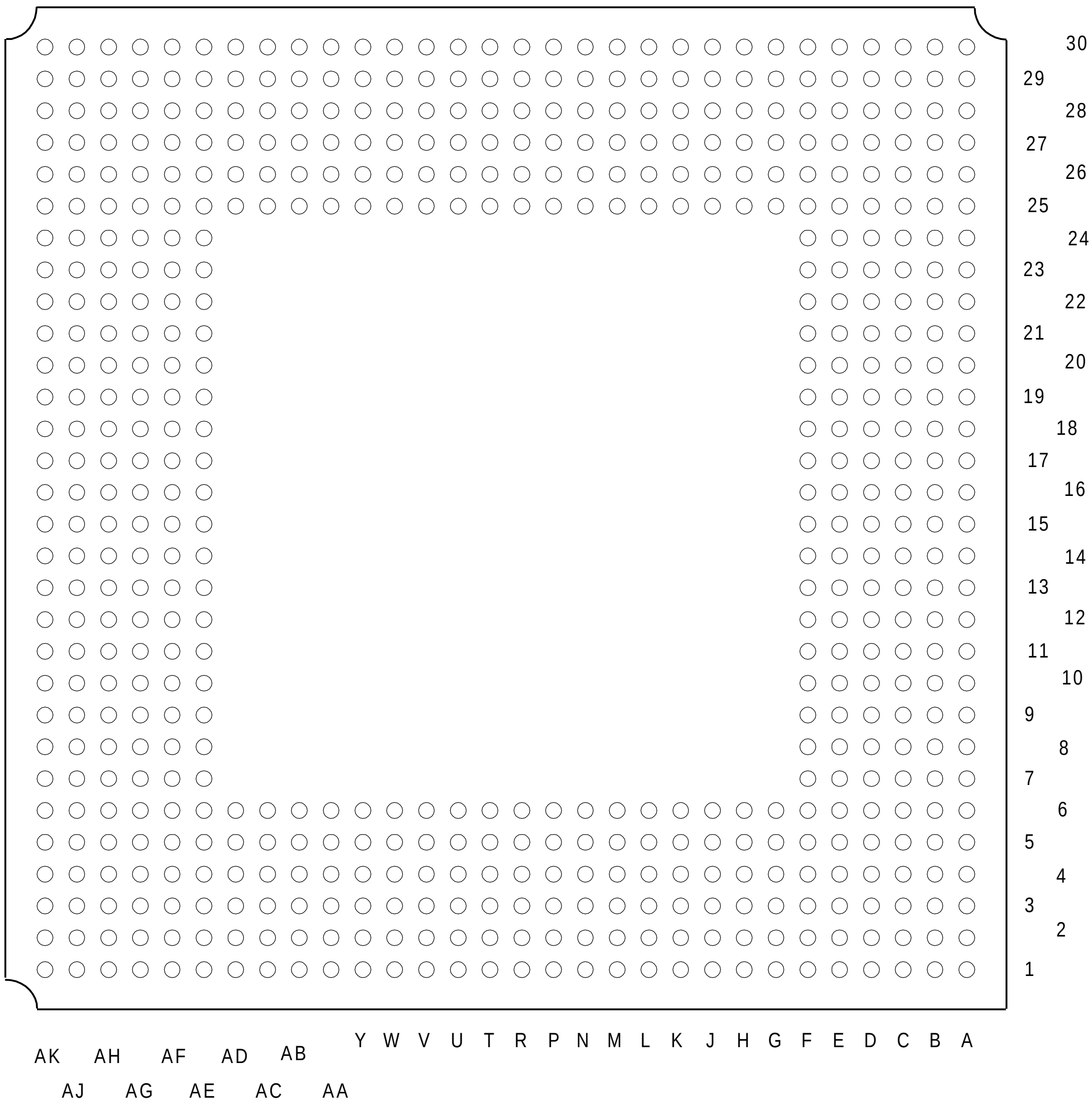
8. PIN DESCRIPTIONS

Pin Diagram
Bottom View



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Pin List By Location: Part 1

Pin	Signal Name	I/O Type	Pin	Signal Name	I/O Type	Pin	Signal Name	I/O Type	Pin	Signal Name	I/O Type
A01	P23RXD0R	I	C13	P20RXCLK	I	E25	P16TXD1	O	K01	DATA40	I/O
A02	VDD		C14	P20TXD0	O	E26	VDD		K02	DATA39	I/O
A03	P23TXD2R	O	C15	P19RXD3	I	E27	P15RXCLK	I	K03	ADDR2	O
A04	P22RXD3R	I	C16	P19RXCLK	I	E28	P15TXD3	O	K04	nCS3	O
A05	P22RXERR	I	C17	P19TXD0	O	E29	P14RXD0	I	K05	VDD	
A06	P22TXD1R	O	C18	P19COL	I	E30	P14TXEN	O	K06	VSS	
A07	P22TXD3R	O	C19	P18RXD1	I	F01	DATA48	I/O	K25	VSS	
A08	P21RXD0	I	C20	P18RXER	I	F02	DATA47	I/O	K26	VDD	
A09	P21TXCLK	I	C21	P18TXD1	O	F03	ARLDI3	I	K27	P13RXD0	I
A10	P21TXD0	O	C22	P17RXD2	I	F04	ARLCLK	O	K28	P13TXCLK	I
A11	P20RXD3	I	C23	P17RXCLK	I	F05	ARLSYNC	O	K29	P13TXD1	O
A12	P20RXD0	I	C24	P17TXD2	O	F06	VSS		K30	P13TXD2	O
A13	P20TXCLK	I	C25	P17CRS	I	F07	P23RXERR	I	L01	DATA38	I/O
A14	P20TXD2	O	C26	P16RXD0	I	F08	VSS		L02	DATA37	I/O
A15	P19RXD1	I	C27	P16TXD3	O	F09	P22RXD1R	I	L03	ADDR3	O
A16	P19RXD0	I	C28	P15RXD2	I	F10	VSS		L04	nCS2	O
A17	P19TXCLK	I	C29	P15TXD0	O	F11	P22CRSR	I/O	L05	VDD	
A18	P19TXD2	O	C30	P15COL	I	F12	VSS		L06	VSS	
A19	VSS		D01	STAT3	O	F13	P21COL	I	L25	P13RXD2	I
A20	P18RXDV	I	D02	DATA51	I/O	F14	VSS		L26	P13RXD1	I
A21	P18TXEN	O	D03	ARLDI0	I	F15	P20TXD3	O	L27	P13TXEN	O
A22	P18CRS	I	D04	P23RXD3R	I	F16	VSS		L28	P13TXD3	O
A23	P17RXD1	I	D05	P23RXCLKR	I/O	F17	VSS		L29	P13COL	I
A24	P17RXER	I	D06	P23TXD0R	O	F18	P18RXD2	I	L30	P12RXD1	I
A25	P17TXD3	O	D07	P23COLR	I/O	F19	VSS		M01	DATA36	I/O
A26	P16RXD2	I	D08	P22RXDVR	I	F20	P18TXD3	O	M02	DATA35	I/O
A27	P16RXER	I	D09	P22TXD0R	O	F21	VSS		M03	nCS0	O
A28	P16TXD0	O	D10	P21RXD2	I	F22	P17TXD0	O	M04	ADDR16	O
A29	P16CRS	I	D11	P21RXER	I	F23	VSS		M05	VDD	
A30	P15RXD0	I	D12	P21TXD3	O	F24	P16TXCLK	I	M06	VSS	
B01	STAT0	O	D13	P20RXDV	I	F25	VSS		M25	VSS	
B02	P23RXD1R	I	D14	P20TXEN	O	F26	P15RXDV	I	M26	VDD	
B03	P23TXCLKR	I/O	D15	P20CRS	I	F27	P15TXD2	O	M27	P13CRS	I
B04	P23TXD3R	O	D16	P19RXDV	I	F28	P14RXD2	I	M28	P12RXD0	I
B05	P22RXD2R	I	D17	P19TXD1	O	F29	P14TXD0	O	M29	P12RXDV	I
B06	P22TXCLKR	I/O	D18	P19CRS	I	F30	P14TXD3	O	M30	P12RXCLK	I
B07	P22TXD2R	O	D19	P18RXD0	I	G01	DATA46	I/O	N01	DATA34	I/O
B08	P21RXD1	I	D20	P18TXCLK	I	G02	DATA45	I/O	N02	DATA33	I/O
B09	P21RXDV	I	D21	P18COL	I	G03	ARLDIR0	O	N03	VDD	
B10	P21TXEN	O	D22	P17RXD0	I	G04	ARLDIR1	O	N04	ADDR15	O
B11	P21TXD2	O	D23	P17TXD1	O	G05	VDD		N05	VDD	
B12	P20RXD1	I	D24	P16RXD3	I	G06	VSS		N06	VSS	
B13	P20RXER	I	D25	P16RXCLK	I	G25	P15RXER	I	N25	P12RXD3	I
B14	P20TXD1	O	D26	P16TXD2	O	G26	P15TXD1	O	N26	P12RXD2	I
B15	P19RXD2	I	D27	P15RXD3	I	G27	P14RXD3	I	N27	P12RXER	I
B16	P19RXER	I	D28	P15TXCLK	I	G28	P14TXCLK	I	N28	P12TXCLK	I
B17	P19TXEN	O	D29	P15CRS	I	G29	P14COL	I	N29	P12TXEN	O
B18	P19TXD3	O	D30	P14RXD1	I	G30	P14CRS	I	N30	P12TXD0	O
B19	VDD		E01	DATA50	I/O	H01	DATA44	I/O	P01	DATA32	I/O
B20	P18RXCLK	I	E02	DATA49	I/O	H02	DATA43	I/O	P02	DATA31	I/O
B21	P18TXD0	O	E03	ARLDI2	I	H03	ADDR0	O	P03	nWE	O
B22	P17RXD3	I	E04	ARLDI1	I	H04	ARLDIV	I	P04	VSS	
B23	P17RXDV	I	E05	VDD		H05	VDD		P05	VDD	
B24	P17TXCLK	I	E06	P23RXDVR	I	H06	VSS		P06	VSS	
B25	P17COL	I	E07	P23TXENR	O	H25	VSS		P25	VSS	
B26	P16RXD1	I	E08	VDD		H26	VDD		P26	VDD	
B27	P16TXEN	O	E09	P22RXD0R	I	H27	P14RXER	I	P27	P12TXD1	O
B28	P16COL	I	E10	VDD		H28	P14TXD1	O	P28	P12TXD2	O
B29	P15RXD1	I	E11	P21RXD3	I	H29	P13RXDV	I	P29	P12TXD3	O
B30	P15TXEN	O	E12	VDD		H30	P13RXCLK	I	P30	P12COL	I
C01	STAT1	O	E13	P21CRS	I	J01	DATA42	I/O	R01	DATA30	I/O
C02	STAT2	O	E14	VDD		J02	DATA41	I/O	R02	DATA29	I/O
C03	P23RXD2R	I	E15	P20COL	I	J03	ADDR1	O	R03	ADDR4	O
C04	VSS		E16	VDD		J04	nCS1	O	R04	nOE	I/O
C05	P23TXD1R	O	E17	VDD		J05	VDD		R05	VDD	
C06	P23CRSR	I/O	E18	P18RXD3	I	J06	VSS		R06	VSS	
C07	P22RXCLKR	I/O	E19	VDD		J25	P14RXDV	I	R25	P12CRS	I
C08	P22TXENR	O	E20	P18TXD2	O	J26	P14RXCLK	I	R26	P11RXD3	I
C09	P22COLR	I/O	E21	VDD		J27	P14TXD2	O	R27	P11RXD2	I
C10	P21RXCLK	I	E22	P17TXEN	O	J28	P13RXD3	I	R28	P11RXD1	I
C11	P21TXD1	O	E23	VDD		J29	P13RXER	I	R29	P11RXD0	I
C12	P20RXD2	I	E24	P16RXDV	I	J30	P13TXD0	O	R30	P11RXDV	I

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Pin List By Location: Part 2

Pin	Signal Name	I/O Type	Pin	Signal Name	I/O Type	Pin	Signal Name	I/O Type	Pin	Signal Name	I/O Type
T01	DATA28	I/O	AB01	DATA16	I/O	AF07	P0TXENR	O	AH19	P4RXD0R	I
T02	DATA27	I/O	AB02	DATA15	I/O	AF08	VDD		AH20	P5TXD3R	I/O
T03	ADDR5	O	AB03	VDD		AF09	P1TXD3R	I/O	AH21	P5TXCLKR	I/O
T04	ADDR14	O	AB04	LED3	I/O	AF10	VDD		AH22	P5RXD3R	I
T05	VDD		AB05	VDD		AF11	P1RXD3R	I	AH23	P6TXD1R	I/O
T06	VSS		AB06	VSS		AF12	VDD		AH24	P6TXCLKR	I/O
T25	VSS		AB25	VSS		AF13	P2RXD1R	I	AH25	P6RXD2R	I
T26	VDD		AB26	VDD		AF14	VDD		AH26	P7TXD3R	I/O
T27	P11RXER	I	AB27	P9TXCLK	I	AF15	VDD		AH27	VDD	
T28	P11TXCLK	I	AB28	P9RXCLK	I	AF16	P3RXD3R	I	AH28	P7RXD0R	I
T29	P11TXEN	O	AB29	P9RXDV	I	AF17	VDD		AH29	P7RXD3R	I
T30	P11RXCLK	I	AB30	P9RXD0	I	AF18	P4RXD2R	I	AH30	P8TXD2	O
U01	DATA26	I/O	AC01	DATA14	I/O	AF19	VDD		AJ01	DATA2	I/O
U02	DATA25	I/O	AC02	DATA13	I/O	AF20	P5RXD1R	I	AJ02	DATA1	I/O
U03	ADDR6	O	AC03	LED2	I/O	AF21	VDD		AJ03	VSS	
U04	ADDR13	O	AC04	LED0	I/O	AF22	P6RXCLKR	I/O	AJ04	P0TXD3R	I/O
U05	VDD		AC05	VDD		AF23	VDD		AJ05	P0RXERR	I
U06	VSS		AC06	VSS		AF24	P7TXD1R	I/O	AJ06	P0RXD1R	I
U25	VSS		AC25	VSS		AF25	P7RXERR	I	AJ07	P1TXD2R	I/O
U26	VDD		AC26	VDD		AF26	VDD		AJ08	P1TXENR	O
U27	P11TXD3	O	AC27	P9TXD3	O	AF27	P8COL	I	AJ09	P1RXDVR	I
U28	P11TXD2	O	AC28	P9TXD0	O	AF28	P8RXCLK	I	AJ10	P2COLR	I/O
U29	P11TXD1	O	AC29	P9TXEN	O	AF29	P8RXDV	I	AJ11	P2TXD0R	I/O
U30	P11TXD0	O	AC30	P9RXER	I	AF30	P8RXD0	I	AJ12	P2RXCLKR	I/O
V01	DATA24	I/O	AD01	DATA12	I/O	AG01	DATA6	I/O	AJ13	P3CRSR	I/O
V02	DATA23	I/O	AD02	DATA11	I/O	AG02	DATA5	I/O	AJ14	P3TXD1R	I/O
V03	ADDR7	O	AD03	LED1	I/O	AG03	CPUIRQ	O	AJ15	P3TXENR	O
V04	ADDR12	O	AD04	LEDVLD0	I/O	AG04	MDC	O	AJ16	P3RXD0R	I
V05	VDD		AD05	VDD		AG05	nRESET	I	AJ17	P4TXD3R	I/O
V06	VSS		AD06	VSS		AG06	P0TXD0R	I/O	AJ18	P4TXENR	O
V25	P10RXD0	I	AD25	P8TXD0	O	AG07	P0RXDVR	I	AJ19	P4RXDVR	I
V26	P10RXD1	I	AD26	P8RXER	I	AG08	P1CRSR	I/O	AJ20	P5COLR	I/O
V27	P10RXD2	I	AD27	P8RXD1	I	AG09	P1TXCLKR	I/O	AJ21	P5TXD1R	I/O
V28	P10RXD3	I	AD28	P9COL	I	AG10	P1RXD1R	I	AJ22	P5RXERR	I
V29	P11CRS	I	AD29	P9TXD2	O	AG11	P2TXD2R	I/O	AJ23	P5RXDVR	I
V30	P11COL	I	AD30	P9TXD1	O	AG12	P2TXCLKR	I/O	AJ24	P6COLR	I/O
W01	DATA22	I/O	AE01	DATA10	I/O	AG13	P2RXD2R	I	AJ25	P6TXD0R	I/O
W02	DATA21	I/O	AE02	DATA9	I/O	AG14	P3TXD3R	I/O	AJ26	P6RXD0R	I
W03	ADDR8	O	AE03	LEDVLD1	I/O	AG15	P3RXERR	I	AJ27	P7CRSR	I/O
W04	ADDR11	O	AE04	LEDCLK	I/O	AG16	P3RXD2R	I	AJ28	P7TXD0R	I/O
W05	VDD		AE05	VSS	I	AG17	P4TXD1R	I/O	AJ29	P7RXDVR	I
W06	VSS		AE06	VSS		AG18	P4RXERR	I	AJ30	P7RXD2R	I
W25	VSS		AE07	P0TXD2R	I/O	AG19	P5CRSR	I/O	AK01	DATA0	I/O
W26	VDD		AE08	VSS		AG20	P5TXENR	O	AK02	CLK50	I
W27	P10TXCLK	I	AE09	P1COLR	I/O	AG21	P5RXD0R	I	AK03	P0COLR	I/O
W28	P10RXER	I	AE10	VSS		AG22	P6TXD2R	I/O	AK04	P0TXD1R	I/O
W29	P10RXCLK	I	AE11	P1RXD2R	I	AG23	P6RXERR	I	AK05	P0RXCLKR	I/O
W30	P10RXDV	I	AE12	VSS		AG24	P6RXD3R	I	AK06	P0RXD2R	I
Y01	DATA20	I/O	AE13	P2RXD0R	I	AG25	P7TXD2R	I/O	AK07	P1TXD1R	I/O
Y02	DATA19	I/O	AE14	VSS		AG26	P7TXCLKR	I/O	AK08	P1RXERR	I
Y03	ADDR9	O	AE15	VSS		AG27	P7RXD1R	I	AK09	P1RXD0R	I
Y04	ADDR10	O	AE16	P4CRSR	I/O	AG28	P8CRS	I	AK10	P2TXD3R	I/O
Y05	VDD		AE17	VSS		AG29	P8TXD1	O	AK11	P2TXENR	O
Y06	VSS		AE18	P4RXD3R	I	AG30	P8TXEN	O	AK12	P2RXDVR	I
Y25	P9RXD2	I	AE19	VSS		AH01	DATA4	I/O	AK13	P3COLR	I/O
Y26	P9RXD3	I	AE20	P5RXD2R	I	AH02	DATA3	I/O	AK14	P3TXD0R	I/O
Y27	P10TXD2	O	AE21	VSS		AH03	MDIO	I/O	AK15	P3RXCLKR	I/O
Y28	P10TXD1	O	AE22	P6RXDVR	I	AH04	WCHDOG	O	AK16	P3RXDVR	I
Y29	P10TXD0	O	AE23	VSS		AH05	P0TXCLKR	I/O	AK17	P4COLR	I/O
Y30	P10TXEN	O	AE24	VSS		AH06	P0RXD0R	I	AK18	P4TXD0R	I/O
AA01	DATA18	I/O	AE25	VSS		AH07	P0RXD3R	I	AK19	P4RXCLKR	I/O
AA02	DATA17	I/O	AE26	P8TXD3	O	AH08	P1TXD0R	I/O	AK20	P4RXD1R	I
AA03	VDD		AE27	P8TXCLK	I	AH09	P1RXCLKR	I/O	AK21	P5TXD2R	I/O
AA04	VSS		AE28	P8RXD2	I	AH10	P2CRSR	I/O	AK22	P5TXD0R	I/O
AA05	VDD		AE29	P8RXD3	I	AH11	P2TXD1R	I/O	AK23	P5RXCLKR	I/O
AA06	VSS		AE30	P9CRS	I	AH12	P2RXERR	I	AK24	P6CRSR	I/O
AA25	VSS		AF01	DATA8	I/O	AH13	P2RXD3R	I	AK25	P6TXD3R	I/O
AA26	VDD		AF02	DATA7	I/O	AH14	P3TXD2R	I/O	AK26	P6TXENR	O
AA27	P9RXD1	I	AF03	CPUDI	I	AH15	P3TXCLKR	I/O	AK27	P6RXD1R	I
AA28	P10CRS	I	AF04	CPUDO	I/O	AH16	P3RXD1R	I	AK28	P7COLR	I/O
AA29	P10COL	I	AF05	VDD		AH17	P4TXD2R	I/O	AK29	P7TXENR	O
AA30	P10TXD3	O	AF06	P0CRSR	I/O	AH18	P4TXCLKR	I/O	AK30	P7RXCLKR	I/O

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Pin List By Name (With Voltage Rating): Part 1

Signal Name	Pin	I/O	Type	Signal Name	Pin	I/O	Type	Signal Name	Pin	I/O	Type	Signal Name	Pin	I/O	Type
ADDR0	H03	3.3V	O	DATA41	J02	3.3V	I/O	P03CRSR	AJ13	3.3V	I/O	P07TXD3R	AH26	3.3V	I/O
ADDR01	J03	3.3V	O	DATA43	H02	3.3V	I/O	P03RXD0R	AJ16	3.3V	I	P08COL	AF27	3.3V	I
ADDR02	K03	3.3V	O	DATA44	H01	3.3V	I/O	P03RXD1R	AH16	3.3V	I	P08CRS	AG28	3.3V	I
ADDR03	L03	3.3V	O	DATA45	G02	3.3V	I/O	P03RXD2R	AG16	3.3V	I	P08RXCLK	AF28	3.3V	I
ADDR04	R03	3.3V	O	DATA46	G01	3.3V	I/O	P03RXD3R	AF16	3.3V	I	P08RXD0	AF30	3.3V	I
ADDR05	T03	3.3V	O	DATA47	F02	3.3V	I/O	P03RXDVR	AK16	3.3V	I	P08RXD1	AD27	3.3V	I
ADDR06	U03	3.3V	O	DATA48	F01	3.3V	I/O	P03RXERR	AG15	3.3V	I	P08RXD2	AE28	3.3V	I
ADDR07	V03	3.3V	O	DATA49	E02	3.3V	I/O	P03TXCLKR	AH15	3.3V	I/O	P08RXD3	AE29	3.3V	I
ADDR08	W03	3.3V	O	DATA50	E01	3.3V	I/O	P03TXD0R	AK14	3.3V	I/O	P08RXDV	AF29	3.3V	I
ADDR09	Y03	3.3V	O	DATA51	D02	3.3V	I/O	P03TXD1R	AJ14	3.3V	I/O	P08RXER	AD26	3.3V	I
ADDR10	Y04	3.3V	O	LED0	AC04	3.3V	I/O	P03TXD2R	AH14	3.3V	I/O	P08TXCLK	AE27	3.3V	I
ADDR11	W04	3.3V	O	LED1	AD03	3.3V	I/O	P03TXD3R	AG14	3.3V	I/O	P08TXD0	AD25	3.3V	O
ADDR12	V04	3.3V	O	LED2	AC03	3.3V	I/O	P03TXENR	AJ15	3.3V	O	P08TXD1	AG29	3.3V	O
ADDR13	U04	3.3V	O	LED3	AB04	3.3V	I/O	P04COLR	AK17	3.3V	I/O	P08TXD2	AH30	3.3V	O
ADDR14	T04	3.3V	O	LEDCLK	AE04	3.3V	I/O	P04CRSR	AE16	3.3V	I/O	P08TXD3	AE26	3.3V	O
ADDR15	N04	3.3V	O	LEDVLD0	AD04	3.3V	I/O	P04RXCLKR	AK19	3.3V	I/O	P08TXEN	AG30	3.3V	O
ADDR16	M04	3.3V	O	LEDVLD1	AE03	3.3V	I/O	P04RXD0R	AH19	3.3V	I	P09COL	AD28	3.3V	I
ARLCLK	F04	3.3V	O	MDC	AG04	3.3V	O	P04RXD1R	AK20	3.3V	I	P09CRS	AE30	3.3V	I
ARLDI0	D03	3.3V	I	MDIO	AH03	3.3V	I/O	P04RXD2R	AF18	3.3V	I	P09RXCLK	AB28	3.3V	I
ARLDI1	E04	3.3V	I	nCS0	M03	3.3V	O	P04RXD3R	AE18	3.3V	I	P09RXD0	AB30	3.3V	I
ARLDI2	E03	3.3V	I	nCS1	J04	3.3V	O	P04RXDVR	AJ19	3.3V	I	P09RXD1	AA27	3.3V	I
ARLDI3	F03	3.3V	I	nCS2	L04	3.3V	O	P04RXERR	AG18	3.3V	I	P09RXD2	Y25	3.3V	I
ARLDIR0	G03	3.3V	O	nCS3	K04	3.3V	O	P04TXCLKR	AH18	3.3V	I/O	P09RXD3	Y26	3.3V	I
ARLDIR1	G04	3.3V	O	nOE	R04	3.3V	I/O	P04TXD0R	AK18	3.3V	I/O	P09RXDV	AB29	3.3V	I
ARLDIV	H04	3.3V	I	nRESET	AG05	3.3V	I	P04TXD1R	AG17	3.3V	I/O	P09RXER	AC30	3.3V	I
ARLSYNC	F05	3.3V	O	nWE	P03	3.3V	O	P04TXD2R	AH17	3.3V	I/O	P09TXCLK	AB27	3.3V	I
CLK50	AK02	3.3V	I	P00COLR	AK03	3.3V	I/O	P04TXD3R	AJ17	3.3V	I/O	P09TXD0	AC28	3.3V	O
CPUDI	AF03	3.3V	I	P00CRSR	AF06	3.3V	I/O	P04TXENR	AJ18	3.3V	O	P09TXD1	AD30	3.3V	O
CPUDO	AF04	3.3V	I/O	P00RXCLKR	AK05	3.3V	I/O	P05COLR	AJ20	3.3V	I/O	P09TXD2	AD29	3.3V	O
CPUIRQ	AG03	3.3V	O	P00RXD0R	AH06	3.3V	I	P05CRSR	AG19	3.3V	I/O	P09TXD3	AC27	3.3V	O
DATA0	AK01	3.3V	I/O	P00RXD1R	AJ06	3.3V	I	P05RXCLKR	AK23	3.3V	I/O	P09TXEN	AC29	3.3V	O
DATA01	AJ02	3.3V	I/O	P00RXD2R	AK06	3.3V	I	P05RXD0R	AG21	3.3V	I	P10COL	AA29	3.3V	I
DATA02	AJ01	3.3V	I/O	P00RXD3R	AH07	3.3V	I	P05RXD1R	AF20	3.3V	I	P10CRS	AA28	3.3V	I
DATA03	AH02	3.3V	I/O	P00RXDVR	AG07	3.3V	I	P05RXD2R	AE20	3.3V	I	P10RXCLK	W29	3.3V	I
DATA04	AH01	3.3V	I/O	P00RXERR	AJ05	3.3V	I	P05RXD3R	AH22	3.3V	I	P10RXD0	V25	3.3V	I
DATA05	AG02	3.3V	I/O	P00TXCLKR	AH05	3.3V	I/O	P05RXDVR	AJ23	3.3V	I	P10RXD1	V26	3.3V	I
DATA06	AG01	3.3V	I/O	P00TXD0R	AG06	3.3V	I/O	P05RXERR	AJ22	3.3V	I	P10RXD2	V27	3.3V	I
DATA07	AF02	3.3V	I/O	P00TXD1R	AK04	3.3V	I/O	P05TXCLKR	AH21	3.3V	I/O	P10RXD3	V28	3.3V	I
DATA08	AF01	3.3V	I/O	P00TXD2R	AE07	3.3V	I/O	P05TXD0R	AK22	3.3V	I/O	P10RXDV	W30	3.3V	I
DATA09	AE02	3.3V	I/O	P00TXD3R	AJ04	3.3V	I/O	P05TXD1R	AJ21	3.3V	I/O	P10RXER	W28	3.3V	I
DATA10	AE01	3.3V	I/O	P00TXENR	AF07	3.3V	O	P05TXD2R	AK21	3.3V	I/O	P10TXCLK	W27	3.3V	I
DATA11	AD02	3.3V	I/O	P01CRSR	AG08	3.3V	I/O	P05TXD3R	AH20	3.3V	I/O	P10TXD0	Y29	3.3V	O
DATA12	AD01	3.3V	I/O	P01RXCLKR	AH09	3.3V	I/O	P05TXENR	AG20	3.3V	O	P10TXD1	Y28	3.3V	O
DATA13	AC02	3.3V	I/O	P01RXD0R	AK09	3.3V	I	P06COLR	AJ24	3.3V	I/O	P10TXD2	Y27	3.3V	O
DATA14	AC01	3.3V	I/O	P01RXD1R	AG10	3.3V	I	P06CRSR	AK24	3.3V	I/O	P10TXD3	AA30	3.3V	O
DATA15	AB02	3.3V	I/O	P01RXD2R	AE11	3.3V	I	P06RXCLKR	AF22	3.3V	I/O	P10TXEN	Y30	3.3V	O
DATA16	AB01	3.3V	I/O	P01RXD3R	AF11	3.3V	I	P06RXD0R	AJ26	3.3V	I	P11COL	V30	3.3V	I
DATA17	AA02	3.3V	I/O	P01RXDVR	AJ09	3.3V	I	P06RXD1R	AK27	3.3V	I	P11CRS	V29	3.3V	I
DATA18	AA01	3.3V	I/O	P01RXERR	AK08	3.3V	I	P06RXD2R	AH25	3.3V	I	P11RXCLK	T30	3.3V	I
DATA19	Y02	3.3V	I/O	P01TXCLKR	AG09	3.3V	I/O	P06RXD3R	AG24	3.3V	I	P11RXD0	R29	3.3V	I
DATA20	Y01	3.3V	I/O	P01TXD0R	AH08	3.3V	I/O	P06RXDVR	AE22	3.3V	I	P11RXD1	R28	3.3V	I
DATA21	W02	3.3V	I/O	P01TXD1R	AK07	3.3V	I/O	P06RXERR	AG23	3.3V	I	P11RXD2	R27	3.3V	I
DATA22	W01	3.3V	I/O	P01TXD2R	AJ07	3.3V	I/O	P06TXCLKR	AH24	3.3V	I/O	P11RXD3	R26	3.3V	I
DATA23	V02	3.3V	I/O	P01TXD3R	AF09	3.3V	I/O	P06TXD0R	AJ25	3.3V	I/O	P11RXDV	R30	3.3V	I
DATA24	V01	3.3V	I/O	P01TXENR	AJ08	3.3V	O	P06TXD1R	AH23	3.3V	I/O	P11RXER	T27	3.3V	I
DATA25	U02	3.3V	I/O	P02COLR	AJ10	3.3V	I/O	P06TXD2R	AG22	3.3V	I/O	P11TXCLK	T28	3.3V	I
DATA26	U01	3.3V	I/O	P02CRSR	AH10	3.3V	I/O	P06TXD3R	AK25	3.3V	I/O	P11TXD0	U30	3.3V	O
DATA27	T02	3.3V	I/O	P02RXCLKR	AJ12	3.3V	I/O	P06TXENR	AK26	3.3V	O	P11TXD1	U29	3.3V	O
DATA28	T01	3.3V	I/O	P02RXD0R	AE13	3.3V	I	P07COLR	AK28	3.3V	I/O	P11TXD2	U28	3.3V	O
DATA29	R02	3.3V	I/O	P02RXD1R	AF13	3.3V	I	P07CRSR	AJ27	3.3V	I/O	P11TXD3	U27	3.3V	O
DATA30	R01	3.3V	I/O	P02RXD2R	AG13	3.3V	I	P07RXCLKR	AK30	3.3V	I/O	P11TXEN	T29	3.3V	O
DATA31	P02	3.3V	I/O	P02RXD3R	AH13	3.3V	I	P07RXD0R	AH28	3.3V	I	P12COL	P30	3.3V	I
DATA32	P01	3.3V	I/O	P02RXDVR	AK12	3.3V	I	P07RXD1R	AG27	3.3V	I	P12CRS	R25	3.3V	I
DATA33	N02	3.3V	I/O	P02RXERR	AH12	3.3V	I	P07RXD2R	AJ30	3.3V	I	P12RXCLK	M30	3.3V	I
DATA34	N01	3.3V	I/O	P02TXCLKR	AG12	3.3V	I/O	P07RXD3R	AH29	3.3V	I	P12RXD0	M28	3.3V	I
DATA35	M02	3.3V	I/O	P02TXD0R	AJ11	3.3V	I/O	P07RXDVR	AJ29	3.3V	I	P12RXD1	L30	3.3V	I
DATA36	M01	3.3V	I/O	P02TXD1R	AH11	3.3V	I/O	P07RXERR	AF25	3.3V	I	P12RXD2	N26	3.3V	I
DATA37	L02	3.3V	I/O	P02TXD2R	AG11	3.3V	I/O	P07TXCLKR	AG26	3.3V	I/O	P12RXD3	N25	3.3V	I
DATA38	L01	3.3V	I/O	P02TXD3R	AK10	3.3V	I/O	P07TXD0R	AJ28	3.3V	I/O	P12RXDV	M29	3.3V	I
DATA39	K02	3.3V	I/O	P02TXENR	AK11	3.3V	O	P07TXD1R	AF24	3.3V	I/O	P12RXER	N27	3.3V	I
DATA40	K01	3.3V	I/O	P03COLR	AK13	3.3V	I/O	P07TXD2R	AG25	3.3V	I/O	P12TXCLK	N28	3.3V	I
DATA42	J01	3.3V	I/O	P03RXCLKR	AK15	3.3V	I/O	P07TXENR	AK29	3.3V	O	P12TXD0	N30	3.3V	O

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Pin List By Name (With Voltage Rating): Part 2

Signal Name	Pin	I/O	Type	Signal Name	Pin	I/O	Type	Signal Name	Pin	I/O	Type	Signal Name	Pin	I/O	Type
P12TXD1	P27	3.3V	O	P17RXER	A24	3.3V	I	P22RXD1R	F09	3.3V	I	VDD	Y05	3.3V	Power
P12TXD2	P28	3.3V	O	P17TXCLK	B24	3.3V	I	P22RXD2R	B05	3.3V	I	VDD	AB26	3.3V	Power
P12TXD3	P29	3.3V	O	P17TXD0	F22	3.3V	O	P22RXD3R	A04	3.3V	I	VDD	AF05	3.3V	Power
P12TXEN	N29	3.3V	O	P17TXD1	D23	3.3V	O	P22RXDVR	D08	3.3V	I	VDD	AF12	3.3V	Power
P13COL	L29	3.3V	I	P17TXD2	C24	3.3V	O	P22RXERR	A05	3.3V	I	VDD	AF19	3.3V	Power
P13CRS	M27	3.3V	I	P17TXD3	A25	3.3V	O	P22TXCLKR	B06	3.3V	I/O	VDD	AF26	3.3V	Power
P13RXCLK	H30	3.3V	I	P17TXEN	E22	3.3V	O	P22TXD0R	D09	3.3V	O	VDD	E05	3.3V	Power
P13RXD0	K27	3.3V	I	P18COL	D21	3.3V	I	P22TXD1R	A06	3.3V	O	VDD	E12	3.3V	Power
P13RXD1	L26	3.3V	I	P18CRS	A22	3.3V	I	P22TXD2R	B07	3.3V	O	VDD	E19	3.3V	Power
P13RXD2	L25	3.3V	I	P18RXCLK	B20	3.3V	I	P22TXD3R	A07	3.3V	O	VDD	E26	3.3V	Power
P13RXD3	J28	3.3V	I	P18RXD0	D19	3.3V	I	P22TXENR	C08	3.3V	O	VDD	M05	3.3V	Power
P13RXDV	H29	3.3V	I	P18RXD1	C19	3.3V	I	P23COLR	D07	3.3V	I/O	VDD	M26	3.3V	Power
P13RXER	J29	3.3V	I	P18RXD2	F18	3.3V	I	P23CRSR	C06	3.3V	I/O	VDD	W05	3.3V	Power
P13TXCLK	K28	3.3V	I	P18RXD3	E18	3.3V	I	P23RXCLKR	D05	3.3V	I/O	VDD	W26	3.3V	Power
P13TXD0	J30	3.3V	O	P18RXDV	A20	3.3V	I	P23RXD0R	A01	3.3V	I	VSS	A19		Ground
P13TXD1	K29	3.3V	O	P18RXER	C20	3.3V	I	P23RXD1R	B02	3.3V	I	VSS	AA04		Ground
P13TXD2	K30	3.3V	O	P18TXCLK	D20	3.3V	I	P23RXD2R	C03	3.3V	I	VSS	AA06		Ground
P13TXD3	L28	3.3V	O	P18TXD0	B21	3.3V	O	P23RXD3R	D04	3.3V	I	VSS	AA25		Ground
P13TXEN	L27	3.3V	O	P18TXD1	C21	3.3V	O	P23RXDVR	E06	3.3V	I	VSS	AB06		Ground
P14COL	G29	3.3V	I	P18TXD2	E20	3.3V	O	P23RXERR	F07	3.3V	I	VSS	AB25		Ground
P14CRS	G30	3.3V	I	P18TXD3	F20	3.3V	O	P23TXCLKR	B03	3.3V	I/O	VSS	AC06		Ground
P14RXCLK	J26	3.3V	I	P18TXEN	A21	3.3V	O	P23TXD0R	D06	3.3V	O	VSS	AC25		Ground
P14RXD0	E29	3.3V	I	P19COL	C18	3.3V	I	P23TXD1R	C05	3.3V	O	VSS	AD06		Ground
P14RXD1	D30	3.3V	I	P19CRS	D18	3.3V	I	P23TXD2R	A03	3.3V	O	VSS	AE05		Ground
P14RXD2	F28	3.3V	I	P19RXCLK	C16	3.3V	I	P23TXD3R	B04	3.3V	O	VSS	AE06		Ground
P14RXD3	G27	3.3V	I	P19RXD0	A16	3.3V	I	P23TXENR	E07	3.3V	O	VSS	AE08		Ground
P14RXDV	J25	3.3V	I	P19RXD1	A15	3.3V	I	STAT0	B01	3.3V	O	VSS	AE10		Ground
P14RXER	H27	3.3V	I	P19RXD2	B15	3.3V	I	STAT1	C01	3.3V	O	VSS	AE12		Ground
P14TXCLK	G28	3.3V	I	P19RXD3	C15	3.3V	I	STAT2	C02	3.3V	O	VSS	AE14		Ground
P14TXD0	F29	3.3V	O	P19RXDV	D16	3.3V	I	STAT3	D01	3.3V	O	VSS	AE15		Ground
P14TXD1	H28	3.3V	O	P19RXER	B16	3.3V	I	VDD	A02	3.3V	Power	VSS	AE17		Ground
P14TXD2	J27	3.3V	O	P19TXCLK	A17	3.3V	I	VDD	AA03	3.3V	Power	VSS	AE19		Ground
P14TXD3	F30	3.3V	O	P19TXD0	C17	3.3V	O	VDD	AA05	3.3V	Power	VSS	AE21		Ground
P14TXEN	E30	3.3V	O	P19TXD1	D17	3.3V	O	VDD	AA26	3.3V	Power	VSS	AE23		Ground
P15COL	C30	3.3V	I	P19TXD2	A18	3.3V	O	VDD	AB03	3.3V	Power	VSS	AE24		Ground
P15CRS	D29	3.3V	I	P19TXD3	B18	3.3V	O	VDD	AB05	3.3V	Power	VSS	AE25		Ground
P15RXCLK	E27	3.3V	I	P19TXEN	B17	3.3V	O	VDD	AC05	3.3V	Power	VSS	AJ03		Ground
P15RXD0	A30	3.3V	I	P1COLR	AE09	3.3V	I/O	VDD	AC26	3.3V	Power	VSS	C04		Ground
P15RXD1	B29	3.3V	I	P20COL	E15	3.3V	I	VDD	AD05	3.3V	Power	VSS	F06		Ground
P15RXD2	C28	3.3V	I	P20CRS	D15	3.3V	I	VDD	AF08	3.3V	Power	VSS	F08		Ground
P15RXD3	D27	3.3V	I	P20RXCLK	C13	3.3V	I	VDD	AF10	3.3V	Power	VSS	F10		Ground
P15RXDV	F26	3.3V	I	P20RXD0	A12	3.3V	I	VDD	AF14	3.3V	Power	VSS	F12		Ground
P15RXER	G25	3.3V	I	P20RXD1	B12	3.3V	I	VDD	AF15	3.3V	Power	VSS	F14		Ground
P15TXCLK	D28	3.3V	I	P20RXD2	C12	3.3V	I	VDD	AF17	3.3V	Power	VSS	F16		Ground
P15TXD0	C29	3.3V	O	P20RXD3	A11	3.3V	I	VDD	AF21	3.3V	Power	VSS	F17		Ground
P15TXD1	G26	3.3V	O	P20RXDV	D13	3.3V	I	VDD	AF23	3.3V	Power	VSS	F19		Ground
P15TXD2	F27	3.3V	O	P20RXER	B13	3.3V	I	VDD	AH27	3.3V	Power	VSS	F21		Ground
P15TXD3	E28	3.3V	O	P20TXCLK	A13	3.3V	I	VDD	B19	3.3V	Power	VSS	F23		Ground
P15TXEN	B30	3.3V	O	P20TXD0	C14	3.3V	O	VDD	E08	3.3V	Power	VSS	F25		Ground
P16COL	B28	3.3V	I	P20TXD1	B14	3.3V	O	VDD	E10	3.3V	Power	VSS	G06		Ground
P16CRS	A29	3.3V	I	P20TXD2	A14	3.3V	O	VDD	E14	3.3V	Power	VSS	H06		Ground
P16RXCLK	D25	3.3V	I	P20TXD3	F15	3.3V	O	VDD	E16	3.3V	Power	VSS	H25		Ground
P16RXD0	C26	3.3V	I	P20TXEN	D14	3.3V	O	VDD	E17	3.3V	Power	VSS	J06		Ground
P16RXD1	B26	3.3V	I	P21COL	F13	3.3V	I	VDD	E21	3.3V	Power	VSS	K06		Ground
P16RXD2	A26	3.3V	I	P21CRS	E13	3.3V	I	VDD	E23	3.3V	Power	VSS	K25		Ground
P16RXD3	D24	3.3V	I	P21RXCLK	C10	3.3V	I	VDD	G05	3.3V	Power	VSS	L06		Ground
P16RXDV	E24	3.3V	I	P21RXD0	A08	3.3V	I	VDD	H05	3.3V	Power	VSS	M06		Ground
P16RXER	A27	3.3V	I	P21RXD1	B08	3.3V	I	VDD	H26	3.3V	Power	VSS	M25		Ground
P16TXCLK	F24	3.3V	I	P21RXD2	D10	3.3V	I	VDD	J05	3.3V	Power	VSS	N06		Ground
P16TXD0	A28	3.3V	O	P21RXD3	E11	3.3V	I	VDD	K05	3.3V	Power	VSS	P04		Ground
P16TXD1	E25	3.3V	O	P21RXDV	B09	3.3V	I	VDD	K26	3.3V	Power	VSS	P06		Ground
P16TXD2	D26	3.3V	O	P21RXER	D11	3.3V	I	VDD	L05	3.3V	Power	VSS	P25		Ground
P16TXD3	C27	3.3V	O	P21TXCLK	A09	3.3V	I	VDD	N03	3.3V	Power	VSS	R06		Ground
P16TXEN	B27	3.3V	O	P21TXD0	A10	3.3V	O	VDD	N05	3.3V	Power	VSS	T06		Ground
P17COL	B25	3.3V	I	P21TXD1	C11	3.3V	O	VDD	P05	3.3V	Power	VSS	T25		Ground
P17CRS	C25	3.3V	I	P21TXD2	B11	3.3V	O	VDD	P26	3.3V	Power	VSS	U06		Ground
P17RXCLK	C23	3.3V	I	P21TXD3	D12	3.3V	O	VDD	R05	3.3V	Power	VSS	U25		Ground
P17RXD0	D22	3.3V	I	P21TXEN	B10	3.3V	O	VDD	T05	3.3V	Power	VSS	V06		Ground
P17RXD1	A23	3.3V	I	P22COLR	C09	3.3V	I/O	VDD	T26	3.3V	Power	VSS	W06		Ground
P17RXD2	C22	3.3V	I	P22CRSR	F11	3.3V	I/O	VDD	U05	3.3V	Power	VSS	W25		Ground
P17RXD3	B22	3.3V	I	P22RXCLKR	C07	3.3V	I/O	VDD	U26	3.3V	Power	VSS	Y06		Ground
P17RXDV	B23	3.3V	I	P22RXD0R	E09	3.3V	I	VDD	V05	3.3V	Power	WCHDOG	AH04		O

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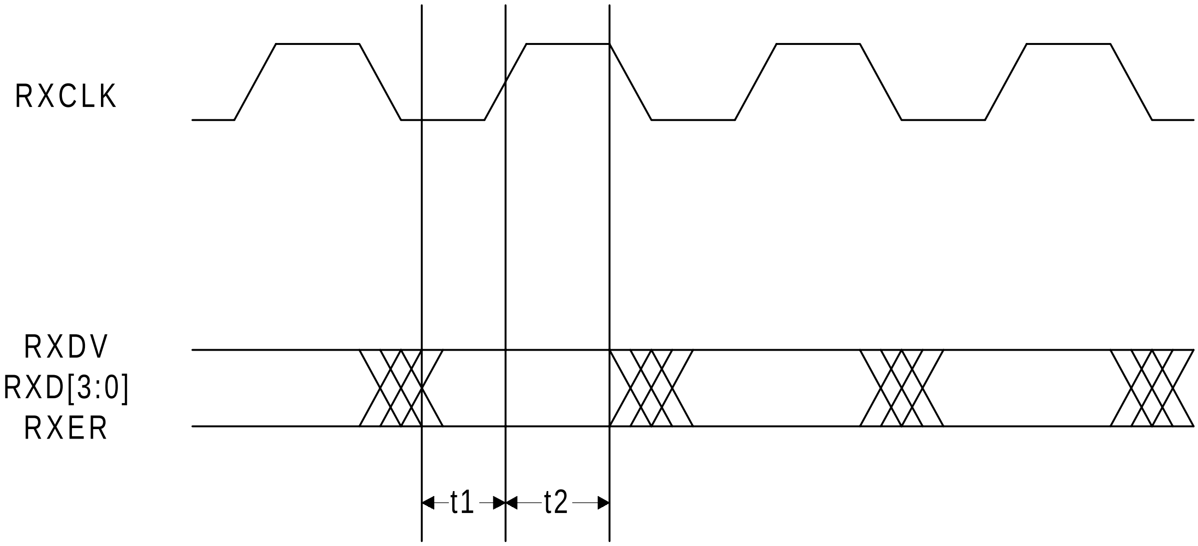
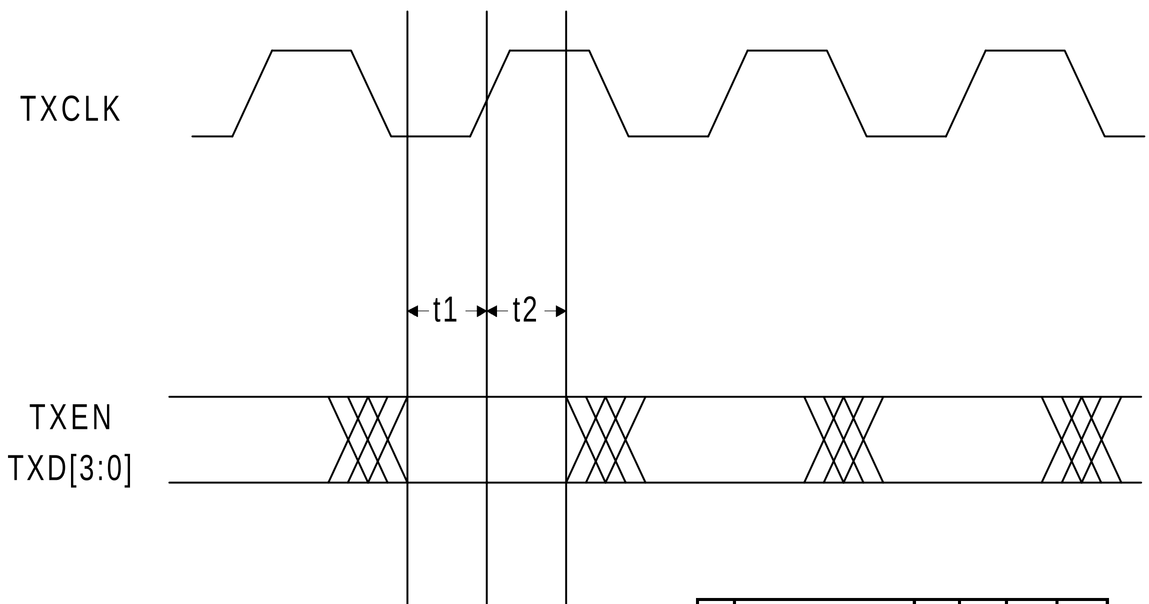
9. TIMING DESCRIPTION

MII Receive Timing



T#	Description:	MIN	TYP	MAX	UNIT
t1	RX_DV, RXD, RX_ER setup time	5	-	-	ns
t2	RX_DV, RXD, RX_ER hold time	5	-	-	ns

MII Transmit Timing



T#	Desciption	Min	Typ	Max	Unit
t1	TXEN, TXD setup time	10	-	-	ns
t2	TXEN, TXD hold time	10	-	-	ns

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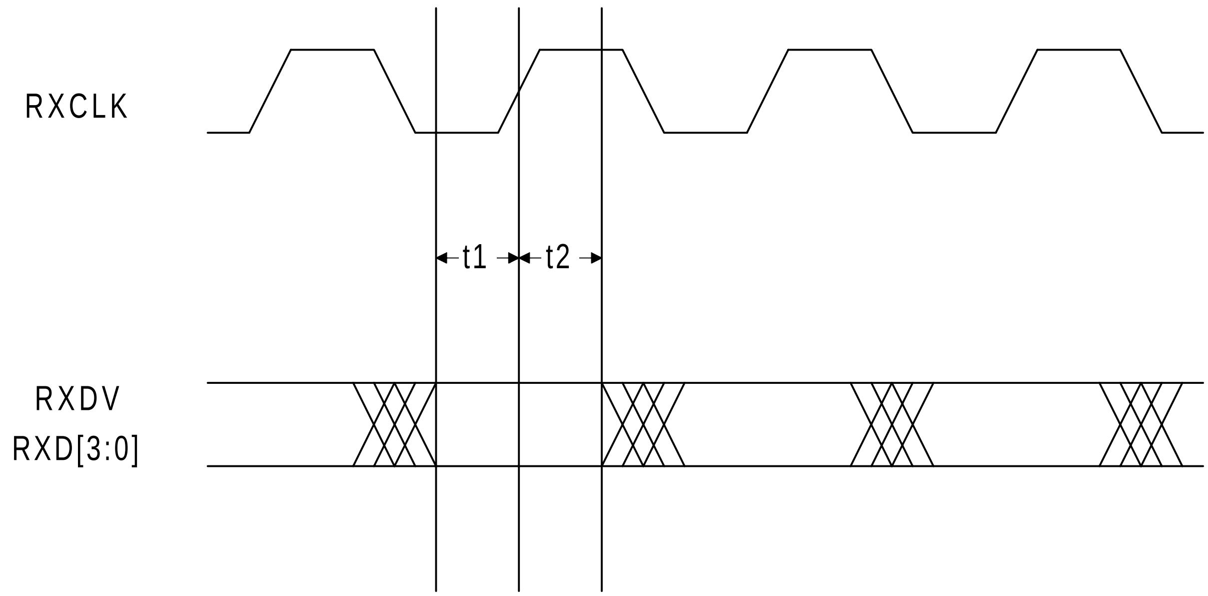
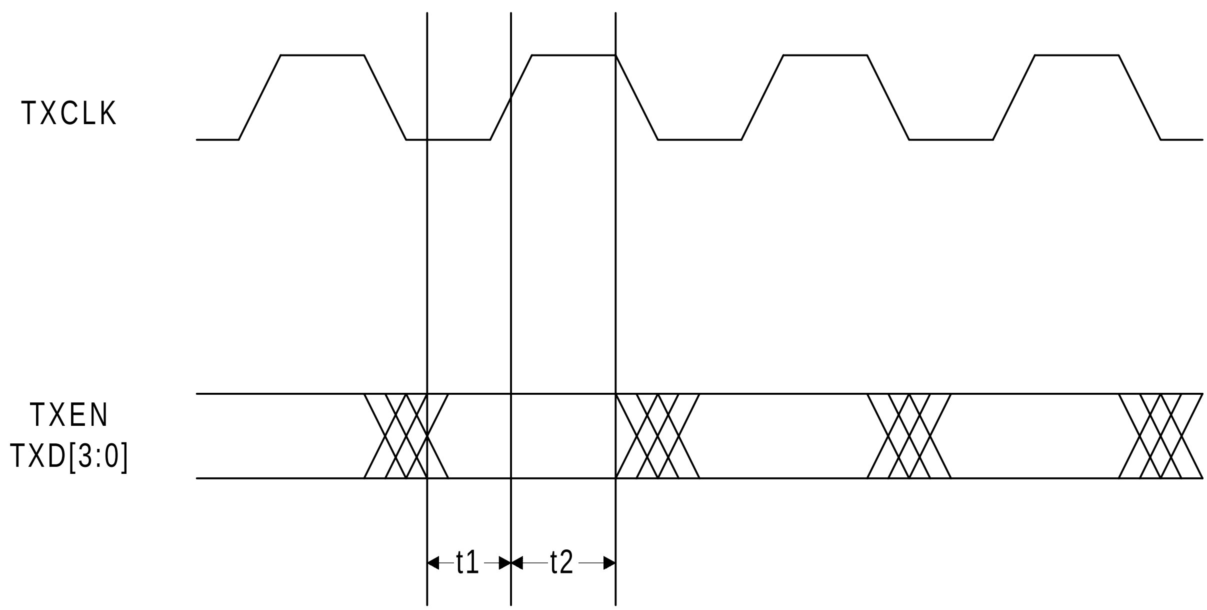
Reversed MII Receive Timing



T#	Description:	MIN	TYP	MAX	UNIT
t1	RXDV, RXD setup time	10	-		ns
T2	RXDV, RXD hold time	10			ns

Reversed MII Transmit Timing



T#	Description:	MIN	TYP	MAX	UNIT
t1	RXDV, RXD setup time	5	-		ns
T2	RXDV, RXD hold time	5			ns

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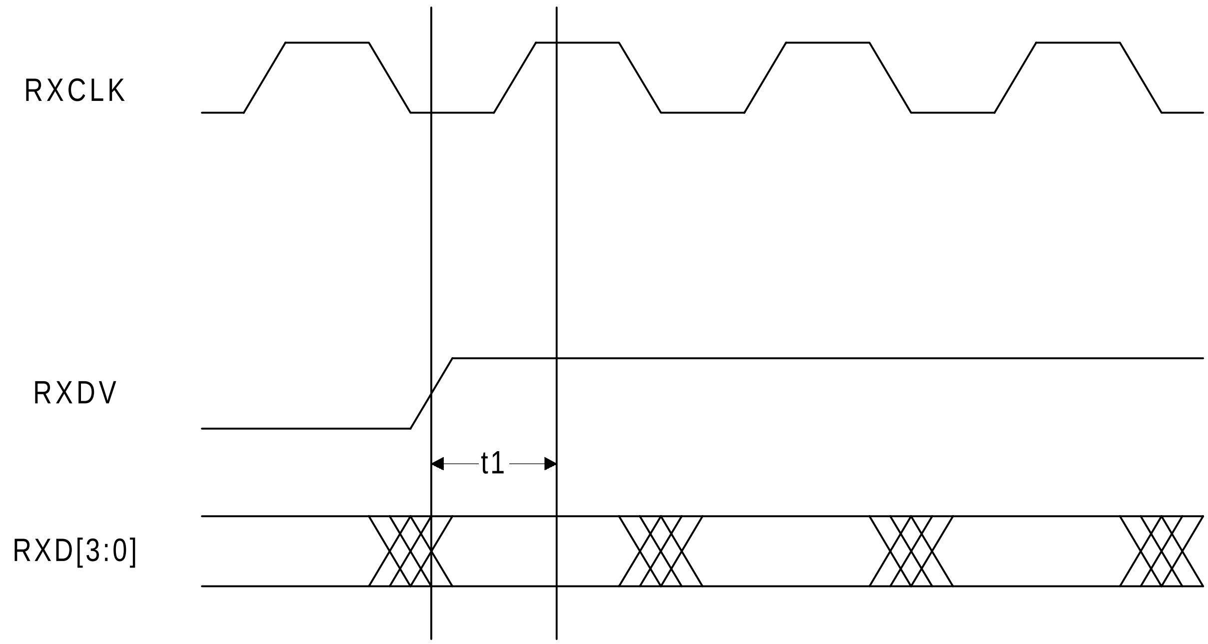
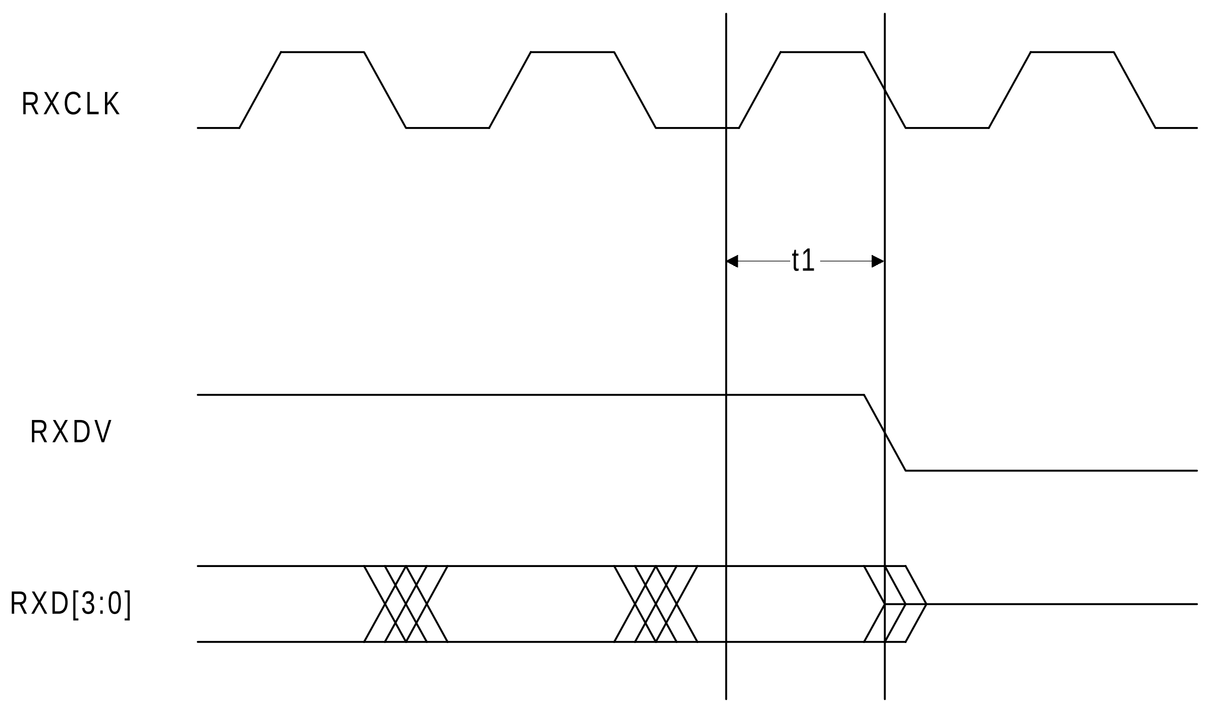
Reversed MII Packet Timing (Start of Packet)



T#	Desciption	Min	Typ	Max	Unit
t1	RXD to RXDV	0	-	-	ns

Reversed MII Packet Timing (End of Packet)



T#	Desciption	Min	Typ	Max	Unit
t1	PXD to RXDV delay time	0	-	-	ns

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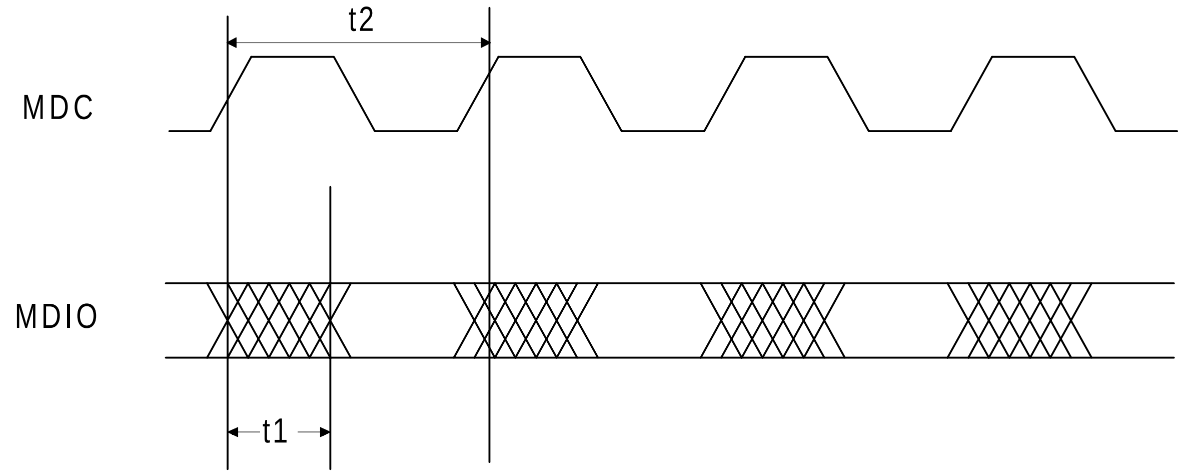
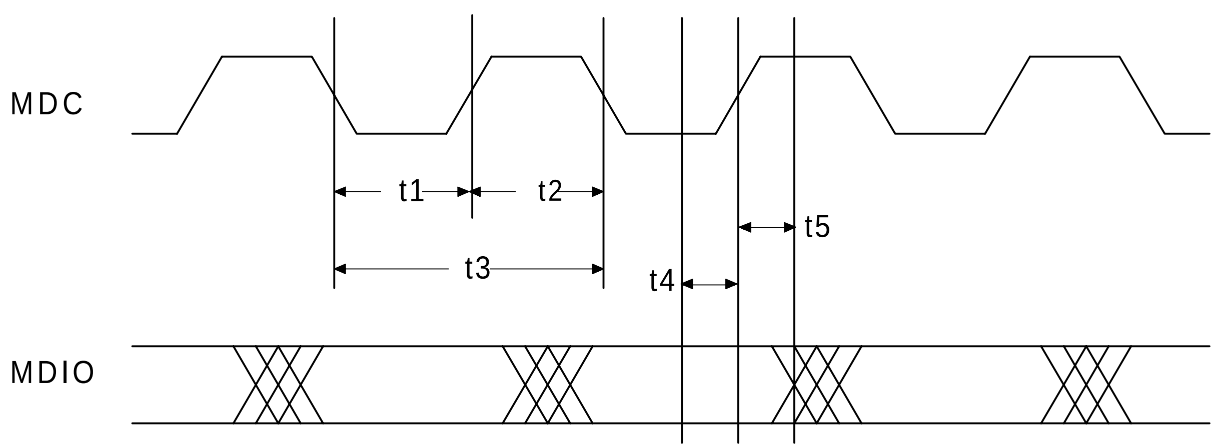
PHY Management Read Timing



T#	Description	MIN	TYP	MAX	UNIT
t1	MDIO setup time	0	-	300	ns
t2	MDC cycle	-	800	-	ns

PHY Management Write Timing



T#	Description	MIN	TYP	MAX	UNIT
t1	MDC High time	-	400	-	ns
t2	MDC Low time	-	400	-	ns
t3	MDC period	-	800	-	ns
t4	MDIO set up time	10	-	-	ns
t5	MDIO hold time	10	-	-	ns

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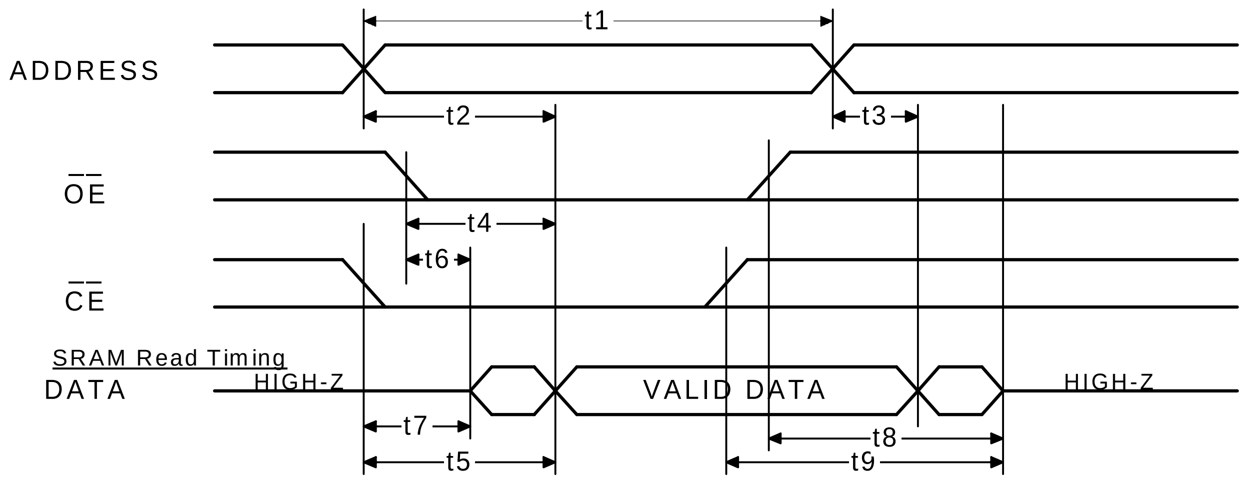
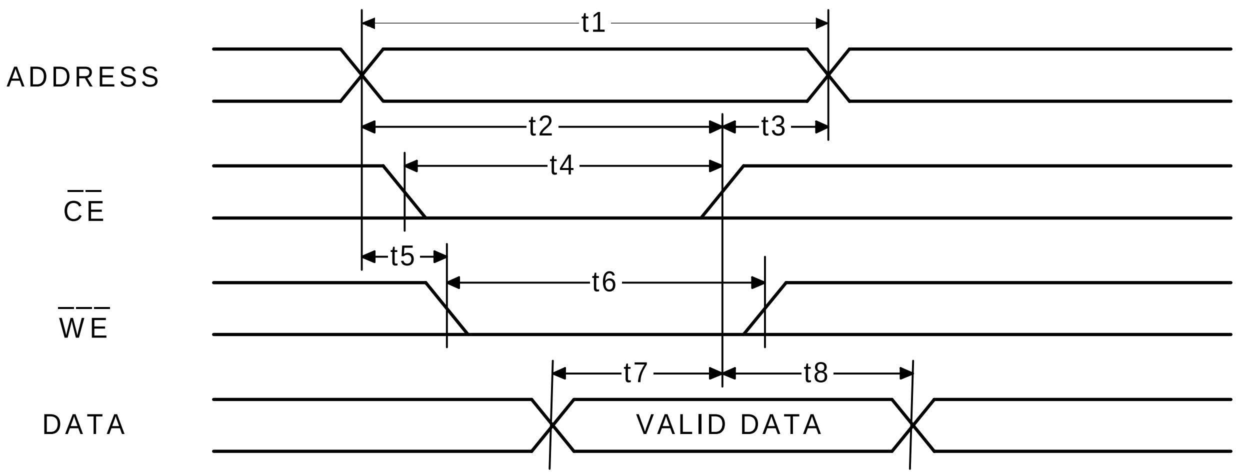
ASRAM Read Timing



T#	Description	MIN	TYP	MAX	UNIT
t1	Read cycle time	-	20	-	ns
t2	Address access time	-	-	12	ns
t3	Output hold time	0	-	-	ns
t4	OE access time	-	-	12	ns
t5	CE access time	-	-	12	ns
t6	OE to Low-Z output	0	-	-	ns
t7	CE to Low-Z output	0	-	-	ns
t8	OE to High-Z output	-	-	6	ns
t9	CE to High-Z output	-	-	6	ns

ASRAM Write Timing



T#	Description	MIN	TYP	MAX	UNIT
t1	Write cycle time	-	20	-	ns
t2	Address Setup to Write End time	12	-	-	ns
t3	Address hold for Write End time	0	-	-	ns
t4	CE to Write End time	12	-	-	ns
t5	Address Setup time	4	-	-	ns
t6	WE pulse width	8	-	-	ns
t7	Data Setup to Write End	8	-	-	ns
t8	Data Hold for Write End	0	-	-	ns

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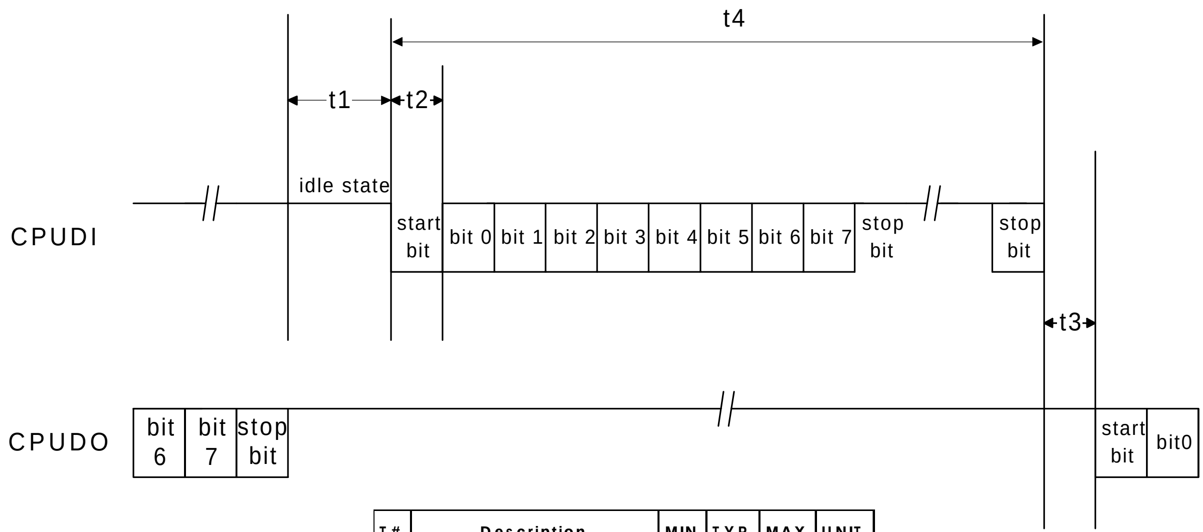
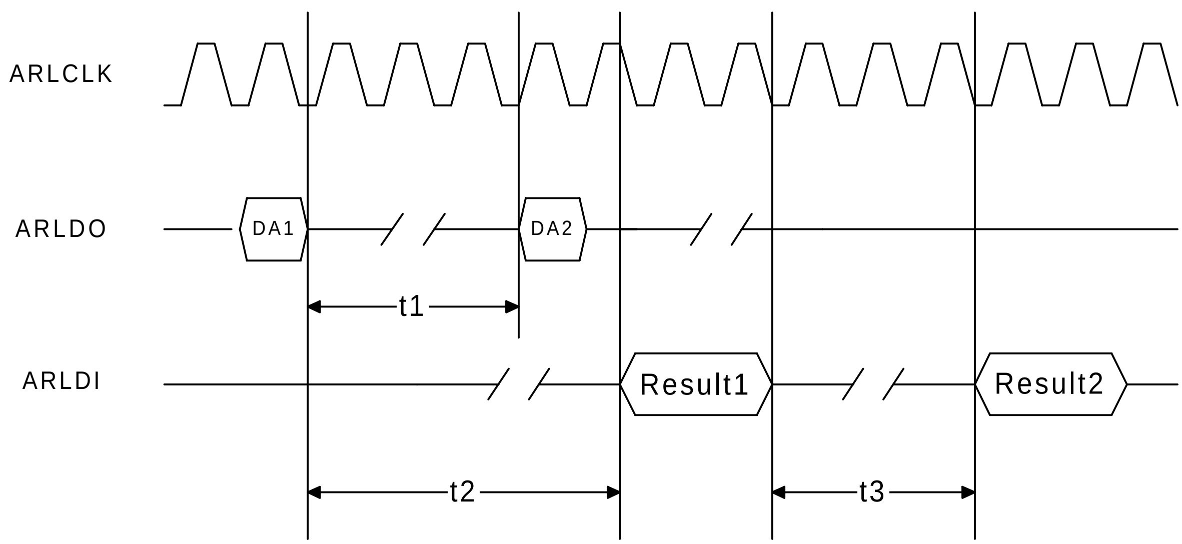
CPU Command Timing



T#	Description	MIN	TYP	MAX	UNIT
t1	CPU idle time	0	-	-	us
t2	CPU command bit time	10	-	-	us
t3	Response time	0	-	20	ms
t4	Command time	-	-	20	ms

ARL Result Timing



T#	Description	MIN	TYP	MAX	UNIT
t1	time between DAs	0	-	-	ns
t2	time for ARL result	0	-	200	ns
t3	time between results	0	-	-	ns

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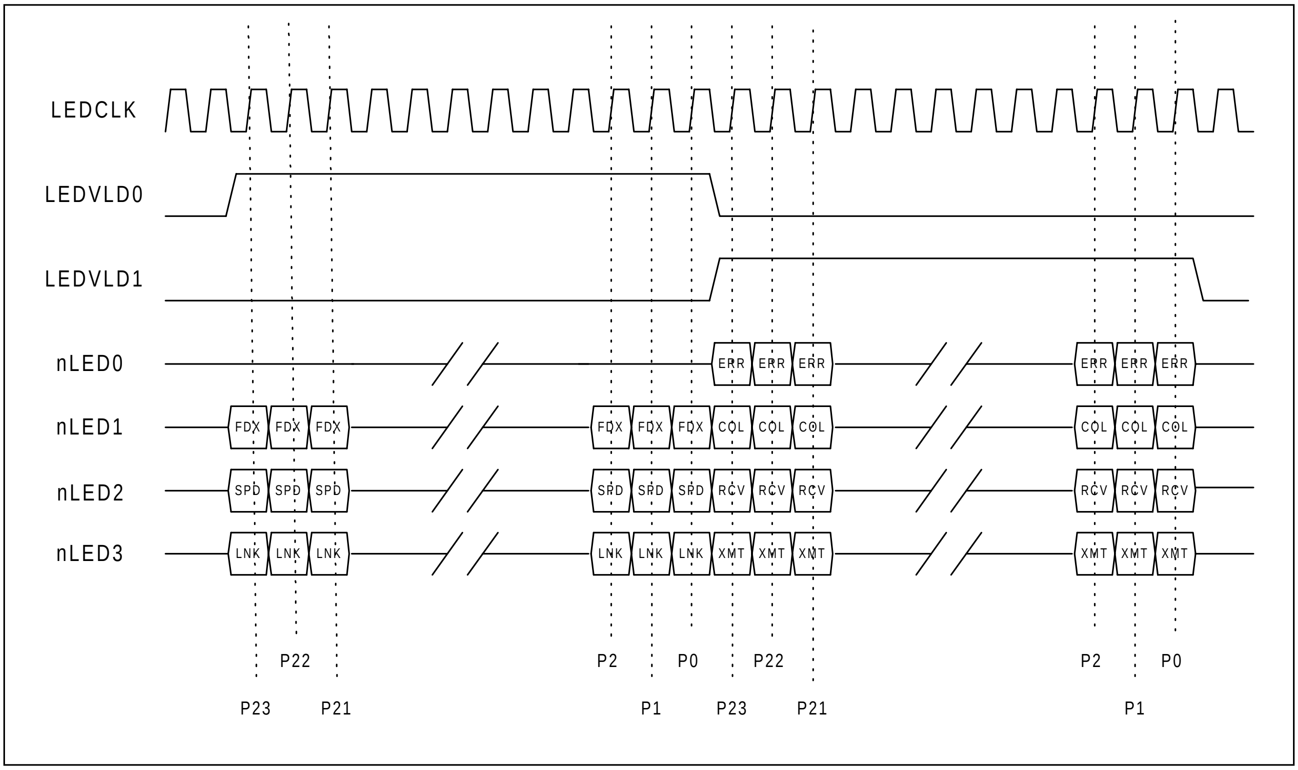
LED Signal Timing



10. ELECTRICAL SPECIFICATION

Absolute Maximum Ratings

Operation at absolute maximum ratings is not implied. Exposure to stresses outside those listed could cause permanent damage to the device.

DC Supply voltage : VDD	-0.3V ~ +5.0V
DC input current: Iin	+/-10 mA
DC input voltage: Vin	-0.3 ~ VDD + 0.3V
DC output voltage: Vout	-0.3 ~ VDD + 0.3V
Storage temperature: Tstg	-40 to +125^{o}C

Recommended Operation Conditions

Supply voltage: VDD	3.3V, +/-0.3V
Operating temperature: Ta	0^{o}C -70 ^{o}C
Maximum power consumption	3.5W

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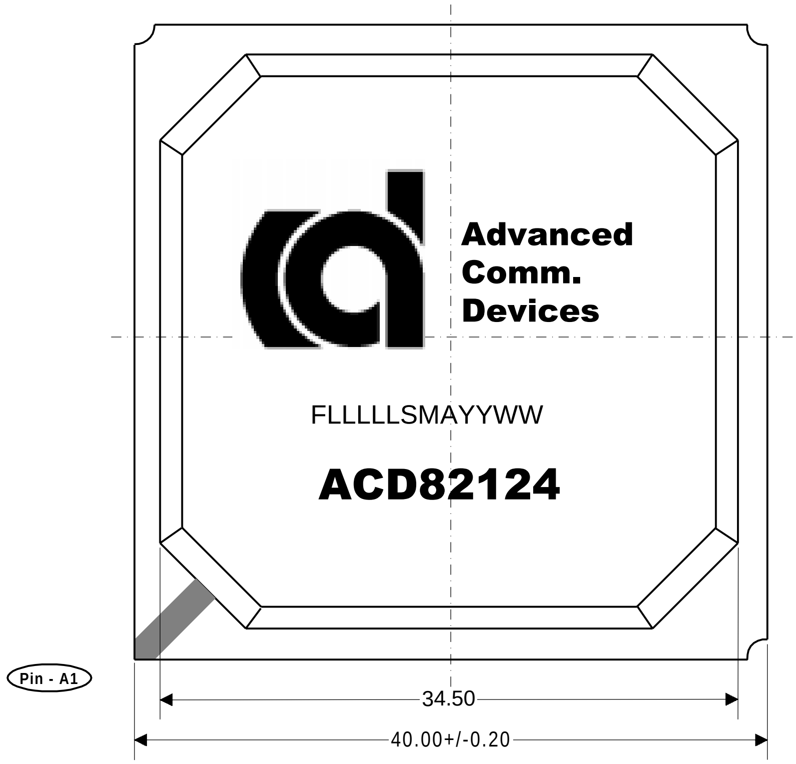
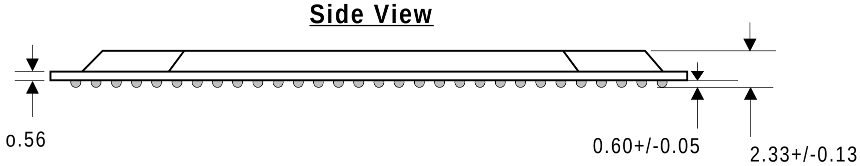
11. PACKAGING

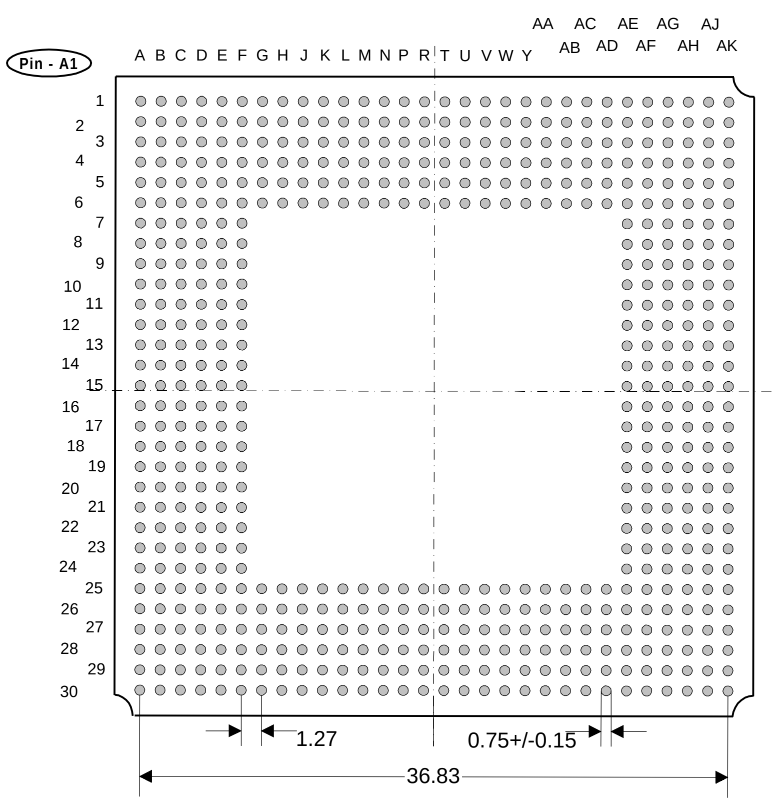
Top View



Side View



Bottom View



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Appendix-A1

Address Resolution Logic

(The built-in ARL with 2048 MAC Addresses)

Data Sheet: ACD82124

INTRODUCTORY

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1. SUMMARY

The internal Address Resolution Logic (ARL) of ACD's switch controllers automatically builds up an address table and maps up to 2,048 MAC addresses into their associated port. It can work by itself without any CPU intervention in an UN-managed system.

For a managed system, the management CPU can configure the operation mode of the ARL, learn all the address in the address table, add new address into the table, control security or filtering feature of each address entry etc.

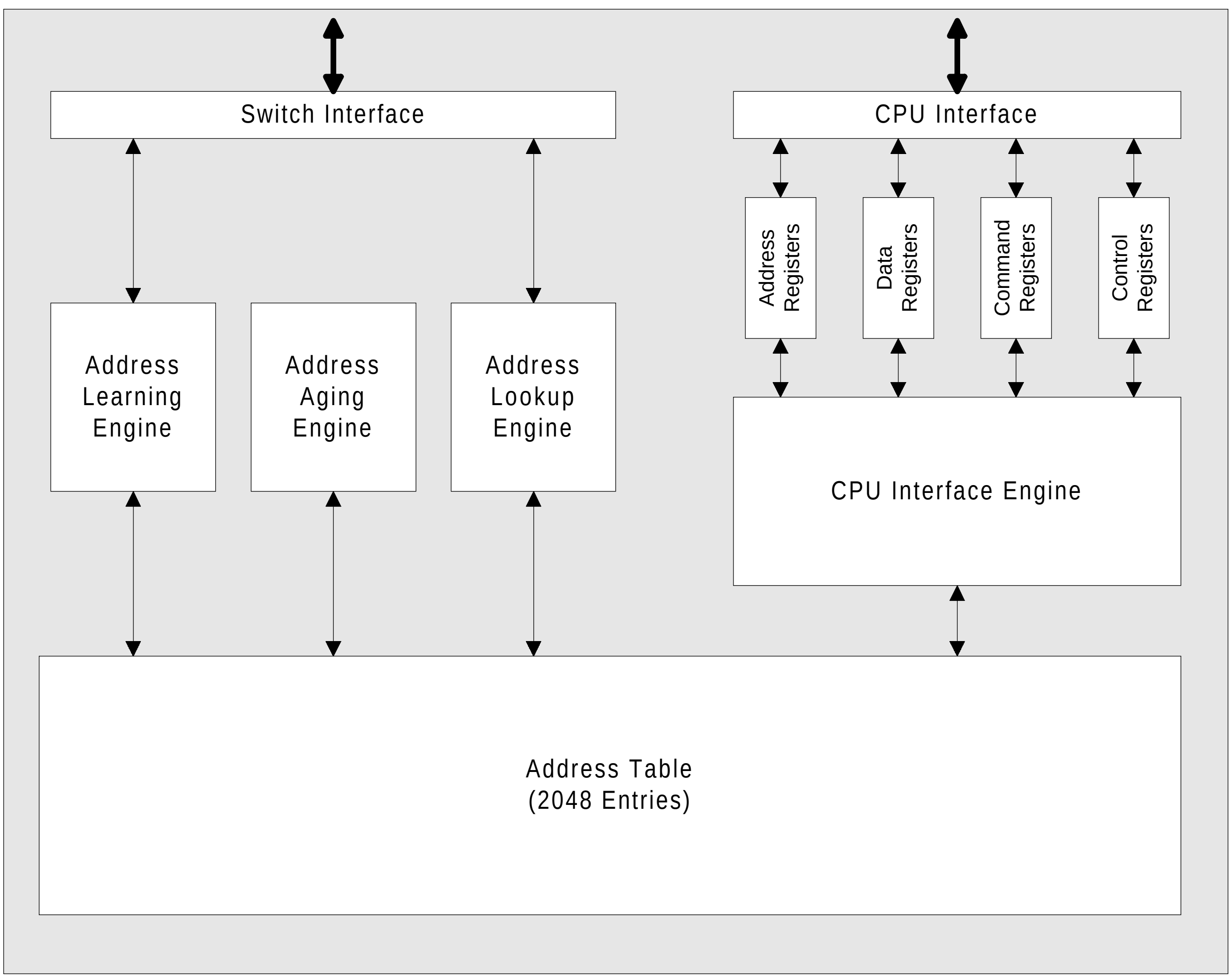
The ARL is designed with such a high performance that it will never slow down the frame switching operation. It helps the switch controllers to reach wire speed forwarding rate under any type of traffic load.

The address space can be expanded to 11K entries by using the external ARL, the ACD80800.

2. FEATURES

- Supports up to 2,048 MAC address lookup
- Provides UART type of interface for the management CPU
- Wire speed address lookup time.
- Wire speed address learning time.
- Address can be automatically learned from switch without the CPU intervention
- Address can be manually added by the CPU through the CPU interface
- Each MAC address can be secured by the CPU from being changed or aged out
- Each MAC address can be marked by the CPU from receiving any frame
- Each newly learned MAC address is notified to the CPU
- Each aged out MAC address is notified to the CPU
- Automatic address aging control, with configurable aging period

Figure-1. ARL Block Diagram



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3. FUNCTIONAL DESCRIPTION

The ARL provides Address Resolution service for ACD's switch controllers. *Figure 2* is a block diagram of the ARL.

Traffic Snooping

All Ethernet frames received by ACD's switch controller have to be stored into memory buffer. As the frame data are written into memory, the status of the data shown on the data bus are displayed by ACD's switch controller through a state bus. The ARL's Switch Controller Interface contains the signals of the data bus and the state bus. By snooping the data bus and the state bus of ACD's switch controller, the ARL can detect the occurrence of any destination MAC address and source MAC address embedded inside each frame.

Address Learning

Each source address caught from the data bus, together with the ID of the ingress port, is passed to the Address Learning Engine of the ARL. The Address Learning Engine will first determine whether the frame is a valid frame. For a valid frame, it will first try to find the source address from the current address table. If that address doesn't exist, or if it does exist but the port ID associated with the MAC address is not the ingress port, the address will be learned into the address table. After an address is learned by the address learning engine, the CPU will be notified to read this newly learned address so that it can add it into the CPU's address table.

Address Aging

After each source address is learned into the address table, it has to be refreshed at least once within each address aging period. Refresh means it is caught again from the switch interface. If it has not occurred for a pre-set aging period, the address aging engine will remove the address from the address table. After an address is removed by the address aging engine, the CPU will be notified through interrupt request that it needs to read this aged out address so that it can remove this address from the CPU's address table.

Address Lookup

Each destination address is passed to the Address Lookup Engine of the ARL. The Address Lookup Engine checks if the destination address matches with any existing address in the address table. If it does, the ARL returns the associated Port ID to ACD's switch controller through the output data bus. Otherwise, a no match result is passed to ACD's switch controller through the output data bus.

CPU Interface

The CPU can access the registers of the ARL by sending commands to the UART data input line. Each command is consisted by action (read or write), register type, register index, and data. Each result of command execution is returned to the CPU through the UART data output line.

CPU Interface Registers

The ARL provides a bunch of registers for the control CPU. Through the registers, the CPU can read all address entries of the address table, delete particular addresses from the table, add particular addresses into the table, secure an address from being changed, set filtering on some addresses, change the hashing algorithm etc. Through a proper interrupt request signal, the CPU can be notified whenever it needs to retrieve data for a newly-learned address or an aged-out address so that the CPU can build an exact same address table learned by the ARL.

CPU Interface Engine

The command sent by the control CPU is executed by the CPU Interface Engine. For example, the CPU may send a command to learn the first newly-learned address. The CPU Interface Engine is responsible to find the newly-learned address from the address table, and passes it to CPU. The CPU may request to learn next newly-learned address. Then, it is again the responsibility of the CPU Interface Engine to search for next newly-learned address from the address table.

Address Table

The address table can hold up to 2,048 MAC addresses, together with the associated port ID, security flag, filtering flag, new flag, aging information etc. The address table resides in the embedded SRAM inside the ARL.

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4. INTERFACE DESCRIPTION

CPU Interface

The CPU can communicate with the ARL through the UART interface of the switch IC. The management CPU can send command to the ARL by writing into associated registers, and retrieve result from ARL by reading corresponding registers. The registers are described in the section of "Register Description." The CPU interface signals are described by *table-1*:

Table-1: CPU Interface

Name	I/O	Description
UARTDI	I	UART input data line.
UARTDO	O	UART output data line.

UARTDI is used by the control CPU to send command into the ARL. The baud rate will be automatically detected by the ARL. The result will be returned through the UARTDO line with the detected baud rate. The format of the command packet is shown as follows:

Header	Address	Data	Checksum

where:

- Header is further defined as:
  b1:b0 - read or write, 01 for read, 11 for write
  b4:b2 - device number, 000 to 111 (0 to 7, same as the host switch controller)
  b7:b5 - device type, 010 for ARL
- Address - 8-bit value used to select the register to access
- Data - 32-bit value, only the LSB is used for write operation, all 0 for read operation
- Checksum - 8-bit value of XOR of all bytes

UARTDO is used to return the result of command execution to the CPU. The format of the result packet is shown as follows:

Header	Address	Data	Checksum

where:

- Header is further defined as:
  b1:b0 - read or write, 01 for read, 11 for write
  b4:b2 - device number, 000 to 111 (0 to 7)
  b7:b5 - device type, 010 for ARL
- Address - 8-bit value for address of the selected register
- Data - 32-bit value, only the LSB is used for read operation, all 0 for write operation
- Checksum - 8-bit value of XOR of all bytes

The ARL will always check the CMD header to see if both the device type and the device number matches with its setting. If not, it ignores the command and will not generate any response to this command.

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5. REGISTER DESCRIPTION

ACD80800 provides a bunch of registers for the CPU to access the address table inside it. Command is sent to ACD80800 by writing into the associated registers. Before the CPU can pass a command to ACD80800, it must check the result register *(register 11)* to see if the command has been done. When the Result register indicates the command has been done, the CPU may need to retrieve the result of previous command first. After that, the CPU has to write the associated parameter of the command into the Data registers. Then, the CPU can write the command type into the command register. When a new command is written into the command register, ACD80800 will change the status of the Result register to 0. The Result register will indicate the completion of the command at the end of the execution. Before the completion of the execution, any command written into the command register is ignored by ACD80800.

The registers accessible to the CPU are described by *table-2*:

Table-2: Register Description

Reg.	Name	Description
0	DataReg0	Byte 0 of data
1	DataReg1	Byte 1 of data
2	DataReg2	Byte 2 of data
3	DataReg3	Byte 3 of data
4	DataReg4	Byte 4 of data
5	DataReg5	Byte 5 of data
6	DataReg6	Byte 6 of data
7	DataReg7	Byte 7 of data
8	AddrReg0	LSB of address value
9	AddrReg1	MSB of address value
10	CmdReg	Command register
11	RsltReg	Result register
12	CfgReg	Configuration register
13	IntSrcReg	Interrupt source register
14	IntMskReg	Interrupt mask register
15	nLearnReg0	Address learning disable register for port 0 - 7
16	nLearnReg1	Address learning disable register for port 8 - 15
17	nLearnReg2	Address learning disable register for port 16 - 23
18	AgeTimeReg0	LSB of aging period register
19	AgeTimeReg1	MSB of aging period register
20	PosCfg	Power On Strobe configuration register 0

The *DataRegX* are registers used to pass the parameter of the command to the ACD80800, and the result of the command to the CPU.

The *AddrRegX* are registers used to specify the address associated with the command.

The *CmdReg* is used to pass the type of command to the ACD80800. The command types are listed in *table-3*. The details of each command is described in the chapter of "Command Description."

Table-3: Command List

Command	Description
0x09	Add the specified MAC address into the address table
0x0A	Set a lock for the specified MAC address
0x0B	Set a filtering flag for the specified MAC address
0x0C	Delete the specified MAC address from the address table
0x0D	Assign a port ID to the specified MAC address
0x10	Read the first entry of the address table
0x11	Read next entry of address book
0x20	Read first valid entry
0x21	Read next valid entry
0x30	Read first new page
0x31	Read next new page
0x40	Read first aged page
0x41	Read next aged page
0x50	Read first locked page
0x51	Read next locked page
0x60	Read first filtered page
0x61	Read next filtered page
0x80	Read first page with specified PID
0x81	Read next page with specified PID
0xFF	System reset

The *RstReg* is used to indicate the status of command execution. The result code is listed as follows:

- *01 - command is being executed and is not done yet*
- *10 - command is done with no error*
- *1x - command is done, with error indicated by x, where x is a 4-bit error code: 0001 for cannot find the entry as specified*

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The *CfgReg* is used to configure the way the ACD80800 works. The bit definition of CfgReg is described as:

- *bit 0 - disable address aging*
- *bit 1 - disable address lookup*
- *bit 2 - disable DA cache*
- *bit 3 - disable SA cache*
- *bit 7:4 - hashing algorithm selection, default is 0000*

The *IntSrcReg* is used to indicate what can cause interrupt request to CPU. The source of interrupt is listed as:

- *bit 0 - aged address exists*
- *bit 1 - new address exists*
- *bit 2 - reserved*
- *bit 3 - reserved*
- *bit 4 - bucket overflowed*
- *bit 5 - command is done*
- *bit 6 - system initialization is completed*
- *bit 7 - self test failure*

The *IntMskReg* is used to enable an interrupt source to generate an interrupt request. The bit definition is the same as IntSrcReg. A 1 in a bit enables the corresponding interrupt source to generate an interrupt request once it is set.

The *nLearnReg[2:0]* are used to disable address learning activity from a particular port. If the bit corresponding to a port is set, ACD80800 will not try to learn new addresses from that port.

The *AgeTimeReg[1:0]* are used to specify the period of address aging control. The aging period can be from 0 to 65535 units, with each unit counted as 2.684 second.

The *PosCfgReg* is a configuration register whose default value is determined by the pull-up or pull-down status of the associated hardware pin. The bits of PosCfgReg0 is listed as follows:

- *bit 3 – BISTEN: "0" = self test disabled, "1" = self test enabled;*
- *bit 2 - TESTEN, "0" = normal operation, "1" = production test enabled;*
- *bit 1* - NOCPU*, "0" = presence of control CPU, "1" = no control CPU;*
- *bit 0 - CPUGO, "0" = wait for System Start command from CPU before starting self initialization, "1" = CPU ready. Only effective when bit-1 (NOCPU) is set to 0;*

Note: When *NOCPU* is set as 0, ACD80800 will not start the initialization process until a System Start command is sent to the command register.

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6. COMMAND DESCRIPTION

Command 09H

Description: Add the specified MAC address into the address table.

Parameter: Store the MAC address into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. Store the associated port number into DataReg6.

Result: the MAC address will be stored into the address table if there is space available. The result is indicated by the Result register.

Command 0AH

Description: Set the Lock bit for the specified MAC address.

Parameter: Store the MAC address into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB.

Result: the state machine will seek for an entry with matched MAC address, and set the Lock bit of the entry. The result is indicated by the Result register.

Command 0BH

Description: Set the Filter flag for the specified MAC address.

Parameter: Store the MAC address into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB.

Result: the state machine will seek for an entry with matched MAC address, and set the Filter bit of the entry. The result is indicated by the Result register.

Command 0CH

Description: Delete the specified MAC address from the address table.

Parameter: Store the MAC address into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB.

Result: the MAC address will be removed from the address table. The result is indicated by the Result register.

Command 0DH

Description: Assign the associated port number to the specified MAC address.

Parameter: Store the MAC address into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. Store the port number into DataReg6.

Result: the port ID field of the entry containing the specified MAC address will be changed accordingly. The result is indicated by the Result register.

Command 10H

Description: Read the first entry of the address table.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of the first entry of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag* bits are stored in DataReg7.The Read Pointer will be set to point to second entry of the address book.

Note - the Flag bits are defined as:

b7	b6	b5	b4	b3	b2	b1	b0
Rsvd	Rsvd	Filter	Lock	New	Old	Age	Valid

where:

- Filter - 1 indicates the frame heading to this address should be dropped.
- Lock - 1 indicates the entry should never be changed or aged out.
- New - 1 indicates the entry is a newly learned address.
- Old - 1 indicates the address has been aged out.
- Age - 1 indicates the address has not been visited for current age cycle.
- Valid - 1 indicates the entry is a valid one.
- Rsvd - Reserved bits.

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Command 11H

Description: Read next entry of address book.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of the address book entry pointed by Read Pointer will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer will be increased by one.

Command 20H

Description: Read first valid entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of first valid entry of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 21H

Description: Read next valid entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of next valid entry from the Read Pointer of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 30H

Description: Read first new page.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of first new entry of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 31H

Description: Read next new entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of next new entry from the Read Pointer of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 40H

Description: Read first aged entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of first aged entry of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 41H

Description: Read next aged entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of next aged entry from the Read Pointer of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

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Command 50H

Description: Read first locked entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of first locked entry of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 51H

Description: Read next locked entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of next locked entry from the Read Pointer of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 60H

Description: Read first filtered page.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of first filtered entry of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 61H

Description: Read next valid entry.

Parameter: None

Result: The result is indicated by the Result register. If the command is completed with no error, the content of next filtered entry from the Read Pointer of the address book will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 80H

Description: Read first entry with specified port number.

Parameter: Store port number into DataReg6.

Result: The result is indicated by the Result register. If the command is completed with no error, the content of first entry of the address book with the said port number will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command 81H

Description: Read next valid entry.

Parameter: Store port number into DataReg6.

Result: The result is indicated by the Result register. If the command is completed with no error, the content of next entry from the Read Pointer of the address book with the said port number will be stored into the Data registers. The MAC address will be stored into DataReg5 - DataReg0, with DataReg5 contains the MSB of the MAC address and DataReg0 contains the LSB. The port number is stored in DataReg6, and the Flag bits are stored in DataReg7. The Read Pointer is set to point to this entry.

Command FFH

Description: System reset.

Parameter: None

Result: This command will reset the ARL system. All entries of the address book will be cleared.

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