Stereo 1.8-W Audio Power Amplifier

Features

- **Low Supply Current, I_{DD} = 12mA**
- **High PSRR (Power Supply Ripple Rejection)**
- **De-pop Circuitry Integrated**
- **Thermal Shutdown Circuitry Integrated**
- **Output Power at 1% THD+N, V_{DD} =5V**
  - 1.6 W/Ch (typ) into a 4W Load
  - 1.1 W/Ch (typ) into an 8W Load
- **Bridge-Tied Load (BTL) or Single-Ended (SE) Modes Operation**
- **Low Shutdown Current, I_{DD} =0.5µA**
- **Short Circuit Protection**
- **SOP-16P with Thermal Pad Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Notebook Computer**
- **LCD Monitor or TV**

General Description

The APA2066 is a stereo bridge-tied audio power amplifier in 16-pin SOP. When connecting to a 5V voltage supply, the APA2066 is capable of delivering 1.6W/1.1W of continuous RMS power per channel into 4/8Ω loads with less than 1% THD+N, respectively. The APA2066 simplifies design and frees up board space for other features. Both of the de-pop circuitry and the thermal shutdown protection circuitry are integrated in the APA2066, that reduces pops and clicks noise during power up and when using the shutdown or mute modes and protects the chip from being destroyed by over-temperature failure.To simplify the audio system design in notebook computer applications, the APA2066 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{BTL}$ input control pin signal. For power sensitive applications, the APA2066 also features a shutdown function, which keeps the supply current only 0.5µA (typ).

Ordering and Marking Information

APA2066 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

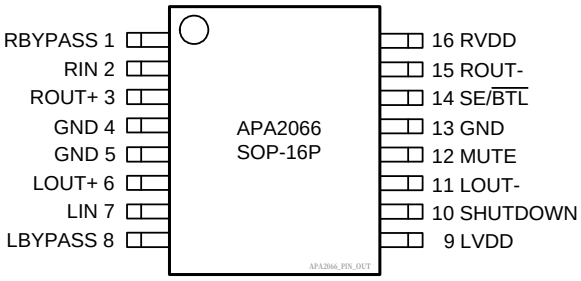
Package Code
KA : SOP-16P
Temperature Range
I : - 40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
L : Lead Free Device
G : Halogen and Lead Free Device

APA2066 KA : APA2066 XXXXX

XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating
V_{DD}	Supply Voltage Range	-0.3V to 6V
V_{IN}	Input Voltage Range at SE/$\overline{BTL}$, HP/$\overline{LINE}$, SHUTDOWN	-0.3V to V_{DD}
T_A	Operating Ambient Temperature Range	-40°C to 85°C
T_J	Maximum Junction Temperature	Internal Limited
T_{STG}	Storage Temperature Range	-65°C to 150°C
T_S	Soldering Temperature, 10 Seconds	260°C
P_D	Power Dissipation	Internal Limited

Note 1: Human body model : C=100pF , R=1500Ω , 3 positive pulses plus 3 negative pulses.
Note 2: Machine model : C=200pF , L=0.5mH , R=0Ω , 3 positive pulses plus 3 negative pulses.

Recommendend Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.5	V

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Thermal Resistance from Junction to Ambient in Free Air	SOP-16P	45	°C/W

Electrical Characteristics

V_{DD}= 5V , -20°C < T_A < 85°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2066			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		4.5	-	5.5	V
I_{DD}	Supply Current	SE/$\overline{BTL}$=5V	-	12	18	mA
		SE/$\overline{BTL}$=5V	-	6	10	mA
I_{SD}	Supply Current in Shutdown Mode	SHUTDOWN = 5V	-	0.5	5	µA
I_{IH}	High Input Current		-	900	-	nA
I_{IL}	Low Input Current		-	900	-	nA
V_{OS}	Output Differential Voltage		-	5	-	mV
V_{IH}	High Level Threshold Voltage	SHUTDOWN, MUTE	2	-	-	V
		SE/$\overline{BTL}$	4	-	-	V
V_{IL}	Low Level Threshold Voltage	SHUTDOWN, MUTE	-	-	1.0	V
		SE/$\overline{BTL}$	-	-	3	V

AC Operating Characteristics , V_{DD}= 5V , T_A= 25°C , R_L= 4Ω (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2066			Unit
			Min.	Typ.	Max.	
P_O	Output Power (each Channel) (Note 3)	THD+N = 10%, BTL, R_L=4Ω R_L=8Ω	-	 2.0 1.4	-	W
		THD+N = 1%, BTL, R_L=4Ω R_L=8Ω	-	 1.6 1.1	-	W
		THD+N = 10%, SE, R_L = 4Ω R_L = 8Ω	-	 650 400	-	mW
		THD+N = 1%, SE, R_L = 4Ω R_L = 8Ω	-	 500 320	-	mW
		THD+N = 0.5%, SE, R_L = 32Ω	-	 90	-	mW
THD+N	Total Harmonic Distortion Plus Noise	P_O = 1.4W, BTL, R_L = 4Ω P_O = 0.9W, BTL, R_L = 8Ω P_O = 78mW, SE, R_L = 32Ω	-	0.3 0.15 0.02	-	%
BOM	Maximum Output Power Bandwidth	A_V = 10, THD+N < 1%	-	>20	-	kHz

Electrical Characteristics (Cont.)

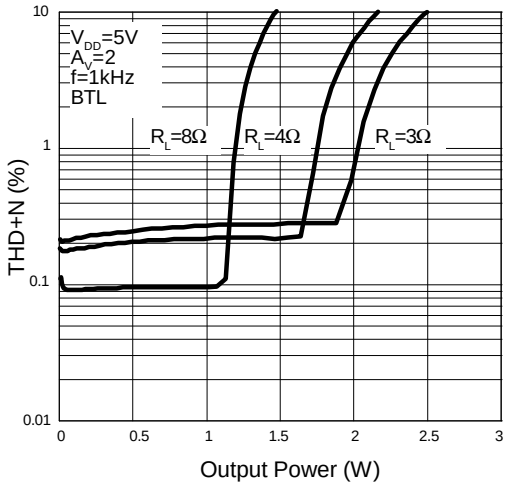
AC Operating Characteristics , V_{DD}= 5V , T_A= 25°C , R_L= 4Ω (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2066			Unit
			Min.	Typ.	Max.	
	Phase Margin	R_L = 4Ω, BTL	-	72	-	°
		R_L = 4Ω, Open Load	-	71	-	
		R_L = 4Ω, SE	-	52	-	
PSRR	Power Supply Ripple Rejection	f = 100 Hz, BTL	-	80	-	dB
		f = 100 Hz, SE	-	55	-	dB
	Mute Attenuation		-	85	-	dB
	Channel-to-Channel Output Separation		-	85	-	dB
	BTL Attenuation in SE Mode		-	80	-	dB
Z_I	Input Impedance		-	2	-	MΩ
S/N	Signal-to-Noise Ratio	Po = 500 mW, BTL mode	-	90	-	dB
V_N	Output Noise Voltage		-	20	-	μV (rms)

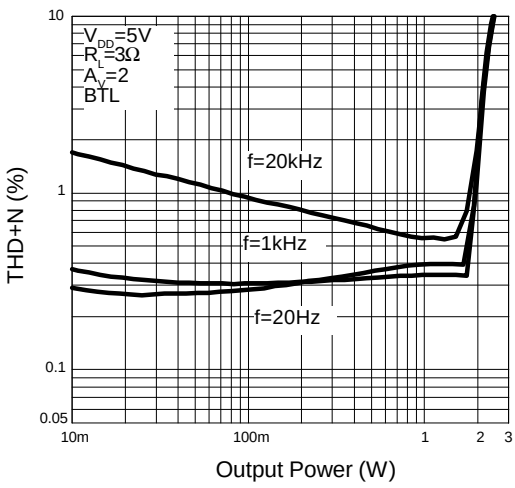
Note3 : Output power is measured at the output terminals of the IC at 1kHz.

Typical Operating Characteristics

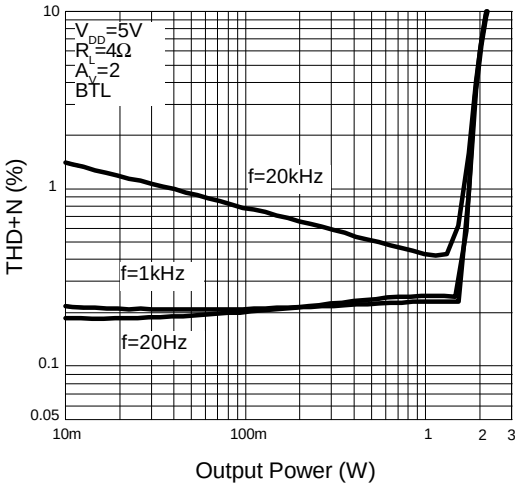
THD+N vs. Output Power



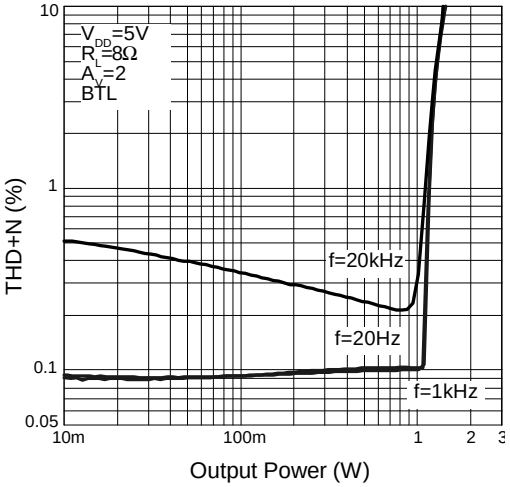
THD+N vs. Output Power



THD+N vs. Output Power

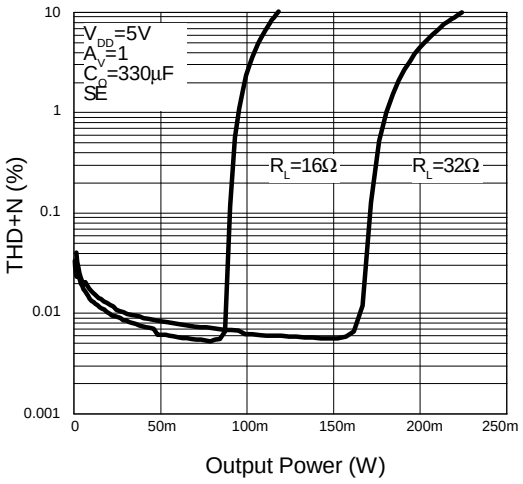


THD+N vs. Output Power

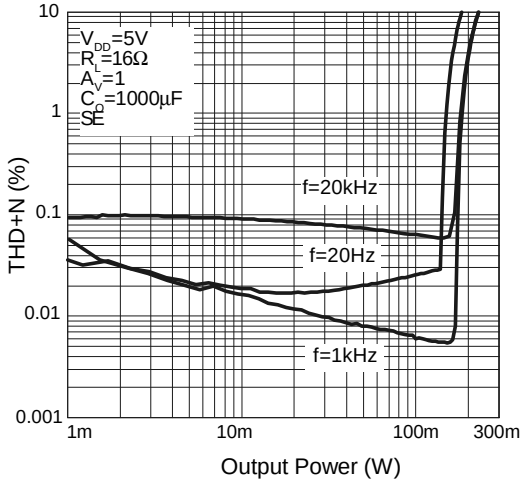


Typical Operating Characteristics (Cont.)

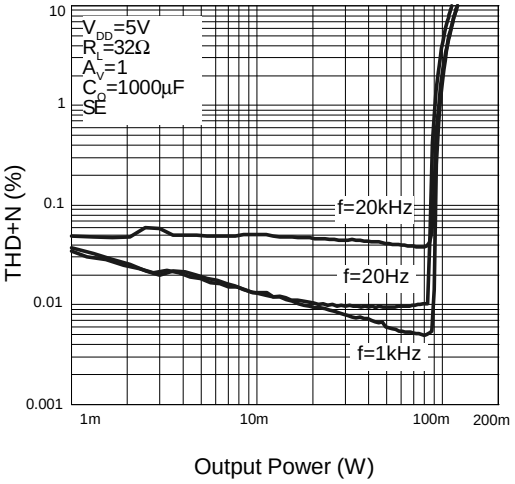
THD+N vs. Output Power



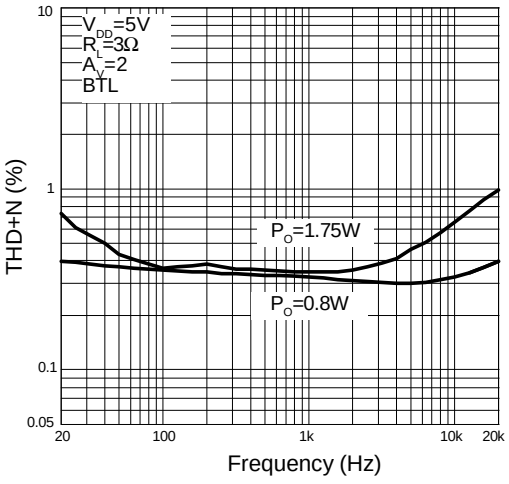
THD+N vs. Output Power



THD+N vs. Output Power

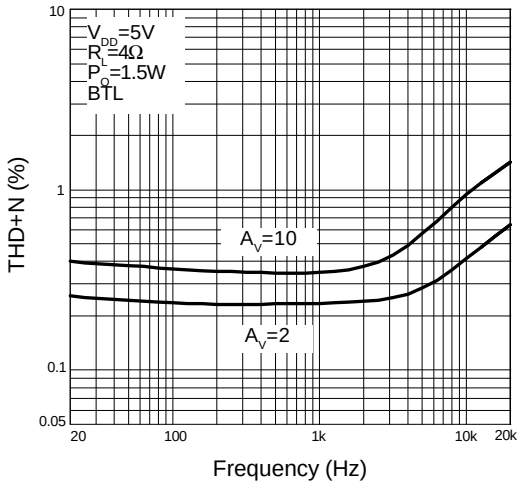


THD+N vs. Frequency

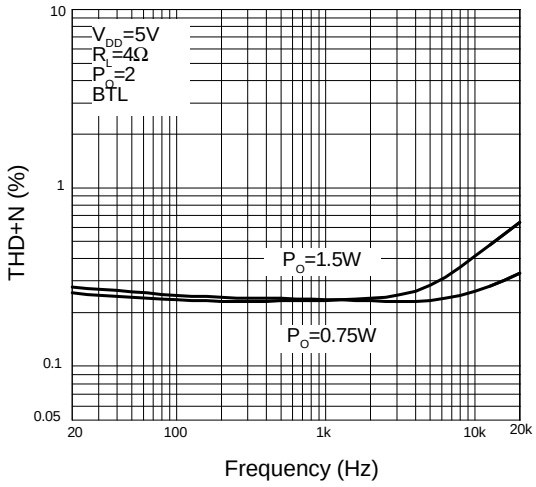


Typical Operating Characteristics (Cont.)

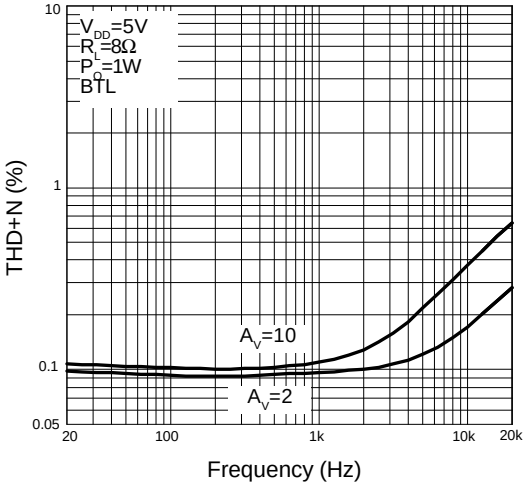
THD+N vs. Frequency



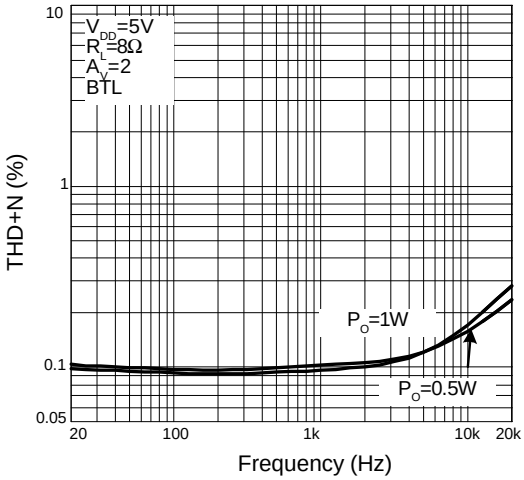
THD+N vs. Frequency



THD+N vs. Frequency

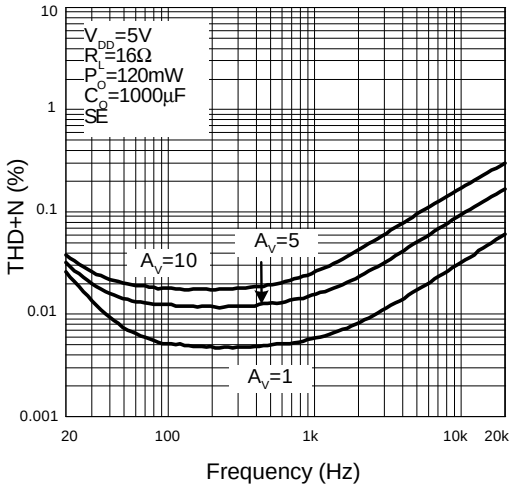


THD+N vs. Frequency

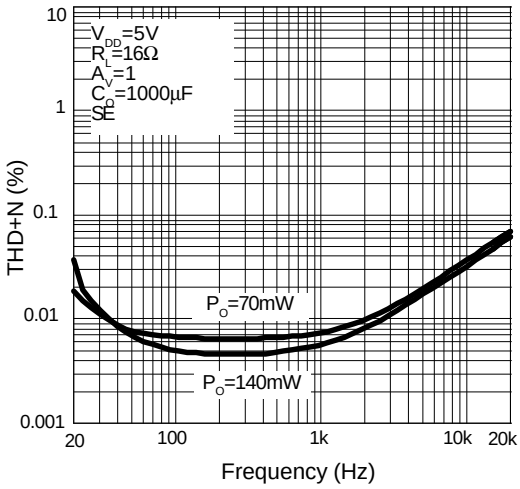


Typical Operating Characteristics (Cont.)

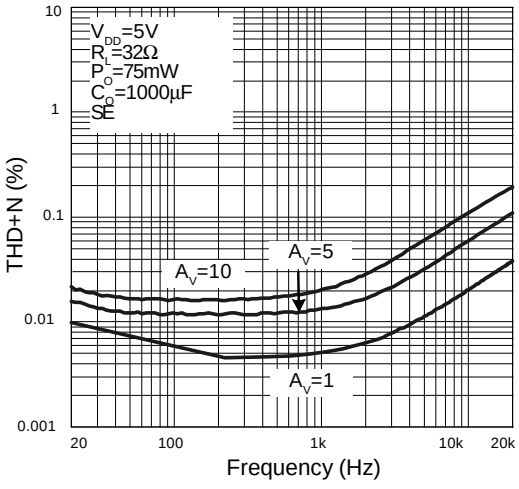
THD+N vs. Frequency



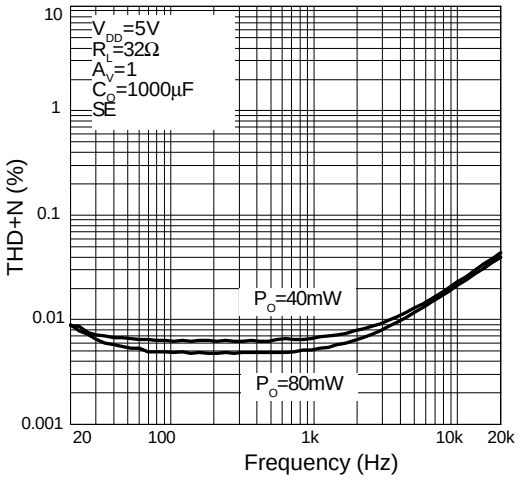
THD+N vs. Frequency



THD+N vs. Frequency

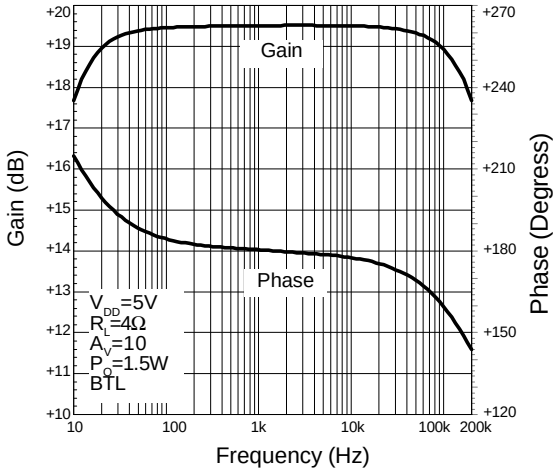


THD+N vs. Frequency

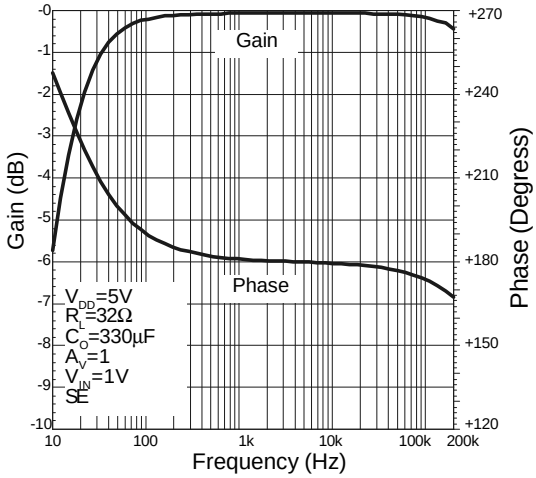


Typical Operating Characteristics (Cont.)

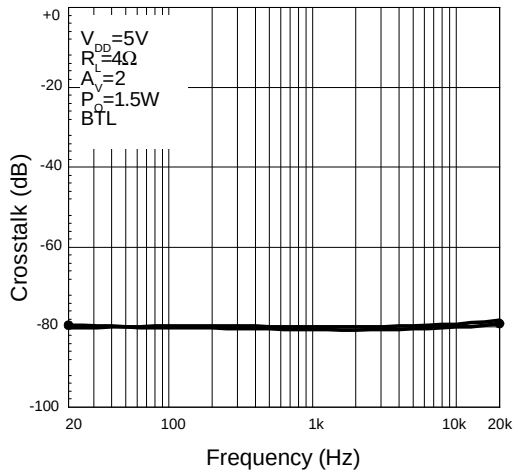
Frequency Response



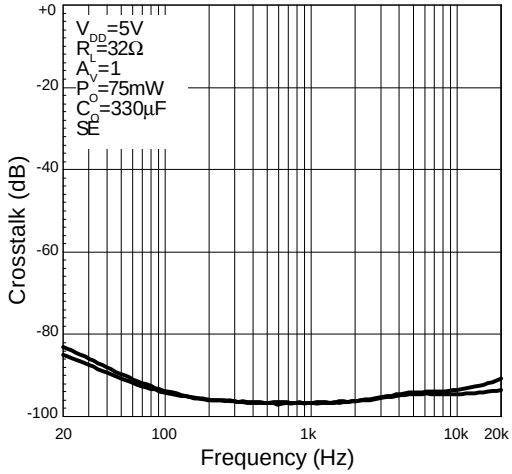
Frequency Response



Crosstalk vs Frequency

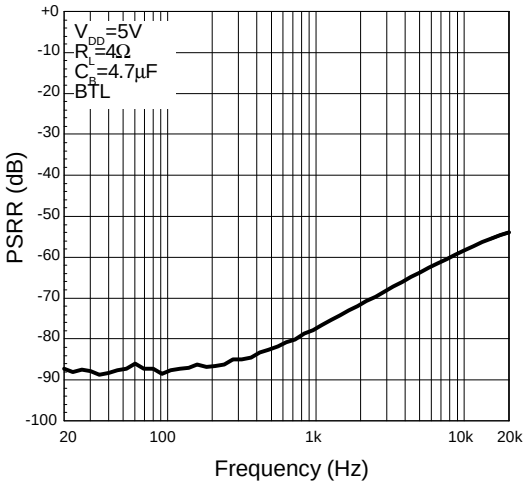


Crosstalk vs Frequency

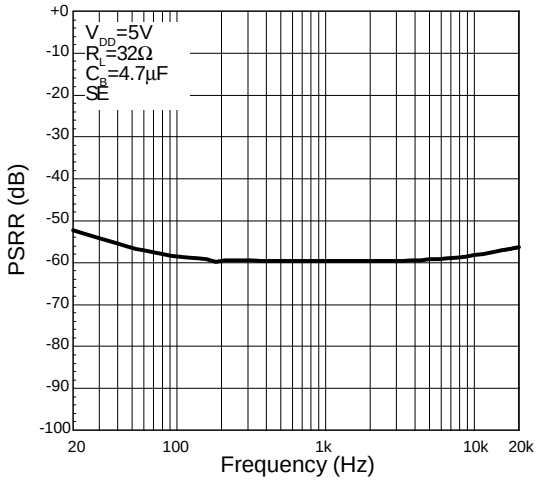


Typical Operating Characteristics (Cont.)

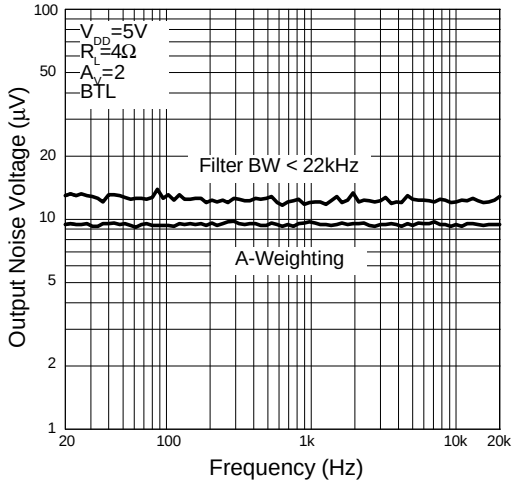
PSRR vs. Frequency



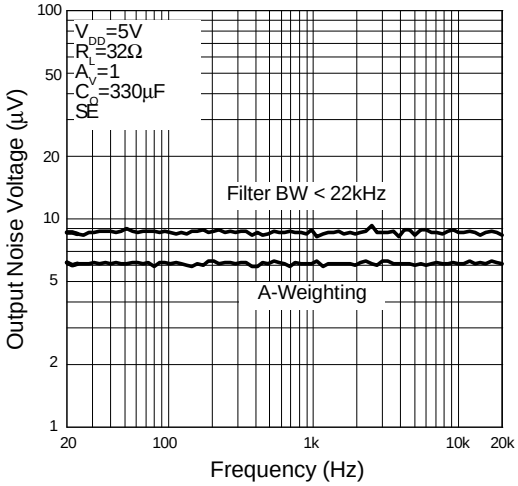
PSRR vs. Frequency



Noise Floor vs. Frequency

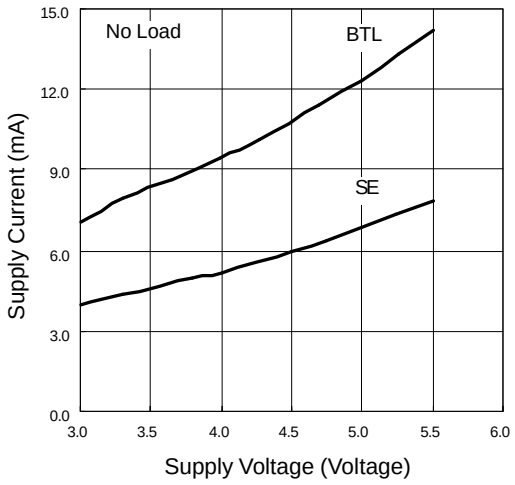


Noise Floor vs. Frequency

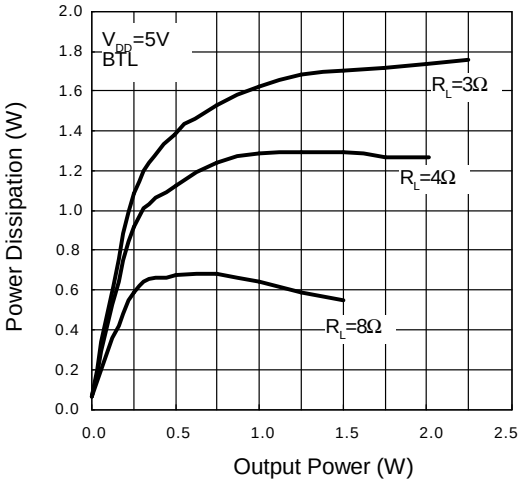


Typical Operating Characteristics (Cont.)

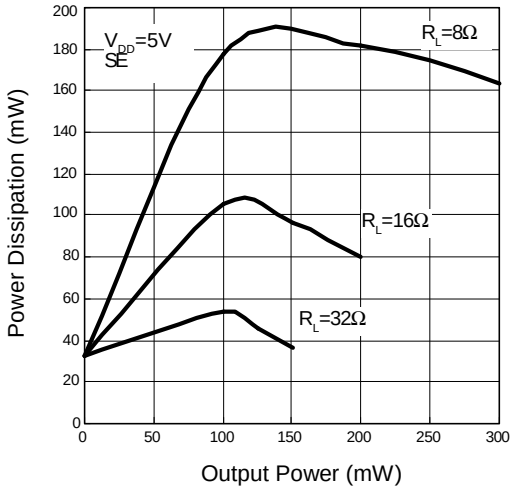
Supply Current vs. Supply Voltage



Power Dissipation vs. Output Power



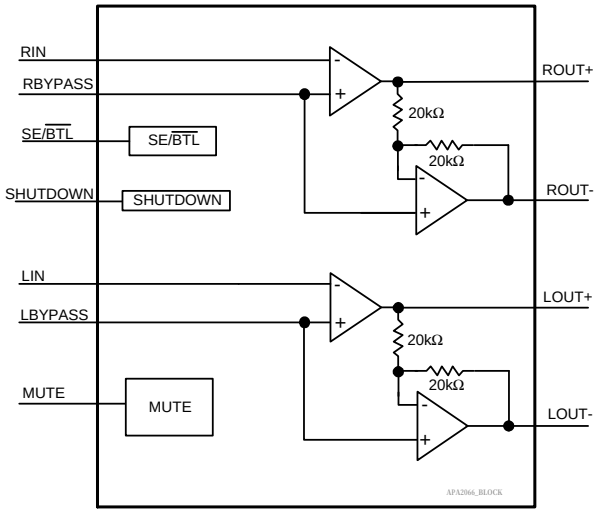
Power Dissipation vs. Output Power



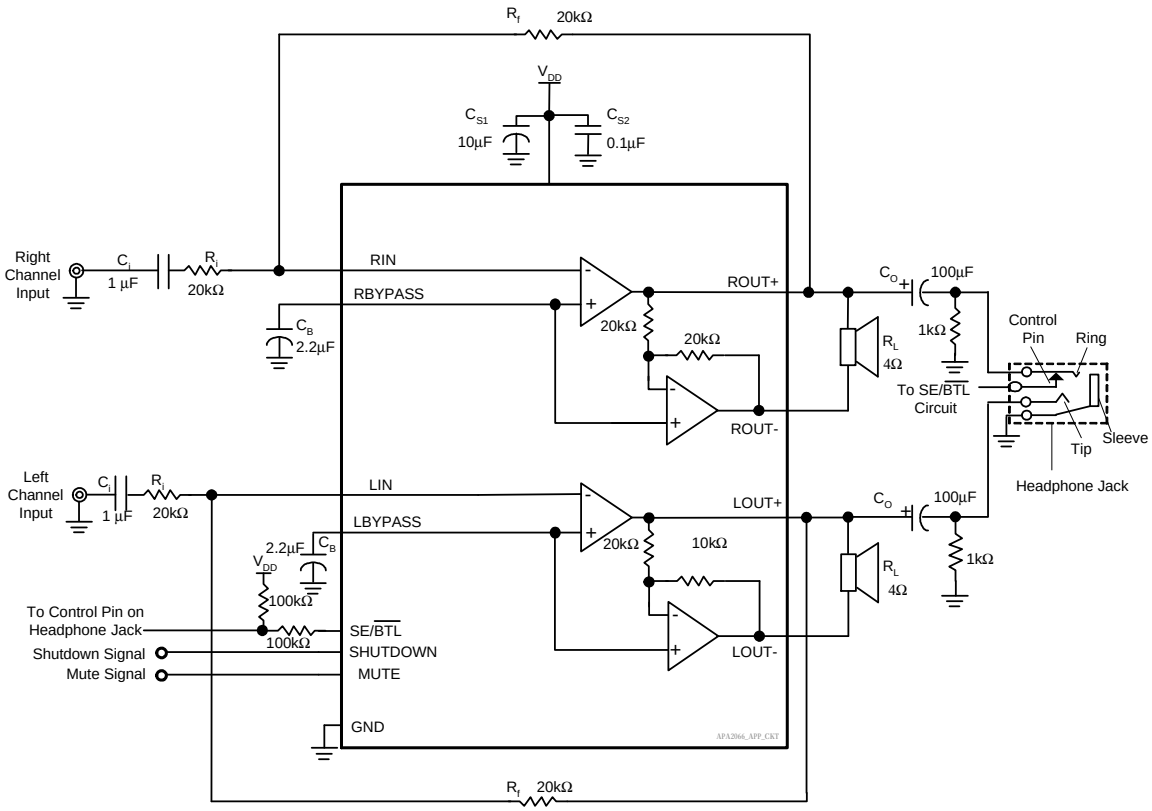
Pin Description

PIN		I/O	FUNCTION
NAME	NO		
RBYPASS	1	-	Connect to voltage divider for right channel internal mild-supply bias.
RIN	2	I	Right channel line input.
ROUT+	3	O	Right channel positive output in BTL mode and SE mode.
GND	4,5,13	-	Ground connection for circuitry, directly connected to thermal pad
LOUT +	6	O	Left channel positive output in BTL mode and SE mode.
LIN	7	I	Left channel input.
LBYPASS	8	-	Connect to voltage divider for left channel internal mid-supply bias.
LV_{DD}	9	-	Supply voltage input for left channel and for primary bias circuits.
SHUTDOWN	10	I	Shutdown mode control signal input, places entire IC in shutdown mode when held high, I_{DD} = 0.5µA.
LOUT -	11	O	Left channel negative output in BTL mode, high-impedance state in SE mode.
MUTE	12	I	Mute control signal input, hold low for normal operation, hold high to mute.
SE/$\overline{BTL}$	14	I	Mode control signal input, hold low for BTL mode, hold high for SE mode.
ROUT-	15	O	Right channel negative output in BTL mode, high impedance state in SE mode.
RV_{DD}	16	-	Supply voltage input for right channel.

Block Diagram



Application Circuit



Application Information

BTL Operation

The APA2066 has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

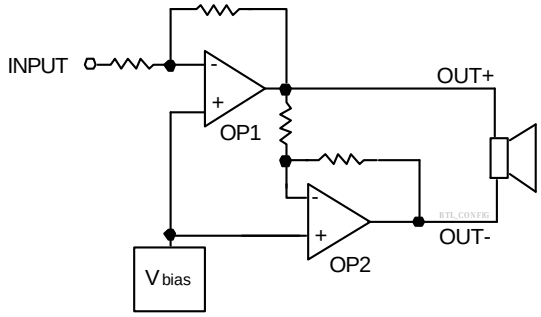


Figure 1: APA2066 internal configuration (each channel)

The first amplifier's OP1 gain is setting by Ri and Rf, while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude but out of phase 180°. Consequently, the differential gain for each channel is 2 X (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration commonly referred to as bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage. Four times the output power is possible as compared to a SE amplifier under the same conditions. A BTL configuration, such as the one used in APA2066, also creates the second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor, which is required in a single supply, SE configuration.

Single-Ended Operation

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the OutputCoupling Capacitor).

The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{C_B x 125k\ \Omega} \leq \frac{1}{C_i x R_i} << \frac{1}{R_L x C_O} \qquad (1)$$

Application Information (Cont.)

Output SE/$\overline{BTL}$ Operation

The ability of the APA2066 to easily switch between BTL and SE modes is one of its most important costs saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

Internal to the APA2066, two separate amplifiers drive OUT+ and OUT- (see Figure 1). The SE/$\overline{BTL}$ input controls the operation of the follower amplifier that drives LOUT- and ROUT-.

- When SE/$\overline{BTL}$ is held low, the OP2 is on and the APA2066 is in the BTL mode.
- When SE/$\overline{BTL}$ is held high, the OP2 is in a high output impedance state, which configures the APA2066 as SE driver from OUT+. I_{DD} is reduced by approximately one-half in SE mode.

Control of the SE/$\overline{BTL}$ input can be a logic-level TTL source or a resistor divider network or the stereo headphone jack with switch pin as shown in Application Circuit.

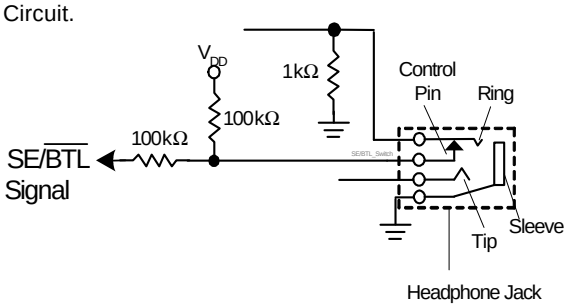


Figure 2: SE/$\overline{BTL}$ input selection by Readphone plug

In Figure 2, input SE/$\overline{BTL}$ operates as follows:

When the Readphone plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{BTL}$ input is pulled high and enables the SE mode. When the input goes high, the OUT- amplifier is shutdown causing the speaker to mute. The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, the voltage divider set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/$\overline{BTL}$ pin, enabling the BTL function.

Gain Setting Resistors, Rf and Ri

$$\text{SE Gain} = -\frac{R_f}{R_i} \quad (2)$$

$$\text{BTL Gain} = -2 \times \frac{R_f}{R_i} \quad (3)$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance Ri form a high-pass filter with the corner frequency determined in the following equation:

$$f_C(\text{highpass}) = \frac{1}{2\pi R_i \times C_i} \quad (4)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where R_i is 100kΩ and the specification calls for a flat bass response down to 40Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi \times 100\,k\Omega \times 40\,Hz} \quad (5)$$

The value of C_i should be 0.04μF and consider the variation of input resistance (R_i). It is better to choose a value in the range from 0.1μF to 1.0μF.

A further consideration for this capacitor is the leakin high gain applications. For this reason, a low-leakage tantalumor ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level of the amplifiers' inputs are held at $V_{DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Application Information (Cont.)

Effective Bypass Capacitor, C_B

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitor location on the bypass and pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor is improved PSRR due to increased half-supply stability.The selection of bypass capacitors, C_B ,is dependent upon desired PSRR requirements, click and pop performance.

On the chip, there are three bypass pins for used, and it is tied together in the internal circuit. The effective capacitance is the $C_B=(C_{BR}//C_{BL})$. In application circuit, the full feature configuration, two bypass capacitors are used for each channel. This provides the maximum separation between right and left channel drive circuits. When absolute minimum cost and/or component space is required, one bypass capacitor can be used.

To avoid start-up pop noise occurred, the bypass voltage should be rise slower then the input bias voltage and the relationship shown in equation should be maintained.

$$\frac{1}{C_B \times 125k\Omega} << \frac{1}{C_i \times 140k\Omega} \quad (6)$$

The capacitor is fed from a 125kΩ source inside the amplifier. Bypass capacitor, C_B, values of 2.2µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N performance.

The bypass capacitance also effect to the start up time. It is determined in the following equation:

$$T_{start\ up} = 5x(C_B x 125k\Omega) \quad (7)$$

Output Coupling Capacitor, C_o

In the typical single-supply SE configuration, an output coupling capacitor (C_O) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by the following equation.

$$f_c(highpass) = \frac{1}{2\pi R_L C_O} \quad (8)$$

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. The main disadvantag from a performance standpoint, is the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_o are required to pass low frequencies into the load.

Power Supply Decoupling, C_s

The APA2066 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types capacitors that target on different type of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device VDD lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Shutdown Function

In order to reduce power consumption while not in using, the APA2066 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the SHUTDOWN pin. The trigger point between a logic high and logic low level is typically 2.0V. It is the best to switch between ground and the supply V_{DD} to provide maximum device performance.

By switching the SHUTDOWN pin to high, the amplifier enters a low-current state, I_{DD}<0.5µA. APA2066 is in shutdown mode. On normal operating, SHUTDOWN pin pulls to low level to keep the IC out of the shutdown mode. The SHUTDOWN pin should be tied to a definite voltage to avoid unwanted state changing.

Application Information (Cont.)

Optimizing Depop Circuitry

Circuitry has been included in the APA2066 to minimize the amount of popping noise at power-up when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the clicks and pops. The value of C_i will also affect turn-on pops (Refer to Effective Bypass Capacitance).

The bypass voltage rises up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of C_B can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_B, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_B and the turn-on time.

In a SE configuration, the output coupling capacitor, C_O, is of particular concern. This capacitor discharges through the internal 10kΩ resistors. Depending on the size of C_O, the time constant can be relatively large. To reduce transients in SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current.

In the most cases, choosing a small value of C_i in the range from 0.33μF to 1μF, C_B being equal to 4.7μF and an external 1kΩ resistor should be placed in parallel with the internal 10kΩ resistor should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Therefore, it is advantageous to use low-gain configurations.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \qquad (9)$$

Where:

$$P_O = \frac{V_{orms} \times V_{orms}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_{orms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L}$$

Efficiency of a BTL configuration:

$$\left(\frac{V_P \times V_P}{2R_L}\right) / \left(V_{DD} \times \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \qquad (10)$$

Table 1 calculates efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

P_o (W)	Efficiency (%)	I_{DD} (A)	V_{PP}(V)	P_D (W)
0. 25	31.25	0.16	2.00	0.55
0. 50	47.62	0.21	2.83	0.55
1. 00	66.67	0.30	4.00	0.5
1. 25	78.13	0.32	4.47	0.35

**High peak voltages cause the THD+N to increase.

Table 1. Efficiency vs. Output Power in 5-V/8Ω BTL Systems

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in the equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Application Information (Cont.)

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern.

In equation11 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode : } P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \quad (11)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus, the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \quad (12)$$

(Since the APA2066 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the APA2066 does not require extra heatsink. The power dissipation from equation12, as suming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation13:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (13)$$

For SOP-16P package with thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of APA2066 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation13. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L)must be increased or the ambient temperature should be reduced.

Thermal Pad Consideration

The thermal pad must be connected to ground. The package with thermal pad of the APA2066 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA2066 will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the APA2066 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 12 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA2066 junction temperature below the thermal shutdown temperature (150°C).

In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions.

Using the power dissipation curves for a 5V/4Ω system, the internal dissipation in the APA2066 and maximum ambient temperatures is shown in Table2.

Peak output power (W)	Average output power (W)	Power dissipation (W /channel)	Max. T_A (℃)
			With thermal pad
2	0.74	1 .1 9	43
2	0.43	1 .0 5	55
2	0.19	0 .8	78

Table2: APA2066 Power information, 5V/4Ω, Stereo, BTL

The maximum ambient temperature depends on the heatsink ability of the PCB system.

To calculate maximum ambient temperatures, first consideration is that the numbers from the dissipation graphs are per channel values, therefore, the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature ($T_{J,MAX}$), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation.

Application Information (Cont.)

Thermal Consideration (Cont.)

The maximum recommended junction temperature for the APA2066 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

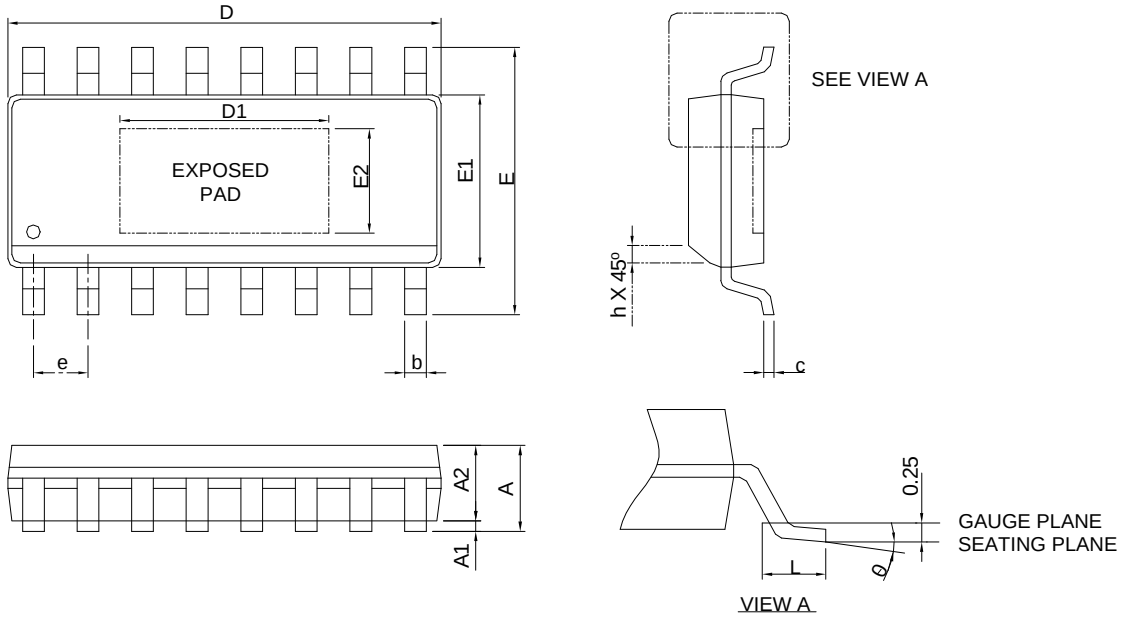
$$T_{A,Max} = T_{J,Max} - \theta_{JA} P_D \quad (14)$$

150 - 45(0.8*2) = 78°C (With thermal pad)

Table 2 shows that for some applications no airflow is required to keep junction temperatures in the specified range. The APA2066 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC. The information in table2 was calculated for maximum listen volume with limited distortion. When the output level is reduced, the numbers in the table change significantly. Also, using 8Ω speakers will dramatically increase the thermal performance by increasing amplifier efficiency.

Package Information

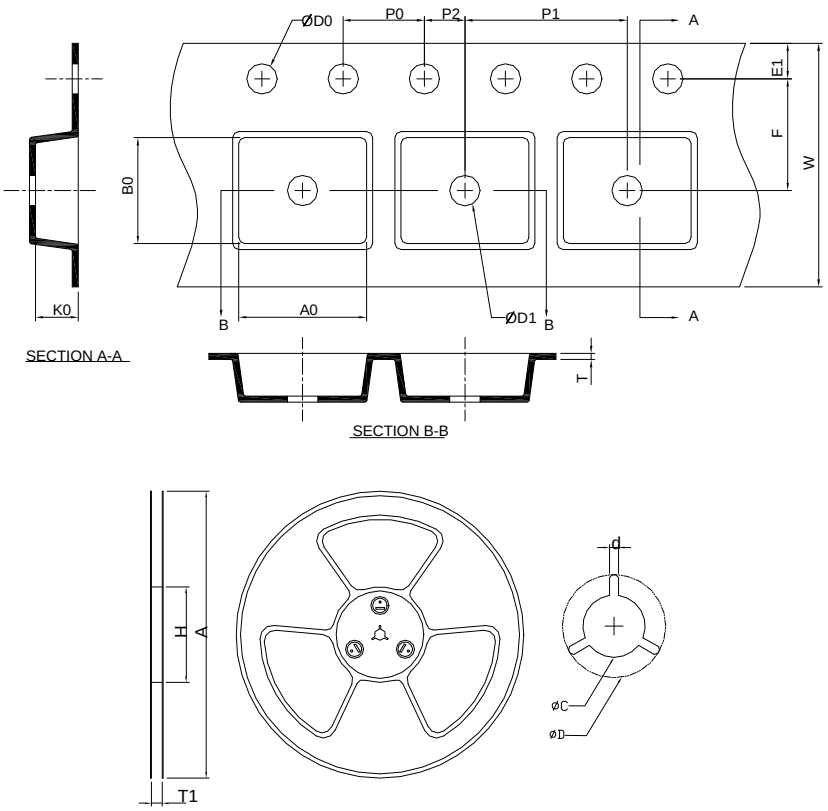
SOP-16P



SYMBOL	SOP-16P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	9.80	10.00	0.386	0.394
D1	3.50	4.50	0.138	0.177
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow from JEDEC MS-012 BC.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



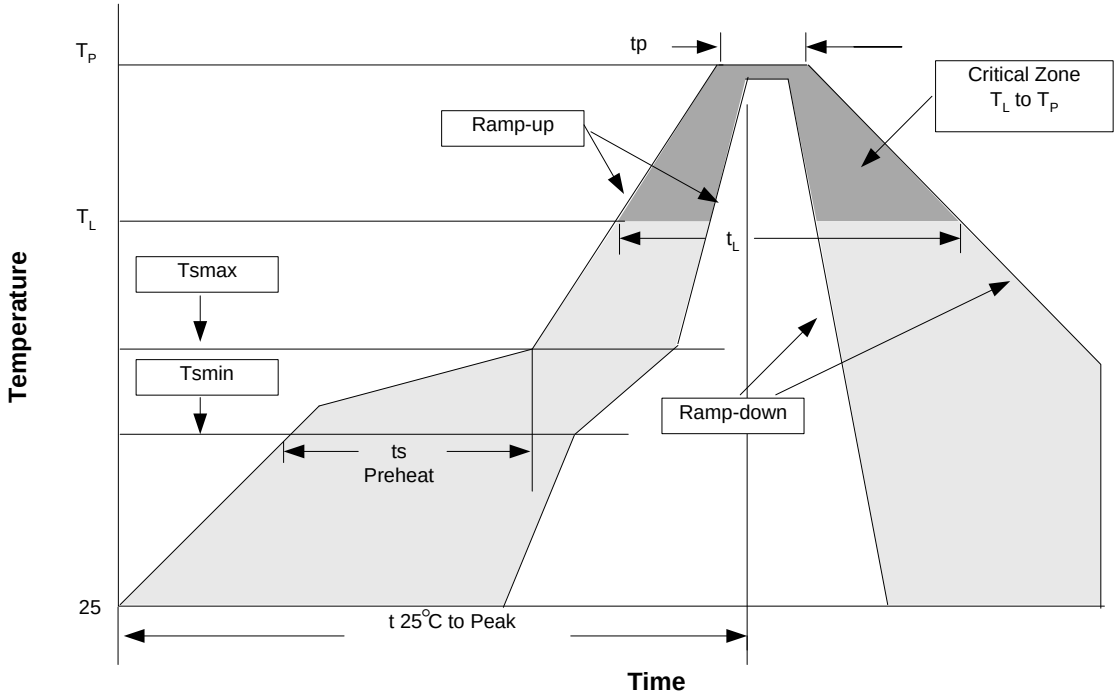
Application	A	H	T1	C	d	D	W	E1	F
SOP-16P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	10.30±0.20	2.10±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP-16P	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

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