May 1999

DS7831DS8832 Dual TRI-STATE Line Driver

National Semiconductor

DS7831/DS8832 Dual TRI-STATE[®] Line Driver

General Description

Through simple logic control, the DS7831/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS8832 does not have the V_{CC} clamp diodes found on the DS7831.

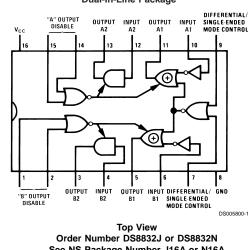
The DS7831 is specified for operation over the -55° C to +125°C military temperature range. The DS8832 is specified for operation over the 0°C to +70°C temperature range.

FeaturesSeries 54/74 compatible

- 17 ns propagation delay
- Very low output impedance high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

Connection and Logic Diagram

Dual-In-Line Package



Order Number DS8832J or DS8832N See NS Package Number J16A or N16A For Complete Military 883 Specificatons, See RETS Data Sheet. Order Number DS7831J/883, DS7831W/883, See NS Package Number J16A or W16A

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Truth Table

"A" Output Disable		Differential/ Single-Ended		Input A1	Output A1	Input A2	Output A2		
		Mode C	ontrol						
0	0	0	0	Logical "1" or	Same as	Logical "1" or	Same as		
				Logical "0"	Input A1	Logical "0"	Input A2		
0	0	Х	1	Logical "1" or	Opposite of	Logical "1" or	Same as		
0		1	X	Logical "0"	Input A1	Logical "0"	Input A2		
1	Х				High		High		
Х	1	X	X	х	Impedance	х	Impedance		
					State		State		

X = Don't Care

Absolute Maximum Ratings (Note 2)

Supply Voltage

Cavity Package

Molded Package

Storage Temperature Range

Lead Temperature (Soldering, 4 sec.)

Maximum Power Dissipation (Note 1) at 25°C

Input Voltage Output Voltage

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Operating	Conditions
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	Min	Max	Units
Supply Voltage (V _{CC})			
DS7831	4.5	5.5	V
DS8831/DS8832	4.75	5.25	V
Temperature (T _A)			
DS7831	-55	+125	°C
DS8832	0	+70	°C
Note 1: Derate cavity package 9.6 age 10.9 mW/°C above 25°C.	8 mW/°C above 2	5°C; derate mo	ded pack-

Electrical Characteristics (Notes 3, 4)

Symbol	Parameter	Conditions			Min	Тур	Max	Units
VIH	Logical "1" Input Voltage	V _{CC} = Min			2.0			V
VIL	Logical "0" Input Voltage	V _{CC} = Min					0.8	V
V _{OH}	Logical "1" Output Voltage	DS7831		$I_{O} = -40 \text{ mA}$	1.8	2.3		V
			V _{CC} = Min	$I_0 = -2 \text{ mA}$	2.4	2.7		V
		DS8832	7	$I_{O} = -40 \text{ mA}$	1.8	2.5		V
				$I_{\rm O} = -5.2 \text{ mA}$	2.4	2.9		V
V _{OL}	Logical "0" Output Voltage	DS7831		I _O = 40 mA		0.29	0.50	V
			V _{CC} = Min	I _O = 32 mA			0.40	V
		DS8832	7	I _O = 40 mA		0.29	0.50	V
				I _O = 32 mA			0.40	V
I _{IH}	Logical "1" Input Current	V _{CC} = Max DS7831, V _{IN} = 5.5V				1	mA	
			DS8832, V _{IN} = 2.4V				40	μA
I _{IL}	Logical "0" Input Current	V _{CC} = Max, V _{IN}	= 0.4V		-1.0	-1.6	mA	
I _{OD}	Output Disable Current	$V_{CC} = Max, V_O = 2.4V \text{ or } 0.4V$			-40		40	μA
I _{sc}	Output Short Circuit Current	V _{CC} = Max, (Note 5)			-40	-100	-120	mA
I _{cc}	Supply Current	V _{CC} = Max in TRI-STATE				65	90	mA
V _{CLI}	Input Diode Clamp Voltage	$V_{CC} = 5.0V, T_A = 25^{\circ}C, I_{IN} = -12 \text{ mA}$					-1.5	V
V _{CLO}	Output Diode Clamp	V _{CC} = 5.0V,	I _{OUT} = -12 mA	DS7831			-1.5	V
	Voltage	T _A = 25°C		DS8832				
			I _{OUT} = 12 mA	DS7831			V _{CC} + 1.5	V

7V

5.5V

5.5V

260°C

1433 mW

1362 mW

-65°C to +150°C

Switching Characteristics $T_{r} = 25^{\circ}C$, $V_{res} = 5V$, upless otherwise note

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd0}	Propagation Delay to a Logical "0"					
	from Inputs A1, A2, B1, B2			13	25	ns
	Differential Single-ended Mode					
	Control to Outputs					
t _{pd1}	Propagation Delay to a Logical "1"					
	from Inputs A1, A2, B1, B2			13	25	ns
	Differential Single-ended Mode					
	Control to Outputs					
t _{1H}	Delay from Disable Inputs to High					
	Impedance State (from Logical "1"	(See Figure 4 and Figure 5)		6	12	ns
	Level)					
t _{oH}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)			14	22	ns

Switching Characteristics (Continued)							
Symbol	C, V _{CC} = 5V, unless otherwise noted Parameter	Conditions	Min	Тур	Max	Units	
t _{H1}	Propagation Delay from Disable Inputs						
	to Logical "1" Level (from High			14	22	ns	
	Impedance State)						
t _{HO}	Propagation Delay from Disable Inputs						
	to Logical "0" Level (from High			18	27	ns	
	Impedance State)						

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation. Note 3: Unless otherwise specified min/max limits apply across the -55°C to +125°C temperature range for the DS7831 and across the 0°C to +70°C range for the DS8832. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 4: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 5: Applies for $T_A = 125^{\circ}C$ only. Only one output should be shorted at a time.

Mode of Operation

To operate as a quad single-ended line driver apply logical "0"s to the output disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs.

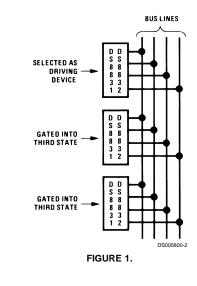
The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

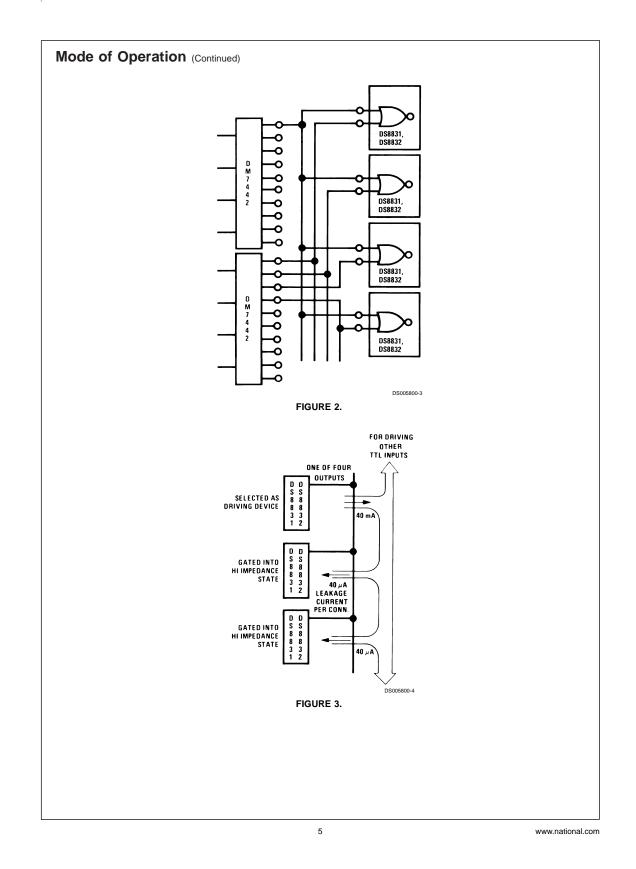
When operating in a bus-organized system with outputs tied directly to outputs of other DS7831, DS8832's (*Figure 1*), all devices except one must be placed in the "high impedance"

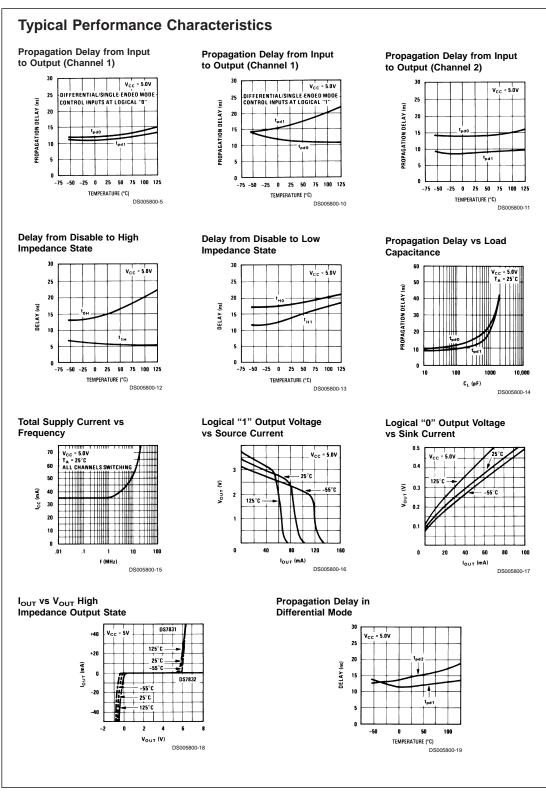
state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831, DS8832's (*Figure 2*).

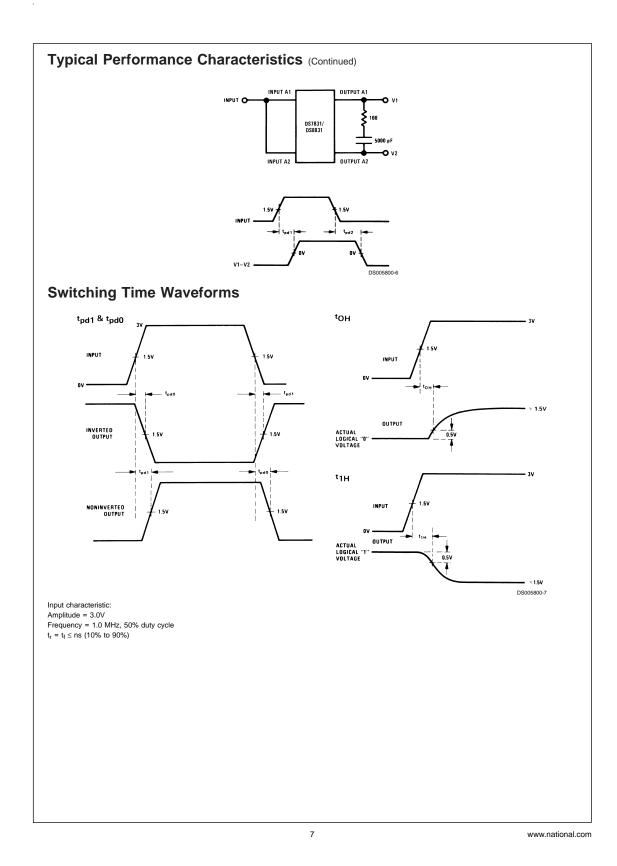
The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μ A), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line (*Figure 3*).

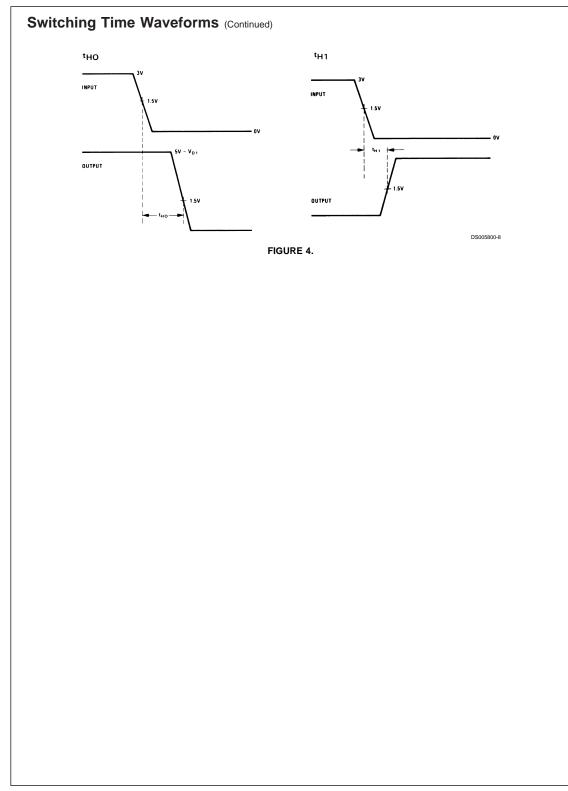


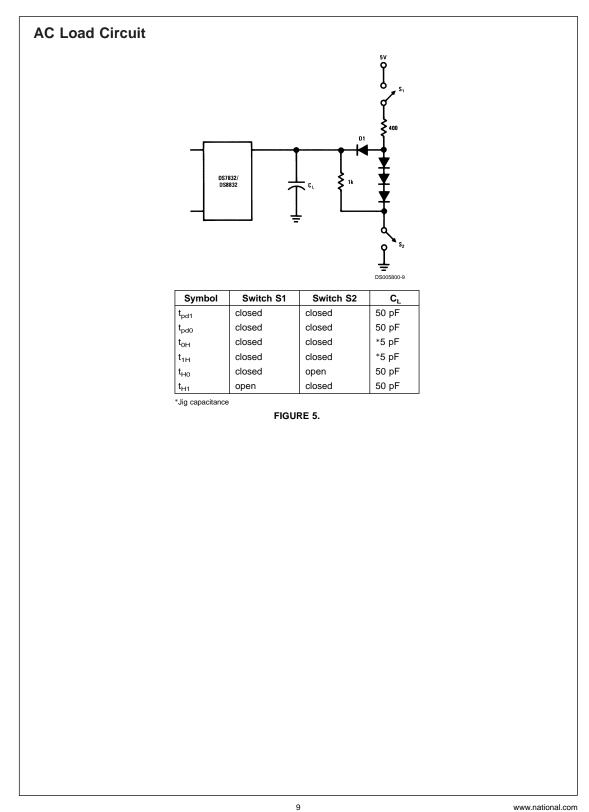
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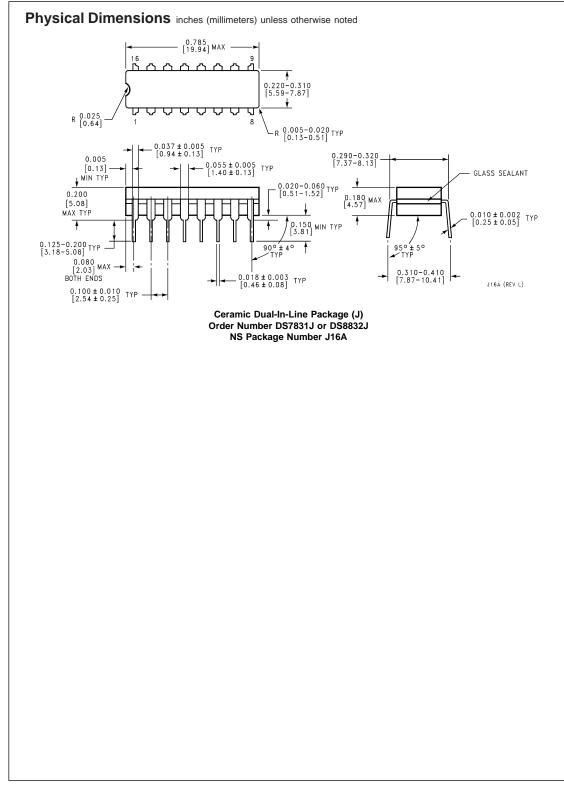


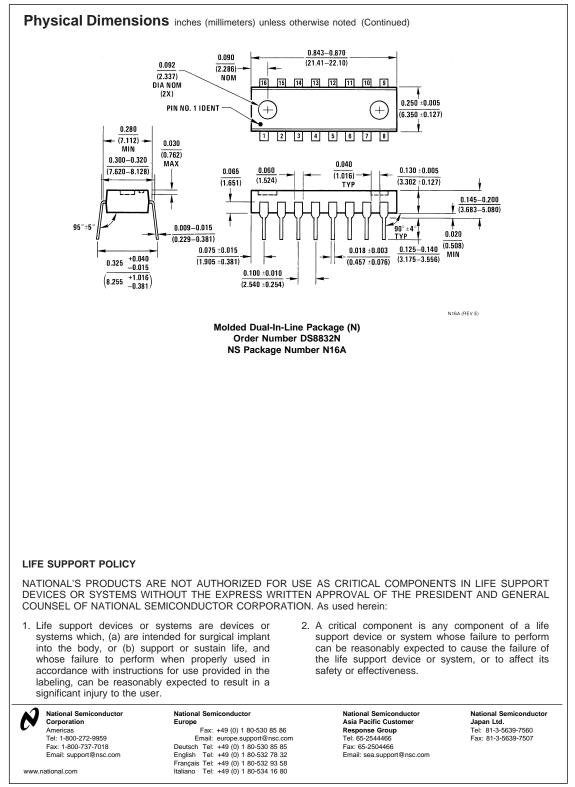












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