

FEATURES

- Temperature measurements require no external components
- Measures temperatures from -55°C to $+125^{\circ}\text{C}$. Fahrenheit equivalent is -67°F to $+257^{\circ}\text{F}$.
- Thermometer accuracy is $\pm 2.0^{\circ}\text{C}$.
- Thermometer resolution is configurable from nine (default) to 12 bits (0.5°C to 0.0625°C resolution)
- 9–bit readout mode features a max conversion time of 150 ms.
- Thermostatic settings are user definable.
- Data is read from/written via a 2–wire serial interface. (open drain I/O lines). 3–bit addressability
- Wide power supply range ($2.7\text{V} - 5.5\text{V}$).
- Applications include personal computers, cellular telephones, office equipment, or any thermally sensitive system.
- Pin/software compatible to LM75CIM–x Thermal Watchdog in 9–bit (default) mode.
- 8–pin 150 mil SOIC package.

DESCRIPTION

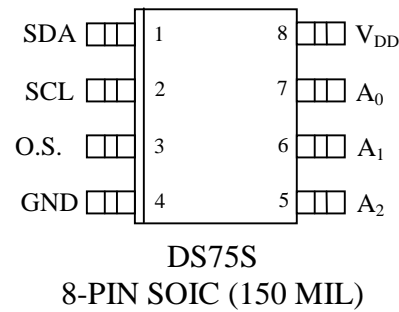
The DS75 2–wire thermal watchdog provides 9–bit temperature readings which indicate the temperature of the device. Thermostat settings and temperature readings are all communicated to/from the DS75 over a simple 2–wire serial interface. No additional components are required; the device is truly a “temperature–to–digital” converter.

The DS75 has three address bits that allow a user to multidrop up to eight sensors along the 2–wire bus, greatly simplifying the bussing of distributed temperature sensing networks.

The open–drain thermal alarm output, O.S., becomes active when the temperature of the device exceeds a user–defined temperature T_{OS} . The number of consecutive faults required to set O.S. active is configurable by the user. The device can also be configured in the interrupt or comparator mode, to customize the method which clears the fault condition.

For applications that require greater temperature resolution, the user can adjust the readout resolution from 9 to 12 bits. This is particularly useful in applications where thermal runaway conditions must be detected quickly.

PIN ASSIGNMENT



PIN DESCRIPTION

SDA	–	2–Wire Serial Data Input/Output
SCL	–	2–Wire Serial Clock
GND	–	Ground
O.S.	–	Thermostat Output Signal
A0	–	Chip Address Input
A1	–	Chip Address Input
A2	–	Chip Address Input
V_{DD}	–	Power Supply Voltage

Applications for the DS75 include personal computers/servers, cellular telephones, office equipment, or any microprocessor–based thermally–sensitive system.

DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	SDA	Data input/output pin for 2–wire serial communication port.
2	SCL	Clock input/output pin for 2–wire serial communication port.
3	O.S.	Thermostat output Becomes active when temperature exceeds T_{OS} . Device configuration defines means to clear over–temperature state.
4	GND	Ground pin.
5	A_2	Address input pin.
6	A_1	Address input pin.
7	A_0	Address input pin.
8	V_{DD}	Supply Voltage 2.7V – 5.5V input power pin.

OVERVIEW

A block diagram of the DS75 is shown in Figure 1. The DS75 consists of five major components:

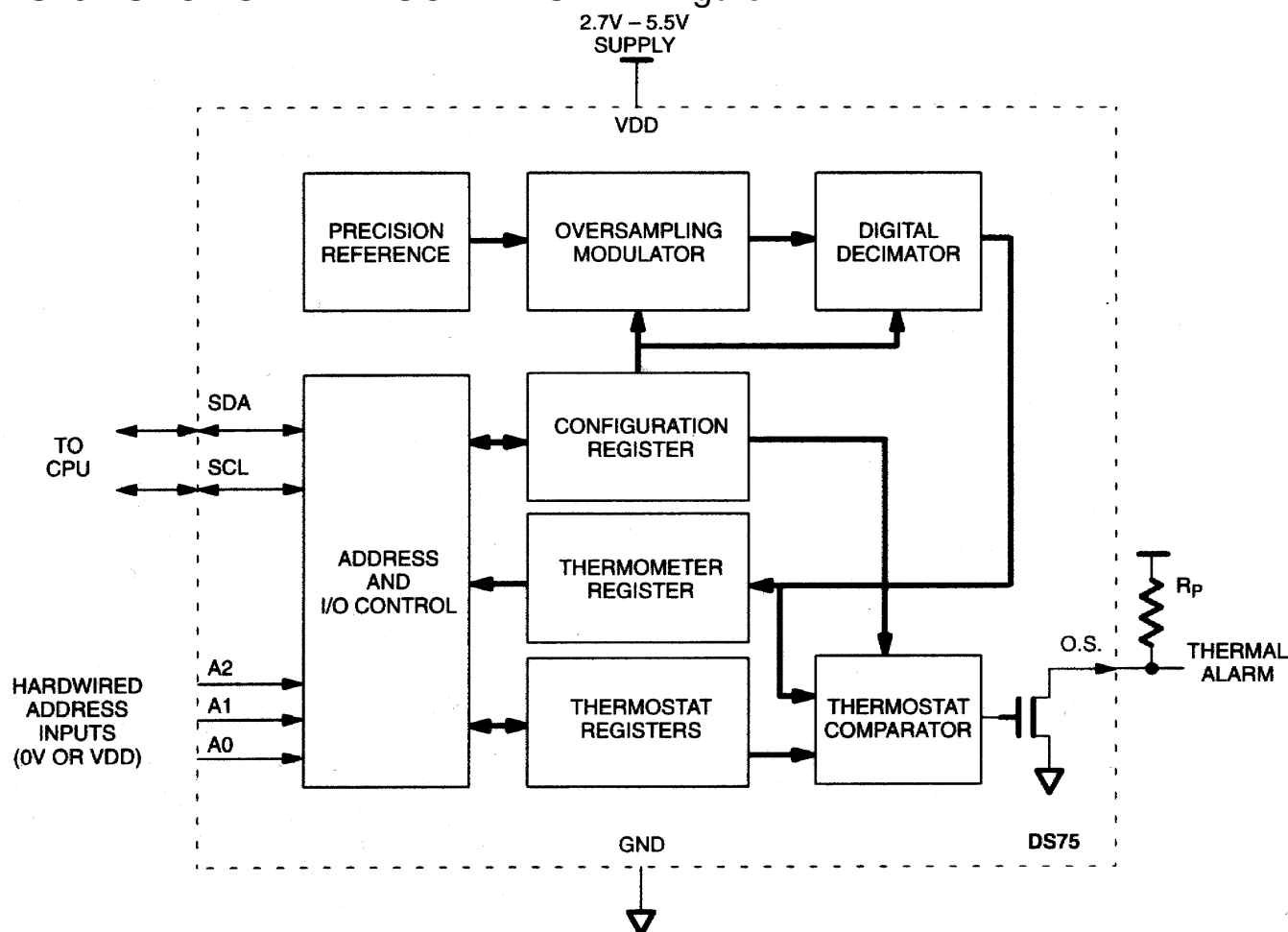
1. Precision temperature sensor
2. Analog–to–digital converter
3. 2–wire interface electronics
4. Data registers
5. Thermostat comparator

The factory–calibrated temperature sensor requires no external components. Upon power–up, the DS75 begins temperature conversions with the default resolution of 9 bits (0.5°C resolution). The host can periodically read the value in the temperature register, which contains the last completed conversion. As conversions are performed in the background, reading the temperature register does not affect the conversion in progress.

In power–sensitive applications, the user can put the DS75 into a shutdown mode, under which the sensor will complete and store the conversion in progress and revert to a low–power standby state. In applications where small incremental temperature changes are critical, the user can change the conversion resolution from 9–bits to 10, 11, or 12. Each additional bit of resolution approximately doubles the conversion time. This is accomplished by programming the configuration register. The configuration register defines the conversion state, thermometer resolution/conversion time, active state of the thermostat output, number of consecutive faults to trigger an alarm condition, and the method to terminate an alarm condition.

The user can also program over–temperature (T_{OS}) and under–temperature (T_{HYST}) setpoints for thermostatic operation. The power–up state of T_{OS} is 80°C and that for T_{HYST} is 75°C. The result of each temperature conversion is compared with the T_{OS} and T_{HYST} setpoints. The DS75 offers two modes for temperature control, the comparator mode and the interrupt mode. This allows the user the flexibility to customize the condition that would generate and clear a fault condition. Regardless of the mode chosen, the O.S. output will become active only after the measured temperature exceeds the respective trippoint a consecutive number of times; the number of consecutive conversions beyond the limit to generate an O.S. is programmable. The power–up state of the DS75 is in the comparator mode with a single fault generating an active O.S. Digital data is written to/read from the DS75 via a 2–wire interface, and all communication is MSb first. Multipoint sensing is possible with the DS75 by uniquely setting the 3–bit address of up to 8 parts on the 2–wire bus.

DS75 FUNCTIONAL BLOCK DIAGRAM Figure 1



OPERATION—Measuring Temperature

The core of DS75 functionality is its direct-to-digital temperature sensor. The DS75 measures temperature through the use of an on-chip temperature measurement technique with an operating range from -55°C to $+125^{\circ}\text{C}$. Temperature conversions are initiated upon power-up, and the most recent result is stored in the thermometer register. Conversions are performed continuously unless the user intervenes by altering the configuration register to put the DS75 into a shutdown mode. Regardless of the mode used, the digital temperature can be retrieved from the temperature register by setting the pointer to that location (00h, power-up default). The DS75 power-up default has the sensor automatically performing 9-bit conversions continuously. Details on how to change the settings after power up are contained in the “OPERATION—Programming” section.

The resolution of the temperature conversion is configurable (9, 10, 11, or 12 bits), with 9-bit readings the default state. This equates to a temperature resolution of 0.5°C , 0.25°C , 0.125°C , or 0.0625°C . Following each conversion, thermal data is stored in the thermometer register in two's complement format; the information can be retrieved over the 2-wire interface with the device pointer set to the temperature register. Table 2 describes the exact relationship of output data to measured temperature. The table assumes the DS75 is configured for 12-bit resolution; if the device is configured in a lower resolution mode, those bits will contain zeros. The data is transmitted serially over the 2-wire serial interface, MSb first. The MSb of the temperature register contains the “sign” (S) bit, denoting whether the temperature is positive or negative. For Fahrenheit usage, a lookup table or conversion routine must be used.

Temperature/Data Relationships Table 2

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	MSB
(UNIT = °C)								
MSb	2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	LSB

TEMPERATURE/DATA RELATIONSHIPS

Table 2 cont'd

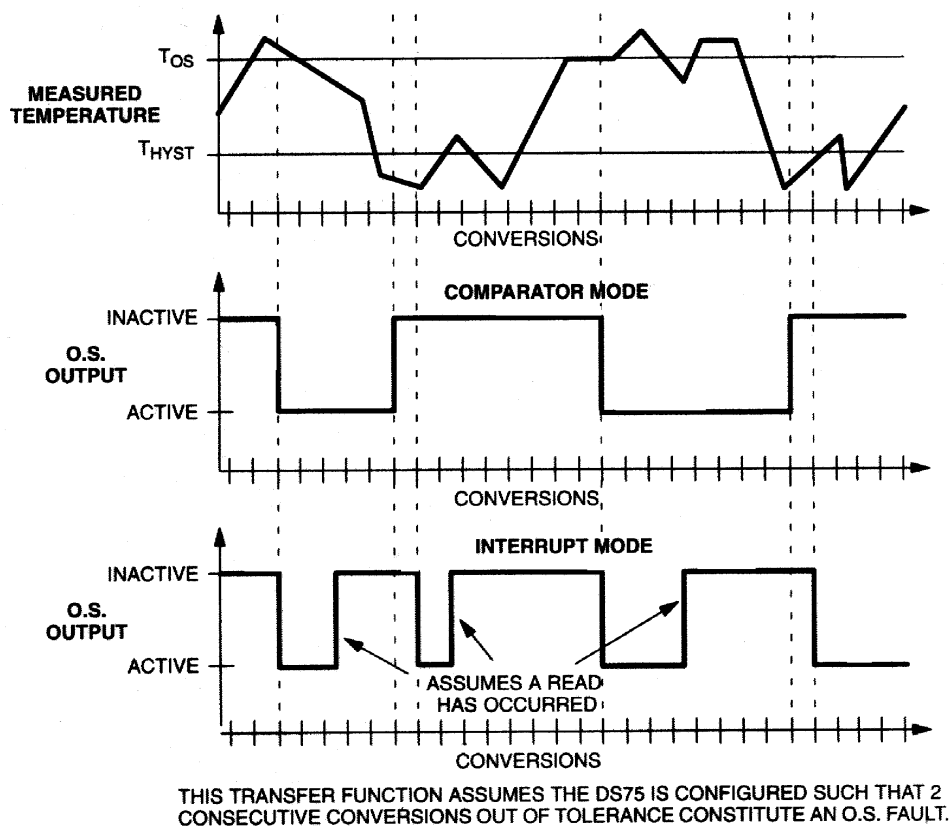
TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	0111 1101 0000 0000	7D00h
+25.0625°C	0001 1001 0001 0000	1910h
+10.125°C	0000 1010 0010 0000	0A20h
+0.5°C	0000 0000 1000 0000	0080h
+0°C	0000 0000 0000 0000	0000h
-0.5°C	1111 1111 1000 0000	FF80h
-10.125°C	1111 0101 1110 0000	E5E0h
-25.0625°C	1110 0110 1111 0000	E6F0h
-55°C	1100 1001 0000 0000	C900h

OPERATION—Thermostat Control

In its comparator operating mode, the DS75 functions as a thermostat with programmable hysteresis, as shown in Figure 2. When the DS75's temperature meets or exceeds the value stored in the high temperature trip register (T_{OS}) a consecutive number of times defined by the configuration register, the output becomes active, and will stay active until the temperature falls below the temperature stored in the low temperature trigger register (T_{HYST}) the first time. In this way, any amount of hysteresis may be obtained. The DS75 powers up in the comparator mode with $T_{OS} = 80^\circ\text{C}$ and $T_{HYST} = 75^\circ\text{C}$, and the device can be used as a standalone thermostat (no 2-wire interface required) with those setpoints.

In the interrupt mode, the O.S. output will first become active following the programmed number of consecutive conversions above T_{OS} . The fault can only be cleared by either setting the DS75 in a shutdown mode or by reading any register (temperature, configuration, T_{OS} , or T_{HYST}) on the device. Following a clear, a subsequent fault can only occur if consecutive conversions fall below T_{HYST} . This interrupt/clear process is thus cyclical (T_{OS} , clear, T_{HYST} , clear, T_{OS} , clear, T_{HYST} , clear, . . .). Only the first of multiple consecutive T_{OS} violations will activate O.S., even if each fault is separated by a clearing function. The same situation applies to multiple consecutive T_{HYST} events.

O.S. OUTPUT TRANSFER FUNCTION Figure 2



Regardless of the mode chosen, the O.S. output is open-drain and the active state is set in the configuration register. The power-up default is active low. Refer to the “OPERATION–Programming” section for instructions in adjusting the thermostat setpoints, thermostat mode, and O.S. active state.

OPERATION–Programming

There are three areas of interest in programming the DS75: Configuration register, T_{OS} register, and the T_{HYST} register. All programming is done via the 2-wire interface by setting the pointer to the appropriate location. Table 3 illustrates the pointer settings for the four registers of the DS75.

Pointer Register Structure Table 3

POINTER	ACTIVE REGISTER
00h	Temperature (default)
01h	Configuration
02h	T_{HYST}
03h	T_{OS}

The DS75 will power up with the temperature register selected. If the host wishes to change the data pointer, it simply addresses the DS75 in the write mode (R/W=0), receives an acknowledge, and writes the 8 bits that correspond to the new desired location. The last pointer location is always maintained so that consecutive reads from the same register do not require the host to always provide a pointer address. The only exception is at power-up, in which case the pointer will always be set to 00h, the temperature register. The pointer address must always precede data in writing to a register, regardless of which address is currently selected. Please refer to the “2-Wire Serial Data Bus” section for details of the 2-wire bus protocol.

Configuration Register Programming

The configuration register is accessed if the DS75 pointer is currently set to the 01h location. Writing to or reading from the register is determined by the R/W bit of the 2-wire control byte (See “2-wire Serial Data Bus” section). Data is read from or written to the configuration register MSb first. The format of the register is illustrated below in Figure 3. The effect each bit has on DS75 functionality is described below along with the power-up state of the bit. The user has read/write access to all bits in the configuration register. The entire register is volatile, and thus it will power-up in the default state.

CONFIGURATION/STATUS REGISTER

Figure 3

0	R1	R0	F1	F0	POL	TM	SD
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MSb

LSb

SD = Shutdown bit. If SD is “0”, the DS75 will continuously perform temperature conversions and store the last completed result in the thermometer register. If SD is changed to “1”, the conversion in progress will be completed and stored; then the device will revert to a low-power standby mode. The O.S. output will be cleared if the device is in the interrupt mode and remain unchanged in the comparator mode. The 2-wire port remains active. The power-up default state is “0” (continuous conversion mode).

TM = Thermostat mode. If TM=“0”, the DS75 is in the comparator mode. TM=“1” sets the device to the interrupt mode. See “OPERATION–Thermostat Control” section for a description of the difference between the two modes. The power-up default state of the TM bit is “0” (comparator mode).

POL = O.S. Polarity Bit. If POL =“1”, the active state of the O.S. output will be high. A “0” stored in this location sets the thermostat output to an active low state. The user has read/write access to the POL bit, and the power-up default state is “0” (active low).

F0, F1 = O.S. Fault Tolerance bits. The fault tolerance defines the number of consecutive conversions returning a temperature beyond limits is required to set the O.S. output in an active state. This may be necessary to add margin in noisy environments. Table 4 below defines the four settings. The DS75 will power up with F0=F1=“0”, such that a single occurrence will trigger a fault.

Fault Tolerance Configuration Table 4

F1	F0	Consecutive conversions beyond limits to generate fault
0	0	1
0	1	2
1	0	4
1	1	6

R0, R1 = Thermometer resolution bits. Table 5 below defines the resolution of the digital thermometer, based on the settings of these two bits. There is a direct trade-off between resolution and conversion time, as depicted in the AC Electrical Characteristics. The default state is R0=0 and R1=0 (9-bit conversions).

“0” = Reserved Location. The master can write to this bit, but it will always read out as a “0”. The power-on default state is “0”.

Thermometer Resolution Configuration

Table 5

R1	R0	Thermometer Resolution	Max Conversion Time
0	0	9-bit	0.15s
0	1	10-bit	0.3s
1	0	11-bit	0.6s
1	1	12-bit	1.2s

Thermostat Setpoints Programming

The thermostat registers (T_{OS} and T_{HYST}) can be programmed or read via the 2-wire interface. T_{OS} is accessed by setting the DS75 data pointer to the 03h location, and that for the T_{HYST} setting is 02h.

The format of the T_{OS} and T_{HYST} registers is identical to that of the Thermometer register; that is, 12-bit 2's complement representation of the temperature in °C. The user can program the number of bits (9, 10, 11, or 12) for each T_{OS} and T_{HYST} that correspond to the thermometer resolution mode chosen. If the 9-bit mode is chosen, for example, the 3 least significant bits of T_{OS} and T_{HYST} will be ignored by the thermostat comparator. The format for both T_{OS} and T_{HYST} is shown below in Table 6. The power-up default of T_{OS} is 80°C and that for T_{HYST} is 75°C.

Thermostat Setpoint (TOS/THYST) Format

Table 6

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0	MSB
(UNIT = °C)								
2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	0	LSB

TEMPERATURE/DATA RELATIONSHIPS

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+80°C	0101 0000 0000 0000	5000h
+75°C	0100 1011 0000 0000	4B00h
+10.125°C	0000 1010 0010 0000	0A20h
+0.5°C	00000000 1000 0000	0080h
+0°C	00000000 0000 0000	0000h
-0.5°C	1111 1111 1000 0000	FF80h
-10.125°C	1111 0101 1110 0000	E5E0h
-25.0625°C	1110 0110 1111 0000	E6F0h
-55°C	1100 1001 0000 0000	C900h

If the user does not wish to take advantage of the thermostat capabilities of the DS75, the 24 bits can be used for general storage of system data that need not be maintained following a power loss. The O.S. output should be left floating if this is done.

2–WIRE SERIAL DATA BUS

The DS75 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master”. The devices that are controlled by the master are “slaves”. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS75 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O lines SDA and SCL.

The following bus protocol has been defined (See Figure 4):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The DS75 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2-WIRE SERIAL BUS Figure 4

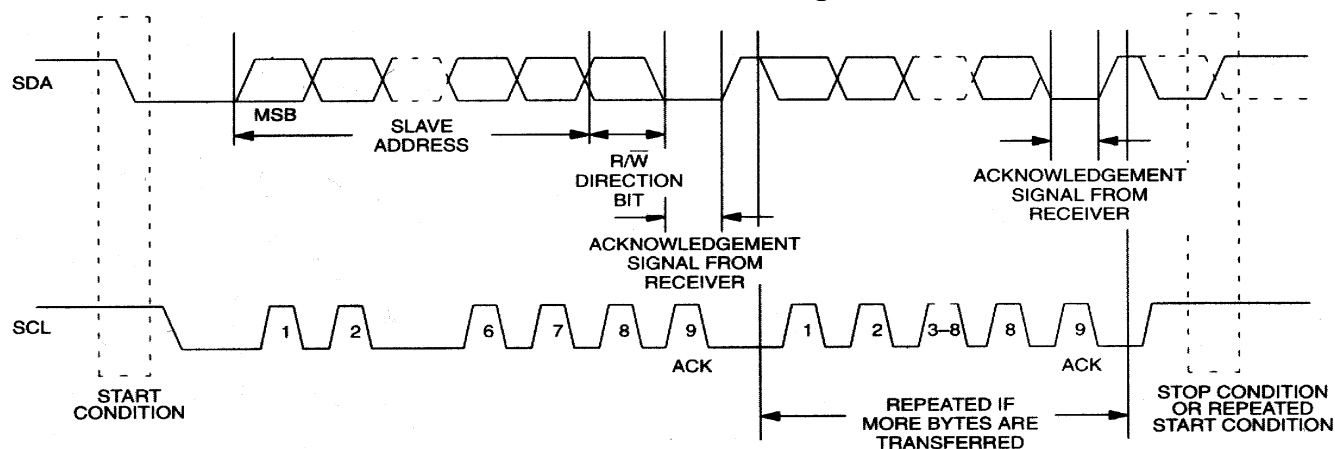


Figure 5 details how data transfer is accomplished on the two-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

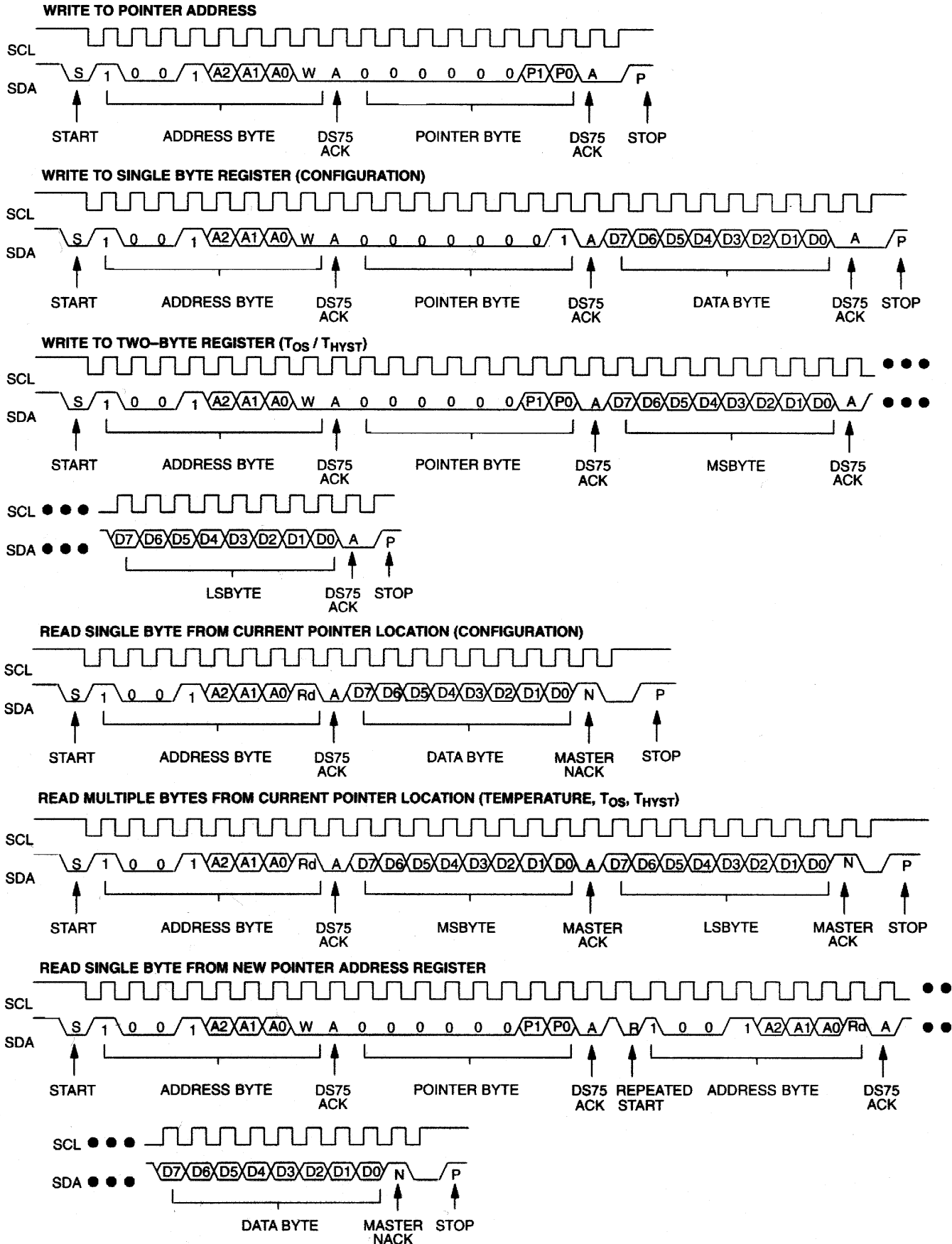
The DS75 may operate in the following two modes:

1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS75 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS75, this is set as 1001 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. The set bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/W) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS75 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1001 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

2-WIRE SERIAL COMMUNICATION WITH DS75 Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD, Relative to Ground	-0.3V to +7.0V
Voltage on any other pin, Relative to Ground	-0.3V to ($V_{DD} + 0.3V$)
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

The Dallas Semiconductor DS75 is built to the highest quality standards and manufactured for long term reliability. All Dallas Semiconductor devices are made using the same quality materials and manufacturing methods. However, the DS75 is not exposed to environmental stresses, such as burn-in, that some industrial applications require. For specific reliability information on this product, please contact the factory in Dallas at (972) 371-4448.

RECOMMENDED DC OPERATING CONDITIONS

(-55°C to +125°C; $2.7V \leq V_{DD} \leq 5.5V$)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}		2.7		5.5	V	

DC ELECTRICAL CHARACTERISTICS (-55°C to +125°C; $2.7V \leq V_{DD} \leq 5.5V$)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Logic High	V_{IH}		$0.7V_{DD}$		$V_{DD}+0.5$	V	1
Input Logic Low	V_{IL}		-0.5		$0.3V_{DD}$	V	1
SDA Output Logic Low Voltage	V_{OL1}	3 mA sink current	0		0.4	V	1
	V_{OL2}	6 mA sink current	0		0.6		
O.S. Saturation Voltage	V_{OL}	4 mA sink current			0.8	V	1, 9
Input current each I/O pin		$0.4 < V_{IO} < 0.9 V_{DD}$	-10		+10	μA	2
I/O Capacitance	$C_{I/O}$				10	pF	
Standby Current	I_{DD1}				1	μA	3, 4
Active Current	I_{DD}	Active Temp. Conversions			1000	μA	3, 4
		Communication only			100		

ELECTRICAL CHARACTERISTICS:**DIGITAL THERMOMETER**(-55°C to +125°C; 2.7V ≤ V_{DD} ≤ 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T _{ERR}	-25 to +100 -55 to +125			± 2.0 ± 3.0	°C	9
Resolution			9		12	bits	
Conversion Time	t _{CONVT}	9-bit conversions		125	150	ms	
		10-bit conversions		250	300		
		11-bit conversions		500	600		
		12-bit conversions		1000	1200		

AC ELECTRICAL CHARACTERISTICS(-55°C to +125°C; 2.7V ≤ V_{DD} ≤ 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL clock frequency	f _{SCL}	Fast Mode Standard Mode			400 100	KHz	
Bus free time between a STOP and START condition	t _{BUF}	Fast Mode Standard Mode	1.3 4.7			μs	
Hold time (repeated) START condition	t _{HD:STA}	Fast Mode Standard Mode	0.6 4.0			μs	5
LOW period of SCL	t _{LOW}	Fast Mode Standard Mode	1.3 4.7			μs	
HIGH period of SCL	t _{HIGH}	Fast Mode Standard Mode	0.6 4.0			μs	
Set-up time for a repeated START	t _{SU:STA}	Fast Mode Standard Mode	0.6 4.7			μs	
Data hold time	t _{HD:DAT}	Fast Mode Standard Mode	0 0		0.9	μs	6
Data set-up time	t _{SU:DAT}	Fast Mode Standard Mode	100 250			ns	7
Rise time of both SDA and SCL signals	t _R	Fast Mode Standard Mode	20 + 0.1C _B		300 1000	ns	8
Fall time of both SDA and SCL signals	t _F	Fast Mode Standard Mode	20 + 0.1C _B		300	ns	8
Set-up time for a STOP	t _{SU:STO}	Fast Mode Standard Mode	0.6 4.0			μs	
Capacitive load for each bus line	C _b				400	pF	8
Input Capacitance	C _I			5		pF	

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{DD} specified with O.S. pin open.
4. I_{DD} specified with V_{DD} at 5.0V and SDA, SCL = 5.0V, 0°C to 70°C.
5. After this period, the first clock pulse is generated.
6. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
7. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} \leq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250$ ns before the SCL line is released.
8. C_b – total capacitance of one bus line in pF.
9. Internal heating caused by O.S. loading will cause the DS75 to read approximately 0.5°C higher if O.S. is sinking the max rated current.

TIMING DIAGRAMS Figure 6