



Chrontel CH7322B CEC

Features

- Complies with Consumer Electronic Control (CEC) version 1.3a
- Less than 10mA in full operation conditions
- Fully programmable through a two-wire serial port
- Programmable power management
- Auto Mode Technology † Supports mandatory CEC functions such as One Touch Play, Power Status etc. without software programming
- Capable of supporting full CEC features by accessing internal registers.
- Report CEC events through an interrupt and registers
- Flexible crystal frequency input between 4 and 50 MHz or external CMOS clock ranging from 1 to 100Mhz
- DDC master to obtain Physical Address
- Serial Port voltage supported from 1.8V to 5V
- Single 3.3V voltage supply
- Adjustable interrupt voltage level from 1.8V to 3.3V
- HBM up to 8KV ESD protection
- Offered in a 16-pin, lead-free SSOP package

Applications

- DVD Players
- DVD Recorders
- Digital Video Cameras
- Personal Computers
- A/V Receivers
- Digital Set-top Boxes

General Description

Chrontel's CH7322B is a low cost, low-power semiconductor device designed for HDMI systems to easily enable Consumer Electronic Control (CEC) features, which allow consumers to manage all of their HDMI CEC peripherals with just one remote control. Through innovative design, the CH7322B can help our customers achieve their HDMI-CEC system requirement by drastically reducing complicated and time-consuming microcontroller programming effort.

To minimize CEC development complexity, the CH7322B incorporates a robust and powerful mechanism for handling CEC Message Opcode Commands. The device's advanced Auto Mode Technology† simply provides HDMI-CEC playback systems with the ability to accomplish three mandatory CEC functions – One Touch Play, Suspend and Resume without programming any of CH7322B registers. For example, when a HDMI-CEC DVD player is in standby mode and if the CEC "Set Stream Path" Message Opcode is received, the CH7322B can generate an interrupt signal to trigger the host controller for system normal operation.

More sophisticated CEC features like Deck Control, Tuner control, Volume adjustment and Recording Functions for AV devices can also be accomplished through programming CH7322B internal registers. Once a CEC message is received, verified and interpreted, the CH7322B will store the requested CEC function into register buffers and send an interrupt signal to notify the host controller. The system firmware can then take an action based on the content of the register through the host controller serial port access.

The CH7322B has a master DDC interface and when the hot plug signal is high, the CH7322B will automatically obtain its Physical Address from a HDMI receiver's EDID and save it in the designated register for future usage.

The CH7322B accepts a wide range of input clock frequencies that are generated from either a crystal or an external clock source for CEC command timing. This low-cost, power-saving and space-saving device is available in a 16 pin lead-free SSOP package.

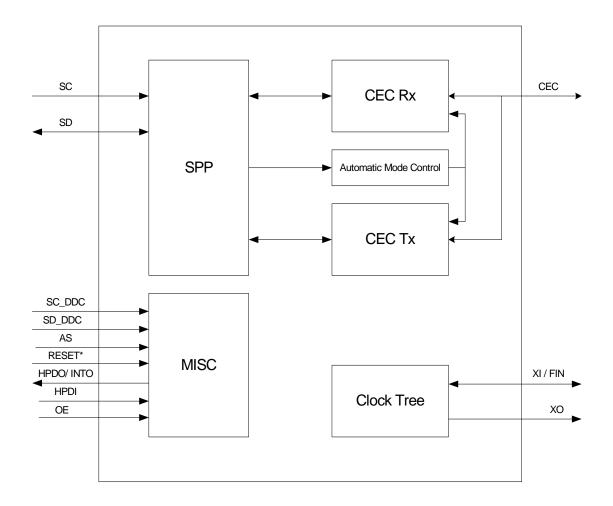


Figure 1: Functional Block Diagram

1.0 Pin-Out

1.1 Package Diagram

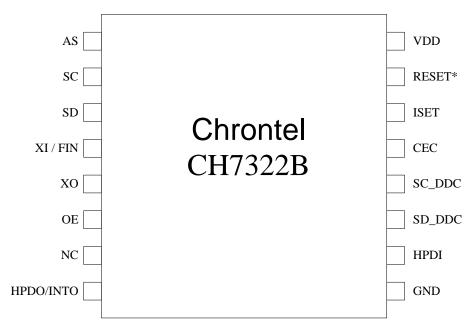


Figure 2: 16-Pin SSOP package

1.2 Pin Description

Table 1: Pin Description

Pin#	Type	Symbol	Description
1	In	AS	Address Select (Internal pull-up)
			This pin determines the serial port address of the device (1,1,1,0,1,AS*,
			AS).
2	In	SC	Serial Port Clock Input
			This pin functions as the clock input of the serial port. This requires an
			external 2.2k ohm pull-up resistor. The voltage for logic 1 can be from
	T (0	an	1.8V to 5V.
3	In/Out	SD	Serial Port Data Input / Output
			This pin functions as the bi-directional data pin of the serial port. This
			requires an external 2.2k ohm pull-up resistor. The voltage for logic 1 can be from 1.8V to 5V.
4	In	XI / FIN	Crystal Input / External Reference Input
4	1111	AI / I'IIV	A parallel resonance crystal can be attached between this pin and XO.
			Crystal range is 4 to 50 MHz. However, an external clock can also drive
			the XI / FIN input and its range can be from 1 to 100 MHz.
5	Out	XO	Crystal Output
			A parallel resonance crystal can be attached between this pin and XI /
			FIN. Crystal range is 4 to 50 MHz. However, if an external CMOS
			clock is attached to XI / FIN, XO should be left open.
6	In	OE	Output Enable (internal pull-up)
			When this pin is low, it will put CH7322B into standby mode.
8	Out	HPDO / INTO	Hot Plug Detect Output / Interrupt Output
			This pin serves as an interrupt for device connection status. However
			this output pin can be programmed for other usage. Supports CMOS logic level from 1.8V to 3.3V
10	In	HPDI	Hot Plug Detect Input (internal pull-down)
10	111		This pin is used to monitor the Hot Plug detection signal. Refer to
			reference schematic for connectivity.
11	In/Out	SD_DDC	Routed Serial Port Data to Port DDC
			This pin attaches to DDC Data bus for obtaining the Physical Address
			from a receiver. Refer to reference schematic for connectivity.
12	In	SC_DDC	Routed Serial Port Clock to Port DDC
			This pin attaches to DDC Clock bus. Refer to reference schematic for
			connectivity.
13	In/Out	CEC	CEC data Input / Output
			This pin will output CEC Message opcodes specified in HDMI
1.4		IGER	Specification 1.3a.
14	In	ISET	Current Set Resistor Input. A 27K-ohm +/- 1% resistor should be connected between this pin and
			GND
15	In	RESET*	Reset* Input (Internal pull-up)
1.5	1111	KESET	When this pin is low, the device is held in the power-on reset condition.
			When this pin is high, reset is controlled through the serial port register.
7	NC	NC	Not connect
16	Power	VDD	Supply Voltage (3.3V)
9	GND	GND	Ground

2.0 Electrical Specifications

2.1 Absolute Maximum Ratings

Symbol	Description	Min	Тур	Max	Units
	VDD power supply relative to GND	-0.5		5	V
	Input voltage of all digital pins	GND - 0.5		VDD + 0.5	V
T _{SC}	Analog output short circuit duration		Indefinite		Sec
TSTOR	Storage temperature	-65		150	°C
TJ	Junction temperature			150	°C
Typs	Vapor phase soldering (1 minute)			TBD	°C

Note:

- 1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5 V can induce destructive latchup.

2.2 Recommended Operating Conditions

Symbol	Description	Min	Тур	Max	Units
VDD	Power supply voltage	3.0	3.3	3.6	V
T _{AMB}	Ambient operating temperature	0		85	°C

Electrical Specifications

(Operating Conditions: $T_{AMB} = 0$ °C-85°C, VDD =3.3V+/- 0.3V, unless otherwise specified)

2.2.1 Supply

Symbol	Description	Min	Тур	Max	Units
IVDD	Total supply current		4	TBD	mA
IPD	Total Power Down Current		0.50		mA

2.2.2 DC Specifications

Symbol Description		Test Condition	Min	Тур	Max	Unit
CEC						
C _{CEC}	CEC pin capacitance			30		pF
I _{leak,CEC}	CEC pin leakage when power removed				1.8	uA
V _{OH,CEC}	CEC output high voltage	Note 1,2,3	2.5	2.7	3.3	V
$V_{OL,CEC}$	CEC output low voltage	Note 1,2,3		0.2	0.6	V
$V_{\text{IH,CEC}}$	CEC input high voltage threshold			1.5	2.0	V

Symbol	Description	Test Condition	Min	Тур	Max	Unit
V _{IL,CEC}	CEC input low voltage threshold		0.8	1.0		V
$V_{\rm IN,hys,CEC}$	CEC input hysteresis			0.5		V
SPP (SD/SC),	DDC (SD_DDC/SC_DDC, apply inp	out specification only)		1		1
$V_{PU,SPP}$	SPP pull up voltage		1.62		5.5	V
$V_{\text{IH,SPP}}$	SPP input high voltage threshold			1.25		V
$V_{IL,SPP}$	SPP input low voltage threshold			1.0		V
$V_{\rm IN,hys,SPP}$	SPP input hysteresis		0.2	0.25		V
$V_{OL,SPP}$	SPP output low voltage	I _{OL} =3.0mA		0.2	0.3	V
R _{PU,SPP}	SPP external pull up resistor		1.1			K ohm
HPD				<u> </u>		
$V_{\text{MAX,HPD}}$	Maximum voltage applicable to pin				5.5	V
$V_{\text{IH},\text{HPD}}$	HPD input high voltage threshold		1.25	1.5	TBD	V
$V_{\text{IL},HPD}$	HPD input low voltage threshold		0.9	1.1	TBD	V
$V_{IN,hys,HPD}$	HPD input hysteresis			0.4		V
R _{PD,HPD}	HPD internal pull down resistor			120		K ohm
HPDO/INTO						
C _L	External load Capacitance				100	pF
AS			•	1		-
V _{IH,AS}	AS input high voltage			0.8*VDD		V
V _{IL,AS}	AS input low voltage			0.25*VDD		V
RESET*				<u> </u>		
$V_{IH,RES}$	RESET* input high voltage threshold		1.2	1.5	TBD	V
$V_{IL,RES}$	RESET* input low voltage threshold		0.9	1.1	TBD	V
$V_{IN,hys,RES}$	RESET* input hysteresis			0.4		V
ISET			•	1		-
R _{ISET}	External ISET resistor			27		K ohm
V _{ISET}	ISET pin voltage output			1.25		V
OE (if applicab	le)					1
V _{IH,OE}	OE input high voltage threshold		1.25	1.5	TBD	V
$V_{IL,OE}$	OE input low voltage threshold		0.9	1.1	TBD	V
$V_{IN,hys,OE}$	OE input hysteresis			0.4		V
I _{L,OE}	OE input low leakage current			-4		uA

Note 1: CEC pin connected to 3.3V via 27Kohm resistor. VDD=3.3V.

Note 3: CEC pin connected to ground via 150Kohm resistor. VDD=3.3V.

Note 2: CEC pin connected to 3.3V via 3Kohm resistor. VDD=3.3V.

2.2.3 AC Specifications

Symbol	Description	Test Condition	Min	Тур	Max	Unit
CEC					•	
$t_{r,CEC}$	CEC output rise time, 10% to 90%	Note 1,2,3		50	250	uS
$t_{f,CEC}$	CEC output fall time, 90% to Note 1,2,3		3	50	uS	
SPP (SD/SC),	DDC (SD_DDC/SC_DDC, apply inp	ut specification only)			•	
t _{glitch}	Maximum pulse width for SPP input glitch suppression		50			nS
XI, XO						
f _{OSC}	Crystal Oscillator Frequency		4		50	MHz
	External Input Clock Frequency		1		100	MHz

Note 1: CEC pin connected to 3.3V via 27Kohm resistor and external 1500pF capacitor to ground. VDD=3.3V.

Note 2: CEC pin connected to 3.3V via 3Kohm resistor and external 7200pF capacitor to ground. VDD=3.3V.

Note 3: CEC pin connected to external 150pF capacitor to ground. VDD=3.3V.

3.0 Package Dimensions

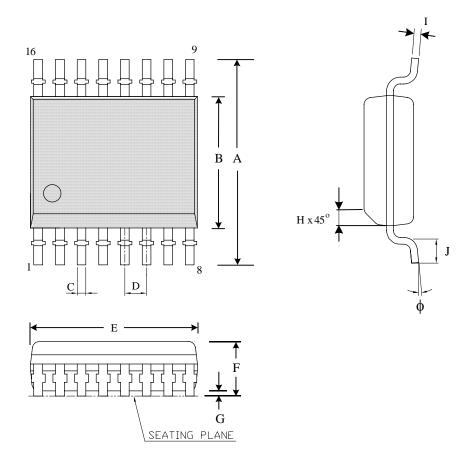


Figure 3: 16-Pin SSOP Package

Table of Dimensions

No. o	f Leads	SYMBOL										
	16	A	В	C	D	E	F	G	Н	I	J	ф
Milli-	MIN	5.80	3.80	0.20	0.635	4.80	1.35	0.10	0.25	0.18	0.40	0 °
meters	MAX	6.20	4.00	0.30	0.033	5.00	1.75	0.25	0.50	0.25	1.27	8°

4.0 Revision History

Table 2: Revision History

Rev. #	Date	Section	Description
1.0	2/18/09	All	Official release.
1.1	2/20/08		Add Ordering Information
1.2	6/29/2009	Features	Add 8KV ESD protection spec.

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ORDERING INFORMATION						
Part Number	Package Type	Number of Pins	Voltage Supply			
7322BMF	BMF Lead Free SSOP		3.3V			
7322BMF-TR	Lead Free SSOP in Tape & Reel	16	3.3V			

Chrontel

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