
CH7318C AC Coupled HDMI Level Shifter

1.0 FEATURES

- Converts low-swing AC coupled differential input to HDMI 1.3 compliant open-drain current steering Rx terminated differential output.
- HDMI TMDS level shifting operation up to 1.65Gb/s per lane (165MHz pixel clock).
- Enable feature to turn off TMDS inputs and outputs and to enter low-power state.
- Transparent operation: no re-timing or configuration required.
- Inter-Pair added skew < 250ps
- Intra-Pair added skew < 10ps
- Switching power only from a single 3.3V supply.
- Integrated 50-ohm termination resistors for AC coupled differential Inputs.
- Pass-gate voltage limiters allow 3.3V termination on GMCH pins, 5V DDC termination on HDMI connector pins.
- Human Body Model ESD protection: 8kV for all output pins and 2kV for all other pins.
- Level shifter for HDMI 1.3 HPD.
- Integrated pull-down resistor on HPD_SINK input guarantees “input low” when no display is plugged in.
- Driver’s current adjustment +10%.
- Inverting buffer for HPD signal
- Configurable pre-emphasis level (0dB, 2.0dB, 4.0 dB, & 6.0dB)
- Offered in a 48-Pin QFN Package.

2.0 GENERAL DESCRIPTION

CH7318C is a high speed HDMI level shifter that converts low-swing AC coupled differential input to HDMI 1.3 compliant open-drain current steering Rx terminated differential output.

The CH7318C features integrated parallel termination resistors (50-ohm), which eliminate the requirement for external termination resistors on the TMDS differential output pins. This device has incorporated a ESD protection for DDC channels as well as TMDS signal lines. In addition, the DDC_EN pin controls bias voltage to enable or disable the DDC passgate level shifter gates. The OE* pin is a two- state output enable control for the differential input and the TMDS signal output. It can activate IN_Dx pins and OUT_Dx pins or switch them into high impedance. A unique pre-emphasis control is also implemented into CH7318C; this feature has four- level adjustment to increase rise and fall times which are degraded during the transmission over a long trace on PCB.

The device operates from a single +3.3V supply, and is characterized the operation temperature range from -10 °C to 50 °C (ambient temperature). The CH7318C is available in a 48-Pin QFN package.

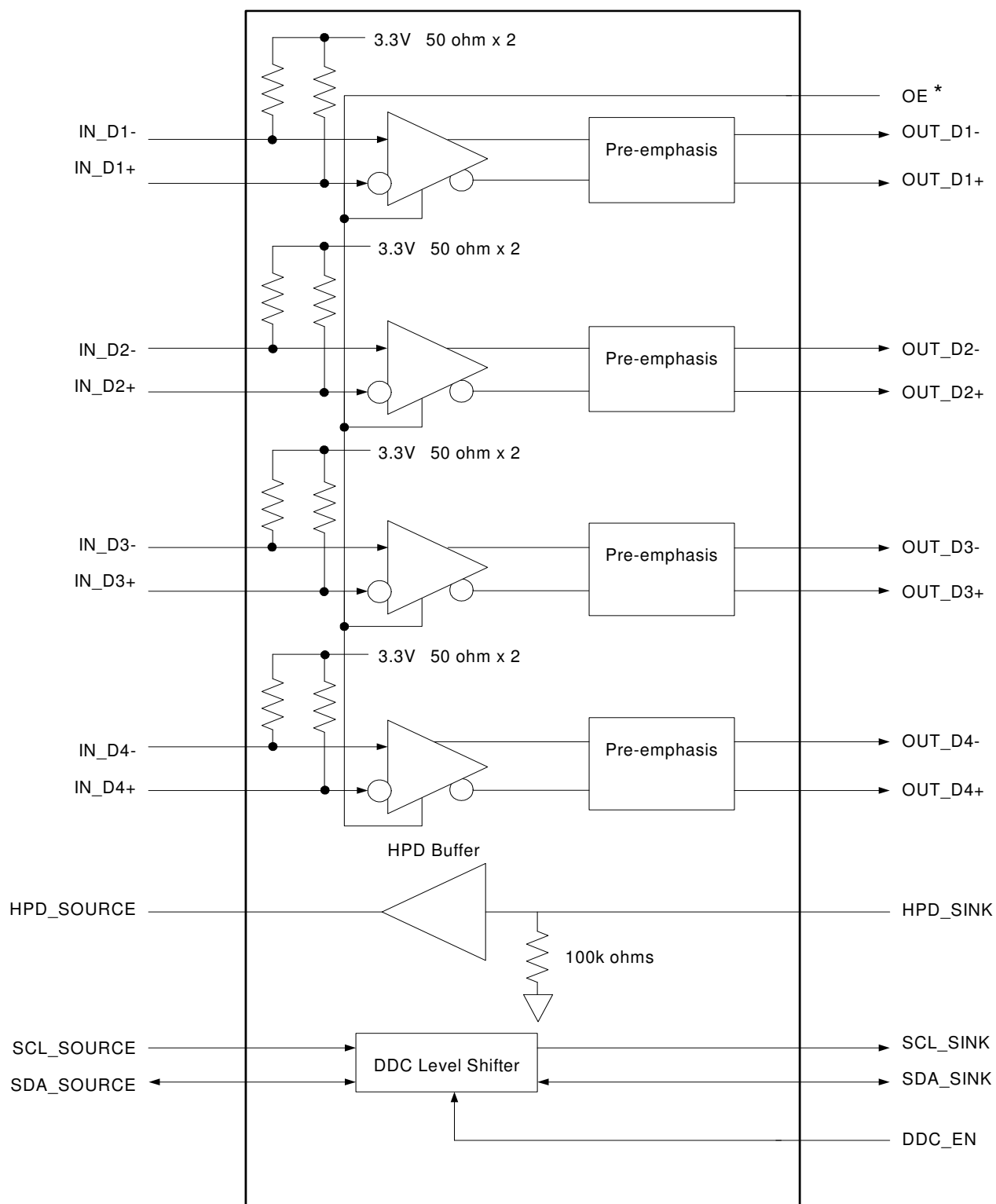


Figure 1: CH7318C Block Diagram

3.0 PIN-OUT

3.1 Package Diagram

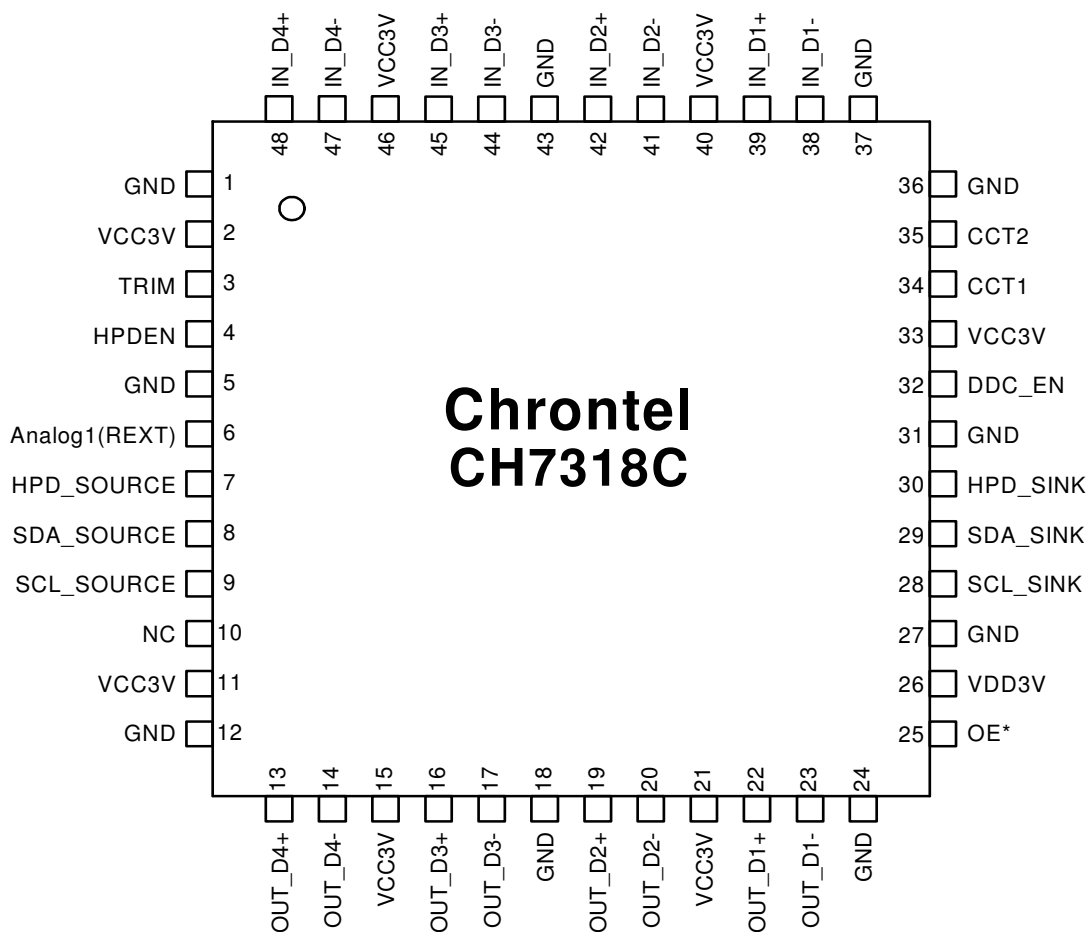


Figure 2: 48-Pin QFN Pin Out

3.2 Pin Descriptions

Table 1: Pin Descriptions

Pin #	Type	Symbol	Description		
1,5,12,18,24,27,31,36,37,43	Ground	GND	Analog ground		
2,11,15,21,26,33,40,46	Power	VCC3V	3.3V DC analog supply		
10		NC	Not connect		
3	In	TRIM	Enable for output current increasing 10%.		
			TRIM	Output current	
			0V	Default	
			3.3V	+10%	
4	In	HPDEN	Enable for different HPD_SOURCE output.		
			HPDEN	HPD_SOURCE	
			0V	Non-inverting output (in terms of HPD_Sink)	
			3.3V	Inverting output (in terms of HPD_Sink) - Open drain	
6		Analog1(REXT)	1.2K resistor tied to GND.		
7	Out	HPD_SOURCE	0V to 3.3V (nominal) output signal. This is level-shifted version of the HPD_SINK		
8	In/Out	SDA_SOURCE	3.3V DDC Data I/O. Pulled up by external termination to 3.3V. Connected to SDA_SINK through voltage-limiting by integrated NMOS passgate.		
9	In	SCL_SOURCE	3.3V DDC Clock I/O. Pulled up by external termination to 3.3V. Connected to SCL_SINK through voltage-limiting by integrated NMOS passgate.		
13,14	Out	OUT_D4+, OUT_D4-	HDMI 1.3 compliant TMDS output. OUT_D4+ makes a differential output signal with OUT_D4-		
16,17	Out	OUT_D3+, OUT_D3-	HDMI 1.3 compliant TMDS output. OUT_D3+ makes a differential output signal with OUT_D3-		
19,20	Out	OUT_D2+, OUT_D2-	HDMI 1.3 compliant TMDS output. OUT_D2+ makes a differential output signal with OUT_D2-		
22,23	Out	OUT_D1+, OUT_D1-	HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1-		
25	In	OE*	Enable for level shifter path. 3.3V tolerant low voltage single-ended input.		
			OE*	IN_D Termination	OUT_D Outputs
			1	High-Z	High-Z
			0	50Ω	Active
28	Out	SCL_SINK	5V DDC Clock I/O. Pulled up by external termination to 5V. Connected to SCL_SOURCE through voltage-limiting by integrated NMOS passgate.		
29	In/Out	SDA_SINK	5V DDC Data I/O. Pulled up by external termination to 5V. Connected to SDA_SOURCE through voltage-limiting by integrated NMOS passgate.		

Pin #	Type	Symbol	Description															
30	In	HPD_SINK	Low frequency, 0V to 5V (nominal) input signal. This signal comes from the HDMI connector. Voltage high indicates “plugged” state; Voltage low indicates “unplugged”. HPD_SINK is pulled down by an integrated 100k ohm resistor.															
32	In	DDC_EN	Enables biases voltage to the DDC passgate level shifter gates. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DDC_EN</th> <th>Passgate</th> </tr> </thead> <tbody> <tr> <td>0V</td> <td>Disabled</td> </tr> <tr> <td>3.3V</td> <td>Enabled</td> </tr> </tbody> </table>	DDC_EN	Passgate	0V	Disabled	3.3V	Enabled									
DDC_EN	Passgate																	
0V	Disabled																	
3.3V	Enabled																	
34	In	CCT1	Pre-emphasis control pin1. CCT1 is pulled down by an integrated 50k ohm resistor. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>CCT1</th> <th>CCT2</th> <th>Pre-emphasis level</th> </tr> </thead> <tbody> <tr> <td>‘0’</td> <td>‘0’</td> <td>0dB(default)</td> </tr> <tr> <td>‘0’</td> <td>‘1’</td> <td>2dB</td> </tr> <tr> <td>‘1’</td> <td>‘0’</td> <td>4dB</td> </tr> <tr> <td>‘1’</td> <td>‘1’</td> <td>6dB</td> </tr> </tbody> </table>	CCT1	CCT2	Pre-emphasis level	‘0’	‘0’	0dB(default)	‘0’	‘1’	2dB	‘1’	‘0’	4dB	‘1’	‘1’	6dB
CCT1	CCT2	Pre-emphasis level																
‘0’	‘0’	0dB(default)																
‘0’	‘1’	2dB																
‘1’	‘0’	4dB																
‘1’	‘1’	6dB																
35	In	CCT2	Pre-emphasis control pin 2. CCT2 is pulled down by an integrated 50k ohm resistor															
38,39	In	IN_D1-, IN_D1+	Low-swing diff input from GMCH PCIe outputs. IN_D1+ makes a differential pair with IN_D1-.															
41,42	In	IN_D2-, IN_D2+	Low-swing diff input from GMCH PCIe outputs. IN_D2+ makes a differential pair with IN_D2-.															
44,45	In	IN_D3-, IN_D3+	Low-swing diff input from GMCH PCIe outputs. IN_D3+ makes a differential pair with IN_D3-.															
47,48	In	IN_D4-, IN_D4+	Low-swing diff input from GMCH PCIe outputs. IN_D4+ makes a differential pair with IN_D4-.															

4.0 FUNCTIONAL DESCRIPTION

4.1 Power Supply

3.3V +/- 10%

4.2 Clocking

This device does not re-time any data. The device contains no state machines. No inputs or outputs of the device are latched or clocked.

4.3 Reset

This device acts as a level shifter, reset is not required.

4.4 OE* Function

When OE* is asserted (low voltage) the IN_D and OUT_D signals are fully functional.

In put termination resistors are enabled and any internal bias circuits are turned on.

When OE* is unasserted (high voltage) the OUT_D outputs are in a high-impedance state. The IN_D input buffers are disabled and IN_D termination is disabled. Internal bias circuits for the differential inputs and outputs are turned off. Power consumption is minimized.

The HPD_SINK input and HPD_SOURCE output are not affected by OE*.

The SCL and SDA passgates are not affected by OE*.

Table 2: OE* Description

OE*	Device State	Comments
Asserted (low voltage)	Differential input buffers and output buffers enabled. Input impedance = 50 ohm.	Normal functioning state for IN_D to OUT_D level shifting function.
Unasserted (high voltage)	Low-power state. Differential input buffers and termination are disabled. Differential input buffers are in a high-impedance state. OUT_D level-shifting outputs are disabled. OUT_D level-shifting outputs are in a high-impedance state. Internal bias currents are turned off.	Intended for lowest power condition when: <ul style="list-style-type: none"> • No display is plugged in or • The level shifted data path is disabled HPD_SINK input and HPD_SOURCE output are not affected by OE*. SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE*.

Table 3: OE* Function

OE*	In_Dx	TMDS_OUTx	Notes
Unasserted (high voltage)	High-Z	High-Z	Device disabled. Low power state. Internal bias currents are disabled.
Asserted (low voltage)	50 ohm Termination	Enabled	Level shifting mode enabled.

4.5 Pre-emphasis Function

The CH7318C has an advanced pre-emphasis control mechanism for reducing jitter and increasing rise/fall times from long or lossy transmission high speed signal. Two pins are used to configure the pre-emphasis level for OUT_Dx outputs:

Table 4: Pre-emphasis Selection Table

CCT1	CCT2	Pre-emphasis Level
'0'	'0'	0dB(default)
'0'	'1'	2dB
'1'	'0'	4dB
'1'	'1'	6dB

5.0 ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Table 5: T_{SC}, T_{AMB}, T_{STOR}, T_J, T_{VPS} Ratings

Symbol	Description	Min	Typ	Max	Units
	All 3.3V power supplies relative to GND	-0.5		5.0	V
T _{SC}	Analog output short circuit duration		Indefinite		Sec
T _{AMB}	Ambient operating temperature	-20		85	°C
T _{STOR}	Storage temperature	-65		150	°C
T _J	Junction temperature			150	°C
T _{VPS}	Vapor phase soldering (5 second)			260	°C
	Vapor phase soldering (11 second)			245	
	Vapor phase soldering (60 second)			225	

Note:

- 1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

5.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VCC3V	3.3V Power Supply	2.97	3.3	3.63	V
ICC	Total current from VCC 3.3V supply	0	60		mA
I _{PD}	Total Power Down Current		10		µA
T _{CASE}	Case temperature range for operation with spec.	-20		85	°C

5.3 Differential Input

Table 7: Differential Input Characteristics for IN_D Signals.

Symbol	Description	Min	Typ	Max	Units	Comments
Tbit	Unit Interval	540			ps	Tbit is determined by the display mode. Nominal bit rate ranges from 250Mb/s to 1.65Gb/s per lane. (1.65Gb/s supported on both TMS and muxed outputs). Nominal Tbit at 1.65Gb/s=606ps. 540ps =606ps-10%.
V _{RX-DIFFp-p}	Differential Input Peak to Peak Voltage	0.175		1.2	V	VRX-DIFFp-p = 2* VRX-D+ - VRX-D- . Applies to IN_D signals.

Symbol	Description	Min	Typ	Max	Units	Comments
T_{RX-EYE}	Minimum Eye Width at IN_D input pair.	0.8			Tbit	The level shifter may add a maximum of 0.02UI jitter
$V_{CM-AC-pp}$	AC Peak Common-Mode Input Voltage			100	mV	$V_{CM-AC-pp} = VRX-D+ + VRX-D- / 2 - VRX-CM-DC$. $VRX-CM-DC = DC(avg) \text{ of } VRX-D++ VRX-D- / 2$ VCM-AC-pp includes all frequencies above 30kHz.
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required IN_D+ as well as IN_D- DC impedance (50 Ω +/- 20% tolerance).
$Z_{RX-HIGH-Z}$	Single-ended input resistance for IN_Dx when inputs are in HIGH-Z state.	100			k Ω	Differential inputs must be in a high impedance state when OE* is HIGH

5.4 TMDS OUTPUTS

The level shifter’s TMDS outputs are required to meet HDMI 1.3 specifications. The HDMI 1.3 Specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Table 8: TMDS Output Characteristics for OUT_D signals

Symbol	Description	Min	Typ	Max	Units	Comments
V_H	Single-ended high level output voltage	AVCC-10mV	AVCC	AVCC+10mV	V	AVCC is the DC termination voltage in the HDMI or DVI Sink. AVCC is nominally 3.3V
V_L	Single-ended low level output voltage	AVcc-600mV	AVcc-500mV	AVcc-400mV	V	The open-drain output pulls down from AVcc
V_{SWING}	Single-ended output swing voltage	450	500	600	mV	
I_{OFF}	Single-ended current in high-Z state			10	μA	Measured with TMDS outputs pulled up to AVCC Max (3.6V) through 50 Ω resistors.
T_R	Rise time	206		0.4Tbit	ps	Max rise/fall time @ 1.65Gb/s = 242ps. 206ps = 242ps – 15%
T_F	Fall time	206		0.4Tbit	ps	Max rise/fall time @ 1.65Gb/s = 242ps. 206ps = 242ps – 15%
$T_{SKEW-INTRA}$	Intra-pair differential skew			10	ps	This differential skew budget is in addition to the skew presented between D+ and D- paired input pins.
$T_{SKEW-INTER}$	Inter-pair differential skew			250	ps	This land-to-lane skew budget is in addition to skew between differential input pairs.
T_{JIT}	Jitter added to TMDS signals			10.8	ps	Jitter budget for TMDS signals as they pass through the level shifter. 12ps = 0.02 Tbit at 1.65Gb/s

5.5 HPD_SINK INPUT; HPD_SOURCE OUTPUT

Table 9: HPD Input and Output Characteristics

Symbol	Description	Min	Typ	Max	Units	Comments
V_{IH-HPD}	Input high level	2	5	5.3	V	Low-speed input changes state on cable plug/unplug.
V_{IL-HPD}	HPD_SINK Input Low Level	0		0.8	V	
I_{IN-HPD}	HPD_SINK Input leakage current			10	μA	Measured with HPD_SINK at V_{IH-HPD} max and V_{IL-HPD} min
$V_{OH-HPDB}$	HPD_SOURCE Output High Level	2.5V		VCC	V	VCC is 3.3v +/- 10%
$V_{OL-HPDB}$	HPD_SOURCE Output Low Level	0		0.2	V	
T_{HPD}	HPD_SINK to HPD_SOURCE propagation delay			200	ns	Time from HPD_SINK changing state to HPD# changing state. Includes HPD_SOURCE rise/fall time.
$T_{RF-HPDB}$	HPD_SOURCE rise/fall time	1		20	ns	Time required to transition from $V_{OH-HPDB}$ to $V_{OL-HPDB}$ or from $V_{OL-HPDB}$ to $V_{OH-HPDB}$

5.6 OE* INPUT

Table 10: OE* Input Characteristics

Symbol	Description	Min	Typ	Max	Units	Comments
V_{IH-EN}	Input high level	2		4	V	
V_{IL-EN}	Input Low Level	0		0.8	V	
I_{IN-EN}	Input leakage current			10	μA	Measured with OE* at V_{IH-EN} max and V_{IL-EN} min

5.7 HPD Input Resistor

Table 11: DDC Termination Resistors

Symbol	Description	Min	Typ	Max	Units	Comments
R_{HPD}	HPD_SINK input pulldown resistor	80k	100k	120k	Ω	Guarantees HPD_SINK is LOW when no display is plugged in.

6.0 PACKAGE DIMENSIONS

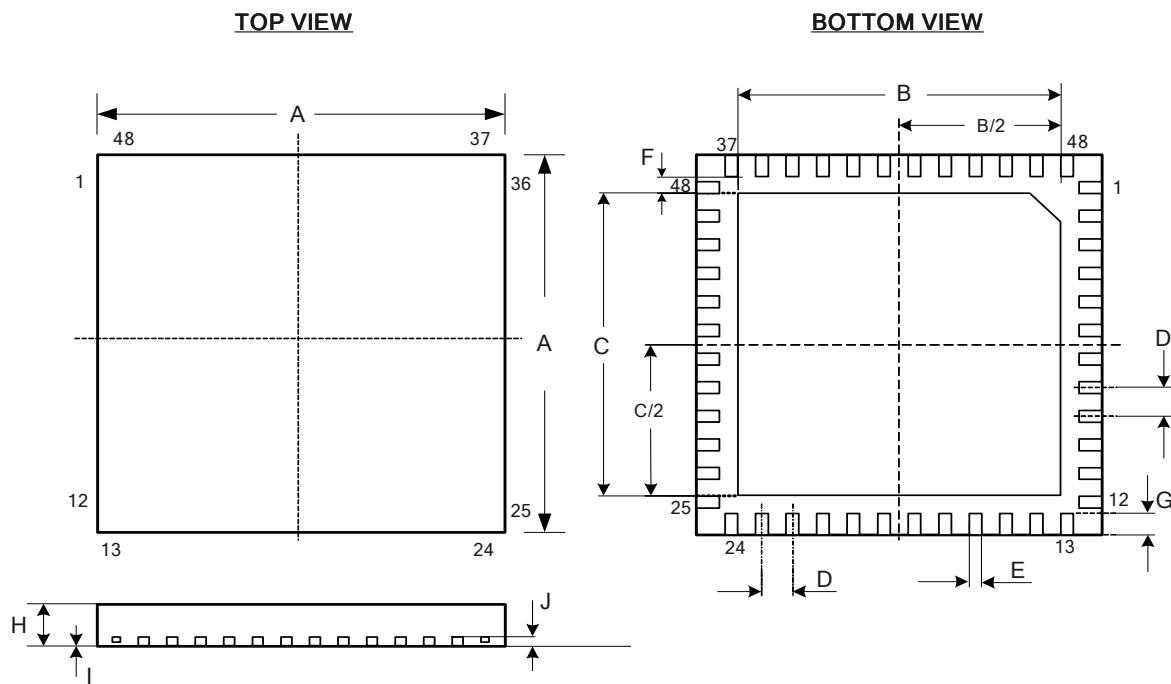


Figure 3: 48 Pin QFN Package

Table of Dimensions

No. of Leads		SYMBOL									
48 (7 X 7 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	7	2.25	2.25	0.5	0.18	0.2	0.30	0.7	0	0.203
	MAX		5.25	5.25		0.30		0.50			

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

7.0 REVISION HISTORY

Table 12: Revisions

Rev. #	Date	Section	Description
1.0	1/23/2008	All	Initial release.
2.0	4/25/2008	All 3.0 3.2	Change to CH7318C. Add Pin 35 CCT2, Pin34 CCT1 and move TRIM to Pin3. Update Table 1. Pin3, Pin34 and Pin35.
2.1	1/23/2009	5.1, 5.1.	Update temperature range.

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ORDERING INFORMATION			
Part Number	Package Type	Number of Pins	Voltage Supply
CH7318C-BF	Lead-free QFN	48	3.3V
CH7318C-BF-TR	Lead-free QFN in Tape & Reel	48	3.3V

Chrontel

Chrontel International Limited

129 Front Street, 5th floor,

Hamilton, Bermuda HM12

www.chrontel.com

E-mail: sales@chrontel.com