CH7305 Single/Dual LVDS Transmitter

Features

- Single / Dual LVDS transmitter
- Supports pixel rate up to 165M pixels/sec
- Supports up to UXGA resolution (1600 x 1200)
- LVDS low jitter PLL
- LVDS 24-bit or 18-bit output
- 2D dither engine for 18-bit output
- Panel protection and power down sequencing
- Programmable power management
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Variable voltage interface to graphics device
- Offered in a 64-pin LQFP package

General Description

The CH7305 is a Display Controller device, which accepts a graphics data stream over one 12-bit wide variable voltage (1.1V to 3.3V) port. The data stream outputs through an LVDS transmitter to an LCD panel. A maximum of 165M pixels per second can be output through a single or dual LVDS link.

The LVDS transmitter supports 24-bit panels; it also includes a programmable dither function for support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specifications. Serialized data output on four or eight differential channels.

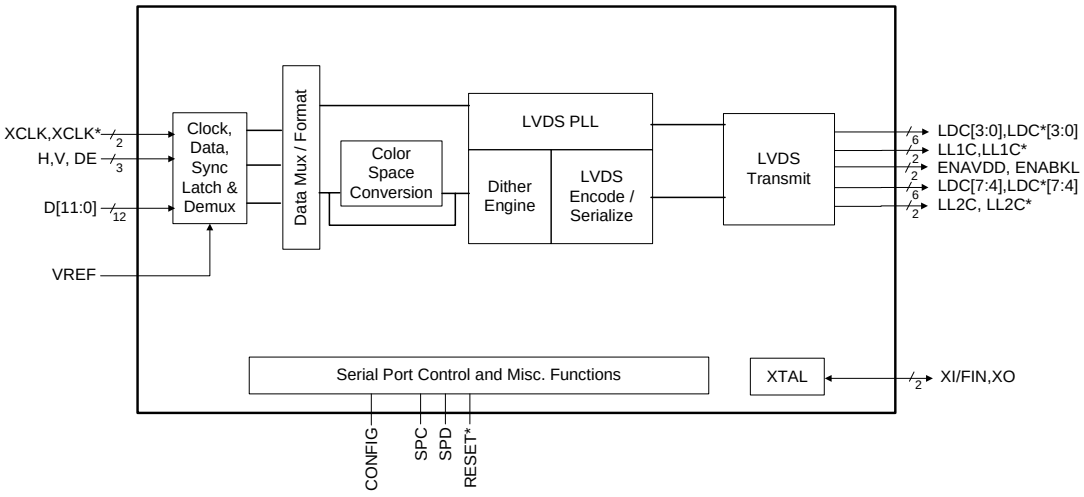

Figure 1: Functional Block Diagram

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1.0 Pin Assignment

Disclaimer: The information contained in this document is preliminary and subject to change without notice. Chrontel Inc. bears no responsibility for any errors in this document. Please contact Chrontel Inc. for design reviews prior to finalize your design.

1.1 Package Diagram

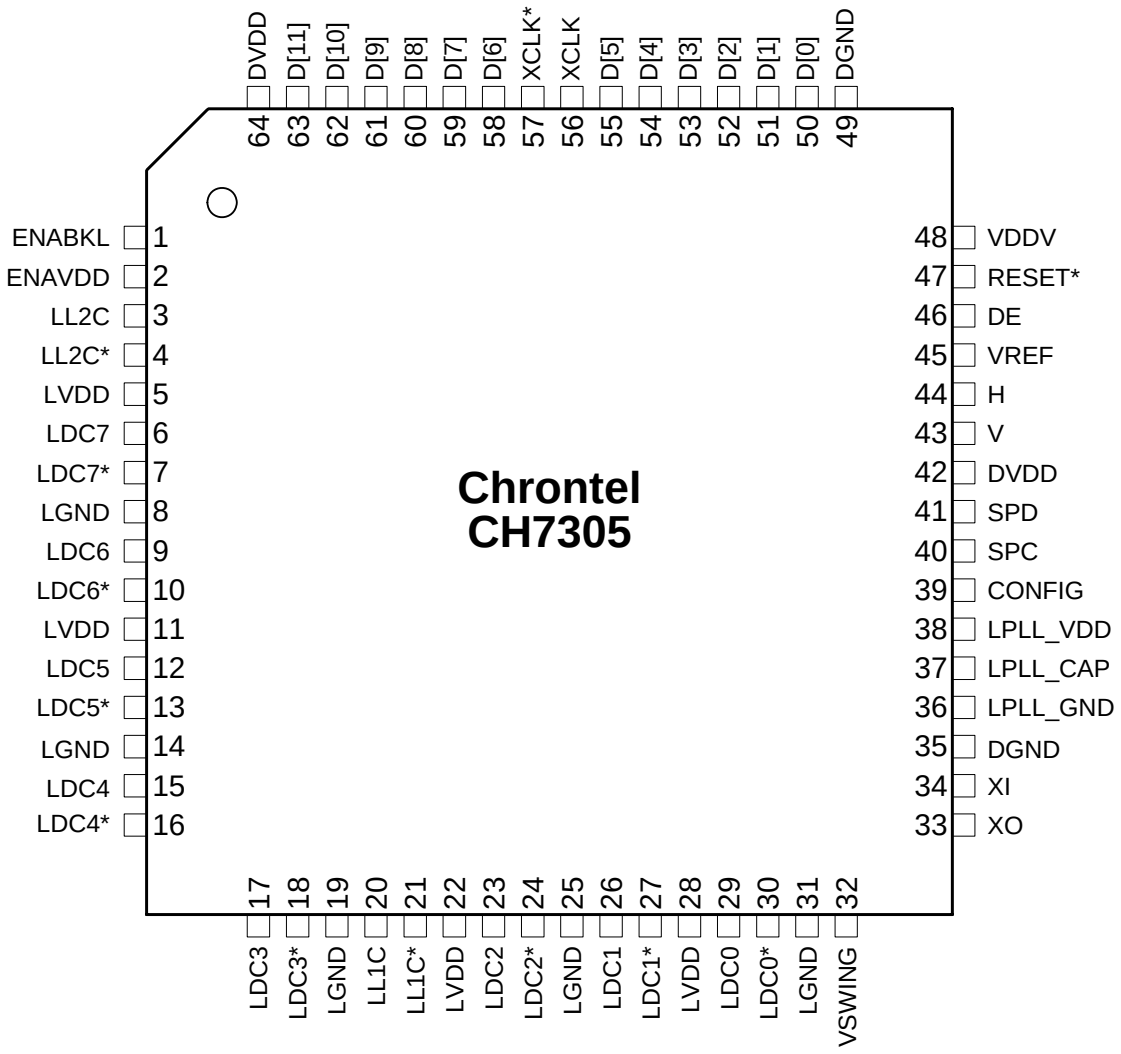

Figure 2: 64 Pin LQFP Package (Top View)

1.2 Pin Description

Table 1: Pin Description

Pin #	# of Pins	Type	Symbol	Description
1	1	Out	ENABLK	**Back Light Enable** Enable Back-Light of LCD Panel. Output is driven from 0 to DVDD.
2	1	Out	ENAVDD	**Panel Power Enable** Enable panel VDD. Output is driven from 0 to DVDD.
3, 4	2	Out	LL2C, LL2C*	**LVDS Differential Clock – channel 2**
6,9,12,15	4	Out	LDC[7:4]	**Positive LVDS differential data[7:4] – channel 2**
7,10,13,16	4	Out	LDC[7:4]*	**Negative LVDS differential data[7:4] – channel 2**
20, 21	2	Out	LL1C, LL1C*	**LVDS Differential Clock – channel 1**
17,23,26,29	4	Out	LDC[3:0]	**Positive LVDS differential data[3:0] – channel 1**
18,24,27,30	4	Out	LDC[3:0]*	**Negative LVDS differential data [3:0] – channel 1**
32	1	In	VSWING	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 31) using short and wide traces.
33	1	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI. However, if an external CMOS clock is attached to XI, XO should be left open.
34	1	In	XI	**Crystal Input / External Reference Input** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI input.
37	1	Analog	LPLL_CAP	**LVDS PLL Capacitor** This pin allows coupling of any signal to the on-chip loop filter capacitor.
39	1	In/Out	CONFIG	**CONFIG / Output** This pin configures the device ID.
40	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and can operate with inputs from 1.1V ~ 3.3V. The serial port address of the CH7305 is 75h. For more details on CH7305 serial port read/write operations, please refer to AN61.
41	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and can operate with inputs from 1.1V ~ 3.3V. Outputs are driven from 0 to VDDV. The serial port address of the CH7305 is 75h. For more details on CH7305 serial port read/write operations, please refer to AN61.
43	1	In	V	**Vertical Sync Input** This pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV. VREF signal is the threshold level.
44	1	In	H	**Horizontal Sync Input** This pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV. VREF is the threshold level for this input.
45	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.

Table 1: Pin Description (continued)

Pin #	# of Pins	Type	Symbol	Description
46	1	In	DE	**Data Enable** This pin accepts a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF is the threshold level.
47	1	In	RESET*	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.
50-55, 58-63	12	In	D[11:0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF is the threshold level.
56, 57	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity can be selected by the MCP control bit **(Register 1Ch)**.
42, 64	2	Power	DVDD	**Digital Supply Voltage** (3.3V)
35, 49	2	Power	DGND	**Digital Ground**
48	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
5,11,22,28	4	Power	LVDD	**LVDS Supply Voltage** (3.3V)
8,14,19,25,31	5	Power	LGND	**LVDS Ground**
38	1	Power	LPLL_VDD	**LVDS PLL Supply Voltage** (3.3V)
36	1	Power	LPLL_GND	**LVDS PLL Ground**

2.0 Functional Description

2.1 Input Data Formats

2.1.1 Overview

Two distinct methods of transferring data to the CH7305 are described. They are:

- Multiplexed data, clock input at 1X the pixel rate
- Multiplexed data, clock input at 2X the pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7305 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7305 is latched with one edge of the clock (also known as single edge transfer mode or SDR). The polarity of the pixel clock can be reversed under serial port control. In single edge transfer modes, the clock edge used to latch data is programmable. In dual edge transfer modes, the clock edge used to latch the first half of each pixel is programmable.

2.1.2 Interface Voltage Levels

The graphics controller interface can operate at a variable voltage level controlled by the voltage on the **VDDV** pin. This should be set to the maximum voltage of the interface (typically 3.3V or adjustable between 1.1 and 1.8V). The VREF pin is the voltage reference for the data, data enable, clock and sync inputs and must be tied to VDDV/2. This is typically done using a resistor divider.

2.1.3 Input Clock and Data Timing Diagram

Figure 3 below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK/XCLK* waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in **Section 4.5**.

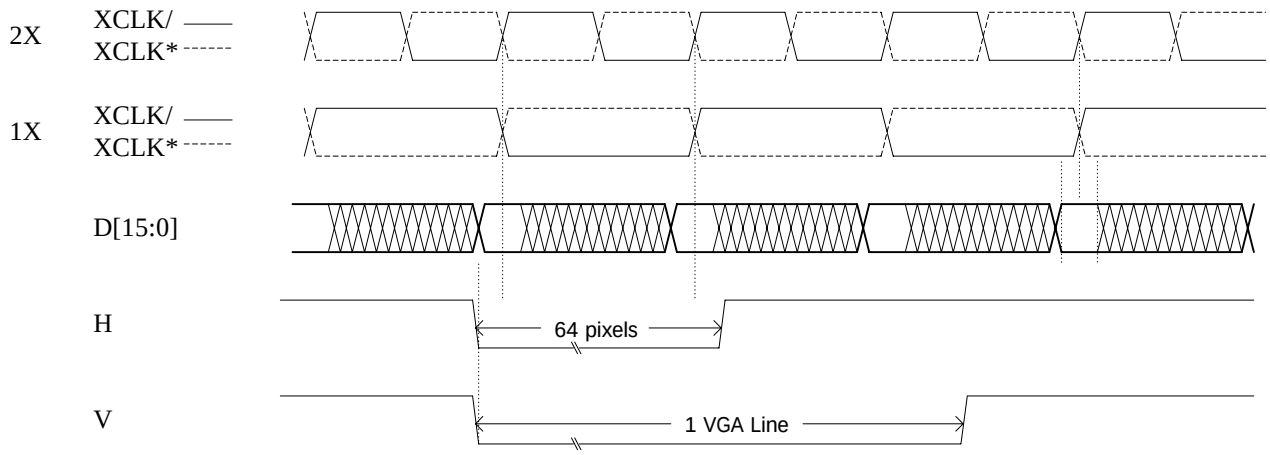

Figure 3: Clock, Data and Interface Timing

2.1.4 Data De-skew Feature

The de-skew feature allows adjustment of the input setup and hold time. The input data D[11:0] can be latched slightly before or after the latching edge of XCLK depending on the amount of the de-skew. Note that the XCLK is not changed, only the time at which the data is latched relative to XCLK. The de-skew is controlled using the XCMD[3:0] bits located in **Register 1Dh**. The delay t_{CD} between clock and data is given by the following formula:

t_{CD} = - XCMD[3:0] * t_{STEP} for $0 \le$ XCMD[3:0] ≤ 7
t_{CD} = (XCMD[3:0] – 8) * t_{STEP} for $8 \le$ XCMD[3:0] ≤ 15

where XCMD is a number between 0 and 15 represented as a binary code
t_{STEP} is the adjustment increment (see **Section 4.5**)

The delay is also tabulated in **Table 9**.

2.1.5 Input Data Formats

The CH7305 supports 5 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge (rising or falling depending on the value of the MCP bit – rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal). Received data is formatted and sent through an internal data bus P[23:0] to the LVDS data path. The input data formats are (IDF[2:0] = 0, 1, 2, 3 and 4):

IDF	Description
0	RGB 8-8-8 (2x12-bit)
1	RGB 8-8-8 (2x12-bit) or RGB 5-6-5 (2x8-bit)
2	RGB 5-6-5 (2x8bit)
3	RGB 5-5-5 (2x8-bit)
4	YCrCb 8-8 (2x8-bit) (refer to **Register 31h**, bit 0)

The input data format is shown in **Figure 4**. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain a complete pixel encoded as shown in **Table 2** through **Table 4**.

For multiplexed input data formats, data can be latched from the graphics controller by either rising only or falling only clock edges, or by both rising and falling clock edges. The MCP bit selects the rising or the falling clock edge, where rising refers to rising edge on the XCLK signals and falling edge on the XCLK*. It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

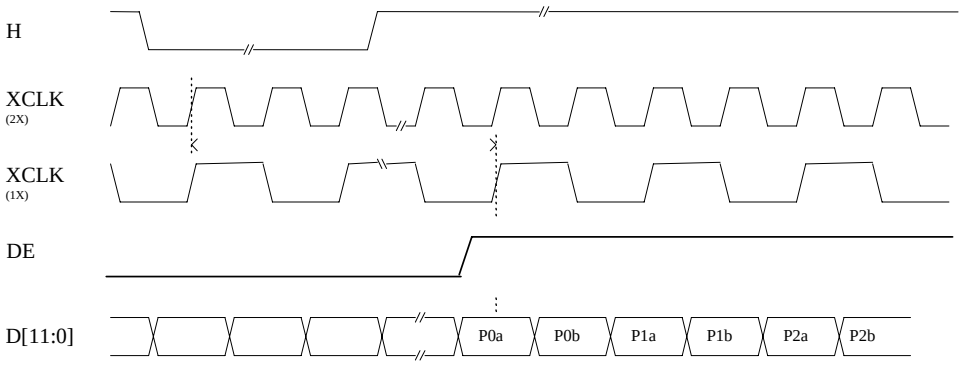

Figure 4: 12-bit Multiplexed Input Data Formats (IDF = 0,1,2,3, 4)

Table 2: Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 RGB 8-8-8 (2x12-bit)				1 RGB 8-8-8 (2x12-bit) or RGB 5-6-5 (2x8-bit)			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 3: Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5 (2x8bit)				3 RGB 5-5-5 (2x8-bit)			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 4: Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

2.2 LVDS-Out

2.2.1 Single LVDS Channel Signal Mapping

Table 5: Signal Mapping for Single LVDS Channel

	24-bit LDI	24-bit SPWG	18-bit
LDC[0](1)	R2	R0	R0
LDC[0](2)	R3	R1	R1
LDC[0](3)	R4	R2	R2
LDC[0](4)	R5	R3	R3
LDC[0](5)	R6	R4	R4
LDC[0](6)	R7	R5	R5
LDC[0](7)	G2	G0	G0
LDC[1](1)	G3	G1	G1
LDC[1](2)	G4	G2	G2
LDC[1](3)	G5	G3	G3
LDC[1](4)	G6	G4	G4
LDC[1](5)	G7	G5	G5
LDC[1](6)	B2	B0	B0
LDC[1](7)	B3	B1	B1
LDC[2](1)	B4	B2	B2
LDC[2](2)	B5	B3	B3
LDC[2](3)	B6	B4	B4
LDC[2](4)	B7	B5	B5
LDC[2](5)	HSYNC	HSYNC	HSYNC
LDC[2](6)	VSYNC	VSYNC	VSYNC
LDC[2](7)	DE	DE	DE
LDC[3](1)	R0	R6	N/A
LDC[3](2)	R1	R7	N/A
LDC[3](3)	G0	G6	N/A
LDC[3](4)	G1	G7	N/A
LDC[3](5)	B0	B6	N/A
LDC[3](6)	B1	B7	N/A
LDC[3](7)	N/A	N/A	N/A

2.2.2 Dual LVDS Channel Signal Mapping

Table 6: Signal Mapping for Dual LVDS Channel

	24-bit LDI	24-bit VESA	18-bit
LDC[0](1)	Ro2	Ro0	Ro0
LDC[0](2)	Ro3	Ro1	Ro1
LDC[0](3)	Ro4	Ro2	Ro2
LDC[0](4)	Ro5	Ro3	Ro3
LDC[0](5)	Ro6	Ro4	Ro4
LDC[0](6)	Ro7	Ro5	Ro5
LDC[0](7)	Go2	Go0	Go0
LDC[1](1)	Go3	Go1	Go1
LDC[1](2)	Go4	Go2	Go2
LDC[1](3)	Go5	Go3	Go3
LDC[1](4)	Go6	Go4	Go4
LDC[1](5)	Go7	Go5	Go5
LDC[1](6)	Bo2	Bo0	Bo0
LDC[1](7)	Bo3	Bo1	Bo1
LDC[2](1)	Bo4	Bo2	Bo2
LDC[2](2)	Bo5	Bo3	Bo3
LDC[2](3)	Bo6	Bo4	Bo4
LDC[2](4)	Bo7	Bo5	Bo5
LDC[2](5)	HSYNC	HSYNC	HSYNC
LDC[2](6)	VSYNC	VSYNC	VSYNC
LDC[2](7)	DE	DE	DE
LDC[3](1)	Ro0	Ro6	N/A
LDC[3](2)	Ro1	Ro7	N/A
LDC[3](3)	Go0	Go6	N/A
LDC[3](4)	Go1	Go7	N/A
LDC[3](5)	Bo0	Bo6	N/A
LDC[3](6)	Bo1	Bo7	N/A
LDC[3](7)	N/A	N/A	N/A
LDC[4](1)	Re0	Re0	Re0
LDC[4](2)	Re1	Re1	Re1
LDC[4](3)	Re2	Re2	Re2
LDC[4](4)	Re3	Re3	Re3
LDC[4](5)	Re4	Re4	Re4
LDC[4](6)	Re5	Re5	Re5
LDC[4](7)	Ge0	Ge0	Ge0
LDC[5](1)	Ge1	Ge1	Ge1
LDC[5](2)	Ge2	Ge2	Ge2
LDC[5](3)	Ge3	Ge3	Ge3
LDC[5](4)	Ge4	Ge4	Ge4
LDC[5](5)	Ge5	Ge5	Ge5
LDC[5](6)	Be0	Be0	Be0
LDC[5](7)	Be1	Be1	Be1
LDC[6](1)	Be2	Be2	Be2
LDC[6](2)	Be3	Be3	Be3
LDC[6](3)	Be4	Be4	Be4
LDC[6](4)	Be5	Be5	Be5
LDC[6](5)	LCTLE [1]	HSYNC	LCTLE [1]
LDC[6](6)	LCTLF [1]	VSYNC	LCTLF [1]
LDC[6](7)	LA6RL [1]	DE	LA6RL [1]
LDC[7](1)	Re0	Re6	N/A
LDC[7](2)	Re1	Re7	N/A
LDC[7](3)	Ge0	Ge6	N/A

LDC[7](4)	Ge1	Ge7	N/A
LDC[7](5)	Be0	Be6	N/A
LDC[7](6)	Be1	Be7	N/A

Note: 1. See description for **Register 65h**.

2.2.3 Dithering

The CH7305 has a dither engine that can convert the 24-bit pixel data to 18-bit pixel data for better image quality on 18-bit panels. Maximum pixel rate supported is 165M Pixels / sec.

2.2.4 Power Sequencing

The CH7305 conforms to SPWG's requirements on power sequencing. The timing specification shown in **Figure 5** is a superset of the requirements dictated by the SPWG specification. The power sequencing block consists of a state machine and 5 hardware timers, which are programmable through the serial port to suit requirements by different panels. It provides 2 signals ENAVDD and ENABKL to the LCD panel.

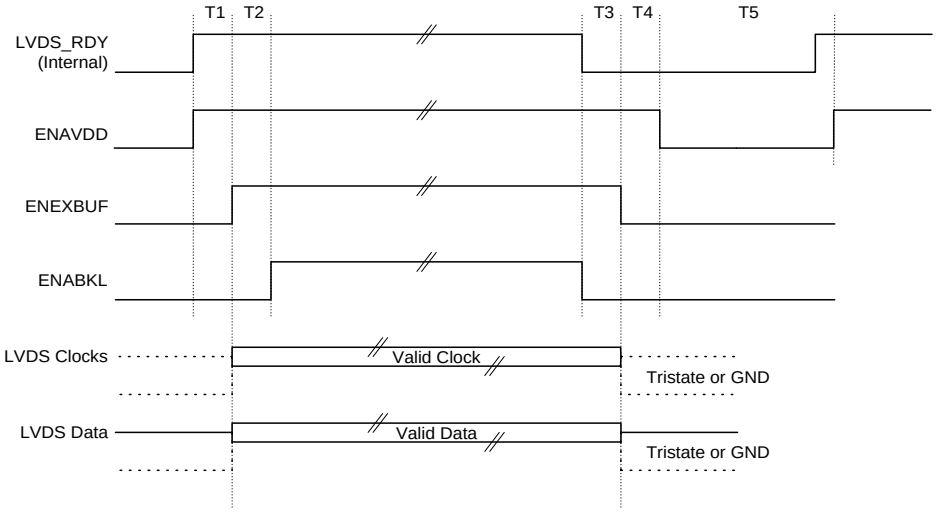

Figure 5: Power Sequencing

Table 7: Power Sequencing

	Range	Increment
T1	2-512 ms	1 ms
T2	2-256 ms	2ms
T3	2-256 ms	2ms
T4	2-512 ms	1 ms
T5	2-1600 ms	50ms

Power-on sequence begins when the LVDS software registers are set properly via the serial port and the internal PLL lock detection circuit and the internal Sync detection circuits (see **Section 2.2.5**) indicate that HSYNC, VSYNC and XCLK are stable. Note that the BKLEN bit **(Register 66h)** must be set in order for the ENABKL signal to be asserted. Power-off sequence begins when any detection circuits indicate an instability in the timing signals (see **Section 2.2.5**), or through software programming. Once power-off sequence starts, the internal state machine will complete the sequence and power-on sequence is allowed only after T5 is passed.

When the LVDS output clock and data signals become invalid, these outputs are tri-stated or grounded depending on the value of the LODP bit.

2.2.5 Panel Protection

The LCD panel can be damaged if HSYNC is absent from the LVDS link. This situation can happen when there is a catastrophic failure in the PC or the graphics system. The CH7305 is designed to prevent damage to the panel under such a failure. If the system fails, the CH7305 does not expect any software instruction from the graphics controller to power down the panel. Detection circuits are used to monitor the three timing signals – HSYNC, VSYNC and XCLK. If any one, combination of, or all of these signals becomes unstable, the CH7305 will commence Power Down Sequencing according to **Section 2.2.4**. A description of these detection circuits is shown in **Figure 6**.

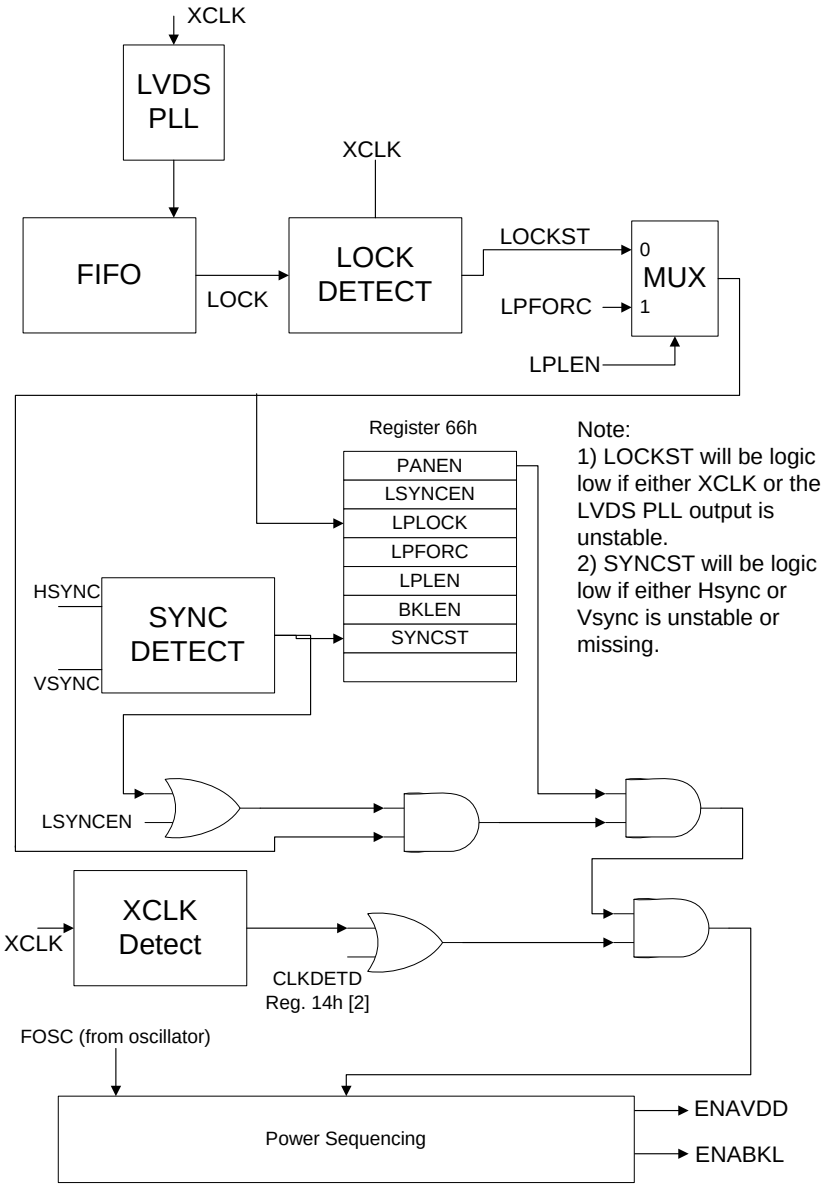

Figure 6: Detection Circuits for Panel Protection

The power up sequence can occur only if (a) XCLK is not missing, (b) there are no missing HSYNC and VSYNC, (c) the PLL CLOCK is stable, and (d) PANEN is set to 1. The power down sequence happens if any of those conditions fails. The power up sequence can also occur if the panel protection circuitry is bypassed.

The panel protection circuitry is comprised of a LOCKDET block, which detects an unstable clock from the LVDS PLL, a SYNCDET block, which detects missing inputs HSYNC and VSYNC and an XCLK Detect block which detects missing XCLK. XCLK stability (assuming it is not missing) is determined by the number of PLL unlock signals generated within one frame. This number is programmable via serial port using the BGLMT register **(Register 7Fh)**.

The SYNCDET block consists of counters to count HSYNC and VSYNC pulses. One counter is used to count the number of HSYNC pulses per frame over 3 frames. The end counts for all 3 frames must be equal to enable the power up sequence. In addition, the SYNCDET block checks for the presence of VSYNC and HSYNC. If VSYNC is missing for 2 frames or if HSYNC is missing for 32us the power up sequence is disabled.

The XCLK Detect block detects if XCLK is missing for more than approximately 1.2us.

The LOCKDET block and SYNCDET block can be defeated or bypassed independently through the LPMC register **(Register 66h)** controls. To defeat the LOCKDET block set LPFORC to '1' and LPLEN to '1'; to defeat the SYNCDET block set LSYNCEN to 1. The XCLK Detect block can be defeated or bypassed independently through the CLKDETD bit in **Register 14h**, bit 2. To defeat the XCLK Detect block set CLKDETD to '1'.

2.2.6 Emission Reduction Clock

LVDS data path can support a +- 2.5% emission reduction clock to reduce EMI emission. The frequency and amplitude of the emission reduction triangle waveform can be programmed via the serial port.

For further details, please contact Chrontel Applications Group.

2.3 Power Down

The CH7305 can be powered down via software control to achieve very low standby current. For a complete description of each individual bit please refer to the appropriate register description in **Registers 63h** and **76h**.

3.0 Register Control

The CH7305 is controlled via a serial port. The serial bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device should retain all register values during power down modes. For registers read/write operation, please refer to applications note AN-61 for details.

3.1 Control Registers Index

The register controls are listed below, divided into three sections: General & Power Down controls, Input/Output controls, and LVDS controls.

GENERAL & POWER DOWN CONTROLS		Address
CLKDETD	XCLK Detection Defeat	14h
DID[7:0]	Device ID register	4Bh
LODPDB[1:0]	LVDS Output Driver Power Down control	76h
LVDSPD	LVDS Power Down	63h
PANEN	Panel Enable (0 – begin Power off sequence, 1 Power-on)	66h
RESETIB	Software SPP (serial port) reset	48h
RESETDB	Software datapath reset	48h
TPBLD [6:0]	Timer – Black Light Disable (T3)	69h
TPBLE [6:0]	Timer – Black Light Enable (T2)	68h
TPOFF [8:0]	Timer – Power Off (T4)	69h-6Ah
TPON [8:0]	Timer - Power On (T1)	67h-68h
TPPWD [5:0]	Timer – Power Cycle (T5)	6Bh
TSTP[1:0]	Enable/select test pattern generation (color bar, ramp)	48h
VID[7:0]	Version ID register	4Ah

INPUT/OUTPUT CONTROLS		Address
IBS	Input buffer type select	1Fh
IDF[2:0]	Input Data Format	1Fh
MCP	XCLK Polarity Control	1Ch
RGB	YCrCb to RGB	31h
XCM	XCLK 1X / 2X select	1Ch
XCMD[3:0]	Delay adjust between XCLK and D[11:0]	1Dh

LVDS CONTROLS		Address
BGLMT[7:0]	Bang Limit control of internal LVDS FIFO over/under run	7Fh
BKLEN	Backlight enable	66h
FRSTB	FIFO Reset Enable	76h
LA3RL	OpenLDI Reserved Bit	65h
LA6RL	OpenLDI Reserved bit	65h
LA7RL	OpenLDI Reserved bit	65h
LCNTLE	OpenLDI Miscellaneous Control Signal	65h
LCNTLF	OpenLDI Miscellaneous Control Signal	65h
LDD	LVDS Dithering Defeat	64h
LDI	Open LDI mode	64h
LDEN[1:0]	LVDS Output Driver enable	73h
LEOSWP	Odd/even sample output swap on LVDS link	64h
L1ODA[2:0]	LVDS Output Driver Amplitude control for bank 1	74h
L2ODA[2:0]	LVDS Output Driver Amplitude control for bank 2	74h
LODP	LVDS Output Driver Pull-down	74h

LODPE	LVDS Output Driver Pre-emphasis	74h
LODST	LVDS Output Driver Source Termination control	75h
LPCP[3]	LVDS PLL Static Phase Error Reduction control	78h
LPCP[2:0]	LVDS PLL Charge pump control	73h
LPFBD[3:0]	LVDS PLL feed back divider controls	71h
LPFFD[1:0]	LVDS PLL feed forward divider controls	71h
LPFORC	Bypass LVDS PLL Lock Detect Sentry	66h
LPLEN	Enable Bypass of LVDS PLL Lock Detect	66h
LPLF[2:0]	LVDS PLL Loop Filter Resistor Value	76h
LPLF[4:3]	LVDS PLL Loop Filter Capacitor Value	78h
LPLOCK	LVDS PLL Lock – read only register	66h
LPPD[4:0]	LVDS PLL phase detector trim	78h
LPPDN	LVDS PLL Power Down	76h
LPPRB	LVDS PLL Reset	76h
LPPSD[1:0]	LVDS PLL post scale divider controls	72h
LPVCO[3:0]	LVDS PLL VCO frequency range controls	72h
LSYNCEN	Bypass Sync Detection	66h
LVDS24	Select 24 bit format	64h
LVDSDC	LVDS Dual Channel Select	64h
SYNCST	HSYNC and VSYNC stability status	66h

3.2 Control Registers Description

Table 8: Serial Port Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14h	Reserved	Reserved	Reserved	Reserved	Reserved	CLKDETD	Reserved	Reserved
1Ch	Reserved	Reserved	Reserved	Reserved	Reserved	MCP	Reserved	XCM
1Dh	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
1Fh	IBS	Reserved	Reserved	Reserved	Reserved	IDF2	IDF1	IDF0
31h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RGB
48h	Reserved	Reserved	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
63h	Reserved	LVDSPD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
64h	Reserved	Reserved	LVDS24	LVDSDC	LDD	Reserved	LEOSWP	LDI
65h	Reserved	Reserved	Reserved	LA3RL	LA6RL	LA7RL	LCNTLE	LCNTLF
66h	Reserved	SYNCST	BKLEN	LPLEN	LPFORC	LPLOCK	LSYNCEN	PANEN
67h	TPON7	TPON6	TPON5	TPON4	TPON3	TPON2	TPON1	TPON0
68h	TPON8	TPBLE6	TPBLE5	TPBLE4	TPBLE3	TPBLE2	TPBLE1	TPBLE0
69h	TPOFF8	TPBLD6	TPBLD5	TPBLD4	TPBLD3	TPBLD2	TPBLD1	TPBLD0
6Ah	TPOFF7	TPOFF6	TPOFF5	TPOFF4	TPOFF3	TPOFF2	TPOFF1	TPOFF0
6Bh	Reserved	Reserved	TPPWD5	TPPWD4	TPPWD3	TPPWD2	TPPWD1	TPPWD0
71h	Reserved	Reserved	LPFFD1	LPFFD0	LPFBD3	LPFBD2	LPFBD1	LPFBD0
72h	Reserved	Reserved	LPPSD1	LPPSD0	LPVCO3	LPVCO2	LPVCO1	LPVCO0
73h	Reserved	Reserved	Reserved	LDEN1	LDEN0	LPCP2	LPCP1	LPCP0
74h	LODP	LODPE	L2ODA2	L2ODA1	L2ODA0	L1ODA2	L1ODA1	L1ODA0
75h	LODST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
76h	FRSTB	LPLF2	LPLF1	LPLF0	LPPDN	LPPRB	LODPDB1	LODPDB0
78h	LPCP3	LPLF4	LPLF3	LPPD4	LPPD3	LPPD2	LPPD1	LPPD0
7Fh	BGLMT7	BGLMT6	BGLMT5	BGLMT4	BGLMT3	BGLMT2	BGLMT1	BGLMT0

3.3 Control Registers Description

Clock Detect Defeat

Symbol: **CDD**
Address: **14h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	CLKDETD	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	0

CLKDETD (bit 2) of **Register CDD** controls the XCLK detection circuit. When CLKDETD is '1' the XCLK detection circuit is turned off, when CLKDETD is 0 the XCLK detection is on.

Clock Mode Register

Symbol: **CM**
Address: **1Ch**

	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	MCP	Reserved	XCM
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

XCM (bit 0) of **Register CM** signifies the XCLK frequency for the D[11:0] input. A value of '0' is used when XCLK is at the pixel frequency (dual edge clocking mode) and a value of '1' is used when XCLK is twice the pixel frequency (single edge clocking mode).

MCP (bit 2) of **Register CM** controls the phase of the XCLK clock input for the D[11:0] input. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

Input Clock Register

Symbol: **IC**
Address: **1Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	XCMD3	XCMD2	XCMD1	XCMD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	1	0	0	0

XCMD[3:0] (bits 3-0) of **Register IC** control the delay applied to the XCLK signal before latching input data D[11:0] per the following table. t_{STEP} is given in **Section 4.5**.

Table 9: Delay applied to XCLK before latching input data

XCMD3	XCMD2	XCMD1	XCMD0	Adjust phase of Clock relative to Data
0	0	0	0	0 * t_{STEP}, XCLK ahead of Data
0	0	0	1	1 * t_{STEP}, XCLK ahead of Data
0	0	1	0	2 * t_{STEP}, XCLK ahead of Data
0	0	1	1	3 * t_{STEP}, XCLK ahead of Data
0	1	0	0	4 * t_{STEP}, XCLK ahead of Data
0	1	0	1	5 * t_{STEP}, XCLK ahead of Data
0	1	1	0	6 * t_{STEP}, XCLK ahead of Data
0	1	1	1	7 * t_{STEP}, XCLK ahead of Data
1	0	0	0	0 * t_{STEP}, XCLK behind Data
1	0	0	1	1 * t_{STEP}, XCLK behind Data
1	0	1	0	2 * t_{STEP}, XCLK behind Data
1	0	1	1	3 * t_{STEP}, XCLK behind Data
1	1	0	0	4 * t_{STEP}, XCLK behind Data
1	1	0	1	5 * t_{STEP}, XCLK behind Data
1	1	1	0	6 * t_{STEP}, XCLK behind Data
1	1	1	1	7 * t_{STEP}, XCLK behind Data

Input Data Format Register

Symbol: **IDF**
Address: **1Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IBS	Reserved	Reserved	Reserved	Reserved	IDF2	IDF1	IDF0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

IDF[2:0] (bits 2-0) of **Register IDF** select the input data format for the input. See **Section 2.1.5** for a listing of available formats.

IBS (bit 7) of **Register IDF** selects the data and clock input buffer type for the D[11:0] data according to the following table:

Table 10: D[11:0] Input Buffer Type Selection

IBS	D[11:0] Input Buffer Type
0	CMOS, single ended type for clock and data
1	Differential (clock) and comparator (data) type

Color Space Control

Symbol: **CSC**
Address: **31h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RGB
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

RGB (bit 0) of **Register CSC** enables the YCrCb to RGB color space conversion for IDF4. This bit must be set to 1 to enable YCrCb to RGB conversion.

RGB = 0 => Disable YCrCb to RGB conversion
= 1 => Enable YCrCb to RGB conversion

Test Pattern Register

Symbol: STP
Address: 48h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	ResetIB	ResetDB	Reserved	TSTP1	TSTP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	0	0	0

TSTP[1:0] (bits 1:0) of **Register STP** enable and select test pattern generation (color bar, ramp). This test pattern can be used for both the LVDS output and the TV Output. The pattern generated is determined by the table below:

Table 11: Test Pattern Selection

TSTP1	TSTP0	Test Pattern
0	0	No test pattern – Input data is used
0	1	Color Bars
1	0	Horizontal Luminance Ramp
1	1	Black screen

ResetDB (bit 3) of **Register STP** resets the datapath. When ResetDB is '0' the datapath is reset. When ResetDB is '1' the datapath is enabled. The datapath is also reset at power on by an internally generated power-on-reset signal.

ResetIB (bit 4) of **Register STP** resets all control registers. When ResetIB is '0' the control registers are reset to the default values. When ResetIB is '1' the control registers operate normally. The control registers are also reset at power on by an internally generated power on reset signal.

Version ID Register

Symbol: VID
Address: 4Ah

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	1	0	0	0	0	0	0	1

Register VID is a read only register containing the version ID number of the CH7305 family.

Product Number	Version ID
CH7305	81h

Device ID Register

Symbol: **DID**
Address: **4Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	X	1	1	0	1	1

Register DID is a read only register containing the device ID number of the CH7305 family. The Device ID depends on the state of the CONFIG pin, pin39 (bit 5 of register 4Bh will update accordingly).

Product Number	CONFIG	Device ID
CH7305	0	3Bh
CH7305	1	1Bh

LVDS Power Down

Symbol: **LPD**
Address: **63h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	LVDSPD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

LVDSPD (bit 6) of **Register LPD** controls the LVDS power down. When LVDSPD is '0' the LVDS path is ON, when LVDSPD is '1' the LVDS path is powered down.

LVDS Encoding 1 Register

Symbol: **LVDSE1**
Address: **64h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	LVDS24	LVDSDC	LDD	Reserved	LEOSWP	LDI
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	1	0	1

LDI (bit 0) of **Register LVDSE1** controls OpenLDI specification selection. A '1' corresponds to OpenLDI, and a '0' corresponds to SPWG. See **Section 2.2.1** for more details.

LEOSWP (bit 1) of **Register LVDSE1** provides the added flexibility to swap odd/even samples output on the LVDS link.

LDD (bit 3) of **Register LVDSE1** bypasses the dither function. A '1' bypasses the dither function. A '0' does not bypass the dither function.

LVDSDC (bit 4) of **Register LVDSE1** allows single or dual channel LVDS to be selected. If the bit is 1, dual channel is selected. If the bit is 0, single channel is selected.

LVDS24 (bit 5) of **Register LVDSE1** selects LVDS 24 bit or 18 bit output format. A '1' provides 24- bit output mode and a ' 0' provides 18- bit output mode.

LVDS Encoding 2 Register

Symbol: **LVDSE2**
Address: **65h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	LA3RL	LA6RL	LA7RL	LCNTLE	LCNTLF
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

LCNTLF and LCNTLE (bits 1-0) of **Register LVDSE2** are OpenLDI miscellaneous control signals, Cntl F and Cntl E, for the Display Source Serializer respectively. Refer to the OpenLDI specification v0.95. See **Section 2.2.2**.

LA3RL (bit 2), LA6RL (bit 3) and LA7RL (bit 4) of **Register LVDSE2** are OpenLDI reserved bits for future use and may take any value. Refer to the OpenLDI specification v0.95, P5. See **Section 2.2.2**.

LVDS PLL Miscellaneous Control Register

Symbol: **LPMC**
Address: **66h**

BIT:	7	6	3	4	3	2	1	0
SYMBOL:	Reserved	SYNCST	BKLEN	LPLEN	LPFORC	LPLOCK	LSYNCEN	PANEN
TYPE:	R/W	R	R/W	R/W	R/W	R	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

The **LPMC register** controls panel protection circuits which control the LVDS panel power up and down sequence. Refer to **Section 2.2.5** Panel Protection and to **Figure 6** for more details.

PANEN (bit 0) of the **LPMC register** controls the LVDS panel enable.
PANEN = 0 => Begin Power off sequence
= 1 => Power-on
LSYNCEN (bit 1) of the **LPMC register** controls the Sync Detection Bypass
LSYNCEN = 0 => Normal Operation. HSYNC and VSYNC detection enabled.
= 1 => HSYNC and VSYNC detection circuit is bypassed enabling forced power up sequence.
LPLOCK (bit 2) of the **LPMC register** indicates the status of the PLL Lock
LPLOCK = 0 => PLL is not stable.
= 1 => PLL is stable and properly locked.
LPFORC (bit 3) of the **LPMC register**: Bypass LVDS Lock Detect Sentry
Bit 3 = 0 => Lock detect sentry is active.
= 1 => Lock detect sentry is overridden if LPLEN is set to '1'.
LPLEN (bit 4) of the **LPMC register** controls LVDS PLL Lock Enable between LPLOCK and LPFORC.
LPLEN = 0 => Select LPLOCK (normal operation)
= 1 => Select LPFORC (Lock detect sentry is overridden if LPFORC is set to '1')
BKLEN (bit 5) of the **LPMC register** enables the panel backlight.
BKLEN = 0 => Disable Backlight
=1 => Enable Backlight

SYNCST(bit 6) of the **LPMC register** is the Hsync and Vsync stability status bit. Refer to **Section 2.2.5**.

SYNCST = 0 => Hsync or Vsync are not stable
= 1 => Hsync and Vsync are stable

Power Sequencing T1

Symbol: **PST1**
Address: **67h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPON7	TPON6	TPON5	TPON4	TPON3	TPON2	TPON1	TPON0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

This register defines Power On time (T1), the time duration between LVDS_RDY (internal signal) to valid LVDS Clock and Data. The entire bit field, TPON[8:0], is comprised of these bits TPON[7:0] plus TPON8 contained in the PST2 Power Sequencing T2 register (**Register 68h**, **bit 7**). Refer to **Figure 5** and **Table 7** in **Section 2.2.4**. The range of T1 is 2ms to 512ms in increments of 1ms.

Power Sequencing T2

Symbol: **PST2**
Address: **68h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPON8	TPBLE6	TPBLE5	TPBLE4	TPBLE3	TPBLE2	TPBLE1	TPBLE0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

TPBLE[6:0] (bits 6:0) of **Register PST2** define the Back Light Enable time (T2), the waiting time after valid LVDS Clock and Data before enabling the LVDS panel back light. Refer to **Figure 5** and **Table 7** in **Section 2.2.4**. The range of T2 is 2ms to 256ms in increments of 2ms.

TPON8 (bit 7) of **Register PST2** defines the MSB of the Power On time (T1). The entire bit field, TPON[8:0], is comprised of this bit, TPON8, plus TPON[7:0] contained in the Power Sequencing T1 register (**Register 67h**). Refer to the description of the PST1 register (**Register 67h**) for more information.

Power Sequencing T3

Symbol: **PST3**
Address: **69h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TP0FF8	TPBLD6	TPBLD5	TPBLD4	TPBLD3	TPBLD2	TPBLD1	TPBLD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

TPBLD[6:0] (bits 6-0) of **Register PST3** define the Back Light Disable time (T3), the required time after disabling the back light before the valid LVDS Clock and Data become tri-stated or disabled. Refer to **Figure 5** and **Table 7** in **Section 2.2.4**. The range of T3 is 2ms to 256ms in increments of 2ms.

TPOFF8 (bit 7) of **Register PST3** defines the MSB of the Power Off time (T4). The entire bit field, TPOFF[8:0], is comprised of this bit, TPOFF8, plus TPOFF[7:0] contained in the Power Sequencing T4 register (**Register 6Ah**). Refer to the description of the PST4 register (**Register 6Ah**) for more information.

Power Sequencing T4

Symbol: **PST4**
Address: **6Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	TPOFF7	TPOFF6	TPOFF5	TPOFF4	TPOFF3	TPOFF2	TPOFF1	TPOFF0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

Register PST4 defines the Power Off time (T4), the required time prior to power off after the valid LVDS Clock and Data become tri-stated or disabled. The entire bit field, TPOFF[8:0], is comprised of these bits, TPOFF[7:0], plus TPOFF8 contained in the Power Sequencing T3 register (**Register 69h**, bit 7). Refer to **Figure 5** and **Table 7** in **Section 2.2.4**.

The range is 2ms to 512ms in increments of 1ms.

Power Sequencing T5

Symbol: **PST5**
Address: **6Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	TPPWD5	TPPWD4	TPPWD3	TPPWD2	TPPWD1	TPPWD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	0	0	0	0	0	1

TPPWD[5:0] (bits 5-0) of **Register PST5** define the Power Cycle time (T5), the waiting time required prior to enabling power on after power has been off. Refer to **Figure 5** and **Table 7** in **Section 2.2.4**. The range is 2ms to 1600ms in increments of 50ms.

LVDS PLL Feed Back Divider Control

Symbol: **LPFBDC**
Address: **71h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	LPFFD1	LPFFD0	LPFBD3	LPFBD2	LPFBD1	LPFBD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	0	0	1	1

LPFBD[3:0] (bits 3-0) of **Register LPFBDC** define the LVDS PLL Feed-Back Divider Control. The recommended settings are shown in **Table 16** in **Section 3.4**.

LPFFD[1:0] (bits 5:4) of **Register LPFBDC** define the LVDS PLL Feed-Forward Divider Control. The recommended settings are shown in **Table 16** in **Section 3.4**.

LVDS PLL VCO Control Register

Symbol: **LPVC**
Address: **72h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	LPPSD1	LPPSD0	LPVCO3	LPVCO2	LPVCO1	LPVCO0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	1	0	1	1	0

LPVCO[3:0] (bits 3-0) of **Register LPVC** determine the LVDS PLL VCO open-loop frequency range. The recommended settings are shown in **Table 16** in **Section 3.4**.

LPPSD[1:0] (bits 5:4) of **Register LPVC** define the LVDS PLL post scale divider controls. The recommended settings are shown in **Table 16** in **Section 3.4**.

Outputs Enable Control Register

Symbol: **OUTEN**
Address: **73h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	LDEN1	LDENO	LPCP2	LPCP1	LPCP0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	0	0	1	0	0	0

LPCP[2:0] (bits 2-0) of **Register OUTEN** control the LVDS PLL Charge Pump current value. The recommended settings are shown in **Table 16** in **Section 3.4**.

LDEN[1:0] (bits 4-3) of **Register OUTEN** control the output drivers of LVDS output Channel 1 (LDC[3:0], LDC*[3:0], LL1C and LL1C*) and Channel 2 (LDC[7:4], LDC*[7:4], LL2C and LL2C*) per the following table:

Table 12: LVDS Output Drivers Enable

LDEN1	LDEN0	Description
0	0	Both LVDS Channel 1 and 2 are 'Off'
0	1	LVDS Channel 1 is 'On' and 2 is 'Off'
1	0	LVDS Channel 1 is 'Off' and 2 is 'On'
1	1	Both LVDS Channel 1 and 2 are 'On'

LVDS Output Driver Amplitude control

Symbol: **LODA**
Address: **74h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	LODP	LODPE	L2ODA2	L2ODA1	L2ODA0	L1ODA2	L1ODA1	L1ODA0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	0	0	0	0	0	0

L1ODA[2:0] (bits 2-0) of **Register LODA** control the Output Driver Amplitude for LVDS Channel 1. See **Table 13**.

L2ODA[2:0] (bits 5-3) of **Register LODA** control the Output Driver Amplitude for LVDS Channel 2. See **Table 13**.

Table 13: LVDS Output Driver Amplitude

LxODA2	LxODA1	LxODA0	Output Driver Amplitude (mV)
0	0	0	305
0	0	1	285
0	1	0	265
0	1	1	245
1	0	0	225
1	0	1	410
1	1	0	370
1	1	1	330

LODPE (bit 6) of **Register LODA** controls LVDS Output Driver Pre-Emphasis for both LDC[7:4] and LDC[3:0] by simultaneous Pull-up and Pull-down diode currents.

LODPE = 0 => Pull up reduced by 33% and pull down reduced by 66%.
= 1 => Default value

LODP (bit 7) of **Register LODA** activates the LVDS Outputs Driver Pull-Down during power-down.
LODP = 0 => Pull-down devices not active
= 1 => Pull-down devices active

LVDS Source Termination

Symbol: LST
Address: 75h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	LODST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

LODST (bit 7) of **Register LST** controls the LVDS Output Drive Source Termination.
LODST = 0 => 100Ω shunt disabled between LVDS outputs LDCx and LDCx*, also LLxC and LLxC*
= 1 => 100Ω shunt enabled between LVDS outputs LDCx and LDCx*, also LLxC and LLxC*

LVDS Power Down

Symbol: LPD
Address: 76h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	FRSTB	LPLF2	LPLF1	LPLF0	LPPDN	LPPRB	LODPDB1	LODPDB0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	1	1	0	1

LODPDB[1:0] (bits 1-0) of **Register LPD** control the LVDS Output Power Down per the following table:

Table 14: LVDS Output Power Down

LODPDB1	LODPDB0	LDC[7:4] & LL2C , LL2C* path	LDC[3:0] , LL1C & LL1C* path
0	0	Power Down	Power Down
0	1	Power Down	Power On
1	0	Power On	Power Down
1	1	Power On	Power On

Note: Outputs are tri-stated in power down mode unless LODP (**Register 74h**, bit 7) is '1', in which case outputs are pulled to ground.

LPPRB (bit 2) of **Register LPD** controls the LVDS PLL Reset.
LPPRB = 0 => LVDS PLL is reset
= 1 => Normal operation

LPPDN (bit 3) of **Register LPD** controls the LVDS PLL Power Down.
LPPDN = 0 => LVDS PLL is powered down
= 1 => Normal operation

LPLF[2:0] (bits 6-4) of **Register LPD** control the LVDS PLL Loop Filter Resistor per the following table:

Table 15: LVDS PLL Loop Filter Resistor

LPLF2	LPLF1	LPLF0	PLL Loop Filter Resistor Value (Ohm)
0	0	0	1800
0	0	1	2600
0	1	0	1000
0	1	1	3200
1	0	0	21,800
1	0	1	42,600
1	1	0	11,000
1	1	1	73,200

The recommended settings are shown in **Table 16** in **Section 3.4**.

FRSTB (bit 7) of **Register LPD** controls the FIFO reset.

FRSTB = 0 => Enable FIFO Reset
= 1 => Normal Operation

LVDS Control

Symbol: LVCTL
Address: 78h

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	LPCP3	LPLF4	LPLF3	LPPD4	LPPD3	LPPD2	LPPD1	LPPD0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	1	0	0	0

LPPD[4:0] (bits 4-0) of **Register LVCTL** define the LVDS PLL Phase Detector Control. The recommended settings are shown in **Table 16** in **Section 3.4**.

LPLF[4:3] (bits 6-5) of **Register LVCTL** control the LVDS PLL Loop Filter Capacitor. The recommended settings are shown in **Table 16** in **Section 3.4**.

LPCP3 (bit 7) of **Register LVCTL** enables the LVDS PLL Static Phase Error Reduction. The default value is recommended.

LPCP3 = 0 => Static Phase Error Reduction Disabled
= 1 => Static Phase Error Reduction Enabled

Bang Limit Control

Symbol: BGLMT
Address: 7Fh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BGLMT7	BGLMT6	BGLMT5	BGLMT4	BGLMT3	BGLMT2	BGLMT1	BGLMT0
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

This register limits the allowable occurrences of internal LVDS FIFO over and under-runs within one VGA frame. The recommended setting is shown in **Table 16** in **Section 3.4**.

3.4 Recommended Settings

The recommended values for the LVDS PLL are shown in **Table 16** below.

Table 16: LVDS Control Settings

Address/Bit	800 x 600	1024 x 768	1280 x 1024	1400 x 1050	1600 x 1200
71h	ADh	ADh	A3h	A3h	A3h
72h	ADh	ADh	ADh	ADh	ADh
73h	C8h	C8h	DBh	DBh	DBh
74h	F6h	F6h	F6h	F6h	F6h
76h	ADh	ADh	AFh	AFh	AFh
78h	80h	80h	80h	80h	80h
7Fh	10h	10h	10h	10h	10h

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All power supplies relative to GND	-0.5		5.0	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	0		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 second)			260	°C
	Vapor phase soldering (11 second)			245	°C
	Vapor phase soldering (60 second)			225	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The temperature requirements of vapor phase soldering apply to all standard and lead free parts.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
LPLL_VDD	LVDS PLL Power Supply Voltage	3.1	3.3	3.6	V
DVDD	Digital Power Supply Voltage	3.1	3.3	3.6	V
LVDD	LVDS Power Supply Voltage	3.1	3.3	3.6	V
VDD	Generic for all of the above supplies	3.1	3.3	3.6	V
VDDV	I/O Power Supply Voltage	1.1	1.8	3.6	V

4.3 Electrical Characteristics
(Operating Conditions: T_A = 0°C – 70°C, VDD =3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
I_{VDD}	Total supply current 1 DVO input for LVDS @ 162 MHz LVDS output @ 162 MHz		210	280	mA
I_{VDD}	Total supply current 1 DVO input for LVDS@65 MHz LVDS output @ 65 MHz		130	175	mA
I_{VDDV}	VDDV (1.8V) current (15pF load)		4		mA
I_{PD}	Total Power Down Current		0.01	0.1	mA

4.4 Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Inputs		0.25			V
V_{DATAIH}	D[11:0] Input High Voltage		Vref+0.25		DVDD+0.5	V
V_{DATAIL}	D[11:0] Input Low Voltage		GND-0.5		Vref-0.25	V
$V_{MISCAIH}$	CONFIG, RESET* Input High Voltage	DVDD=3.3V	2.7		VDD + 0.5	V
$V_{MISCAIL}$	CONFIG, RESET* Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
$I_{MISCAPU}$	Pull Up Current (CONFIG, RESET*)	V_{IN} = 0V	0.5		5	uA
$V_{MISCAOH}$	CONFIG, ENAVDD, ENABKL, Output High Voltage	I_{OH} = -0.4mA	VDD-0.2			V
$V_{MISCAOL}$	CONFIG, ENAVDD, ENABKL, Output Low Voltage	I_{OL} = 3.2mA			0.2	V

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{XCLK}	Input (XCLK) frequency		25		165	MHz
t_{PIXEL}	Pixel time period		6.06		40	ns
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2$ns	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	0.5			ns
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	0.5			ns
t_{STEP}	De-skew time increment		50		80	ps

4.6 LVDS Output Specifications

The LVDS specifications meet the requirements of ANSI/EIA/TIA-644. Refer to Figure 7 for definitions of parameters.

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$\| V_t \|$	Steady State Differential Output Magnitude for logic 1	100Ω differential load	247		453	mV
$\| V_t^* \|$	Steady State Differential Output Magnitude for logic 0	100Ω differential load	247		453	mV
$\| V_t \| - \| V_t^* \|$	Steady State Magnitude of Difference between Logic 1 and 0 Outputs	100Ω differential load			50	mV
$\|V_{OS}\|$	Steady State Magnitude of Offset Voltage for Logic 1	Measured at center-tap of two 50Ω resistors connected between outputs	1.125		1.375	V
$\|V_{OS}^*\|$	Steady State Magnitude of Offset Voltage for Logic 0	Measured at center-tap of two 50Ω resistors connected between outputs	1.125		1.375	V
$\|V_{OS}\| - \|V_{OS}^*\|$	Steady State Magnitude of Offset Difference between Logic States	Measured at center-tap of two 50Ω resistors connected between outputs			50	mV
f_{LLC}	LVDS Output Clock Frequency		25		108 [1]	MHz
t_{UI}	LVDS data unit time interval	25MHz < f_{LLC} < 108MHz	1.3		5.7	ns
t_R	LVDS data rise time t_{UI} > 5ns 1.3ns < t_{UI} < 5ns	100Ω and 5pF differential load 20% -> 80% V_{SWING}			 0.3* t_{UI} 1.5	 ns ns
t_F	LVDS data fall time t_{UI} > 5ns 1.3ns < t_{UI} < 5ns	100Ω and 5pF differential load 80% -> 20% V_{SWING}			 0.3* t_{UI} 1.5	 ns ns
V_{RING}	Voltage ringing after transition	100Ω and 5pF differential load			20% V_{SWING}	

Note 1: Corresponds to maximum pixel rate f_{XCLK} for single channel operation. Dual channel operation is required for pixel rates greater than 108MHz.

4.7 Timing Information

4.7.1 LVDS Output Timing

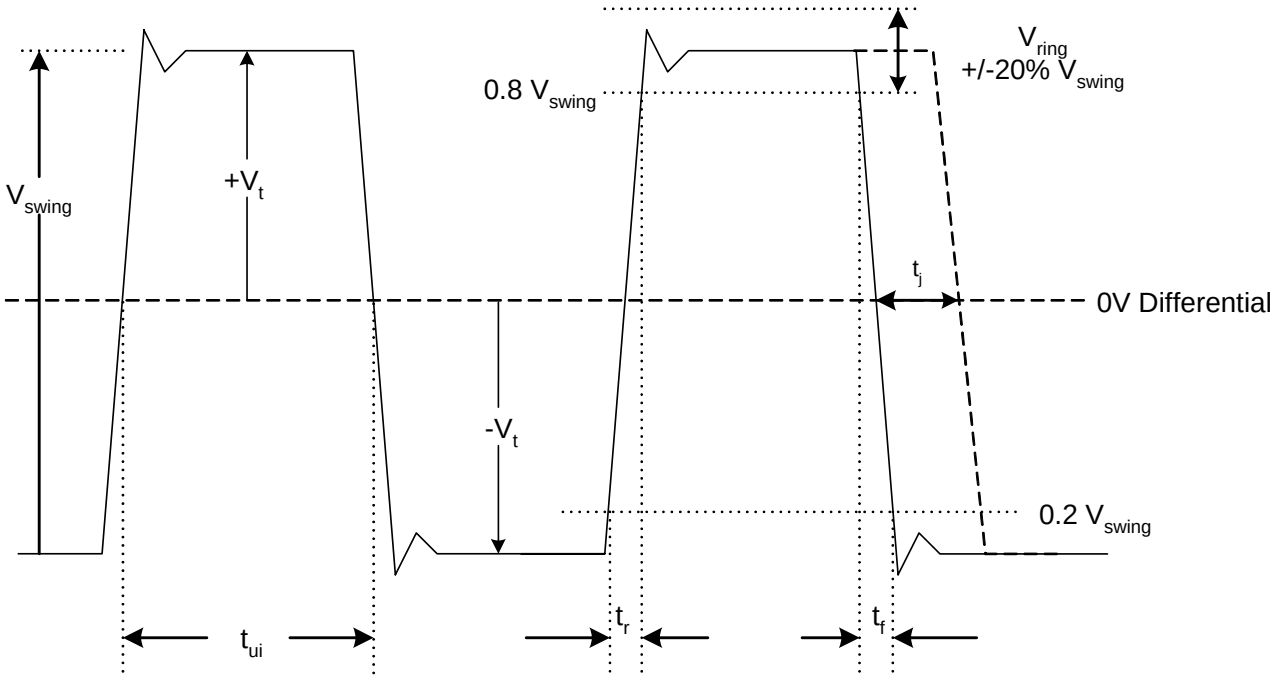

Figure 7: AC Timing for LVDS Outputs

Table 17: AC Timing for LVDS Outputs

Symbol	Parameter	Min	Typ	Max
$\| V_t \|$	Steady State Differential Output Magnitude	see section 4.6		
V_{SWING}	Voltage Difference between the two Steady State Values of Output			
t_{Ui}	Unit time interval	see section 4.6		
t_r	Rise time	see section 4.6		
t_f	Fall time	see section 4.6		
t_j	Jitter peak to peak[1]			350ps

Note 1: Maximum jitter with EMI reduction turned off.

4.7.2 LVDS Input Timing: Clock – Slave, Sync – Slave Mode

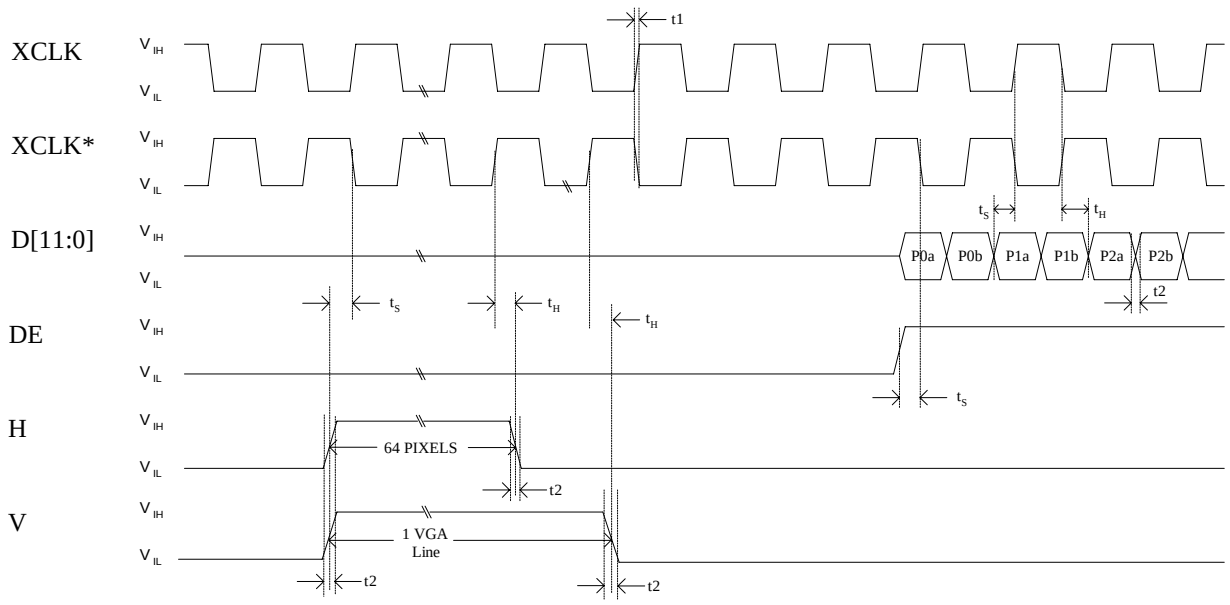

Figure 8: Timing for Clock - Slave, Sync - Slave Mode

Table 18: Timing for Clock

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Section 4.5**			
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	see **Section 4.5**			
t1	XCLK & XCLK* rise/fall time w/15pF load		1		ns
t2	D[11:0], H, V & DE rise/fall time w/ 15pF load		1		ns

5.0 Package Dimensions

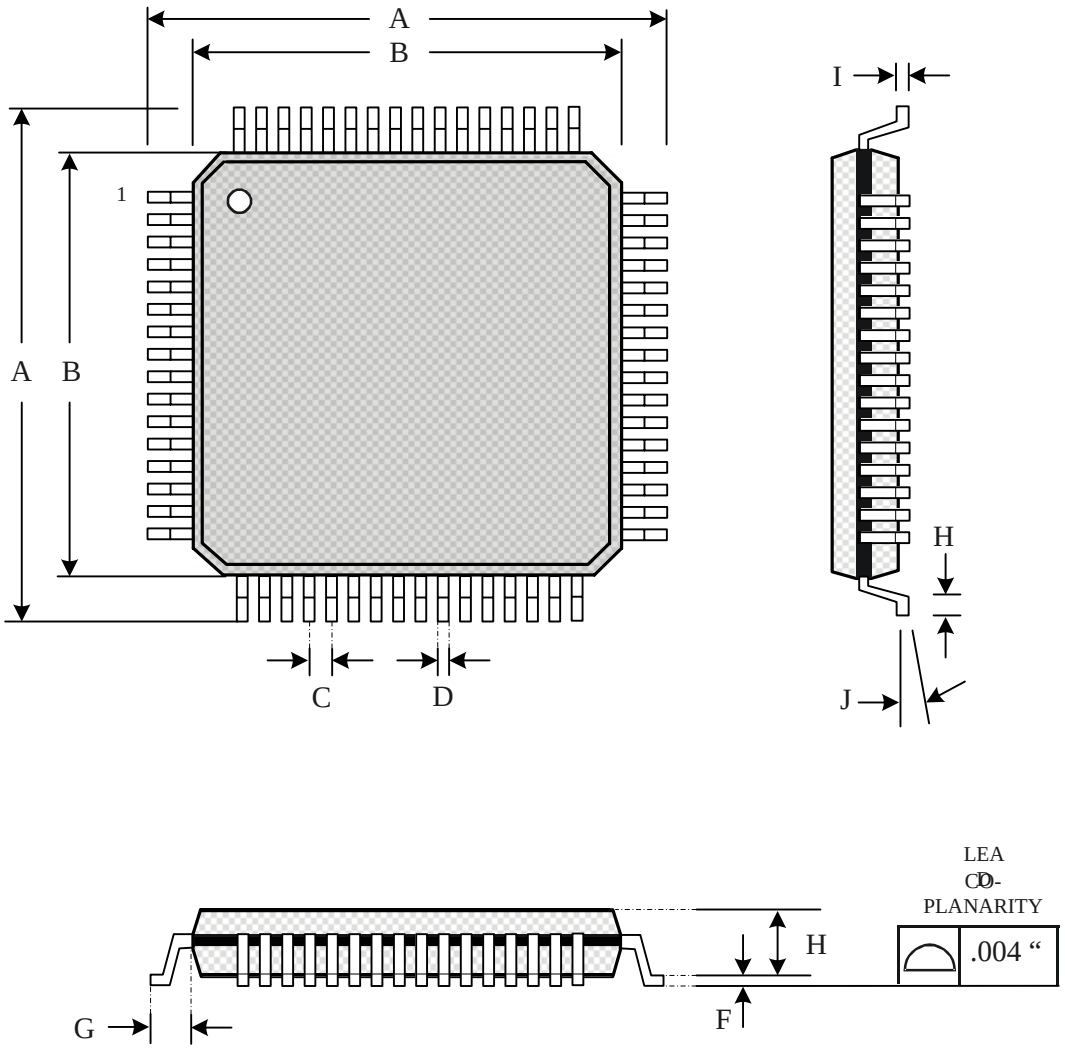

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Figure 9: 64 Pin LQFP Package

6.0 Revision History

Rev. #	Date	Section	Description
1.0	4/9/03	All	First official release, Revision 1.0.
1.1	5/15/03	Figure 1	Deleted AS pin from Figure 1
		4.3	Added supply current limits
	6/23/03		Added Table of Contents
1.2	2/3/04	4.6, 4.7.1	Added section 4.6 and 4.7.1.
		Register 4Bh	Corrected description of DID.
		2.2.2	Corrected the VESA 24-bit LVDS output mapping of LDC[6](7:5) – changed to HSYNC, VSYNC and DE
		All	Removed all references to the GOENB and GPIOL bits.
		All	Changed pin name of GPIO to CONFIG
		Figure 1	Renamed GPIO pin to CONFIG
		Back Page	Added ordering information
1.3	11/9/04	Back Page	Added lead free and take & reel order information
1.31	6/14/2006	Back Page	Corrected part number of lead free and tape & reel.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply
CH7305A-TF	LQFP, Lead free	64	3.3V
CH7305A-TF-TR	LQFP, Lead free, Tape&Reel	64	3.3V

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