Genesys Logic, Inc.

GL846

High Speed USB 2.0
2-in-1 Scanner Controller
With Fast ADF

Datasheet
Revision 1.05
January 18, 2008

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Revision History

Revision	Date	Description
0.01	06/16/2006	Preliminary version
0.02	06/20/2006	Preliminary version-1
0.03	07/26/2006	Modify AFE
1.00	10/04/2006	Modify CCD/CIS descriptions
1.01	04/12/2007	Modify register descriptions
1.02	10/08/2007	1. Modify R_{PU} & R_{PD} of DC Characteristics (Digital Pins) 2. Function block diagram
1.03	11/05/2007	Modify function description
1.04	11/16/2007	GL846 can not support a standard 8051 MCU. So, modify external MCU description.
1.05	01/18/2008	Modify gamma and pin descriptions

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CHAPTER 1　GERERAL DESCRIPTION

Genesys Logic's single-chip GL846 (GeneScan^{TM} series) is a high speed, high performance and rich scalability controller for scanner with fast ADF function. It successfully integrates scanner function ASIC and USB 2.0 interface controller into one single-chip. With its high performance design architecture, GL846 is not only ready for supporting CIS or CCD image sensors (600, 1200, 2400, 3200, 3600, 4800 and 9600dpi resolution) that are used in sheet fed, flatbed or transparency scanners, but is able to co-work with unipolar or bipolar stepping motors. Advanced features of GL846 include five motor acceleration/ deceleration curve tables for high speed motor moving.

CHAPTER 2   FEATURES

- Highly integrated scanner controller chip (2-in-1; Scanner Controller and USB 2.0 Interface)
- USB 2.0 High Speed (480Mbit) compliant
- Designed for sheetfed, flatbed and transparency scanners
- Embedded RISC CPU for USB protocol handling
- Support MCU with SPI interfaces for special application in 208-pin package
- Support single AFE for dual head scanning
- Support two chips application for fast dual head scanning
- Supports external 24Kbytes flash ROM or internal 24Kbyte mask ROM
- Firmware online-download for external flash ROM programming
- 12MHz low frequency clock input for better EMI
- Adjustable working clock of scanner controller for different usage (12M, 24M, 30M, 40M, 48M, 60MHz)
- Supports linear or stagger CCD, such as NEC, Toshiba or Sony CCD
- Available sensor types: 600, 1200, 2400, 3200, 3600, 4800 and 9600 dpi color CIS or CCD
- Multi-TG control for CCD (separately controls the R/G/B exposure time)
- Shutter-control for CCD (separately controls the R/G/B exposure time)
- Supports two scanning types: pixel-by-pixel (pixel rate), line-by-line (line rate)
- Support 48-bits color, 16-bits gray and 1-bit line-art
- "True gray" with R, G and B weightings
- 16 bits white/dark shading and 16 bits Gamma correction
- Supports RS232 interface for special applications
- Supports EEPROM (93C46) interface for special applications
- Supports ADF (Auto-Document-Feeder) function with document, ADF and cover sensors
- Supports auto-ADF with automatically feeding in, automatically scanning and automatically feeding out
- Lines packing for stagger CCD or R/G/B line differences
- Fine CDS sampling adjustment to avoid the digital noise influence (8.33ns adjustment)
- Digital average and hardware deletion for various resolutions
- Hardware deletion for various resolutions (from 9600~1dpi with 1dpi decrement)
- Supports 1M*16, 4M*16, 8M*16, 16M*16 and 32M*16 SDRAM
- Supports up to 1 G bits size SDRAM (implements two SDRAM)
- Supports 5 acceleration/deceleration motor tables for high speed motor moving and wall hitting protection
- Supports controllable bipolar motor in full, half, quarter and eighth steps moving
- Supports controllable unipolar motor in full and half steps moving
- Supports V-reference automatic control for motor driver Ics
- Build-in PWM control phase for unipolar motors
- Programmable dummy lines to resolve start/stop (discontinuous) problem

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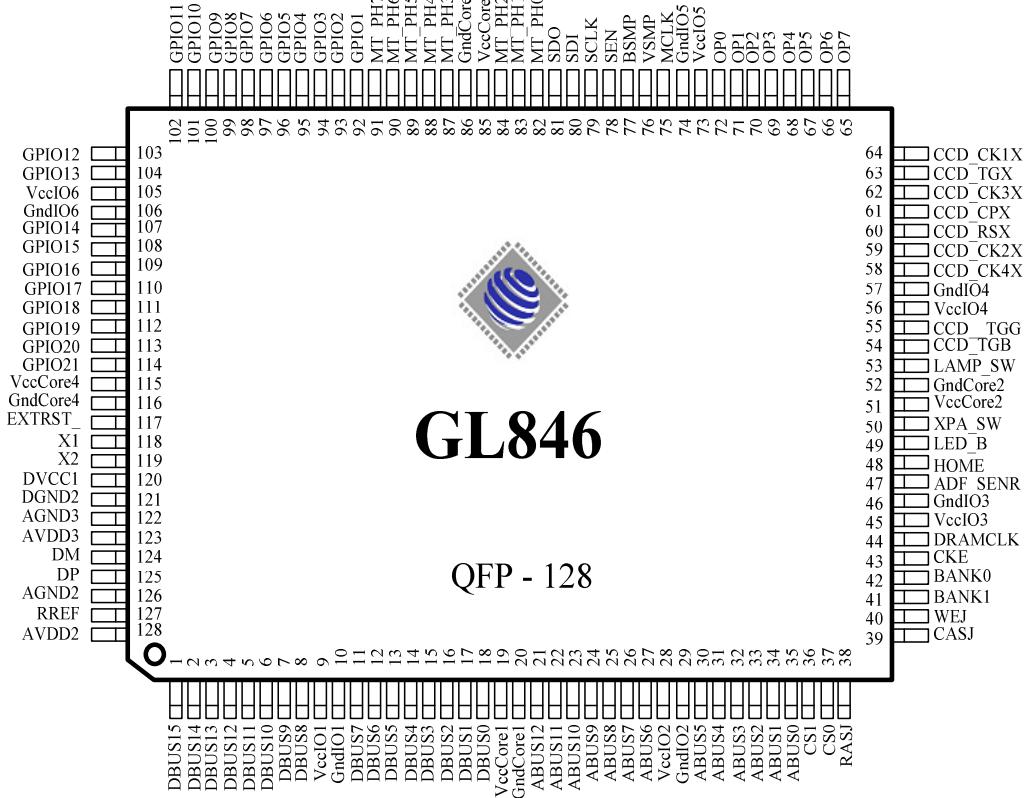
- Watchdog protection for lamp, motor and ASIC

- Lamp time-out (sleeping) control

- Supports 22 GPIO pins and 6 GPO pins for 128-pin package

- Supports 27 GPIO pins and 6 GPO pins for 208-pin package

- Supports PWM outputs for flatbed/transparency lamp control with programmable duties and frequencies

- Supports LED blinking

- Supports back-scanning

- Supports multi-film scanning

CHAPTER 3   PIN ASSIGNMENT

3.1 Pinouts

Figure 3.1 – 128 Pin QFP Pinout Diagram

Figure 3.1 – 208 Pin QFP Pinout Diagram

3.2 Pin List

Table 3.1 – 128 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DBUS15	I/O	33	ABUS2	O	65	OP7	I	97	GPIO6	I/O
2	DBUS14	I/O	34	ABUS1	O	66	OP6	I	98	GPIO7	I/O
3	DBUS13	I/O	35	ABUS0	O	67	OP5	I	99	GPIO8	I/O
4	DBUS12	I/O	36	CS1	O	68	OP4	I	100	GPIO9	I/O
5	DBUS11	I/O	37	CS0	O	69	OP3	I	101	GPIO10	I/O
6	DBUS10	I/O	38	RASJ	O	70	OP2	I	102	GPIO11	I/O
7	DBUS9	I/O	39	CASJ	O	71	OP1	I	103	GPIO12	I/O
8	DBUS8	I/O	40	WEJ	O	72	OP0	I	104	GPIO13	I/O
9	VccIO1	P	41	BANK1	O	73	VccIO5	P	105	VccIO6	P
10	GndIO1	P	42	BANK0	O	74	GndIO5	P	106	GndIO6	P
11	DBUS7	I/O	43	CKE	O	75	MCLK	O	107	GPIO14	I/O
12	DBUS6	I/O	44	DRAMCLK	O	76	VSMP	O	108	GPIO15	I/O
13	DBUS5	I/O	45	VccIO3	P	77	BSMP	O	109	GPIO16	I/O
14	DBUS4	I/O	46	GndIO3	P	78	SEN	O	110	GPIO17	I/O
15	DBUS3	I/O	47	ADF_SENR	I/O	79	SCLK	O	111	GPIO18	I/O
16	DBUS2	I/O	48	HOME	I	80	SDI	O	112	GPIO19	I/O
17	DBUS1	I/O	49	LED_B	O	81	SDO	O	113	GPIO20	I/O
18	DBUS0	I/O	50	XPA_SW	O	82	MT_PH0	O	114	GPIO21	I/O
19	VccCore1	P	51	VccCore2	P	83	MT_PH1	O	115	VccCore4	P
20	GndCore1	P	52	GndCore2	P	84	MT_PH2	O	116	GndCore4	P
21	ABUS12	O	53	LAMP_SW	O	85	VccCore3	P	117	EXTRST_	O
22	ABUS11	O	54	CCD_TGB	O	86	GndCore3	P	118	X1	I
23	ABUS10	O	55	CCD_TGG	O	87	MT_PH3	O	119	X2	O
24	ABUS9	O	56	VccIO4	P	88	MT_PH4	O	120	DVCC1	P
25	ABUS8	O	57	GndIO4	P	89	MT_PH5	O	121	DGND2	P
26	ABUS7	O	58	CCD_CK4X	O	90	MT_PH6	O	122	AGND3	P
27	ABUS6	O	59	CCD_CK2X	O	91	MT_PH7	O	123	AVDD3	P
28	VccIO2	P	60	CCD_RSX	O	92	GPIO1	I/O	124	DM	I/O
29	GndIO2	P	61	CCD_CPX	O	93	GPIO2	I/O	125	DP	I/O
30	ABUS5	O	62	CCD_CK3X	O	94	GPIO3	I/O	126	AGND2	P
31	ABUS4	O	63	CCD_TGX	O	95	GPIO4	I/O	127	RREF	I/O
32	ABUS3	O	64	CCD_CK1X	O	96	GPIO5	I/O	128	AVDD2	P

Table 3.2 – 208 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DBUS15	I/O	33	TWODAT14	I/O	65	TWODAT7	I/O	97	FSH_OEB	O
2	DBUS14	I/O	34	ABUS7	O	66	TWODAT6	I/O	98	CCD_CK2X	O
3	DBUS13	I/O	35	ABUS6	O	67	ADF_SENR	I/O	99	CCD_RSX	O
4	DBUS12	I/O	36	VccIO2	P	68	FSHA2	O	100	CCD_CPX	O
5	DBUS11	I/O	37	GndIO2	P	69	FSHA3	O	101	CCD_CK3X	O
6	DBUS10	I/O	38	ABUS5	O	70	TWODAT5	I/O	102	CCD_TGX	O
7	DBUS9	I/O	39	ABUS4	O	71	HOME	I	103	CCD_CK1X	O
8	DBUS8	I/O	40	ABUS3	O	72	FSHA4	O	104	NC	
9	VccIO1_0	P	41	TWODAT13	I/O	73	FSHA5	O	105	NC	
10	VccIO1_1	P	42	TWODAT12	I/O	74	LED_B	O	106	NC	
11	GndIO1_0	P	43	ABUS2	O	75	FSHA6	O	107	OP7	I
12	GndIO1_1	P	44	ABUS1	O	76	FSHA7	O	108	OP6	I
13	DBUS7	I/O	45	ABUS0	O	77	XPA_SW	O	109	TWODAT0	I/O
14	DBUS6	I/O	46	TWODAT11	I/O	78	FSHA8	O	110	SPI_DO	I
15	DBUS5	I/O	47	TWODAT10	I/O	79	VccCore2	P	111	OP5	I
16	DBUS4	I/O	48	CS1	O	80	GndCore2	P	112	OP4	I
17	DBUS3	I/O	49	CS0	O	81	FSHA9	O	113	SPI_SCK	I
18	DBUS2	I/O	50	RASJ	O	82	LAMP_SW	O	114	SPI_DI	O
19	DBUS1	I/O	51	NC		83	TWODAT4	I/O	115	OP3	I
20	DBUS0	I/O	52	NC		84	TWODAT3	I/O	116	OP2	I
21	VccCore1_0	P	53	CASJ	O	85	FSHA10	O	117	OP1	I
22	VccCore1_1	P	54	WEJ	O	86	FSHA11	O	118	OP0	I
23	GndCore1_0	P	55	TWODAT9	I/O	87	CCD_TGB	O	119	VccIO5	P
24	GndCore1_1	P	56	TWODAT8	I/O	88	FSHA12	O	120	GndIO5	P
25	ABUS12	O	57	BANK1	O	89	FSHA13	O	121	MCLK	O
26	ABUS11	O	58	BANK0	O	90	CCD_TGG	O	122	FSH_WEB	O
27	ABUS10	O	59	FSHA0	O	91	VccIO4	P	123	FSHD0	I/O
28	IMG_RD	I/O	60	FSHA1	O	92	GndIO4	P	124	VSMP	O
29	EMPTY	I/O	61	CKE	O	93	FSHA14	O	125	BSMP	O
30	ABUS9	O	62	DRAMCLK	O	94	CCD_CK4X	O	126	SEN	O
31	ABUS8	O	63	VccIO3	P	95	TWODAT2	I/O	127	SCLK	O
32	TWODAT15	I/O	64	GndIO3	P	96	TWODAT1	I/O	128	SDI	O

129	SDO	O	161	NC		193	EXTRST_	O			
130	FSHD1	I/O	162	NC		194	X1	I			
131	FSHD2	I/O	163	NC		195	X2	O			
132	MT_PH0	O	164	NC		196	DVCC1	P			
133	MT_PH1	O	165	NC		197	DGND1	P			
134	MT_PH2	O	166	SERIF_SDAO	O	198	DGND2	P			
135	VccCore3	P	167	GPIO12	I/O	199	VBUS	F			
136	GndCore3	P	168	GPIO13	I/O	200	AGND3	P			
137	MT_PH3	O	169	FSHD3	I/O	201	AVDD3	P			
138	MT_PH4	O	170	FSHD4	I/O	202	DM	I/O			
139	MT_PH5	O	171	VccIO6_0	P	203	DP	I/O			
140	MT_PH6	O	172	VccIO6_1	P	204	AGND1	P			
141	MT_PH7	O	173	GndIO6_0	P	205	AGND2	P			
142	SPI_CS	I	174	GndIO6_1	P	206	RREF	I/O			
143	SERIF_CSJ	O	175	GPIO14	I/O	207	AVDD1	P			
144	GPIO1	I/O	176	GPIO15	I/O	208	AVDD2	P			
145	GPIO2	I/O	177	FSHD5	I/O						
146	GPIO3	I/O	178	GPIO16	I/O						
147	GPIO4	I/O	179	GPIO17	I/O						
148	GPIO5	I/O	180	GPIO22	I/O						
149	GPIO6	I/O	181	GPIO23	I/O						
150	SERIF_SCKO	O	182	GPIO18	I/O						
151	SERIF_SDAI	I	183	GPIO19	I/O						
152	GPIO7	I/O	184	FSHD6	I/O						
153	GPIO8	I/O	185	FSHD7	I/O						
154	GPIO9	I/O	186	GPIO20	I/O						
155	GPIO10	I/O	187	GPIO21	I/O						
156	GPIO11	I/O	188	VccCore4	P						
157	NC		189	GndCore4	P						
158	NC		190	GPIO24	I/O						
159	NC		191	GPIO25	I/O						
160	NC		192	GPIO26	I/O						

3.3 Pin Descriptions

Table 3.3 - Pin Descriptions

Pin Name	Type	Description
GPIO1/ROM_SK/LCM_D0	B	General Purpose Input/Output; EEPROM serial data clock; LCM data bit0.
GPIO2/ROM_D/LCM_D1	B	General Purpose Input/Output; EEPROM serial data input; LCM data bit1.
GPIO3/LCM_D2	B	General Purpose Input/Output; LCM data bit2.
GPIO4/LCM_D3	B	General Purpose Input/Output; LCM data bit3.
GPIO5(VBUS)	B	General Purpose Input/Output; USB Vbus 5V detection pin.
GPIO6/TXD/MOTORTGO	B	General Purpose Input/Output; RS232 transmit data output; Output motor trigger for ADF scanning.
GPIO7	B	General Purpose Input/Output.
GPIO8/ICG1/LEDBLINK/SH_ENB	B	General Purpose Input/Output; CCD shutter control ICG1; LED control with Blinking function; Output SH_ENB for external CPLD.
GPIO9/VREF3/SW1/LEDBLINK/SH_ENBX	B	General Purpose Input/Output; Vref3 control for motor driver IC Imax; SW1 output for special CCD application; LED control with Blinking function; Output SH_ENBX for external CPLD.
GPIO10/LCD_C12/SW2/LEDBLINK /CCD_SW2	B	General Purpose Input/Output; LCD common voltage control; SW2 output for special CCD application; LED control with Blinking function; CCD SW2 control for Toshiba CCD TCD2954/TCD2962.
GPIO11/VREF0	B	General Purpose Input/Output; Vref0 control for motor driver IC Imax;

GPIO12/VREF1	B	General Purpose Input/Output; Vref1 control for motor driver IC Imax.
GPIO13/VREF2	B	General Purpose Input/Output; Vref2 control for motor driver IC Imax.
GPIO14/CCD_SW4/CCD_CNT0	B	General Purpose Input/Output; CCD SW4 control for Toshiba CCD TCD2954/TCD2962; Output CCD_CNT0 for external CPLD.
GPIO15/CCD_SW5/CCD_CNT1	B	General Purpose Input/Output; CCD SW5 control for Toshiba CCD TCD2962; Output CCD_CNT1 for external CPLD.
GPIO16/COVERSNR	B	General Purpose Input/Output; Cover sensor for ADF
GPIO17/ROM_CS	B	General Purpose Input/Output; 93C46 chip select
GPIO18/LCM_CS/LCD_SCK	B	General Purpose Input/Output; LCM chip select; LCD shift register clock
GPIO19/LCM_RS/LCD_SI	B	General Purpose Input/Output; LCM register select; LCD serial data input.
GPIO20/LCM_EN/LCD_RCK	B	General Purpose Input/Output; LCM enable; LCD latch clock.
GPIO21/SC_SYNC/LEDBLINK	B	General Purpose Input/Output; ASIC synchronization for two chips operation; LED control with Blinking function.
GPIO22/DATA_ENB/LEDBLINK	B	General Purpose Input/ Output; Scanning information for two chips operation; LED control with Blinking function; It only exists in 208 pins package.
GPIO23/BF_FULLY/LEDBLINK	B	General Purpose Input/ Output; Buffer-full information for two chips operation; LED control with Blinking function; It only exists in 208 pins package
GPIO24/SS_FULLY/LEDBLINK	B	General Purpose Input/ Output; Buffer-full information for two chips operation;

		LED control with Blinking function; It only exists in 208 pins package
GPIO25/SC_INT/LEDBLINK	B	General Purpose Input/Output; Scanner controller output interrupt signal including watch-dog, document-jam and ADF-sensor to external MCU; LED control with Blinking function; It only exists in 208 pins package.
GPIO26/RISC_INT	B	General Purpose Input/Output; Interrupt registers (wrote by MCU) output interrupt signal to external ICE; It only exists in 208 pins package.
GPIO27/ADF_SENR	B	General Purpose Input/Output; ADF sensor for ADF operation.
LED_B/ RXD /MOTORDIR/GPO28	O	CIS Blue LED control; RS232 receive data input; Motor direction control for moving TMA or ADF application; General Purpose Output.

MT_PH0-5	O	Bi-polar (3967): MT_PH5=RESETJ
		                       MT_PH4=ENABLEJ
		                       MT_PH3=DIR
		                       MT_PH2=STEP
		                       MT_PH1=MS2
		                       MT_PH0=MS1
		Bi-polar (3955): MT_PH7=PHASE_A
		                       MT_PH6=PHASE_
		                       MT_PH5=D2A
		                       MT_PH4=D1A
		                       MT_PH3=D0A
		                       MT_PH2=D2B
		                       MT_PH1=D1B
		                       MT_PH0=D0B
		Bi-polar(1939): MT_PH3=IN1
		                       MT_PH2=IN2
		                       MT_PH1=ENA1
		                       MT_PH0=ENA2
		Bi-polar (2916 or 6219): MT_PH5=PHASE1

		MT_PH4=PHASE2
		MT_PH3=I11
		MT_PH2=I01
		MT_PH1=I12
		MT_PH0=I02
		Uni-polar(2003): MT_PH3=PHASE A
		MT_PH2=PHASE B
		MT_PH1=PHASE / A
		MT_PH0=PHASE /B
MT_PH6/LCD_C11/GPO29		Motor phase 6, LCD COM1 control or General Purpose Output.
MT_PH7/LCD_C21/GPO30		Motor phase 7, LCD COM2 control or General Purpose Output
BSMP/CDSCLK1/GPO31	O	Video sample synchronization pulse for Wolfson WM1645 AFE or CDS Reference level sampling clock for Analog Device AFE; General Purpose Output.
HOME/DOC_SENR	I	Document sensor for ADF operation; Home sensor for flatbed operation.
CCD_CK1X	O	CCD Shift register clock1 or CIS clock output.
CCD_CPX/GPO32	O	CCD Clamp gate clock or CIS clock output; General Purpose Output.
CCD_TGX/TSTSEL0	B	When power-on initiates the scanner, this pin is used as mode-select pin. Normally, it is for CCD Transfer gate clock for R channel or CIS Line start pulse.
CCD_CK2X/TSTSEL1		When power-on initiates the scanner, this pin is used as mode-select pin. Normally, it is for CCD Shift register clock2 or CIS clock output.
CCD_RSX/TSTSEL2		When power-on initiates the scanner, this pin is used as mode-select pin. Normally, it is for CCD Reset gate clock or CIS clock output.
CCD_CK3X/TSTSEL3		When power-on initiates the scanner, this pin is used as mode-select pin. Normally, it is for CCD Shift register clock3.
		Normal mode is TSTSEL[3:0] = 4'b0000
CCD_CK4X/GPO33/MTR_SEL0	B	When power-on initiates the scanner, this pin is used as motor-select pin. Normally, it is for CCD Shift register clock4, or General Purpose Output.

CCD_TGG/MTR_SEL1		When power-on initiates the scanner, this pin is used as motor-select pin. Normally, it is for CCD Transfer gate clock of G channel.
CCD_TGB/MTR_SEL2		When power-on initiates the scanner, this pin is used as motor-select pin. Normally, it is for CCD Transfer gate clock of B channel.
		MTR_SEL[2:0]=111 select Phase Table to output any motor driver timing
		MTR_SEL[2:0]=110 select 3972
		MTR_SEL[2:0]=101 select 3972
		MTR_SEL[2:0]=100 select 3967
		MTR_SEL[2:0]=011 select LB1939T/LB1940T
		MTR_SEL[2:0]=010 select Bi_polar 3955
		MTR_SEL[2:0]=001 select Bi_polar 2916 or 6219
		MTR_SEL[2:0]=000 select Uni_polar　2003
LAMP_SW	O	Flatbed lamp power control or CIS Red LED array control
XPA_SW	O	Transparency lamp power control or CIS Green LED array control
OP0~7	I	AFE digital data input.
SEN/SLOAD	O	Serial interface load pulse.
SCLK	O	Serial interface clock output.
SDI	O	Serial data output.
SDO	I	Serial data input.
VSMP/CDSCLK2	O	Wolfson WM1645 type : Video sample synchronization pulse. Analog Device : CDS Data level sampling clock.
MCLK/ADCCLK	O	Wolfson WM1645 type : Master clock. Analog Device : A/D Converter sampling clock.
SERIF_CSJ		ASIC is as a master and outputs CS for external 25C16/24C16.
SERIF_SCKO		ASIC is as a master and outputs SCK for external 25C16/24C16.
SERIF_SDAI		ASIC is as a master and inputs SDAI for external 25C16/24C16.
SERIF_SDAO		ASIC is as a master and outputs SDAO for external 25C16/24C16.
SPI_CS		ASIC is as a slave and inputs SPI CS from external MCU.
SPI_SCK		ASIC is as a slave and inputs SPI SCK from external MCU.
SPI_DI		ASIC is as a slave and outputs SPI DI to external MCU.
SPI_DO		ASIC is as a slave and inputs SPI DO from external MCU.
IMG_RD		Image read for two chips operation;
EMPTY		Buffer empty for two chips operation;

TWODAT[15:0]		Data bus for two chips operation;
DBUS0~15	B	DRAM data bus
ABUS0~12	O	DRAM address bus
RASJ	O	SDRAM row address strobe
CASJ	O	SDRAM column address strobe
WEJ	O	SDRAM write enable
BANK0-1	O	SDRAM bank select
CKE	O	SDRAM clock enable
RAMCLK	O	SDRAM clock
X1	I	Clock input for crystal (12MHz)
X2	O	Clock output for crystal
EXTRST_	I	Hardware reset input
AVDD1, AVDD2, AVDD3	P	Analog power input for USB2.0 transceiver 3.3V
AGND1, AGND2, AGND3	P	Analog ground input for USB2.0 transceiver
DVCC1	P	Digital power input for USB2.0 controller 1.8V
DGND1, DGND2	P	Digital ground input for USB2.0 controller.
VccCore1, VccCore2, VccCore3, VccCore4	P	Digital power input for scanner controller logic core 1.8V
GndCore1, GndCore2, GndCore3, GndCore4	P	Digital ground input for scanner controller logic core.
VccIO1, VccIO2, VccIO3, VccIO4, VccIO5, VccIO6	P	Digital power input for scanner controller I/O pads 3.3V
GndIO1, GndIO2, GndIO3, GndIO4, GndIO5, GndIO6	P	Digital ground input for scanner controller I/O pads.
DP	B	Positive USB differential data
DM	B	Negative USB Differential Data
RREF	B	715 Ohm 1% reference resistor input which should be tied to analog ground
VBUS	F	Floating
FSHD0-7	B	Flash data bus
FSHA0-14	O	Flash address bus
FSH_WEB	O	Flash write enable
FSH_OEB	O	Flash data output enable

Notation: Type   **O**   Output
       I   Input
       B   Bi-directional
       I/O   Bi-directional
       P   Power / Ground
       F   Floating

CHAPTER 4   REGISTERS

4.1 Registers Base Address

Table 4.1 - Base Address for Registers

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
01h	CISSET	DOGENB	DVDSET	STAGGER	COMPENB	TRUEGRAY	SHDAREA	SCAN	8'h00
02h	NOTHOME	ACDCDIS	AGOHOME	MTRPWR	FASTFED	MTRREV	HOMENEG	LONGCURV	8'h00
03h	LAMPDOG	AVEENB	XPASEL	LAMPPWR	LAMPTIM[3:0]				8'h8F
04h	LINEART	BITSET	AFEMOD[1:0]		FILTER[1:0]		FESET[1:0]		8'h00
05h	DPIHW[1:0]		MTLLAMP[1:0]		GMMENB	ENB20M	MTLBASE[1:0]		8'h40
06h	SCANMOD[2:0]			PWRBIT	GAIN4	OPTEST[2:0]			8'h00
07h	LAMPSIM	RESERVE[6:0]							8'h00
08h	DRAM2X	SCNUMENB	MPENB	CIS_LINE	X	X	COLUMN	ENB24M	8'h00
09h	MCNTSET[1:0]		EVEN1ST	BLINE1ST	BACKSCAN	ENHANCE	SHORTTG	NWAIT	8'h00
0Ah	LCDSEL	LCMSEL	ADFSEL	LPWMEN	EPROMSEL	RS232SEL	BAUDRAT[1:0]		8'h00
0Bh	CLKSET[2:0]			RFHDIS	ENBDRAM	DRAMSEL[2:0]			8'h01
0Ch	X	X	X	X	CCDLMT[3:0]				8'h00
0Dh	X	SCSYNC	CLRERR	FULLSTP	SEND	CLRMCNT	CLRDOCJM	CLRLNCNT	-
0Eh	SCANRESET								-
0Fh	MOVE								-
10h	EXPR[15:8]								8'h00
11h	EXPR[7:0]								8'h00
12h	EXPG[15:0]								8'h00
13h	EXPG[7:0]								8'h00
14h	EXPB[15:8]								8'h00
15h	EXPB[7:0]								8'h00
16h	CTRLHI	TOSHIBA	TGINV	CK1INV	CK2INV	CTRLINV	CKDIS	CTRLDIS	8'h33
17h	TGMODE[1:0]		TGW[5:0]						8'h14
18h	CNSET	DCKSEL[1:0]		CKTOGGLE	CKDELAY[1:0]		CKSEL[1:0]		8'h10
19h	EXPDMY[7:0]								8'h00
1Ah	SW2SET	SW1SET	MANUAL3	MANUAL1	CK4INV	CK3INV	LINECLP	X	8'h10
1Bh	GRAY2C	SEL12C	BGRENB	ICGENB	ICGDLY[3:0]				8'h00
1Ch	CK4MTGL	CK3MTGL	CK1MTGL	CKAREA	MTLWD	TGTIME[2:0]			8'h00
1Dh	CK4LOW	CK3LOW	CK1LOW	TGSHLD[4:0]					8'h04
1Eh	WDTIME[3:0]				LINESEL[3:0]				8'h80
1Fh	SCANFED[7:0]								8'h00
20h	BUFSEL[7:0]								8'h00
21h	STEPNO[7:0]								8'h00
22h	FWDSTEP[7:0]								8'h00
23h	BWDSTEP[7:0]								8'h00
24h	FASTNO[7:0]								8'h00
25h	X	X	X	X	LINCNT[19:16]				8'h08
26h	LINCNT[15:8]								8'h00
27h	LINCNT[7:0]								8'h00
2Ch	X	X	DPISET[13:8]						8'h00

2Dh				DPISET[7:0]				8'h00
2Eh				BWHI[7:0]				8'h00
2Fh				BWLOW[7:0]				8'h00
30h				STRPIXEL[15:8]				8'h00
31h				STRPIXEL[7:0]				8'h00
32h				ENDPIXEL[15:8]				8'h00
33h				ENDPIXEL[7:0]				8'h00
34h				DUMMY[7:0]				8'h00
35h				MAXWD[25:18]				8'h00
36h				MAXWD[17:10]				8'h00
37h				MAXWD[9:2]				8'h00
38h				LPERIOD[15:8]				8'h2A
39h				LPERIOD[7:0]				8'h30
3Ah	X	X	X	X	X	X	X	FEWRDATA[8]	8'h00
3Bh				FEWRDATA[7:0]				8'h00
3Dh	X	X	X	X	FEEDL[19:16]				8'h00
3Eh				FEEDL[15:8]				8'h37
3Fh				FEEDL[7:0]				8'h00
40h	DOCSNR	ADFSNR	COVERSNR	CHKVER	DOCJAM	HISPDFLG	MOTMFLG	DATAENB	-
41h	PWRBIT	BUFEMPTY	FEEDFSH	SCANFSH	HOMESNR	LAMPSTS	FEBUSY	MOTORENB	-
42h	X	X	X	X	X	X	VALIDWORD[25:24]		8'h00
43h				VALIDWORD[23:16]				8'h00
44h				VALIDWORD[15:8]				8'h00
45h				VALIDWORD[7:0]				8'h00
46h	X	X	X	X	X	X	X	FERDDATA[8]	-
47h				FERDDATA[7:0]				-
48h	X	X	X	FEDCNT[20:16]					8'h00
49h				FEDCNT[15:8]				8'h00
4Ah				FEDCNT[7:0]				8'h00
4Bh	X	X	X	X	SCANCNT[19:16]				8'h00
4Ch				SCANCNT[15:8]				8'h00
4Dh				SCANCNT[7:0]				8'h00
4Fh	SPI_M_BSY	SLAVEERR	DOGON	ROMBSY	LCMBSY	TX232BSY	RX232BSY	RXREADY	8'h00
50h	X	X	FERDA[5:0]						8'h00
51h	X	X	FEWRA[5:0]						8'h00
52h	X	X	X	RHI[4:0]					8'h00
53h	X	X	X	RLOW[4:0]					8'h00
54h	X	X	X	GHI[4:0]					8'h00
55h	X	X	X	GLOW[4:0]					8'h00
56h	X	X	X	BHI[4:0]					8'h00
57h	X	X	X	BLOW[4:0]					8'h00
58h	VSMP[4:0]					VSMPW[2:0]			8'h00
59h	BSMP[4:0]					BSMPW[2:0]			8'h00
5Ah	ADCLKINV	RLCSEL	CDSREF[1:0]		RLC[3:0]				8'h00
5Dh				HISPD[7:0]				8'h00
5Eh	DECSEL[2:0]			STOPTIM[4:0]					8'hA4
5Fh				FMOVDEC[7:0]				8'h00

Addr								Default
60h	STEPSEL[2:0]			Z1MOD[20:16]				8'h20
61h	Z1MOD[15:8]							8'h00
62h	Z1MOD[7:0]							8'h00
63h	FSTPSEL[2:0]			Z2MOD[20:16]				8'h00
64h	Z2MOD[15:8]							8'h00
65h	Z2MOD[7:0]							8'h00
66h	PHFREQ[7:0]							8'h00
67h	X	X	MTRPWM[5:0]					8'h3F
68h	X	X	FASTPWM[5:0]					8'h3F
69h	FSHDEC[7:0]							8'h00
6Ah	FMOVNO[7:0]							8'h00
6Bh	MULTFILM	GPOM13	GPOM12	GPOM11	GPOCK4	GOPCP	GPOLEDB	GPOADF	8'h00
6Ch	GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	8'h00
6Dh	GPIO8	GPIO7	GPOI6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	8'h00
6Eh	GPOE16	GPOE15	GPOE14	GPOE13	GPOE12	GPOE11	GPOE10	GPOE9	8'h00
6Fh	GPOE8	GPOE7	GPOE6	GPOE5	GPOE4	GPOE3	GPOE2	GPOE1	8'h00
70h	X	X	X	RSH[4:0]					8'h06
71h	X	X	X	RSL[4:0]					8'h08
72h	X	X	X	CPH[4:0]					8'h08
73h	X	X	X	CPL[4:0]					8'h0A
74h	X	X	X	X	X	X	CK1MAP[17:16]		8'h00
75h	CK1MAP[15:8]							8'h00
76h	CK1MAP[7:0]							8'h00
77h	X	X	X	X	X	X	CK3MAP[17:16]		8'h00
78h	CK3MAP[15:8]							8'h00
79h	CK3MAP[7:0]							8'h00
7Ah	X	X	X	X	X	X	CK4MAP[17:16]		8'h00
7Bh	CK4MAP[15:8]							8'h00
7Ch	CK4MAP[7:0]							8'h00
7Dh	CK1NEG	CK3NEG	CK4NEG	RSNEG	CPNEG	BSMPNEG	VSMPNEG	DLYSET	8'h00
7Eh	GPOLED25	GPOLED24	GPOLED23	GPOLED22	GPOLED21	GPOLED10	GPOLED9	GPOLED8	8'h00
7Fh	BSMPDLY[1:0]		VSMPDLY[1:0]		LEDCNT[3:0]				8'h00
80h	VRHOME[1:0]		VRMOVE[1:0]		VRBACK[1:0]		VRSCAN[1:0]		8'h00
81h	X	X	X	X	X	X	X	ROFFSET[8]	8'h00
82h	ROFFSET[7:0]							8'h00
83h	X	X	X	X	X	X	X	GOFFSET[8]	8'h00
84h	GOFFSET[7:0]							8'h00
85h	X	X	X	X	X	X	X	BOFFSET[8]	8'h00
86h	BOFFSET[7:0]							8'h00
87h	X	X	X	ACYCNRLC	ENOFFSET	LEDADD	CK4ADC	AUTOCONF	8'h00
88h	X	X	X	RDNUM[4:0]					8'h00
89h	RS232WD[7:0]							8'h00
8Ah	RS232RD[7:0]							-
8Bh	ROMADDR [7:0]							8'h00
8Ch	ROMWD[15:8]							8'h00
8Dh	ROMWD[7:0]							8'h00

									Default
8Eh	X	X	X	X	X	X	X	X	-
8Fh	X	X	X	X	PREFED[19:16]				8'h00
90h	PREFED[15:8]								8'h00
91h	PREFED[7:0]								8'h00
92h	PSTFED[15:8]								8'h00
93h	PSTFED[7:0]								8'h00
94h	MTRPLS [7:0]								8'h1F
95h	X	X	X	X	SCANLEN[19:16]				8'h00
96h	SCANLEN[15:8]								8'h00
97h	SCANLEN[7:0]								8'h00
98h	ONDUR[15:8]								8'h00
99h	ONDUR[7:0]								8'h00
9Ah	OFFDUR[15:8]								8'h00
9Bh	OFFDUR[7:0]								8'h00
9Ch	LCMWD[7:0]								8'h00
9Dh	RAMDLY[1:0]		MOTLAG	CMODE	STEPTIM[2:0]			IFRS	8'h00
9Eh	X	X	TGSTIME[2:0]			TGWTIME[2:0]			8'h00
9Fh	MASTER	SLAVE	SPI_MOT	FULLPAGE	AUTOADF	MOTMPU	MULDMYLN	DPI9600	8'h00
A0h	X	X	LNOFSET[5:0]						8'h00
A1h	SNRSYN[2:0]			STGSET[4:0]					8'h80
A2h	X	X	X	RFHSET[4:0]					8'h00
A3h	TRUER[7:0]								8'h00
A4h	TRUEG[7:0]								8'h00
A5h	TRUEB[7:0]								8'h00
A6h	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	8'h00
A7h	GPOE24	GPOE23	GPOE22	GPOE21	GPOE20	GPOE19	GPOE18	GPOE17	8'h00
A8h	X	GPO36	GPOE27	GPOE26	GPOE25	GPO27	GPO26	GPO25	8'h00
A9h	GPO35	GPO34	GPO33	GPO32	GPO31	GPO30	GPO29	GPO28	8'h00
AAh	RESERVE[7:0]								8'h00
ABh	GPOM9	MULSTOP[2:0]			NODECEL	TB3TB1	TB5TB2	FIX16CLK	8'h00
ACh	VRHOME3	VRHOME2	VRMOME3	VRMOME2	VRBACK3	VRBACK2	VRSCAN3	VRSCAN2	8'h00
ADh	RISC_INT_O	SC_INT_O	RESERVED	SWSH[4:0]					8'h00
AEh	X	X	STOPPWM[5:0]						8'h3F
AFh	X	X	X	X	X	X	X	X	-
B0h	X	X	X	X	X	X	COLLEN[9:8]		8'h00
B1h	COLLEN[7:0]								8'h00
B2h	X	X	X	X	X	X	COLJMP[9:8]		8'h00
B3h	COLJMP[7:0]								8'h00
B8h	ILX580	TSH_EN	TSH_SEL[1:0]		SW2_EN	SW2_SEL	SW4_EN	SW4EXCHG	8'h00
B9h	TCK_EN	TCK_SEL	TCK4_DIS	TCK3_DIS	TCK1_DIS	TSHMSKB[2:0]			8'h00
BAh	CCD_OUT	AV_EN	TSHMSKG[2:0]			TSHMSKR[2:0]			8'h00
BBh	S580_SEL[1:0]		MT_OFF [13:8]						8'h00
BCh	MT_OFF [7:0]								8'hFF
BDh	SW5_EN	SW5_SEL	SW5EXCHG	X	X	BGMM_N	GGMM_N	RGMM_N	8'h1F
BEh	SW2INV	SW4INV	SW5INV	X	X	BGMM_F	GGMM_F	RGMM_F	8'h00
BFh	TSH_AMT[1:0]		SC_NUM[5:0]						-
C0h	SPI_MOTOR_W1 [19:16]				SPI_MOTOR_W0 [19:16]				8'h00

Address	Register	Default
C1h	SPI_MOTOR_W0 [15:8]	8'h00
C2h	SPI_MOTOR_W0 [7:0]	8'h00
C3h	SPI_MOTOR_W1 [15:8]	8'h00
C4h	SPI_MOTOR_W1 [7:0]	8'h00
C5h	RGMM_Z[15:8]	8'h00
C6h	RGMM_Z[7:0]	8'h00
C7h	GGMM_Z[15:8]	8'h00
C8h	GGMM_Z[7:0]	8'h00
C9h	BGMM_Z[15:8]	8'h00
CAh	BGMM_Z[7:0]	8'h00
D0h	SH0DWN[7:0]	8'h00
D1h	SH1DWN[7:0]	8'h00
D2h	SH2DWN[7:0]	8'h00
D3h	SH3DWN[7:0]	8'h00
D4h	SH4DWN[7:0]	8'h00
D5h	SH5DWN[7:0]	8'h00
D6h	SH6DWN[7:0]	8'h00
D7h	SH7DWN[7:0]	8'h00
D8h	SH8DWN[7:0]	8'h00
D9h	SH9DWN[7:0]	8'h00
DAh	PROTLN[15:8]	8'h00
DBh	PROTLN[7:0]	8'h00
DCh	X X X X X X X X	8'h00
DDh	X X X X X X X X	8'h00
DEh	ROMRD[15:8]	-
DFh	ROMRD[7:0]	-
E0h	R1DWN[15:8]	8'h00
E1h	R1DWN[7:0]	8'h00
E2h	R1UP[15:8]	8'h00
E3h	R1UP[7:0]	8'h00
E4h	R2DWN[15:8]	8'h00
E5h	R2DWN[7:0]	8'h00
E6h	R2UP[15:8]	8'h00
E7h	R2UP[7:0]	8'h00
E8h	G1DWN[15:8]	8'h00
E9h	G1DWN[7:0]	8'h00
EAh	G1UP[15:8]	8'h00
EBh	G1UP[7:0]	8'h00
ECh	G2DWN[15:8]	8'h00
EDh	G2DWN[7:0]	8'h00
EEh	G2UP[15:8]	8'h00
EFh	G2UP[7:0]	8'h00
F0h	B1DWN[15:8]	8'h00
F1h	B1DWN[7:0]	8'h00
F2h	B1UP[15:8]	8'h00
F3h	B1UP[7:0]	8'h00
F4h	B2DWN[15:8]	8'h00

F5h	B2DWN[7:0]		8'h00
F6h	B2UP[15:8]		8'h00
F7h	B2UP[7:0]		8'h00
F8h	MAXSEL[3:0]	MINSEL[3:0]	-
FDh	MAINTSK[3:0]	SUBTSK[3:0]	-
FEh	MOTTGST[3:0]	AUTO_O[3:0]	-
FFh	AUTO_S[7:0]		8'h00

Notation:

R/W	Read / Write
R/O	Read Only
W/O	Write Only
R/W1C	Readable and Write-1-Clear
R/W/C	Read / Write and hardware automatic Clear
X	Don't care and should be wrote by logic "0"

4.2 Register Descriptions

Offset 01h

CISSET	DOGENB	DVDSET	STAGGER	COMPENB	TRUEGRAY	SHDAREA	SCAN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 CISSET
- 0 CCD scan type.
- 1 CIS scan type.

6 DOGENB
- 0 Disable watchdog function.
- 1 Enable watchdog function (set time out duration in Reg1E[7:4]).

5 DVDSET
- 0 Disable shading function.
- 1 Enable shading function (include whole line shading and area shading).

4 STAGGER
- 1 Enable double shading.
- 0 Disable double shading.

3 COMPENB
- 0 Disable data compression.
- 1 Enable lossless data compression.

2 TRUEGRAY
- 0 Disable true gray function.
- 1 Enable true gray function. The weightings are stored in Reg A3,A4 and A5.

1 SHDAREA
- 0 Select whole-line shading.
- 1 Select area-shading (depend on scan area and scan dpi).

0 SCAN
- 0 Disable scanning process.
- 1 Enable scanning process.

Offset 02h

NOTHOME	ACDCDIS	AGOHOME	MTRPWR	FASTFED	MTRREV	HOMENEG	LONGCURV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 NOTHOME
- 0 In auto-go-home function, carriage will not stop until touching the home sensor.
- 1 In auto-go-home function, moving steps of carriage depends on steps setting from software (Reg 3D, 3E and 3F).

6 ACDCDIS
- 0 Enable carriage backtracking when image buffer is full.
- 1 Disable carriage backtracking when image buffer is full.

5 AGOHOME
- 0 Disable auto-go-home function.
- 1 Enable auto-go-home function. It's for carriage to go home automatically

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after scanning finished.

4	MTRPWR	0	Turn off MOTOR power and phase to idle state.
		1	Turn on MOTOR power and phase.
3	FASTFED	0	Move to scanning window by only one acceleration/deceleration tables.
		1	Move to scanning window by two acceleration/deceleration tables.
2	MTRREV	0	Set motor to move in forward direction.
		1	Set motor to move in reverse direction.
1	HOMENEG	0	Motor will be decelerated when home sensor input (HOME) changes from low to high (rising edge).
		1	Motor will be decelerated when home sensor input (HOME) changes from high to low (falling edge).
0	LONGCURV	0	The deceleration curve of the fast moving is defined in table 4 or use default curve.
		1	The deceleration curve of the fast moving is defined in table 5 to protect wall-hitting.

Offset 03h …………………………………………..………..……………. Default value = 8'h94

LAMPDOG	AVEENB	XPASEL	LAMPPWR	LAMPTIM3	LAMPTIM2	LAMPTIM1	LAMPTIM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	LAMPDOG	0	To disable sleep mode of lamp.
		1	To start sleep mode of lamp (default on).
6	AVEENB	0	Select dpi deletion function
		1	Select dpi average function.
5	XPASEL	0	Select flatbed lamp on.
		1	Select transparency lamp on.
4	LAMPPWR	0	Turn off LAMP power.
		1	Turn on LAMP power.
3-0	LAMPTIM [3:0]		Counter of the sleep mode of lamp (default: 4). The unit is minute.

Offset 04h …………………………………………..………..………..……… Default value = 8'h00

LINEART	BITSET	AFEMOD1	AFEMOD0	FILTER1	FILTER0	FESET1	FESET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	LINEART	0	Color/Gray scanning.
		1	Black/White scanning.
6	BITSET	0	8 bits image data type (= byte).
		1	16 bits image data type (= word).
5-4	AFEMOD [1:0]		AFE operation mode.

Wolfson WM1645 Type					
AFEMOD	SCANMOD	Description	CDS Available	Max Sample Rate	Timing Requirements
2	0,1,7	Slow color Pixel-by-pixel	Yes	5MSPS *3 channel	MCLK:VSMP Rate is 8:1
1	0,1,6,7	Color pixel-by-pixel	Yes	6.67MSPS *3 channel	MCLK:VSMP Rate is 6:1
0	0,1,4,5,6	Fast Mono	Yes	13.3MSPS *1 channel	MCLK:VSMP Rate is 3:1

Analog Device Type					
AFEMOD	SCANMOD	Description	CDS Available	Max Sample Rate	Timing Requirements
2	0,1,6,7	Slow color Pixel-by-pixel	Yes		MCLK:VSMP Rate is 3:1
1	0,1,6,7	Mono	Yes		MCLK:VSMP Rate is 2:1
0	0,1,6,7	Fast Mono	Yes		MCLK:VSMP Rate is 1:1

3-2 FILTER [1:0]   Scan color type:
        00   Color
        01   R
        10   G
        11   B

1-0 FESET [1:0]   Front end operation type:
        00   Wolfson type 1
        01   Wolfson type2
        10   ADI type
        11   Reserved

Offset 05h …………………………………………..…………..……..………. Default value = 8'h00

DPIHW1	DPIHW0	MTLLAMP1	MTLLAMP0	GMMENB	ENB20M	MTLBASE1	MTLBASE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 DPIHW [1:0]   To set CCD/CIS resolution.
        00   600 dpi
        01   1200 dpi
        10   2400 dpi
        11   4800 dpi

5-4 MTLLAMP [1:0]   Multiply coefficient for time-out counter of lamp.
        00   1* LAMPTIM
        01   2* LAMPTIM
        10   4* LAMPTIM
        11   Reserved

3 GMMENB   0   Disable gamma correction.
        1   Enable gamma correction.

2 ENB20M   0   CCD_CK1X output clocks according to designer's settings .
        1   CCD_CK1X generate 20MHz clock to CCD or CIS sensors.

1-0 MTLBASE [1:0]   To set output CCD pixel number under each system pixel time.
        00   1 CCD pixel/sstem pixel time.
        01   2 CCD pixel/sstem pixel time.
        10   3 CCD pixel/sstem pixel time.
        11   4 CCD pixel/sstem pixel time.

Offset 06h …………………………………………..…………..……..………. Default value = 8'h00

SCANMOD2	SCANMOD1	SCANMOD0	PWRBIT	GAIN4	OPTEST2	OPTEST1	OPTEST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5 SCANMOD [2:0]   To set operation mode.
        000   12 clocks/pixel ; normal mode operation for scanning.

<div style="margin-left:2em">

Color scanning : 24 bits image with gamma correction

Gray scanning : 8 bits image with gamma correction

16 bits image without gamma correction

Line art scanning : 1 bit image with gamma correction

001 12 clocks/pixel ; bypass mode operation for calibration.

Include color(pixel rate) , gray line-art.

010 8 clocks/pixel ; fast mode operation for scanning

Color scanning : 24 or 48 bits image with gamma correction for CIS

Gray scanning : 8 or 16 bits image with gamma correction for CIS or

CCD scanning.

011 Reserved

100 Reserved

101 Reserved

110 18 clocks/pixel.

Color scanning : 24 bits image with gamma correction

48 bits image without gamma correction

Gray scanning : 8 bits image with gamma correction

16 bits image without gamma correction

Line art scanning : 1 bit image with gamma correction

111 16 clocks/pixel.

Color scanning : 24 bits image with gamma correction

48 bits image without gamma correction

Gray scanning : 8 bits image with gamma correction

16 bits image without gamma correction

Line art scanning : 1 bit image with gamma correction

</div>

4 PWRBIT The hardware will reset this bit during power-on initial process. It can be set and checked by S/W to know if the power had been turned off or not.
Default is reset.

3 GAIN4 0 Digital shading gain=8 times system.
1 Digital shading gain=4 times system.
Note: If you want to get more precise image quality,you can set GAIN4 bit.

2-0 OPTEST [2:0] Select ASIC operation type.
000 Set normal mode to capture AFE image.
001 Set SDRAM bank testing and power-on moving testing for ASIC simulation
010 Pixel count pattern for ASIC image test.
011 Line count pattern for ASIC image test.
100 Counter and adder test for ASIC simulation test.
101 Reserved.
110 Reserved.
111 Reserved.

Offset 07h ……………………………………………..…………..……..………. Default value = 8'h00

LAMPSIM	RESERVE6	RESERVE5	RESERVE4	RESERVE3	RESERVE2	RESERVE1	RESERVE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 LAMPSIM for timer simulation

6-0 RESERVE [6:0] These bits are reserved for special application

Note: Please do not write other values than 00H into this register under normal condition.

Offset 08h ……………………………………………..…………..……..………. Default value = 8'h00

DRAM2X	SCNUMENB	MPENB	CIS_LINE	X	X	COLUMN	ENB24M
R/W	R/W	R/W	R/W	X	X	R/W	R/W

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7	**DRAM2X**	0 Select single chip of SDRAM
		1 Enable two chips of SDRAM
6	**SCNUMENB**	Enable page count which is stored in memory for ADF operation
5	**MPENB**	Enable motor phase generating function which is stored in memory
4	**CIS_LINE**	Set CIS_LINE to "1" and set CISSET to "1" at the same time to enable CIS scanning, and work on line by line mode.
1	**COLUMN**	Reserved
0	**ENB24M**	0 Disable 24MHz CCD/CIS Clock output
		1 Enable 24MHz CCD/CIS Clock output

Offset 09h ……………………………………………..………..…….….………. **Default value = 8'h00**

MCNTSET1	MCNTSET0	EVEN1ST	BLINE1ST	BACKSCAN	ENHANCE	SHORTTG	NWAIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6	**MCNTSET [1:0]**	To select the unit of motor table counter.
		00 Pixel count.
		01 System clock*2.
		10 System clock*3.
		11 System clock*4.
5	**EVEN1ST**	0 The first pixel of stagger CCD is located at odd sensor line.
		1 The first pixel of stagger CCD is located at even sensor line.
4	**BLINE1ST**	0 The first sensor of CCD is red line.
		1 The first sensor of CCD is blue line.
3	**BACKSCAN**	0 Select forward scanning function.
		1 Select backward scanning function.
2	**ENHANCE**	0 Select normal mode for embedded EPP interface.
		1 Select enhance mode for embedded EPP interface.
1	**SHORTTG**	0 Disable this function.
		1 Enable short CCD SH(TG) period for film scanning.
0	**NWAIT**	0 No delay for nWait.
		1 To delay nWait (H_BUSY) for one clock.

Offset 0Ah …………………………………………..…………..……..………. **Default value = 8'h00**

LCDSEL	LCMSEL	ADFSEL	LPWMEN	EPROMSEL	RS232SEL	BAUDRAT1	BAUDRAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	**LCDSEL**	0 Disable LCD display function.
		1 Enable LCD display function and the specific GPIOs are defined to drive LCD.
6	**LCMSEL**	0 Disable LCM display function.
		1 Enable LCM display function and the specific GPIOs are defined to drive LCM.
5	**ADFSEL**	0 Disable ADF function.
		1 Enable ADF function and the specific GPIOs are defined to drive ADF module.
4	**LPWMEN**	0 Disable ADF function.
		1 Enable PWM function of lamp.
3	**EPROMSEL**	0 Disable external EEPROM (93C46) interface.
		1 Enable external EEPROM (93C46) interface and the specific GPIOs are defined to connect EEPROM.
2	**RS232SEL**	0 Disable RS232 interface.
		1 Enable RS232 interface for special application and the specific GPIOs are defined to implement RS232 protocol.

1-0 BAUDRAT [1:0] Set boud rate of RS232.

                00   2400bps.
                01   4800bps.
                10   9600bps.
                11   19200bps.

Offset 0Bh ………………………………………..………..……..………. Default value = 8'h00

CLKSET2	CLKSET1	CLKSET0	RFHDIS	ENBDRAM	DRAMSEL2	DRAMSEL1	DRAMSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5 CLKSET [2:0] To select the system clock frequency.

                000   24MHz.
                001   30MHz.
                010   40MHz.
                011   48MHz.
                100   60MHz.
                101   Reserved.
                110   Reserved.
                111   Reserved.

4 RFHDIS   0   Enable auto-refresh mode for SDRAM.
                    1   Enable self-refresh mode for SDRAM.

3 ENBDRAM   A rising edge from low to high: to start power on sequence of SDRAM.

2-0 DRAMSEL [2:0] Select the SDRAM size.

                000   Reserved.
                001   16M bits.
                010   64M bist.
                011   128M bits.
                 100   256M bits.
                 101   512M bits.
                 110   1G bits.
                 111   Reserved.

Offset 0Ch ………………………………………..………..……..………. Default value = 8'h00

X	X	X	X	CCDLMT3	CCDLMT2	CCDLMT1	CCDLMT0
X	X	X	X	R/W	R/W	R/W	R/W

7-4 Reserved   -

3-0 CCDLMT [3:0] To set the lines count which is synchronized for CCD timing(like NEC8884).

Offset 0Dh

X	SCSYNC	CLRERR	FULLSTP	SEND	CLRMCNT	CLRDOCJM	CLRLNCNT
X	W	W	W	W	W	W	W

Command: Scanner command.

7 Reserved   -

6 SCSYNC   To synchronize base-clock and pixel-count for two chips operation

5 CLRERR   Reserved

4 FULLSTP   To reset steps type to full step.

3 SEND   To send the RS232 data.

---

2 CLRMCNT To clear FEDCNT(Reg48,Reg49,Reg4A) counter information.
1 CLRDOCJM To clear document jam message for ADF module.
0 CLRLNCNT To clear SCANCNT (Reg4B,Reg4C,Reg4D).

Note: 1.For each scanning, designers must clear SCANCNT before starting process.
2.They are write-one commands.

Offset 0Eh

SCANRESET
W

Command: Scanner software reset.

It can initiate AISC system including lamp and motor, control registers, internal circuit; but not including tables in DRAM, like gamma table, shading table and acceleration/deceleration table.

Note: In normal condition, it is unnecessary to reset scanner unless the scanner is out of control.

Offset 0Fh

MOVE
W

Command: Motor moving.

Start motor forward/backward moving.

Offset 10h …………………………………………..…………..……..…………. Default value = 8'h00

EXPR15	EXPR14	EXPR13	EXPR12	EXPR11	EXPR10	EXPR9	EXPR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPR [15:8] Exposure time setting (in pixel time) for Red-LED of CIS or Red channel of CCD.
Note: It cannot be programmed to logic zero.

Offset 11h …………………………………………..…………..……..…………. Default value = 8'h00

EXPR7	EXPR6	EXPR5	EXPR4	EXPR3	EXPR2	EXPR1	EXPR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPR [7:0] Exposure time setting (in pixel time) for Red-LED of CIS or Red channel of CCD.
Note: It cannot be programmed to logic zero.

Offset 12h …………………………………………..…………..……..…………. Default value = 8'h00

EXPG15	EXPG14	EXPG13	EXPG12	EXPG11	EXPG10	EXPG9	EXPG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPG [15:8] Exposure time setting (in pixel time) for Green-LED of CIS or Red channel of CCD.
Note: It cannot be programmed to logic zero.

Offset 13h …………………………………………..…………..……..…………. Default value = 8'h00

EXPG7	EXPG6	EXPG5	EXPG4	EXPG3	EXPG2	EXPG1	EXPG0

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPG [7:0]   Exposure time setting (in pixel time) for Green-LED of CIS or Red channel of CCD.

Note: It cannot be programmed to logic zero.

Offset 14h ……………………………………..………..……...………. Default value = 8'h00

EXPB15	EXPB14	EXPB13	EXPB12	EXPB11	EXPB10	EXPB9	EXPB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPB [15:8]   Exposure time setting (in pixel time) for Blue-LED of CIS or Red channel of CCD.

Note: It cannot be programmed to logic zero.

Offset 15h ……………………………………..………..……...………. Default value = 8'h00

EXPB7	EXPB6	EXPB5	EXPB4	EXPB3	EXPB2	EXPB1	EXPB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPB [7:0]   Exposure time setting (in pixel time) for Blue-LED of CIS or Red channel of CCD.

Note: It cannot be programmed to logic zero.

Offset 16h ……………………………………..………..……...………. Default value = 8'h32

CTRLHI	TOSHIBA	TGINV	CK1INV	CK2INV	CTRLINV	CKDIS	CTRLDIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 CTRLHI   0   CCD CP & RS will be low when TG goes high.
                        1   CCD CP & RS will be high when TG goes high.

6 TOSHIBA   0   Not TOSHIBA CIS.
                        1   To indicate the image sensor is TOSHIBA CIS.
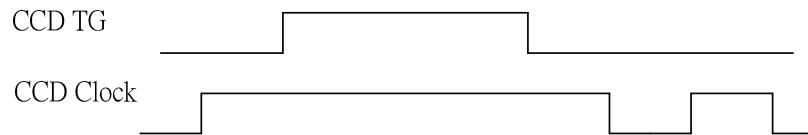
5 TGINV   0   Don't reverse.
                        1   To reverse CCD TG.

4 CK1INV   0   Don't reverse.
                        1   To reverse CCD Clock 1.
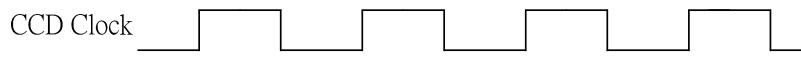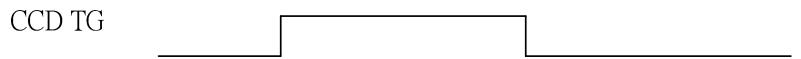
3 CK2INV   0   Don't reverse.
                        1   To reverse CCD Clock 2.

2 CTRLINV   0   Don't reverse.
                        1   To reverse CCD CP & RS.
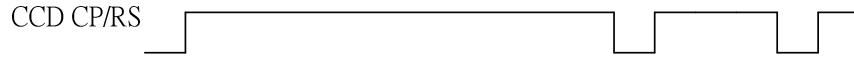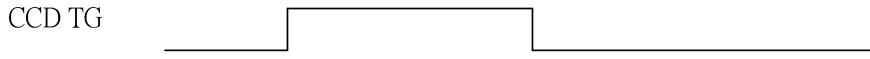
1 CKDIS   0   Disable clock1 and 2 under CCD TG position as illustrated.
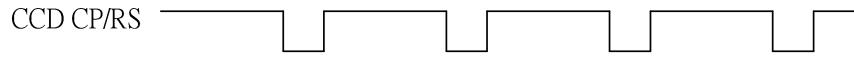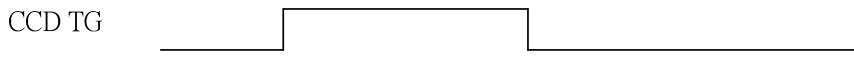
CCD TG

CCD Clock

                   0   Enable clock 1 and 2 under CCD TG position as illustrated.

CCD TG

CCD Clock

0   CTRLDIS   1   Disable CCD CP & RS signals under CCD TG position as illustrated.

CCD TG

CCD CP/RS

0   Enable CCD CP & RS signals under CCD TG position as illustrated.

CCD TG

CCD CP/RS

Offset 17h ……………………………………………..………..………..……. Default value = 8'h14

TGMODE1	TGMODE0	TGW5	TGW4	TGW3	TGW2	TGW1	TGW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 TGMODE [1:0] To set CCD TG mode.
   00   normal CCD TG type.
   01   CCD TG control with dummy line.
   10   CCD TG control with dummy lines for transparency scanning type.
   11   reserved for ASIC simulation.
5-0 TGW [5:0]   To set CCD TG plus width (in pixel time).
   Note: It cannot be programmed to logic zero.

Offset 18h …………………………………………..………..………..………. Default value = 8'h00

CNSET	DCKSEL1	DCKSEL0	CKTOGGLE	CKDELAY1	CKDELAY0	CKSEL1	CKSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7   CNSET   0   Select TG and clock to be non-Canon CIS style.
                     1   Select TG and clock to be Canon CIS style.
6-5 DCKSEL1 [1:0] 00   Speed 1: one CCD clock per system pixel time in shifting dummy lines.
                     01   Speed 2: two CCD clock per system pixel time in shifting dummy lines.
                     10   Speed 3: three CCD clock per system pixel time in shifting dummy lines.
                     11   Speed 4: four CCD clock per system pixel time in shifting dummy lines.
4   CKTOGGLE   0   One cycle per pixel.
                     1   Half cycle per pixel for CCD clock 1 & 2.
3-2 CKDELAY [1:0] 00   No delay
                     01   Delay one system clock for CCD Clock 1/2.
                     10   Delay two systems clock for CCD Clock 1/2.
                     11   Delay three systems clock for CCD Clock 1/2.
1-0 CKSEL [1:0] 00   Speed 1: one CCD clock per system pixel time in capturing image.
                     01   Speed 2: two CCD clock per system pixel time in capturing image.

10   Speed 3: three CCD clock per system pixel time in capturing image.
11   Speed 4: four CCD clock per system pixel time in capturing image.

Note: Speed limitation of CCD clock in different scanning modes:
    1. SCANMOD=0,1 : 12 clocks/pixel   a. toggle CCD : supports speed 1,2,3,4.
                                                    b. non-toggle CCD : supports speed 1,2,3.
    2. SCANMOD=2   : Reserved.
    3. SCANMOD=3   : Reserved.
    4. SCANMOD=4   : Reserved.
    5. SCANMOD=5   : Reserved.
    6. SCANMOD=6   : 18 clocks/pixel   a. toggle CCD : supports speed 1,2,3.
                                                    b. non-toggle CCD : supports speed 1,2,3,4.
    7. SCANMOD=7   : 16 clocks/pixel   a. toggle CCD : supports speed up 1,2,4.
                                                    b. non-toggle CCD : supports speed 1,2,4.
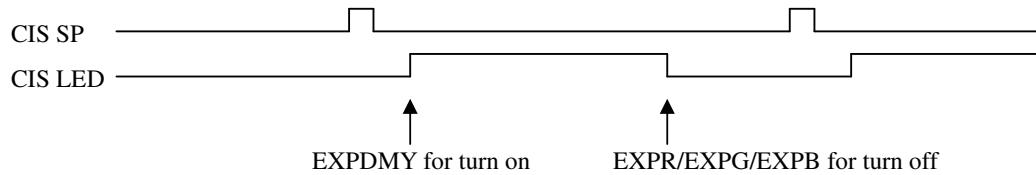
Note: Toggle CCD → CCD which can output one pixel in one half cycle of CCD clock.
        Non-toggle CCD → CCD which always output one pixel in one CCD clock cycle.

Offset 19h …….………………………………..………….…….……… Default value = 8'h00

EXPDMY7	EXPDMY6	EXPDMY5	EXPDMY4	EXPDMY3	EXPDMY2	EXPDMY1	EXPDMY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 EXPDMY[7:0]   To set exposure time of dummy lines (unit = 256 pixels time) or CIS LED
                              turn-on tme.

CIS SP

CIS LED

                  EXPDMY for turn on   EXPR/EXPG/EXPB for turn off
Note: It cannot be programmed to logic zero.

Offset 1Ah …….………………………………..………….…….……….. Default value = 8'h00

SW2SET	SW1SET	MANUAL3	MANUAL1	CK4INV	CK3INV	LINECLP	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	X

7 SW2SET   Set CCD SW2 output for special CCD control.

6 SW1SET   Set CCD SW1 output for special CCD control.

5 MANUAL3   0   CCD Clock 3,Clock4 automatic output.
                       1   CCD Clock 3,Clock4 manual output.

4 MANUAL1   0   CCD Clock 1,Clock2 automatic output.
                       1   CCD Clock 1,Clock2 manual output.

3 CK4INV   0   Don't reverse.
                       1   To reverse CCD Clock4.

2 CK3INV   0   Don't reverse.
                       1   To reverse CCD Clock 3.

1 LINECLP   0   To select CCD pixel clamping.
                       1   To select CCD line clamping.

Offset 1Bh …….…………………………………..………….…….…….…… Default value = 8'h00

GRAYSET	CHANSEL	BGRENB	ICGENB	ICGDLY3	ICGDLY2	ICGDLY1	ICGDLY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	GRAYSET	0	Select single channel output.
		1	Select two channel output.
6	CHANSEL	0	Fast true gray latch is 2 and 3 position.
		1	Fast true gray latch is 1 and 2 position.
5	BGRENB	0	The order is R-G-B.
		1	The order of latching A/D data is B-G-R.
4	ICGENB	0	To disable ICG control.
		1	To enable CCD shutter control signal ICG.
3-0	ICGDLY [3:0]		CCD ICG delay for rising/falling edge.

Offset 1Ch …....……………………………………..………....…....………. Default value = 8'h00

CK4MTGL	CK3MTGL	CK1MTGL	CKAREA	MTLWD	TGTIME2	TGTIME1	TGTIME0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	CK4MTGL	0	Disable toggle function in CCD clock 4.
		1	Enable toggle function in CCD clock 4.
6	CK3MTGL	0	Disable toggle function in CCD clock 3.
		1	Enable toggle function in CCD clock 3.
5	CK1MTGL	0	Disable toggle function in CCD clock 1 & 2.
		1	Enable toggle function in CCD clock 1 &2.
4	CKAREA	0	This function is disabled.
		1	CCD clock speed depends on CKSEL in scan area and DCKSEL in non-scan area.
3	MTLWD	0	Set the watchdog time-out as WDTIME[3:0].
		1	Set the watchdog time-out as WDTIME[3:0] * 2.
2-0	TGTIME [2:0]		CCD line period selection.
		000	1*LPERIOD(Reg38,Reg39)
		001	2*LPERIOD
		010	4*LPERIOD
		011	8*LPERIOD
		100	16*LPERIOD
		101	32*LPERIOD
		110	Reserved.
		111	Reserved.

Offset 1Dh …....……………………………………..………....…....………. Default value = 8'h04

CK4LOW	CK3LOW	CK1LOW	TGSHLD4	TGSHLD3	TGSHLD2	TGSHLD1	TGSHLD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	CK4LOW	0	Clock 4 will be high when TG goes high.
		1	Clock 4 will be low when TG goes high.
6	CK3LOW	0	Clock 3 will be high when TG goes high.
		1	Clock 3 will be low when TG goes high.
5	CK1LOW	0	Clock 1 & 2 will be high when TG goes high.
		1	Clock 1 & 2 will be low when TG goes high.

4-0 TGSHLD [4:0] CCD TG shoulder width (in pixel time). Please refer to Reg34.

Note: Designers have to program the TGSHLD >= 2 (more than two).

Offset 1Eh ……...……….......…..……….. Default value = 8'h20

WDTIME3	WDTIME2	WDTIME1	WDTIME0	LINESEL3	LINESEL2	LINESEL1	LINESEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-4 WDTIME [3:0] To set watch-dog time.
The unit is 30 seconds.

3-0 LINESEL [3:0] To set vertical resolution for CIS or dummy lines for CCD.

CIS : LINESEL = 0   full resolution.
= 1   1/2 resolution.
= 2   1/3 resolution .
…..
= 15   1/16 resolution.
CCD : LINESEL = 0   no dummy line.
= 1   1 dummy line.
= 2   2 dummy lines.
…..
= 15   15 dummy lines.

Note: In contrary to dummy line feature in CCD, for low resolution in CIS, the
scanning speed is improved by implementing fast motor moving.

Offset 1Fh ……...……….......…..…….… Default value = 8'h00

SCANFED7	SCANFED6	SCANFED5	SCANFED4	SCANFED3	SCANFED2	SCANFED1	SCANFED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 SCANFED [7:0] Steps number setting for moving to scanning position.
Please refer to description of Reg6A
Note: 1.it cannot be programmed to logic zero.
2.it can be multiplied by$2*^{STEPTIM}$

Offset 20h ……...……….......…..…….… Default value = 8'h00

BUFSEL7	BUFSEL6	BUFSEL5	BUFSEL4	BUFSEL3	BUFSEL2	BUFSEL1	BUFSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BUFSEL [7:0] To set buffer condition.
When buffer is full, scanner will stop and wait for host to read out image data
from SDRAM.
The valid data count (has not been read) is represented by VALIDWORD (in word).
If VALIDWORD < buffer condition, then the scanner will re-start to scan.

Following are the units of this register under various SDRAM size.
16M bits SDRAM   : 4k words
64M bits SDRAM   : 16k words
128M bits SDRAM   : 32K words
256M bits SDRAM   : 64K words
512M bits SDRAM   : 128K words

Offset 21h ……...……….......…..…….… Default value = 8'h00

STEPNO7	STEPNO6	STEPNO5	STEPNO4	STEPNO3	STEPNO2	STEPNO1	STEPNO0

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 STEPNO [7:0] Steps number of "table one" for the acceleration/deceleration of scanning moving.
Please refer to section 6.19 and the descriptions of Reg24 & Reg6A.
Note: 1.It cannot be programmed to logic zero.
2.it can be multiplied by2*^{STEPTIM}

Offset 22h …...……………………………………..…………..…….…..….…… Default value = 8'h00

FWDSTEP7	FWDSTEP6	FWDSTEP5	FWDSTEP4	FWDSTEP3	FWDSTEP2	FWDSTEP1	FWDSTEP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FWDSTEP [7:0] Steps number for forward moving when buffer condition is met.
Please refer to section 6.19 and the descriptions of Reg20 & Reg24.
Note: 1.It cannot be programmed to logic zero.
2.it can be multiplied by2*^{STEPTIM}

Offset 23h …...……………………………………..…………..…….…..….…… Default value = 8'h00

BWDSTEP7	BWDSTEP6	BWDSTEP5	BWDSTEP4	BWDSTEP3	BWDSTEP2	BWDSTEP1	BWDSTEP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BWDSTEP [7:0] Steps number for backward moving when image buffer is full.
Please refer to section 6.19 and the descriptions of Reg24.
Note: 1.It cannot be programmed to logic zero.
2.it can be multiplied by2*^{STEPTIM}
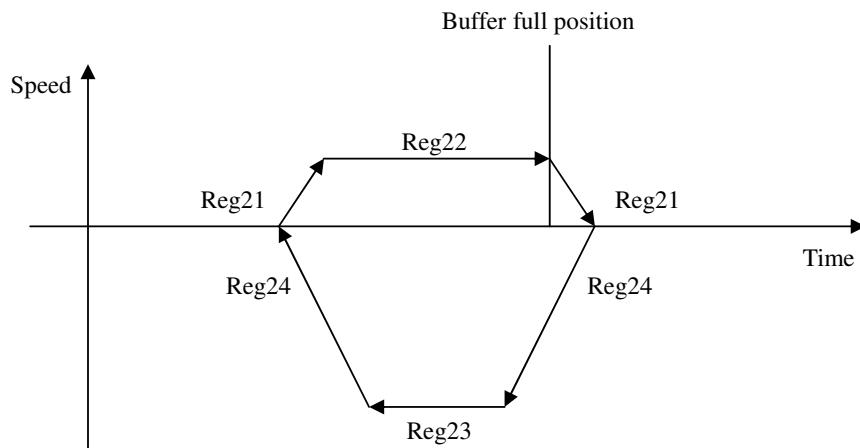
Offset 24h …...……………………………………..…………..…….…..….…… Default value = 8'h00

FASTNO7	FASTNO6	FASTNO5	FASTNO4	FASTNO3	FASTNO2	FASTNO1	FASTNO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FASTNO [7:0] Steps number of "table two" for the acceleration/deceleration when image buffer is full.
Please refer to section 6.19 and the descriptions of Reg20.
Note: It cannot be programmed to logic zero.

Offset 25h …….…..………………………….………..……….……….…. **Default value = 8'h00**

X	X	X	X	LINCNT19	LINCNT18	LINCNT17	LINCNT16
X	X	X	X	R/W	R/W	R/W	R/W

  7-4 RESERVED -

  3-0 LINCNT [19:16] Scanning lines count specified by designers.
                         Note: It cannot be programmed to logic zero.

Offset 26h …….…..………………………….………..……….……….…. **Default value = 8'h00**

LINCNT15	LINCNT14	LINCNT13	LINCNT12	LINCNT11	LINCNT10	LINCNT9	LINCNT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

  7-0 LINCNT [15:8] Scanning lines count specified by designers.
                       Note: It cannot be programmed to logic zero.

Offset 27h …….…..………………………….………..……….……….…. **Default value = 8'h00**

LINCNT7	LINCNT6	LINCNT5	LINCNT4	LINCNT3	LINCNT2	LINCNT1	LINCNT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

  7-0 LINCNT [7:0] Scanning lines count specified by designers.
                       Note: It cannot be programmed to logic zero.

Offset 2Ch …….…..………………………….………..……….……….…. **Default value = 8'h00**

X	X	DPISET13	DPISET12	DPISET11	DPISET10	DPISET9	DPISET8
X	X	R/W	R/W	R/W	R/W	R/W	R/W

  7-5 RESERVED -

  4-0 DPISET [13:8] Set resolution in dpi for average or deletion type.
               A. average type : digital average function support 1/2,1/3,1/4,1/5,1/6,1/8,1/10,1/12,1/15.
                   a. 9600 dpi mode CCD:support 4800,3200,2400,1920,1600,1200,960,800,640 dpi.
                   b. 4800 dpi mode CCD:support 2400,1600,1200,960,800,480,400,320 dpi.
                   c. 2400 dpi mode CCD:support 1200,800,600,480,400,300,240,200,160 dpi.
                   d. 1200 dpi mode CCD:support 600,400,300,240,200,150,120,100,80 dpi.
                   e. 600 dpi mode CCD:support 300,200,150,120,100,75,60,50,40 dpi.
              B. deletion type : 9600,4800,2400,1200 or 600dpi to 1 dpi setting decrement by
              one dpi.
              Note: It cannot be programmed to logic zero.

Offset 2Dh …….…..………………………….………..……….……….…. **Default value = 8'h00**

DPISET7	DPISET6	DPISET5	DPISET4	DPISET3	DPISET2	DPISET1	DPISET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

  7-0 DPISET [7:0] Set resolution in dpi for average or deletion type.
              A. average type : digital average function support 1/2,1/3,1/4,1/5,1/6,1/8,1/10,1/12,1/15.
                   a. 9600 dpi mode CCD:support 4800,3200,2400,1920,1600,1200,960,800,640 dpi.
                   b. 4800 dpi mode CCD:support 2400,1600,1200,960,800,480,400,320 dpi.
                   c. 2400 dpi mode CCD:support 1200,800,600,480,400,300,240,200,160 dpi.
                   d. 1200 dpi mode CCD:support 600,400,300,240,200,150,120,100,80 dpi.
                   e. 600 dpi mode CCD:support 300,200,150,120,100,75,60,50,40 dpi.
              B. deletion type : 9600,4800,2400,1200 or 600dpi to 1 dpi setting decrement by

one dpi.
Note: It cannot be programmed to logic zero.

Offset 2Eh …….……...................................…..……...........…..….…… **Default value = 8'h00**
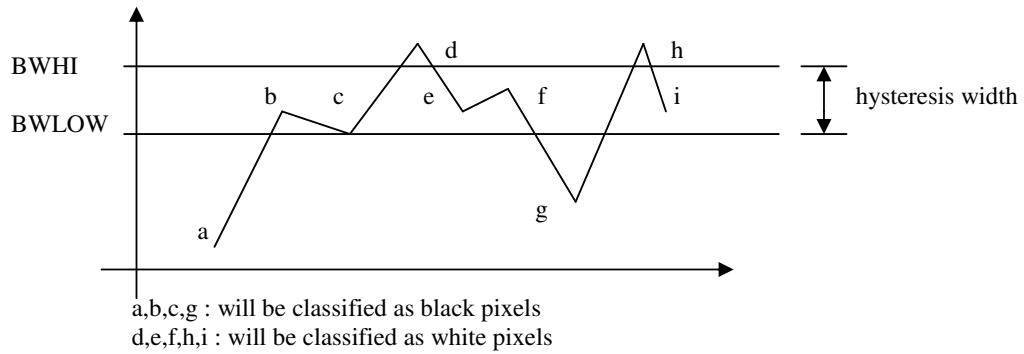
BWHI7	BWHI6	BWHI5	BWHI4	BWHI3	BWHI2	BWHI1	BWHI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BWHI [7:0]　　　　High level of Black & White threshold.

Offset 2Fh …….……...................................…..……...........…..….…… **Default value = 8'h00**

BWLOW7	BWLOW6	BWLOW5	BWLOW4	BWLOW3	BWLOW2	BWLOW1	BWLOW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 BWLOW [7:0]　Low level of Black & White threshold.

a,b,c,g : will be classified as black pixels
d,e,f,h,i : will be classified as white pixels

Offset 30h …….……...................................…..……...........…..….…… **Default value = 8'h00**

STRPIXEL15	STRPIXEL14	STRPIXEL13	STRPIXEL12	STRPIXEL11	STRPIXEL10	STRPIXEL9	STRPIXEL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 STRPIXEL [15:8] The start pixel position of horizontal line (unit : pixel count).
　　　　　　　　　STRPIXEL=(TGW+2*TGSHLD)+start pixels number (count from CCD pixel 0)
　　　　　　　　　Note: 1.It cannot be programmed to logic zero.
　　　　　　　　　　　　2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.

Offset 31h …….……...................................…..……...........…..….…… **Default value = 8'h00**

STRPIXEL7	STRPIXEL6	STRPIXEL5	STRPIXEL4	STRPIXEL3	STRPIXEL2	STRPIXEL1	STRPIXEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 STRPIXEL [7:0] The start pixel position of horizontal line (unit : pixel count).
　　　　　　　　　STRPIXEL=(TGW+2*TGSHLD)+start pixels number (count from CCD pixel 0)
　　　　　　　　　Note: 1.It cannot be programmed to logic zero.
　　　　　　　　　　　　2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.

Offset 32h …….……...................................…..……...........…..….…… **Default value = 8'h00**

ENDPIXEL15	ENDPIXEL14	ENDPIXEL13	ENDPIXEL12	ENDPIXEL11	ENDPIXEL10	ENDPIXEL9	ENDPIXEL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 **ENDPIXEL [15:8]** The end pixel position of horizontal line (unit : pixel count).

> ENDPIXEL=(TGW+2*TGSHLD)+end pixels number (count from CCD pixel 0)
> Note: 1.It cannot be programmed to logic zero.
> 2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.

Offset 33h …….………………………………..………..….…..….…… **Default value = 8'h00**

ENDPIXEL7	ENDPIXEL6	ENDPIXEL5	ENDPIXEL4	ENDPIXEL3	ENDPIXEL2	ENDPIXEL1	ENDPIXEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 **ENDPIXEL [7:0]** The end pixel position of horizontal line (unit : pixel count).

> ENDPIXEL=(TGW+2*TGSHLD)+end pixels number (count from CCD pixel 0)
> Note: 1.It cannot be programmed to logic zero.
> 2.If the DPI9600 control bit is set to "1",the STRPIXEL is doubled.
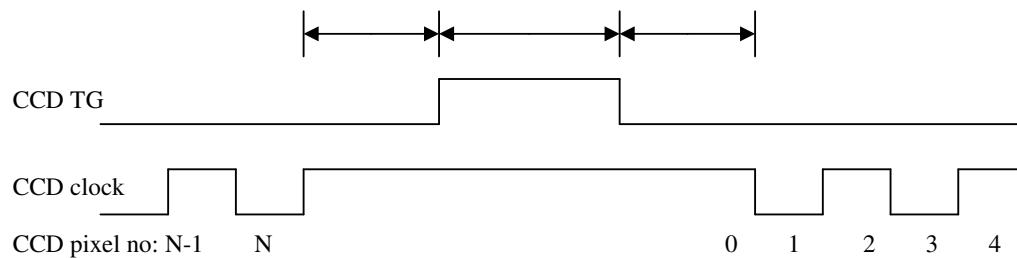
Offset 34h …….………………………………..………..….…..….…… **Default value = 8'h00**

DUMMY7	DUMMY6	DUMMY5	DUMMY4	DUMMY3	DUMMY2	DUMMY1	DUMMY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 **DUMMY [7:0]** The CCD dummy & optical black pixels number (unit : pixel count).

> Note: It cannot be programmed to logic zero.
>
> Setting rule of Reg30,31,32,33 and 34.

For example, start pixel is 65 ,end pixel is 100 and CCD dummy pixel is 64,
Then STRPIXEL = (TGW+2*TGSHLD) + 65.
ENDPIXEL= (TGW+2*TGSHLD) + 100.
DUMMY = (TGW+2*TGSHLD) + 64.

Offset 35h …….………………………………..………..….…..….…… **Default value = 8'h00**

MAXWD25	MAXWD24	MAXWD23	MAXWD22	MAXWD21	MAXWD20	MAXWD19	MAXWD18
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 **MAXWD [25:18]** Maximum word size per line for ASIC estimation. The unit is 4 words.
> If available buffer size < MAXWD, then "buffer full" state will be set. The scanner execute backtracking.

Offset 36h …….………………………………..………..….…..….…… **Default value = 8'h00**

MAXWD17	MAXWD16	MAXWD15	MAXWD14	MAXWD13	MAXWD12	MAXWD11	MAXWD10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 **MAXWD [17:10]** Maximum word size per line for ASIC estimation. The unit is 4 words.

If available buffer size < MAXWD, then "buffer full" state will be set. The
scanner execute backtracking.

Offset 37h …….…..………………….……..………..………..………..……..…. **Default value = 8'h00**

MAXWD9	MAXWD8	MAXWD7	MAXWD6	MAXWD5	MAXWD4	MAXWD3	MAXWD2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

 7-0 **MAXWD [9:2]**   Maximum word size per line for ASIC estimation. The unit is 4 words.
                       If available buffer size < MAXWD, then "buffer full" state will be set. The
                       scanner execute backtracking.

Offset 38h …….…..………………….……..………..………..………..……. **Default value = 8'h2A**

LPERIOD15	LPERIOD14	LPERIOD13	LPERIOD12	LPERIOD11	LPERIOD10	LPERIOD9	LPERIOD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

 7-0 **LPERIOD [15:8]** Line period (or exposure time) for CCD or CIS.
                        Unit : pixel count
                        Note: It cannot be programmed to logic zero.

Offset 39h …….…..………………….……..………..…………..……………. **Default value = 8'h30**

LPERIOD7	LPERIOD6	LPERIOD5	LPERIOD4	LPERIOD3	LPERIOD2	LPERIOD1	LPERIOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

 7-0 **LPERIOD [7:0]** Line period (or exposure time) for CCD or CIS.
                       Unit : pixel count
                       Note: It cannot be programmed to logic zero.

Offset 3Ah

X	X	X	X	X	X	X	FEWRDATA8
X	X	X	X	X	X	X	W

 7-1 **RESERVED**   -
  0 **FEWRDATA [8]** This port is for designers to write control register of front-end.

Offset 3Bh

FEWRDATA7	FEWRDATA6	FEWRDATA5	FEWRDATA4	FEWRDATA3	FEWRDATA2	FEWRDATA1	FEWRDATA0
W	W	W	W	W	W	W	W

 7-0 **FEWRDATA [7:0]** This port is for designers to write control register of front-end.

Offset 3Dh …….…..…..………………….……..………..………..……..……..… **Default value = 8'h00**

X	X	X	X	FEEDL19	FEEDL18	FEEDL17	FEEDL16
X	X	X	X	R/W	R/W	R/W	R/W

 7-4 **RESERVED**   -
 3-0 **FEEDL [19:16]** Steps number of motor moving.

Note: It cannot be programmed to logic zero.

Offset 3Eh …….….…..….……..….……..….……..….…..….…… **Default value = 8'h00**

FEEDL15	FEEDL14	FEEDL13	FEEDL12	FEEDL11	FEEDL10	FEEDL9	FEEDL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FEEDL [15:8]   Steps number of motor moving.
Note: It cannot be programmed to logic zero.

Offset 3Fh …….….…..….……..….……..….……..….…..….…… **Default value = 8'h00**

FEEDL7	FEEDL6	FEEDL5	FEEDL4	FEEDL3	FEEDL2	FEEDL1	FEEDL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FEEDL [7:0]   Steps number of motor moving.
Note: It cannot be programmed to logic zero.

Offset 40h

DOCSNR	ADFSNR	COVERSNR	CHKVER	DOCJAM	HISPDFLG	MOTMFLG	DATAENB
R	R	R	R	R	R	R	R

7 DOCSNR   Respond to document sensor status for ADF function.
6 ADFSNR   Respond to ADF sensor status for ADF function.
5 COVERSNR   Respond to cover sensor status for ADF function.
4 CHKVER   It is fixed to '1' to indicate that the value in Reg00 is valid.
3 DOCJAM   Respond to document feeding status for ADF function.
       0   No jam happened.
       1   Document jammed.
2 HISPDFLG   0   Motor is not in high-speed moving.
       1   Motor is in high-speed moving.
1 MOTMFLG   0   Motor is stop.
       1   Motor is moving.
0 DATAENB   0   Scanner is in command mode. Designers can access other data in SDRAM
          rather than image data.
       1   Scanner is in scanning mode. Designers can only read the image data.

Offset 41h

PWRBIT	BUFEMPTY	FEEDFSH	SCANFSH	HOMESNR	LAMPSTS	FEBUSY	MOTORENB
R	R	R	R	R	R	R	R

7 PWRBIT   To indicate power status. If it is reset, the power had been turned off.
Power on initial process will set PWRBIT to 0. This bit will have the same value
as bit 4 of Reg06 except for it's read only.
6 BUFEMPTY   0   The image buffer is not empty.
       1   The image buffer is empty.
5 FEEDFSH   0   Motor feeding is not finished.
       1   Motor feeding is finished.
4 SCANFSH   0   Scanning is not finished.
       1   Scanning is finished.

3	HOMESNR	0	Home sensor is on (is not located in home position).
		1	Home sensor is off (located in home position).
2	LAMPSTS	0	Lamp is off.
		1	Llamp is on.
1	FEBUSY	0	Front end is ready for read/write operations.
		1	Front end is busy and can not perform read/write operations.
0	MOTORENB	0	Motor is not operation.
		1	Motor is operation.

Offset 42h …….….…………..……….…………..…………..……….….……..………… **Default value = 8'h00**

X	X	X	X	X	X	VALIDWORD 25	VALIDWORD 24
X	X	X	X	X	X	R	R

1-0 VALIDWORD [25:24] The available image data stored in SDRAM for host to read. The unit is in word.

Offset 43h …….….…………..……….…………..…………..……….….……..………… **Default value = 8'h00**

VALIDWORD 23	VALIDWORD 22	VALIDWORD 21	VALIDWORD 20	VALIDWORD 19	VALIDWORD 18	VALIDWORD 17	VALIDWORD 16
R	R	R	R	R	R	R	R

7-0 VALIDWORD [23:16] The available image data stored in SDRAM for host to read. The unit is in word.

Offset 44h …….….…………..……….…………..…………..……….….……..………… **Default value = 8'h00**

VALIDWORD 15	VALIDWORD 14	VALIDWORD 13	VALIDWORD 12	VALIDWORD 11	VALIDWORD 10	VALIDWORD 9	VALIDWORD 8
R	R	R	R	R	R	R	R

7-0 VALIDWORD [15:8] The available image data stored in SDRAM for host to read. The unit is in word.

Offset 45h

VALIDWORD 7	VALIDWORD 6	VALIDWORD 5	VALIDWORD 4	VALIDWORD 3	VALIDWORD 2	VALIDWORD 1	VALIDWORD 0
R	R	R	R	R	R	R	R

7-0 VALIDWORD [7:0] The available image data stored in SDRAM for host to read. The unit is in word.

Offset 46h

X	X	X	X	X	X	X	FERDDATA8
X	X	X	X	X	X	X	R

7-1 RESERVED -

0 FERDDATA [8] This port is for designers to read control register from front-end.

Offset 47h

FERDDATA7	FERDDATA6	FERDDATA5	FERDDATA4	FERDDATA3	FERDDATA2	FERDDATA1	FERDDATA0
R	R	R	R	R	R	R	R

7-0 FERDDATA [7:0] This port is for designers to read control register from front-end.

Offset 48h …….…….……….……..……….…………..……….…..……….… **Default value = 8'h00**

X	X	X	FEDCNT20	FEDCNT19	FEDCNT18	FEDCNT17	FEDCNT16
X	X	X	R	R	R	R	R

7-5 RESERVED   -
4-0 FEDCNT [20:16] Steps number which motor has moved.

> For example, after setting the moving steps number (Reg 3D, 3E 3F) and execute the moving command (Reg 0F), designers can get steps number which has been moved via these registers. It can be reset to zero by CLRMCNT command.
> The unit is in quarter step.

Offset 49h …….…….……….……..……….…………..……….…..……….… **Default value = 8'h00**

FEDCNT15	FEDCNT14	FEDCNT13	FEDCNT12	FEDCNT11	FEDCNT10	FEDCNT9	FEDCNT8
R	R	R	R	R	R	R	R

7-0 FEDCNT [15:8] Steps number which motor has moved.

Offset 4Ah …….…….……….……..……….…………..……….…..……….… **Default value = 8'h00**

FEDCNT7	FEDCNT6	FEDCNT5	FEDCNT4	FEDCNT3	FEDCNT2	FEDCNT1	FEDCNT0
R	R	R	R	R	R	R	R

7-0 FEDCNT [7:0]   Steps number which motor has moved.

Offset 4Bh …….…….……….……..……….…………..……….…..……….… **Default value = 8'h00**

X	X	X	X	SCANCNT19	SCANCNT18	SCANCNT17	SCANCNT16
X	X	X	X	R	R	R	R

7-4 RESERVED   -
3-0 SCANCNT [19:16] Line number which scanner has finished.

> For example, after setting the line number (Reg 25, 26 27) and execute the scanning enable (bit 0 of Reg 01), designers can get line number which has been finished via these registers. It can be reset to zero by CLRLNCNT command.

Offset 4Ch …….…….……….……..……….…………..……….…..……….… **Default value = 8'h00**

SCANCNT15	SCANCNT14	SCANCNT13	SCANCNT12	SCANCNT11	SCANCNT10	SCANCNT9	SCANCNT8
R	R	R	R	R	R	R	R

7-0 SCANCNT [15:8] Line number which scanner has finished.

Offset 4Dh …….…….……….……..……….…………..……….…..……….… **Default value = 8'h00**

SCANCNT7	SCANCNT6	SCANCNT5	SCANCNT4	SCANCNT3	SCANCNT2	SCANCNT1	SCANCNT0
R	R	R	R	R	R	R	R

7-0 SCANCNT [7:0] Line number which scanner has finished.

Offset 4Fh

SPI_M_BSY	SLAVEERR	DOGON	ROMBSY	LCMBSY	TX232BSY	RX232BSY	RXREADY
R	R	R	R	R	R	R	R

7 SPI_M_BSY Indicate that the SPI data output is busy or not when SPI_MOT is set to "1" and work on 3972 of motor driver IC.

6 SLAVEERR **Reserved**

5 DOGON
  0 Lamp dog hasn't occurred
  1 Lamp dog has occurred

4 ROMBSY
  0 EEPROM is ready for access.
  1 EEPROM (93C46) is busy and can not be accessed.

3 LCMBSY
  0 LCM interface is ready for access.
  1 LCM interface is busy and can not be accessed.

2 TX232BSY
  0 RS232 transmitter is ready for access.
  1 RS232 transmitter is busy and can not be accessed.

1 RX232BSY
  0 RS232 receiver is ready for access.
  1 RS232 receiver is busy and can not be accessed.

0 RXREADY
  0 The receiving has not been completed.
  1 Has received data number specified in Reg 88 from RS232.

Offset 50h …….…..……….…….…….…...………..………..…….…...….……… **Default value = 8'h00**

X	X	FERDA5	FERDA4	FERDA3	FERDA2	FERDA1	FERDA0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED   -

5-0 FERDA [5:0] Address of control register of front-end in read operation.
Before reading control register of front-end (Reg 46, 47), designers have to
specify address of the control register by writing address to this port.

Offset 51h …….…..……….…….…….…...………..………..…….….……..……… **Default value = 8'h00**

X	X	FEWRA5	FEWRA4	FEWRA3	FEWRA2	FEWRA1	FEWRA0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED   -

5-0 FEWRA [5:0] Address of control register of front-end in write operation.
Before writing control register of front-end (Reg 3A, 3B), designers have to
specify address of the control register by writing address to this port.

Offset 52h …….…..……….…….…….…...………..………..…….……..……… **Default value = 8'h00**

X	X	X	RHI4	RHI3	RHI2	RHI1	RHI0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -

4-0 RHI [4:0]   The latch point for high-byte of R channel of AFE in every pixel.
For example, if a system is designed to have 12 clocks/pixel, and designer wants
to latch the high-byte of R channel at 1'st clock in every pixel, designer has to fill
'00001' to RHI [4:0].

Offset 53h …….…..…..….…….……….…….…..…………….…..….…..… Default value = 8'h00

X	X	X	RLOW4	RLOW3	RLOW2	RLOW1	RLOW0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -

4-0 RLOW [4:0]   The latch point for low-byte of R channel of AFE in every pixel
For example, if a system is designed to have 12 clocks/pixel, and designer wants
to latch the high-byte of R channel at 1'st clock in every pixel, designer has to fill
'00001' to RHI [4:0].

Offset 54h …….…..…..….…….……….…….…..…………….…..….…..… Default value = 8'h00

X	X	X	GHI4	GHI3	GHI2	GHI1	GHI0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -

4-0 GHI [4:0]   The latch point for high-byte of G channel of AFE in every pixel.

Offset 55h …….…..…..….…….……….…….…..…………….…..….…..… Default value = 8'h00

X	X	X	GLOW4	GLOW3	GLOW2	GLOW1	GLOW0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -

4-0 GLOW [4:0]   The latch point for low-byte of G channel of AFE in every pixel.

Offset 56h …….…..…..….…….……….…….…..…………….…..….…..… Default value = 8'h00

X	X	X	BHI4	BHI3	BHI2	BHI1	BHI0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -

4-0 BHI [4:0]   The latch point for high-byte of B channel of AFE in every pixel.

Offset 57h …….…..…….……….…….…..…….…………….…..….…..… Default value = 8'h00

X	X	X	BLOW4	BLOW3	BLOW2	BLOW1	BLOW0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -

4-0 BLOW [4:0]   The latch point for low-byte of B channel of AFE in every pixel.

(1). Color, gray or line-art : 12 clocks (phase)/pixel mode

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

R[15:8] R[7:0] G[15:8] G[7:0] B[15:8] B[7:0] R[15:8] R[7:0] G[15:8] G[7:0] B[15:8]

RHI = 01H RLOW = 03H
GHI = 05H GLOW = 07H
BHI = 09H BLOW = 11H
Note: 16 clocks (phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12
    clocks(phase)/pixel mode.

Offset 58h …….……..…………….…………..…………..…………..……..…… Default value = 8'h00

VSMP4	VSMP3	VSMP2	VSMP1	VSMP0	VSMPW2	VSMPW1	VSMPW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
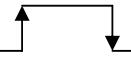
7-3 **VSMP [4:0]**   Rising edge position of image sampling for AFE.

2-0 **VSMPW [2:0]**   Pulse width of image sampling.

(1). Color, gray or line-art : 12 clocks (phase)/pixel mode

| 5 | 6 | 7 | 8 | 9 | 10 | 11 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 0 | 1 | 2 | 3 | 4 |

AFE   VSMP

Reg58=52H : VSMP[4:0]=10H   VSMPW[2:0]=2H
Note: 16 clocks (phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12
    clocks(phase)/pixel mode.

Offset 59h …….……..…………….…………..…………..…………..……..…… Default value = 8'h00

BSMP4	BSMP3	BSMP2	BSMP1	BSMP0	BSMPW2	BSMPW1	BSMPW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
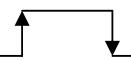
7-3 **BSMP [4:0]**   Rising edge position of dark voltage sampling for AFE.

2-0 **BSMPW [2:0]**   Pulse width of dark voltage sampling.

(1). Color, gray or line-art : 12 clocks (phase)/pixel mode

| 5 | 6 | 7 | 8 | 9 | 10 | 11 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 0 | 1 | 2 | 3 | 4 |

AFE   BSMP

Reg59=52H : BSMP[4:0]=10H   BSMPW[2:0]=2H
Note: 16 clocks (phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12
    clocks(phase)/pixel mode.

Offset 5Ah …….……..…………….…………..…………..……….……..……..…… Default value = 8'h00

ADCLKINV	RLCSEL	CDSREF1	CDSREF0	RLC3	RLC2	RLC1	RLC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 **ADCLKINV**   0 ADC clock in not reversed.

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1   ADC clock is reversed.

6   RLCSEL   0   Do not select.
                     1   Select reset level clamp on a pixel-by-pixel basis.

5-4   CDSREF [1:0]   Front-end CDS reference for line rate scanning type.

3-0   RLC [3:0]   Front-end RLC for line rate scanning type.

Offset 5Dh …….……….………..………..………..……..……..…..…..… Default value = 8'h00

HISPD7	HISPD6	HISPD5	HISPD4	HISPD3	HISPD2	HISPD1	HISPD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   HISPD [7:0]   To change of the speed of motor during moving
                        Note: It cannot be programmed to logic zero.

Offset 5Eh …….……….………..……..………..……..……..…..…..… Default value = 8'h00

DECSEL2	DECSEL1	DECSEL0	STOPTIM4	STOPTIM3	STOPTIM2	STOPTIM1	STOPTIM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5   DECSEL [2:0]   Deceleration steps number after touching home sensor.
                         000   1 steps deceleration
                         001   2 steps deceleration
                         010   4 steps deceleration
                         011   8 steps deceleration
                         100   16 steps deceleration
                         101   32 steps deceleration
                         110   64 steps deceleration
                         111   128 steps deceleration

4-0   STOPTIM [4:0]   Stop time between forward and backward direction in backtracking.

   Note: In ASIC simulation process, STOPTIM has to be set to tgtime=6,7.
          It cannot be programmed to logic zero.

Offset 5Fh …….………………..………..………..………..……..… Default value = 8'h00

FMOVDEC7	FMOVDEC6	FMOVDEC5	FMOVDEC4	FMOVDEC3	FMOVDEC2	FMOVDEC1	FMOVDEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   FMOVDEC [7:0]   Deceleration steps in table 5 for auto-go-home.
                          Note: 1.It cannot be programmed to logic zero.
                                2.It can be multiplied by $2 *^{STEPTIM}$

Offset 60h …….………………..………..………..………..……..… Default value = 8'h20

STEPSEL2	STEPSEL1	STEPSEL0	Z1MOD20	Z1MOD19	Z1MOD18	Z1MOD17	Z1MOD16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5   STEPSEL [2:0]   For type selection of table one, table two and table three in scanning mode.
                          (1) For bipolar motors:
                              000   Full step (for 1939, 1940, 2916, 6219, 3955, 3967).
                              001   Half step (for 1939, 1940, 2916, 6219, 3955, 3967).
                              010   Quarter step (for 2916, 6219, 3955, 3967).
                              011   Eighth step (for 3955, 3967).
                              100   Sixteenth step (for 3972)

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(2) For unipolar motors:
- 000   Two-phase-on full step.
- 001   Half step.
- 010   Reserved.
- 011   Single-phase-on full step.
- 100   Reserved.

4-0   Z1MOD [20:16]   "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when buffer-full occurs.
Note: It should be less than LPERIOD.

Offset 61h …….……………………..………..…………..…….…..…….….… **Default value = 8'h00**

Z1MOD15	Z1MOD14	Z1MOD13	Z1MOD12	Z1MOD11	Z1MOD10	Z1MOD7	Z1MOD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   Z1MOD [15:8]   "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when buffer-full occurs.
Note: It should be less than LPERIOD.

Offset 62h …….………………..………..…….…………..…….…..…….….… **Default value = 8'h00**

Z1MOD7	Z1MOD6	Z1MOD5	Z1MOD4	Z1MOD3	Z1MOD2	Z1MOD1	Z1MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   Z1MOD [7:0]   "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when buffer-full occurs.
Note: It should be less than LPERIOD.

Offset 63h …….………………..………..…….…………..…….…..…….….… **Default value = 8'h00**

FSTPSEL2	FSTPSEL1	FSTPSEL0	Z2MOD20	Z2MOD19	Z2MOD18	Z2MOD17	Z2MOD16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5   FSTPSEL [2:0]   For type selection of table four and table five in command mode.
   (1) For bipolar motors:
- 000   Full step (for 1939, 1940, 2916, 6219, 3955, 3967).
- 001   Half step (for 1939, 1940, 2916, 6219, 3955, 3967).
- 010   Quarter step (for 2916, 6219, 3955, 3967).
- 011   Eighth step (for 3955, 3967).
- 100   Sixteenth step (for 3972)

   (2) For unipolar motors:
- 000   Two-phase-on full step.
- 001   Half step.
- 010   Reserved.
- 011   Single-phase-on full step.
- 100   Reserved.

7-0   Z2MOD [20:16]   "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when scanner start to move.
Note: It should be less than LPERIOD.

Note:for ACDCDIS=1,designer must subtract any small offset value from Z2MOD to

solve the first time start/stop motor position problem.

Offset 64h …….……………………...…………...…………...……….……..…… **Default value = 8'h00**

Z2MOD15	Z2MOD14	Z2MOD13	Z2MOD12	Z2MOD11	Z2MOD10	Z2MOD9	Z2MOD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 Z2MOD [15:8] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when scanner start to move.
Note: It should be less than LPERIOD.

Note:for ACDCDIS=1,designer must subtract any small offset value from Z2MOD to

solve the first time start/stop motor position problem.

Offset 65h …….……………………...…………...…………...……….……..…… **Default value = 8'h00**
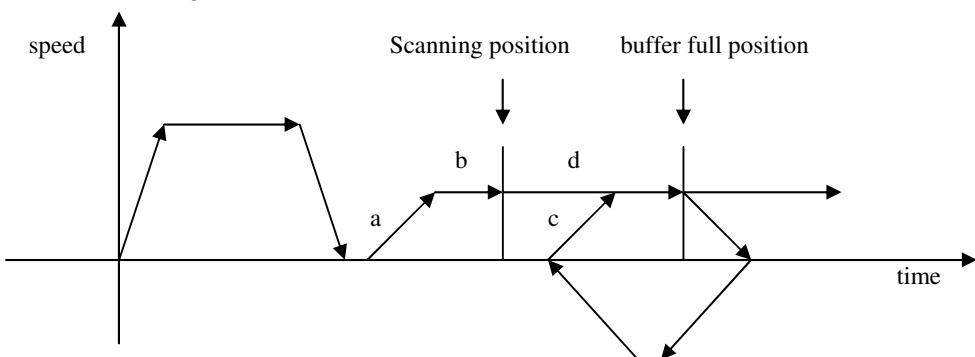
| Z2MOD7	Z2MOD6	Z2MOD5	Z2MOD4	Z2MOD3	Z2MOD2	Z2MOD1	Z2MOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 Z2MOD [7:0] "remainder value" of MOD operation in acceleration/deceleration tables.
ASIC calculate the moving time by MOD operation when scanner start to move.
Note: It should be less than LPERIOD.
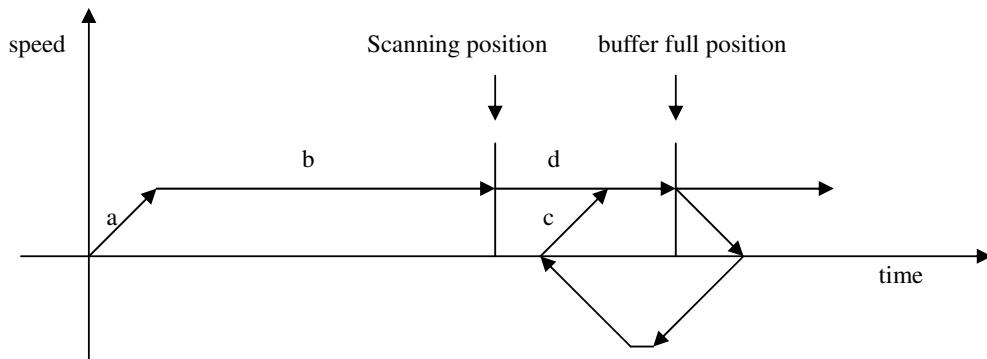
Note:for ACDCDIS=1,designer must subtract any small offset value from Z2MOD to

solve the first time start/stop motor position problem.

(1). Two table moving :

(2). One table moving :

{a + (b-1)} mode {LPERIOD * (CCDLMT+1)} = Z2MOD
{c + (d-1)} mode {LPERIOD * (CCDLMT+1)} = Z1MOD
 For example, c (STEPNO   = 4 steps for table 1)   = 60H, 48H, 30H, 18H
                      d (FWDSTEP = 3 steps for moving)   = 18H, 18H, 18H
                      LPERIOD   = 30H
      Then Z1MOD = {(60H + 48H + 30H + 18H) + (18H +18H)} MOD {30H} = 00H

   Note: If MCNTSET [1:0] = 01 or 10 or 11, then (each step curve value + 1)/VCNT.
         VCNT= system clocks per pixel / (MCNTSET+1).

Offset 66h …….………………….…….……….……….……….……….…… **Default value = 8'h00**

PHFREQ7	PHFREQ6	PHFREQ5	PHFREQ4	PHFREQ3	PHFREQ2	PHFREQ1	PHFREQ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

 7-0 PHFREQ [7:0]   PWM frequency for motor phase of unipolar motors
                         Frequency: (system clock frequency)/[(PHFREQ+1)*4

Offset 67h …….……….………….…….……….……….……….……….…… **Default value = 8'h7F**

X	X	MTRPWM5	MTRPWM4	MTRPWM3	MTRPWM2	MTRPWM1	MTRPWM0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

 7-6 RESERVED -

 5-0 MTRPWM [5:0]   PWM duty cycle selection of table one, table two and table three of motor phase
                         of unipolar motors in scanning mode.
                         MTRPWM = 0   1/64 duty
                                       = 1   2/64 duty
                                       = 2   3/64 duty
                                       ……
                                       = 63   64/64 duty
                         Note: If PHFREQ < 0FH, then PWM setting must < (PHFREQ+1)*4

Offset 68h …….……….………….…….……….……….……….……….…… **Default value = 8'h7F**

X	X	FASTPWM5	FASTPWM4	FASTPWM3	FASTPWM2	FASTPWM1	FASTPWM0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

 7-6 RESERVED -

 5-0 FASTPWM [5:0]   PWM duty cycle selection of table four and table five of motor phase of unipolar
                          motors in scanning mode.
                          FASTPWM = 0   1/64 duty
                                        = 1   2/64 duty
                                        = 2   3/64 duty
                                        ……
                                        = 63   64/64 duty
                          Note: If PHFREQ < 0FH, then PWM setting must < (PHFREQ+1)*4

Offset 69h …….……….…………..…….……….……….……….……….…… **Default value = 8'h00**

FSHDEC7	FSHDEC6	FSHDEC5	FSHDEC4	FSHDEC3	FSHDEC2	FSHDEC1	FSHDEC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 FSHDEC [7:0] Deceleration steps after scanning finished (table three).
Note: It cannot be programmed to logic zero.
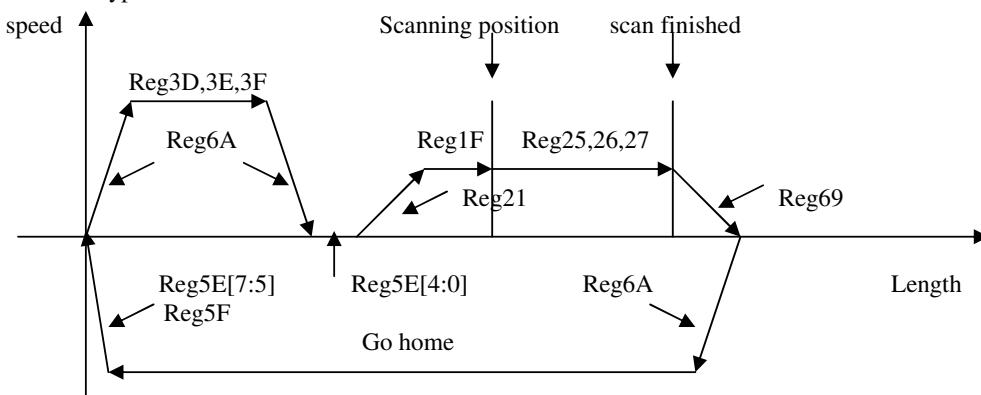
Offset 6Ah …….………..……………..…………...…..………..…….…..……..…. Default value = 8'h00

FMOVNO7	FMOVNO6	FMOVNO5	FMOVNO4	FMOVNO3	FMOVNO2	FMOVNO1	FMOVNO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
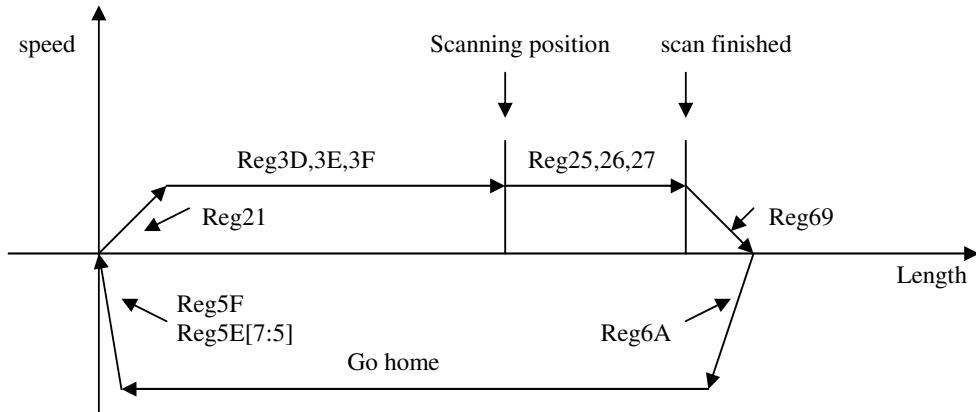
7-0 FMOVNO [7:0] Acceleration/deceleration steps for fast moving (table four).
Note: 1.It cannot be programmed to logic zero.
2.It can be multiplied by 2* ^{STEPTIM}

(1). Two table type:

(2). One table type:

Offset 6Bh …….………..…………….………...…..………..…………..…..……. Default value = 8'h00

MULTFILM	GPOM13	GPOM12	GPOM11	GPOCK4	GPOCP	GPOLEDB	GPOADF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

  7 MULTFILM   0   Disable multi-film scanning mode.
                       1   Enable multi-film scanning mode. Motor power will not be turned off in this mode.
  6 GPOM 13   0   Select GPIO13 as general purpose I/O.
                       1   Select GPIO13 as V-ref control of bipolar motor driver IC to control Imax.

5   GPOM12   0   Select GPIO12 as general purpose I/O.
                         1   Select GPIO12 as V-ref control of bipolar motor driver IC to control Imax.

4   GPOM11   0   Select GPIO11 as general purpose I/O..
                         1   Select GPIO11 as V-ref control of bipolar motor driver IC to control Imax.

Note: GPIO12: 1. Add a pull up resistor on GPIO12 will indicate ASIC to turn on lamp power in power-on initial state. This behavior is independent to setting of GPOM12.

                2. Add a pull down resistor on GPIO12 will indicate ASIC to turn off lamp power in power-on initial state. This behavior is independent to setting of GPOM12.

                3. This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref for controlling Imax current when GPOM12 is set to '1'.

GPIO11: This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref for controlling Imax current when GPOM11 is set to '1'.

3   GPOCK4   0   Select pin62 as CCD_CK4X
                         1   Select CCD_CK4X as GPO33

2   GPOCP   0   Select this pin68 as CCD_CPX.
                         1   CCD_CPX   as GPO32.

1   GPOLEDB   0   Select this pin as LED_B for CIS.
                         1   Select LED_B as GPO28.

0   GPOADF   0   Select normal function for GPIO6 and GPO28.
                         1   Select GPIO6 as motor STEP output of 3967 and GPO28(LED_B) as DIR output of 3967.

Offset 6Ch …….….…..….…….…..……..….……..……..….……..….…… Default value = 8'h00

GPIO16	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO [16:9]   GPIO16~9 input/output ports

Offset 6Dh …….….…..….…….…..……..….……..……..….……..….…… Default value = 8'h00

GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO [8:1]   GPIO8~1 input/output ports

Offset 6Eh …….….…..….…….…..……..….……..……..….……..….…… Default value = 8'h00

GPOE16	GPOE15	GPOE14	GPOE13	GPOE12	GPOE11	GPOE10	GPOE9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPOE [16:9]   Select directions of GPIO16~9 ports. They can be set to different values independently.
                        0   Set as input port.
                        1   Set as output port.

Offset 6Fh …….….…..….…….…..……..….……..……..….……..….…… Default value = 8'h00

GPOE8	GPOE7	GPOE6	GPOE5	GPOE4	GPOE3	GPOE2	GPOE1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPOE [8:1]   Select directions of GPIO8~1 ports. They can be set to different values

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independently.
0   Set as input port.
1   Set as output port.

Offset 70h …….……………….…..…………….………….……….…..….…. **Default value = 8'h06**

X	X	X	RSH4	RSH3	RSH2	RSH1	RSH0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -
4-0 RSH [4:0]   Rising edge position of CCD RS.
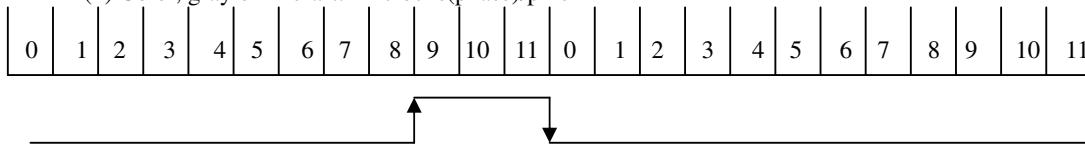
Offset 71h …….……………….…..…………….………….……….…..….…. **Default value = 8'h08**

X	X	X	RSL4	RSL3	RSL2	RSL1	RSL0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -
4-0 RSL [4:0]   Falling edge position of CCD RS.

   (1) Color, gray or line-art: 12 clocks(phase)/pixel

0	1	2	3	4	5	6	7	8	9	10	11	0	1	2	3	4	5	6	7	8	9	10	11

CCD RS : RSH=08H   RSL=0BH

Note: 16 clocks(phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12 clocks(phase)/pixel mode.

Offset 72h …….……………….…..…………….………….……….…..….…. **Default value = 8'h08**

X	X	X	CPH4	CPH3	CPH2	CPH1	CPH0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -
4-0 CPH [4:0]   Rising edge position of CCD CP.
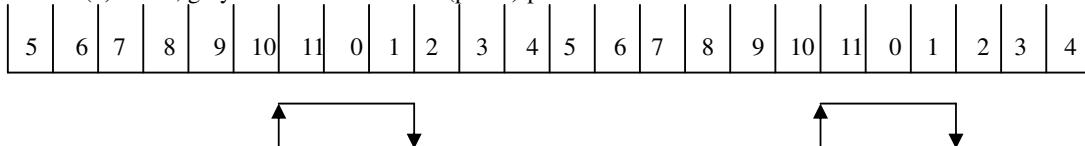
Offset 73h …….……………….…..…………….………….……….……. **Default value = 8'h0A**

X	X	X	CPL4	CPL3	CPL2	CPL1	CPL0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED   -
4-0 CPL [4:0]   Falling edge position of CCD CP.

   (1) Color, gray or line-art: 12 clocks(phase)/pixel

5	6	7	8	9	10	11	0	1	2	3	4	5	6	7	8	9	10	11	0	1	2	3	4

CCD CP : CPH=0AH   CPL=01H

Note: 16 clocks(phase)/pixel and 18 clocks(phase)/pixel modes are similar to 12 clocks(phase)/pixel mode.

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Offset 74h ……..…..……….………..……..……...…………..………..…..…. Default value = 8'h00

X	X	X	X	X	X	CK1MAP17	CK1MAP16
X	X	X	X	X	X	R/W	R/W

7-2 RESERVED -

1-0 CK1MAP [17:16] Bits mapping setting for CCD clock 1 or 2.

Offset 75h ……..…..……….………..……..……...…………..………..…..…. Default value = 8'h00

CK1MAP15	CK1MAP14	CK1MAP13	CK1MAP12	CK1MAP11	CK1MAP10	CK1MAP9	CK1MAP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK1MAP [15:8] Bits mapping setting for CCD clock 1 or 2.

Offset 76h ……..…..……….………..……..……...…………..………..…..…. Default value = 8'h00

CK1MAP7	CK1MAP6	CK1MAP5	CK1MAP4	CK1MAP3	CK1MAP2	CK1MAP1	CK1MAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK1MAP [7:0] Bits mapping setting for CCD clock 1 or 2.

Offset 77h ……..…..……….………..……..……...…………..………..…..…. Default value = 8'h00

X	X	X	X	X	X	CK3MAP17	CK3MAP16
X	X	X	X	X	X	R/W	R/W

7-2 RESERVED -

1-0 CK3MAP [17:16] Bits mapping setting for CCD clock 3.

Offset 78h ……..…..……….………..……..……...…………..………..…..…. Default value = 8'h00

CK3MAP15	CK3MAP14	CK3MAP13	CK3MAP12	CK3MAP11	CK3MAP10	CK3MAP9	CK3MAP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK3MAP [15:8] Bits mapping setting for CCD clock 3.

Offset 79h ……..…..……….………..……..……...…………..………..…..…. Default value = 8'h00

CK3MAP7	CK3MAP6	CK3MAP5	CK3MAP4	CK3MAP3	CK3MAP2	CK3MAP1	CK3MAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK3MAP [7:0] Bits mapping setting for CCD clock 3.

Offset 7Ah ……..…..……….………..……..……...…………..………..…..…. Default value = 8'h00

X	X	X	X	X	X	CK4MAP17	CK4MAP16
X	X	X	X	X	X	R/W	R/W

7-2 RESERVED -

1-0 CK4MAP [17:16] Bits mapping setting for CCD clock 4.

Offset 7Bh …….……..…….….…….……...…….…….……..…….……..…..… **Default value = 8'h00**

CK4MAP15	CK4MAP14	CK4MAP13	CK4MAP12	CK4MAP11	CK4MAP10	CK4MAP9	CK4MAP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK4MAP [15:8] Bits mapping setting for CCD clock 4.

Offset 7Ch …….……..…….….…….……...…….……..………….……..…..… **Default value = 8'h00**

CK4MAP7	CK4MAP6	CK4MAP5	CK4MAP4	CK4MAP3	CK4MAP2	CK4MAP1	CK4MAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 CK4MAP[7:0] Bits mapping setting for CCD clock 4.

Offset 7Dh …….……..…….….…….……..…….……...…….……..…….……..…..… **Default value = 8'h00**

CK1NEG	CK3NEG	CK4NEG	RSNEG	CPNEG	BSMPNEG	VSMPNEG	DLYSET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 CK1NEG
0 CCD clock1,clock2 output are synchronized with rising edge of system clock.
1 CCD clock1 & clock2 output are synchronized with falling edge of system clock.

6 CK3NEG
0 CCD clock3 output is synchronized with rising edge of system clock.
1 CCD clock3 output is synchronized with falling edge of system clock.

5 CK4NEG
0 CCD clock4 output is synchronized with rising edge of system clock.
1 CCD clock4 output is synchronized with falling edge of system clock.

4 RSNEG
0 CCD RS output is synchronized with rising edge of system clock.
1 RS output is synchronized with falling edge of system clock.

3 CPNEG
0 CCD CP output is synchronized with rising edge of system clock.
1 CCD CP output is synchronized with falling edge of system clock.

2 BSMPNEG
0 AFE video sample output is synchronized with rising edge of system clock.
1 AFE video sample output is synchronized with falling edge of system clock.

1 VSMPNEG
0 AFE dark sample output is synchronized with rising edge of system clock.
1 AFE dark sample output is synchronized with falling edge of system clock.

0 DLYSET
0 The function is disabled.
1 To enable VSMP and BSMP to delay output by 8.33ns unit. Please refer to Reg 7F.

Offset 7Eh …….……..…….….…….……..…….……...………….……..…….……..…..… **Default value = 8'h00**

GPOLED25	GPOLED24	GPOLED23	GPOLED22	GPOLED21	GPOLED10	GPOLED9	GPOLED8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 GPOLED25
0 Set GPIO25 as general purpose I/O.
1 Set GPIO25 as LED output.

6 GPOLED24
0 Set GPIO24 as general purpose I/O.
1 Set GPIO24 as LED output.

5 GPOLED23
0 Set GPIO23 as general purpose I/O.
1 Set GPIO23 as LED output.

4 GPOLED22
0 Set GPIO22 as general purpose I/O.
1 Set GPIO22 as LED output.

3 GPOLED21
0 Set GPIO21 as general purpose I/O.

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		1	Set GPIO21 as LED output.
2	**GPOLED10**	0	Set GPIO10 as general purpose I/O.
		1	Set GPIO10 as LED output.
1	**GPOLED9**	0	Set GPIO9 as general purpose I/O.
		1	Set GPIO9 as LED output.
0	**GPOLED8**	0	Set GPIO8 as general purpose I/O.
		1	Set GPIO8 as LED output.

Offset 7Fh …….……..…………….....………...…………..………….…..…… Default value = 8'h00

BSMPDLY1	BSMPDLY0	VSMPDLY1	VSMPDLY0	LEDCNT3	LEDCNT2	LEDCNT1	LEDCNT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 BSMPDLY[1:0]   BSMP output delay.
   00   No delay.
   01   Delay 8.33ns
   10   Delay 16.67ns
   11   Delay 25ns.

5-4 VSMPDLY[1:0]   VSMP output delay.
   00   No delay.
   01   Delay 8.33ns
   10   Delay 16.67ns
   11   Delay 25ns.

3-0 LEDCNT[1:0]   LED blinking period = (LEDCNT)*(100ms on + 100ms off).
   LED will not blink if LEDCNT=0.

Offset 80h …….……..…………….....………...…………..………….…..…… Default value = 8'h00

VRHOME1	VRHOME0	VRMOVE1	VRMOVE0	VRBACK1	VRBACK0	VRSCAN1	VRSCAN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 VRHOME[1:0]   Vref. of the motor driver IC for go-home moving.

5-4 VRMOVE[1:0]   Vref. of the motor driver IC for fast forward moving.

3-2 VRBACK[1:0]   Vref. of the motor driver IC for backward moving when the image buffer is full.

1-0 VRSCAN[1:0]   Vref. of the motor driver IC forward scanning moving.

Offset 81h …….……..…….…..………...………..………….…..………….…..…… Default value = 8'h00

X	X	X	X	X	X	X	ROFFSET8
X	X	X	X	X	X	X	R/W

7-1   RESERVED   -
0   ROFFSET [8]   R channel offset of the AFE for CIS color scanning

Offset 82h …….……..…….…..………...………..………….…..………….…..…… Default value = 8'h00

ROFFSET7	ROFFSET6	ROFFSET5	ROFFSET4	ROFFSET3	ROFFSET2	ROFFSET1	ROFFSET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7   ROFFSET [7:0]   R channel offset of the AFE for CIS color scanning

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Offset 83h …….…..…..…..…..…..……..…….….…….…..…….….…….……. **Default value = 8'h00**

X	X	X	X	X	X	X	GOFFSET8
X	X	X	X	X	X	X	R/W

7-1 RESERVED -
0 GOFFSET [8] G channel offset of the AFE for CIS color scanning

Offset 84h …….…..…..…..…..……..…….….…….…..…….….…….……. **Default value = 8'h00**

GOFFSET7	GOFFSET6	GOFFSET5	GOFFSET4	GOFFSET3	GOFFSET2	GOFFSET1	GOFFSET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 GOFFSET [7:0] G channel offset of the AFE for CIS color scanning

Offset 85h …….…..…..…..…..……..…….….…….…..…….….…….……. **Default value = 8'h00**

X	X	X	X	X	X	X	BOFFSET8
X	X	X	X	X	X	X	R/W

7-1 RESERVED -
0 BOFFSET [8] Bchannel offset of the AFE for CIS color scanning

Offset 86h …….…..…..…..…..……..…….….…….…..…….….…….……. **Default value = 8'h00**

BOFFSET7	BOFFSET6	BOFFSET5	BOFFSET4	BOFFSET3	BOFFSET2	BOFFSET1	BOFFSET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 BOFFSET [7:0] B channel offset of the AFE for CIS color scanning

Offset 87h …….…..…..…..…..……..…….….…….…..…….….…….……. **Default value = 8'h00**

X	X	X	ACYCNRLC	ENOFFSET	LEDADD	CK4ADC	AUTOCONF
X	X	X	R/W	R/W	R/W	R/W	R/W

4 ACYCNRLC   0 Disable this function.
              1 Generate RLC/ACYC pulse through BSMP pin to trigger WM1645
                 auto-cycling for line-by-line color scanning.
3 ENOFFSET   0 To disable this function.
              1 To select automatic offset configuration for CIS color scanning.
2 LEDADD   0 Normal gray by controlling CIS single color LED array.
            1 Enable true gray weighting in CIS by separately controlling the exposure times
               of R, G, B LED array. Please refer to Reg 10~15.
1 CK4ADC   0 Select MCLK (ADCCLK) to output default timing for specified AFE.
            1 Select MCLK (ADCCLK) pin to output according to pattern defined by
               CK4MAP (Reg 7A,7B,7C).
0 AUTOCONF   0 To disable these functions.
              1 Enable automatic channel switching and offset configuration for CIS color
                 scanning.

Note: If YBIT=1, then YENB=1 => PH_Y=1; YENB=0 => PH_Y=0.
    If YBIT=0, then YENB=1 => PH_Y=0; YENB=0 => PH_Y=1.

Offset 88h …….………..……………….....………..………..….………..…..…. **Default value = 8'h00**

X	X	X	RDNUM4	RDNUM3	RDNUM2	RDNUM1	RDNUM0
X	X	X	R/W	R/W	R/W	R/W	R/W

  7-5 RESERVED -
  4-0 RDNUM[4:0] Set the receiving length in bytes of RS232 interface.

Offset 89h

RS232WD7	RS232WD6	RS232WD5	RS232WD4	RS232WD3	RS232WD2	RS232WD1	RS232WD0
-	-	-	-	-	-	-	-

  7-0 RS232WD[7:0] This port is for designers to write data to RS232 interface.

Offset 8Ah

RS232RD7	RS232RD6	RS232RD5	RS232RD4	RS232RD3	RS232RD2	RS232RD1	RS232RD0
-	-	-	-	-	-	-	-

  7-0 RS232RD[7:0] This port is for designers to read data to RS232 interface.

Offset 8Bh …….………..……………….....………..………..….………..…..…. **Default value = 8'h00**

ROMADDR7	ROMADDR6	ROMADDR5	ROMADDR4	ROMADDR3	ROMADDR2	ROMADDR1	ROMADDR0
-	-	-	-	-	-	-	-

  7-0 ROMADDR[7:0] This port is for designers to write address and commands to 93C46.

Offset 8Ch

ROMWD15	ROMWD14	ROMWD13	ROMWD12	ROMWD11	ROMWD10	ROMWD9	ROMWD8
-	-	-	-	-	-	-	-

  7-0 ROMWD[15:8] This port is for designers to write data to 93C46.

Offset 8Dh

ROMWD7	ROMWD6	ROMWD5	ROMWD4	ROMWD3	ROMWD2	ROMWD1	ROMWD0
-	-	-	-	-	-	-	-

  7-0 ROMWD[7:0] This port is for designers to write data to 93C46.

Offset 8Fh …….………..……………….....………..………..….………..…..…. **Default value = 8'h00**

X	X	X	X	RREFED19	RREFED18	RREFED17	RREFED16
X	X	X	X	R/W	R/W	R/W	R/W

  7-4 RESERVED -

3-0 RREFED [19:16]   Pre-feed steps for ADF (or sheetfed scanner).

Offset 90h …….…….………………….....……….…………….…………….….…. **Default value = 8'h00**
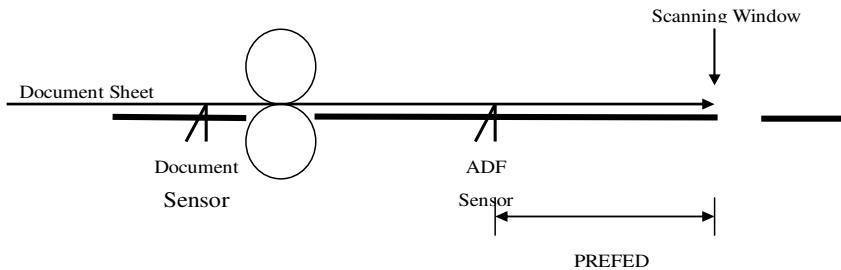
RREFED15	RREFED14	RREFED13	RREFED12	RREFED11	RREFED10	RREFED9	RREFED8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 RREFED [15:8] Pre-feed steps for ADF (or sheetfed scanner).

Offset 91h …….…….………………….....……….…………….…………….….…. **Default value = 8'h00**

RREFED7	RREFED6	RREFED5	RREFED4	RREFED3	RREFED2	RREFED1	RREFED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 RREFED [7:0]   Pre-feed steps for ADF (or sheetfed scanner).

Note: If the DPI9600 control bit is set to "1", the STRPIXEL is doubled.

**Offset 92h** …….…….………………….....……….…………….…………….….…. **Default value = 8'h00**
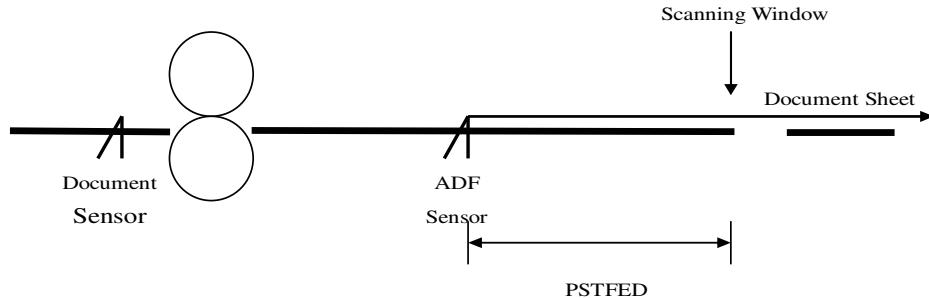
PSTFED15	PSTFED14	PSTFED13	PSTFED12	PSTFED11	PSTFED10	PSTFED9	PSTFED8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 PSTFED [15:8]   Past scanning steps for ADF (or sheetfed scanner).

Offset 93h …….…….………………….....……….…………….…………….….…. **Default value = 8'h00**

PSTFED7	PSTFED6	PSTFED5	PSTFED4	PSTFED3	PSTFED2	PSTFED1	PSTFED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 PSTFED [7:0]   Past scanning steps for ADF (or sheetfed scanner).

MTRPLS7	MTRPLS6	MTRPLS5	MTRPLS4	MTRPLS3	MTRPLS2	MTRPLS1	MTRPLS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 MTRPLS [7:0] Pulse width of ADF motor trigger signal (GPIO6). It's valid when ADFSEL = 1.

X	X	X	X	SCANLEN19	SCANLEN18	SCANLEN17	SCANLEN16
X	X	X	X	R/W	R/W	R/W	R/W

7-4 RESERVED   -

4-0 SCANLEN [19:16] Scanning length limitation of ADF (or sheetfed scanner). If the scanned lines are lager than this value but document sensor is still active (ADF_SENR is high), the paper-jam bit (bit 3 in Reg 40) will be set.

SCANLEN15	SCANLEN14	SCANLEN13	SCANLEN12	SCANLEN11	SCANLEN10	SCANLEN9	SCANLEN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 SCANLEN [8:15] Scanning length limitation of ADF (or sheetfed scanner).

SCANLEN7	SCANLEN6	SCANLEN5	SCANLEN4	SCANLEN3	SCANLEN2	SCANLEN1	SCANLEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 SCANLEN [7:0] Scanning length limitation of ADF (or sheetfed scanner).

ONDUR15	ONDUR14	ONDUR13	ONDUR12	ONDUR11	ONDUR10	ONDUR9	ONDUR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 ONDUR [15:8] On duration (in system clock) of PWM for LAMP control.

ONDUR7	ONDUR6	ONDUR5	ONDUR4	ONDUR3	ONDUR2	ONDUR1	ONDUR0

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 ONDUR [7:0]   On duration (in system clock) of PWM for LAMP control.

Offset 9Ah …….……..……………....………..………..…………..…..… Default value = 8'h00

OFFDUR15	OFFDUR14	OFFDUR13	OFFDUR12	OFFDUR11	OFFDUR10	OFFDUR9	OFFDUR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 OFFDUR [15:8] Off duration (in system clock) of PWM for LAMP control.

Offset 9Bh …….……..……………....………..………..…………..…..… Default value = 8'h00

OFFDUR7	OFFDUR6	OFFDUR5	OFFDUR4	OFFDUR3	OFFDUR2	OFFDUR1	OFFDUR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 OFFDUR [7:0]   Off duration (in system clock) of PWM for LAMP control.

Offset 9Ch

LCMWD7	LCMWD6	LCMWD5	LCMWD4	LCMWD3	LCMWD2	LCMWD1	LCMWD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 LCMWD [7:0]   This port is for designers to write data to LCM.

Offset 9Dh …….……..……………....………..………..…………..…..… Default value = 8'h00

RAMDLY1	RAMDLY0	MOTLAG	CMODE	STEPTIM2	STEPTIM1	STEPTIM0	IFRS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RAMDLY [1:0] Select timing delay for SCLK of SDRAM.

5 MOTLAG   0 Do not force the trigger position of motor trigger.
                    1 Force motor to locate its trigger at the end of line when dummy lines function
                       is activated.

4 CMODE   0 Select two-pin type control for COM1 & COM2 of LCD (GPO29&30).
                    1 Select three-pin type control for COM1 & COM2 of LCD (GPIO10,
                       GPO29&30).

3-1 STEPTIM [2:0] Select the multiplier of slope table. For Reg 21, 24, 5F, 69, 6A, the real slope
                    steps are register values multiplied by STEPTIM.
                    STEPTIM[2:0]   =000 : Slope steps = register values
                                   =001 : Slope steps = register values * 2
                                   =010 : Slope steps = register values * 4
                                   =011 : Slope steps = register values * 8
                                   =100 : Slope steps = register values * 16
                                   =101 : Slope steps = register values * 32

0 IFRS   0 Select data writing for LCM.
                    1 Select address writing for LCM.

Offset 9Eh …….……..……………....………..………..…………..…..… Default value = 8'h00

X	X	TGSTIME2	TGSTIME1	TGSTIME0	TGWTIME2	TGWTIME1	TGWTIME0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -
5-3 TGSTIME [2:0] To set the times of TGSHLD[4:0] . So , the width is TGSHLD[4:0]* 2 ^{TGSTIME}
2-0 TGWTIME [2:0] To set the times of TGW[5:0] . So, the width is TGW [5:0]* 2 ^{TGWTIME}

Offset 9Fh ……...……...…………......………...………...………...……...…… **Default value = 8'h00**

MASTER	SLAVE	SPI_MOT	FULLPAGE	AUTOADF	MOTMPU	MULDMYLN	DPI9600
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	**MASTER**	To select the chip to act as a master during two-chip operation
6	**SLAVE**	To select the chip to act as a slave during two-chip operation
5	**SPI_MOT**	To output SPI timing for 3972 motor driver IC according to SPI_MOTOR_W1 and SPI_MOTOR_W0 registers setting
4	**FULLPAGE**	0 To select general operation of motor when the Start/Stop occurs 1 To enable full-page operation of motor during ADF scanning
3	**AUTOADF**	0 To select one-page scanning under ADF operation 1 To enable multi-page scanning under ADF operation
2	**MOTMPU**	To select motor trigger output to MPU. The MPU can process the trigger signal. Note: If designer set MOTMPU=1 then he must set ACDCDIS=1.
1	**MULDMYLN**	0 Set dummy lines are equal to LINESEL. 1 Set dummy lines are equal to LINESEL*2
0	**DPI9600**	To enable 9600d resolution.

Offset A0h ……...……...…………......………...………...………...……...…… **Default value = 8'h00**

X	X	LNOFSET5	LNOFSET4	LNOFSET3	LNOFSET2	LNOFSET1	LNOFSET0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6 RESERVED -
5-0 LNOFSET [5:0] Line difference of R, G, B in packing three channels to one color line.

Offset A1h ……...……...…………......………...………...………...……...…… **Default value = 8'h80**

SNRSYN2	SNRSYN1	SNRSYN0	STGSET4	STGSET3	STGSET2	STGSET1	STGSET0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5 SNRSYN [2:0] Sensor debouncing such as HOME sensor.
4-0 STGSET [4:0] Line difference of stagger CCD between even and odd lines in packing them to the same color line.

Offset A2h ……...……...…………......………...………...………...……...…… **Default value = 8'h00**

X	X	X	RFHSET4	RFHSET3	RFHSET2	RFHSET1	RFHSET0
X	X	X	R/W	R/W	R/W	R/W	R/W

7-5 RESERVED -
4-0 RFHSET[4:0] Refresh time of SDRAM.
The unit is 2us.

Offset A3h ……...……...…………......………...………...………...……...…… **Default value = 8'h00**

TRUER7	TRUER6	TRUER5	TRUER4	TRUER3	TRUER2	TRUER1	TRUER0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 TRUER [7:0]   Weighting of R channel in true gray scanning.

Offset A4h …….....………..……………....…….....…………..………….....…. **Default value = 8'h00**

TRUEG7	TRUEG6	TRUEG5	TRUEG4	TRUEG3	TRUEG2	TRUEG1	TRUEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 TRUEG [7:0]   Weighting of G channel in true gray scanning.

Offset A5h …….....………..……………....…….....…………..………….....…. **Default value = 8'h00**

TRUEB7	TRUEB6	TRUEB5	TRUEB4	TRUEB3	TRUEB2	TRUEB1	TRUEB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 TRUEB [7:0]   Weighting of B channel in true gray scanning.

Offset A6h …….....………..……………....…….....…………..………….....…. **Default value = 8'h00**

GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPIO [24:17]   GPIO24~17 input/output ports.

Offset A7h …….....………..……………....…….....…………..………….....…. **Default value = 8'h00**

GPOE24	GPOE23	GPOE22	GPOE21	GPOE20	GPOE19	GPOE18	GPOE17
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPOE [24:17]   Select directions of GPIO24~17 ports. They can be set to different values
  independently.
  0   Set as input port.
  1   Set as output port.

Offset A8h …….....………..……………....…….....…………..………….....…. **Default value = 8'h00**

X	GPO36	GPOE27	GPOE26	GPOE25	GPIO27	GPIO26	GPIO25
X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7   RESERVED   -
6   GPO36   General output port.
5-3 GPOE [27:25]   Select directions of GPIO27~25 ports. They can be set to different values
  independently.
  0   Set as input port.
  1   Set as output port.
2-0 GPIO [27:25]   GPIO27~25 input/output ports.

Offset A9h …….....………..……………....…….....…………..………….....…. **Default value = 8'h00**

GPO35	GPO34	GPO33	GPO32	GPO31	GPO30	GPO29	GPO28
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 GPO [35:28] GPO35~28 output ports.

Offset AAh …….......….…………......………...….………...…………....…..… **Default value = 8'h00**

RESERVE7	RESERVE6	RESERVE5	RESERVE4	RESERVE3	RESERVE2	RESERVE1	RESERVE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 RESERVE7 [7:0] The 8 bits registers are reserved for special application

Offset ABh …….......….…………......………...….………...…………....…..… **Default value = 8'h00**

GPOM9	MULSTOP2	MULSTOP1	MULSTOP0	NODECEL	TB3TB1	TB5TB2	FIX16CLK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 GPOM9   0   Select GPIO9 as general purpose I/O.
                         1   Select GPIO9 as V-ref control of bipolar motor driver IC to control Imax

6-4 MULSTOP [2:0] Select stop time of motor start/stop. The stop time = $STOPTIM * 2^{MULSTOP}$
  3 NODECEL   0   Motor decelate when carriage touch home sensor
                               1   Motor doesn't decelate when carriage touch home sensor
  2 TB3TB1   0   Don't replace.
                               1   Use table 1 of motor table to replace table 3.
  1 TB5TB2   0   Don't replace.
                               1   Use table 2 of motor table to replace table 5.
  0 FIX16CLK   To enable 16 system clocks/pixel recover function

Offset ACh …….......….…………......………...….………...…………....…..… **Default value = 8'h00**

VRHOME3	VRHOME2	VRMOVE3	VRMOVE2	VRBACK3	VRBACK2	VRSCAN3	VRSCAN2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 VRHOME [3:2]   Vref of the motor driver IC for go-home moving
5-4 VRMOVE [3:2]   Vref of the motor driver IC for fast forward moving
3-2 VRBACK [3:2]   Vref of the motor driver IC for backward moving when the image buffer is full

Offset ADh …….......….…………......………...….………...…………....…..… **Default value = 8'h00**

RISC_INT_O	SC_INT_O	RESERVE5	SWSH4	SWSH3	SWSH2	SWSH1	SWSH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7 RISC_INT_O   Output internal RISC CPU interrupt signal to external MCU through GPIO26 for handshake handling
6 SC_INT_O   Output internal scanner controller interrupt signal to external MCU to notice interrupt events of scanner controller occurs
5 RESERVE5   This bit is reserved for special application
4-0 SWSH [4:0]   To set the distance from SW to TG for NEC/Toshiba CCD. The width is $SWSH[4:0]*2^{TGSTIME}$

Offset AEh …….…….……….…….……....…..……….…..……….….……..…..…. **Default value = 8'h00**

X	X	STOPPWM5	STOPPWM4	STOPPWM3	STOPPWM2	STOPPWM1	STOPPWM0
X	X	R/W	R/W	R/W	R/W	R/W	R/W

7-6   RESERVED   -

5-0   STOPPWM [5:0]   Set the PWM control of motor driver IC during motor stopping.

Offset B0h …….…….……….…….……....…..……….…..……….….……..…..…. **Default value = 8'h00**

X	X	X	X	X	X	COLLEN9	COLLEN8
X	X	X	X	X	X	R/W	R/W

7-2   RESERVED   -

1-0   COLLEN [9:8]   Reserved

Offset B1h …….…….……….…….……....…..……….…..……….….……..…..…. **Default value = 8'h00**

COLLEN7	COLLEN6	COLLEN5	COLLEN4	COLLEN3	COLLEN2	COLLEN1	COLLEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   COLLEN [7:0]   Reserved

Offset B2h …….…….……….…….……....…..……….…..……….….……..…..…. **Default value = 8'h00**

X	X	X	X	X	X	COLJMP9	COLJMP8
X	X	X	X	X	X	R/W	R/W

7-2   RESERVED   -

1-0   COLJMP [9:8]   Reserved

Offset B3h …….…….……….…….……....…..……….…..……….….……..…..…. **Default value = 8'h00**

COLJMP7	COLJMP6	COLJMP5	COLJMP4	COLJMP3	COLJMP2	COLJMP1	COLJMP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   COLJMP [7:0]   Reserved

Offset B8h …….…….……….…….……....…..……….…..……….….……..…..…. **Default value = 8'h00**

ILX580	TSH_EN	TSH_SEL1	TSH_SEL0	SW2_EN	SW2_SEL	SW4_EN	SW4EXCHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7   ILX580   Enable Sony ILX580 CCD timing

6   TSH_EN   Enable Special CCD timing of CCD TG for Toshiba's application

5-4   TSH_SEL [1:0] Select special CCD timing of CCD RS and CCD SW4 for Toshiba's application

when TSH_EN is set to "1"

3	SW2_EN		Enable special CCD timing of CCD SW2 for Toshiba's application
2	SW2_SEL	0	CCD SW2 and CCD SW5 timing control is based on internal CCD_CNX counter of ASIC
		1	CCD SW2 and CCD SW5 timing control is based on internal SH_CNT counter of ASIC
1	SW4_EN		Enable special CCD timing of CCD SW4 for Toshiba's application
0	SW4EXCHG		Control CCD SW4 shutter for Multi-SH apllication

Offset B9h …….……..………….……....………..…………..….………..…..…. Default value = 8'h00

TCK_EN	TCK_SEL	TCK4_DIS	TCK3_DIS	TCK1_DIS	TSHMSKB2	TSHMSKB1	TSHMSKB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	TCK_EN	0	Select traditional CCD PHI clocks timing
		1	Select special CCD PHI clocks timing such as NEC 8884 or Toshiba CCD
6	TCK_SEL	0	CCD PHI clocks timing is based on internal CCD_CNX counter of ASIC
		1	CCD PHI clocks timing is based on internal SH_CNT counter of ASIC
5	TCK4_DIS	0	Enable CCD PHI4 clock output when ASIC works on special CCD timing operation
		1	Disable CCD PHI4 clock output when ASIC works on special CCD timing operation
4	TCK3_DIS	0	Enable CCD PHI3 clock output when ASIC works on special CCD timing operation
		1	Disable CCD PHI3 clock output when ASIC works on special CCD timing operation
3	TCK1_DIS	0	Enable CCD PHI1 & 2 clocks output when ASIC works on special CCD timing operation
		1	Disable CCD PHI1 & 2 clocks output when ASIC works on special CCD timing operation
2-0	TSHMSKB [2:0]		Select SH3 operation behavior for special CCD application when CCD works on different exposure time and TSH_EN is set to "1" at the same time

Offset BAh …….……..………….……....………..…………..….………..…..…. Default value = 8'h00

CCD_OUT	AV_EN	TSHMSKG2	TSHMSKG1	TSHMSKG0	TSHMSKR2	TSHMSKR1	TSHMSKR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	CCD_OUT	Enable internal CCD signal outputs including sh_enb, sh_enbx and ccd_cnt[2:0] for external CPLD implementation to meet special CCD timing
6	AV_EN	Enable switch control for special CCD or CIS

4-3   **TSHMSKG [2:0]** Select SH2 operation behavior for special CCD application when CCD works on different exposure time and TSH_EN is set to "1" at the same time

2-0   **TSHMSKR [2:0]** Select SH1 operation behavior for special CCD application when CCD works on different exposure time and TSH_EN is set to "1" at the same time

Offset BBh …….…….…………….....………..…………..………….…..… **Default value = 8'h00**

S580_SEL1	S580_SEL0	MT_OFF13	MT_OFF12	MT_OFF11	MT_OFF10	MT_OFF9	MT_OFF8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5   **S580_SEL [1:0]** Control the gap between two CCD TGs for the application of Sony 580 CCD

4-0   **MT_OFF [13:8]** Output motor-off timing when motor releases the power for motor phase table operation

Offset BCh …….…….…………….....………..…………..………….…..… **Default value = 8'hFF**

MT_OFF7	MT_OFF6	MT_OFF5	MT_OFF4	MT_OFF3	MT_OFF2	MT_OFF1	MT_OFF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **MT_OFF [7:0]** Output motor-off timing when motor releases the power for motor phase table operation

Offset BDh …….…….…………….....………..…………..………….…..… **Default value = 8'h1F**

SW5_EN	SW5_SEL	SW5EXCHG	X	X	BGMM_N	GGMM_N	RGMM_N
R/W	R/W	R/W	X	X	R/W	R/W	R/W

7   **SW5_EN**   Enable special CCD timing of CCD SW5 for Toshiba's application

6   **SW5_SEL**   Control CCD SW5 output which is based on internal CCD_CNX0 or CCD_CNX1 of ASIC

5   **SW5EXCHG**   Control output position of CCD SW5 which is based on CCD SH

2   **BGMM_N**   If this bit is set to "1", it indicates that table[256] of B gamma in RAM is ignored and replaced by "-1"

1   **GGMM_N**   If this bit is set to "1", it indicates that table[256] of G gamma in RAM is ignored and replaced by "-1"

0   **RGMM_N**   If this bit is set to "1", it indicates that table[256] of R gamma in RAM is ignored and replaced by "-1"

Offset BEh …….…….…………….....………..…………..………….…..… **Default value = 8'h00**

SW2INV	SW4INV	SW5INV	X	X	BGMM_F	GGMM_F	RGMM_F
X	R/W	R/W	X	X	R/W	R/W	R/W

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7	**SW2INV**	Invert CCD SW2 output
6	**SW4INV**	Invert CCD SW4 output
5	**SW5INV**	Invert CCD SW5 output
2	**BGMM_F**	If this bit is set to "1", it indicates that table[256] of B gamma in RAM is ignored and replaced by "0x10000"
1	**GGMM_F**	If this bit is set to "1", it indicates that table[256] of G gamma in RAM is ignored and replaced by "0x10000"
0	**RGMM_F**	If this bit is set to "1", it indicates that table[256] of R gamma in RAM is ignored and replaced by "0x10000"

Offset BFh …….……..……………....……..………….……….…..…..… **Default value = 8'h00**

TSH_AMT1	TSH_AMT0	SC_NUM5	SC_NUM4	SC_NUM3	SC_NUM2	SC_NUM1	SC_NUM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-6 **TSH_AMT [1:0]** Set the number of CCD SH

5-0 **SC_NUM [5:0]** Page count scanned when scanner works on ADF mode

Offset C0h …….……..……………....……..………….……….…..…..… **Default value = 8'h00**

SPI_MOTOR_W1 19	SPI_MOTOR_W1 18	SPI_MOTOR_W1 17	SPI_MOTOR_W1 16	SPI_MOTOR_W0 19	SPI_MOTOR_W0 18	SPI_MOTOR_W0 17	SPI_MOTOR_W0 16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-4 **SPI_MOTOR_W1 [19:16]** Bit19~16 Register setting for WORD1 of 3972 motor driver IC

3-0 **SPI_MOTOR_W0 [19:16]** Bit19~16 Register setting for WORD0 of 3972 motor driver IC

Offset C1h …….……..……………....……..………….……….…..…..… **Default value = 8'h00**

SPI_MOTOR_W0 15	SPI_MOTOR_W0 14	SPI_MOTOR_W0 13	SPI_MOTOR_W0 12	SPI_MOTOR_W0 11	SPI_MOTOR_W0 10	SPI_MOTOR_W0 9	SPI_MOTOR_W0 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 **SPI_MOTOR_W0 [15:8]** Bit15~8 Register setting for WORD0 of 3972 motor driver IC

Offset C2h …….……..……………....……..………….……….…..…..… **Default value = 8'h00**

SPI_MOTOR_W0 7	SPI_MOTOR_W0 6	SPI_MOTOR_W0 5	SPI_MOTOR_W0 4	SPI_MOTOR_W0 3	SPI_MOTOR_W0 2	SPI_MOTOR_W0 1	SPI_MOTOR_W0 0
X	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 **SPI_MOTOR_W0 [7:0]** Bit7~0 Register setting for WORD0 of 3972 motor driver IC

Offset C3h …….……..……………....……..………….……….…..…..… **Default value = 8'h00**

SPI_MOTOR_W1	SPI_MOTOR_W1	SPI_MOTOR_W1	SPI_MOTOR_W1	SPI_MOTOR_W1	SPI_MOTOR_W1	SPI_MOTOR_W1	SPI_MOTOR_W1

15	14	13	12	11	10	9	8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   SPI_MOTOR_W1 [15:8]   Bit15~8 Register setting for WORD1 of 3972 motor driver IC

Offset C4h …….....….……..………......…….......…………..……………....…..… **Default value = 8'h00**

SPI_MOTOR_W1 7	SPI_MOTOR_W1 6	SPI_MOTOR_W1 5	SPI_MOTOR_W1 4	SPI_MOTOR_W1 3	SPI_MOTOR_W1 2	SPI_MOTOR_W1 1	SPI_MOTOR_W1 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   SPI_MOTOR_W1 [7:0]   Bit7~0 Register setting for WORD1 of 3972 motor driver IC

Offset C5h …….....….……..………......…….......…………..……………....…..… **Default value = 8'h00**

RGMM_Z15	RGMM_Z14	RGMM_Z13	RGMM_Z12	RGMM_Z11	RGMM_Z10	RGMM_Z9	RGMM_Z8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   RGMM_Z [15:8]   Bit15~8 setting of table[0] for R gamma

Offset C6h …….....….……..………......…….......…………..……………....…..… **Default value = 8'h00**

RGMM_Z7	RGMM_Z6	RGMM_Z5	RGMM_Z4	RGMM_Z3	RGMM_Z2	RGMM_Z1	RGMM_Z0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   RGMM_Z [7:0]   Bit7~0 setting of table[0] for R gamma

Offset C7h …….....….……..………......…….......…………..……………....…..… **Default value = 8'h00**

GGMM_Z15	GGMM_Z14	GGMM_Z13	GGMM_Z12	GGMM_Z11	GGMM_Z10	GGMM_Z9	GGMM_Z8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5   GGMM_Z [15:8]   Bit15~8 setting of table[0] for G gamma

Offset C8h …….....….……..………......…….......…………..……………....…..… **Default value = 8'h00**

GGMM_Z7	GGMM_Z6	GGMM_Z5	GGMM_Z4	GGMM_Z3	GGMM_Z2	GGMM_Z1	GGMM_Z0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   GGMM_Z [7:0]   Bit7~0 setting of table[0] for G gamma

Offset C9h …….....….……..………......…….......…………..……………....…..… **Default value = 8'h00**

BGMM_Z15	BGMM_Z14	BGMM_Z13	BGMM_Z12	BGMM_Z11	BGMM_Z10	BGMM_Z9	BGMM_Z8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   BGMM_Z [15:8]   Bit15~8 setting of table[0] for B gamma

Offset CAh …….……..……………………...………..…………..…………..…..…… Default value = 8'h00

BGMM_Z7	BGMM_Z6	BGMM_Z5	BGMM_Z4	BGMM_Z3	BGMM_Z2	BGMM_Z1	BGMM_Z0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   BGMM_Z [7:0]   Bit7~0 setting of table[0] for B gamma

Offset D0h …….……..……………………...………..…………..…………..…..…… Default value = 8'h00

SH0DWN7	SH0DWN6	SH0DWN5	SH0DWN4	SH0DWN3	SH0DWN2	SH0DWN1	SH0DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-5   SH0DWN [7:0]   Shading bank0 address setting for CCD. Unit is in 4k words**.**

It is also R-Channel shading bank0 address setting for CIS

Offset D1h …….……..……………………...………..…………..…………..…..…… Default value = 8'h00

SH1DWN7	SH1DWN6	SH1DWN5	SH1DWN4	SH1DWN3	SH1DWN2	SH1DWN1	SH1DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   SH1DWN [7:0]   Shading bank1 address setting for CCD. Unit is in 4k words**.**

It is also G-Channel shading bank0 address setting for CIS

Offset D2h …….……..……………………...………..…………..…………..…..…… Default value = 8'h00

SH2DWN7	SH2DWN6	SH2DWN5	SH2DWN4	SH2DWN3	SH2DWN2	SH2DWN1	SH2DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   SH2DWN [7:0]   Shading bank2 address setting for CCD. Unit is in 4k words**.**

It is also B-Channel shading bank0 address setting for CIS

Offset D3h …….……..……………………...………..…………..…………..…..…… Default value = 8'h00

SH3DWN7	SH3DWN6	SH3DWN5	SH3DWN4	SH3DWN3	SH3DWN2	SH3DWN1	SH3DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   SH3DWN [7:0]   Shading bank3 address setting for CCD. Unit is in 4k words**.**

It is also Channel-4 shading bank0 address setting for CIS

Offset D4h …….……..……………………...………..…………..…………..…..…… Default value = 8'h00

SH4DWN7	SH4DWN6	SH4DWN5	SH4DWN4	SH4DWN3	SH4DWN2	SH4DWN1	SH4DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   SH4DWN [7:0]   Shading bank4 address setting for CCD. Unit is in 4k words**.**

It is also Channel-5 shading bank0 address setting for CIS

Offset D5h …….…..…...…………...………..………..………..…..… **Default value = 8'h00**

SH5DWN7	SH5DWN6	SH5DWN5	SH5DWN4	SH5DWN3	SH5DWN2	SH5DWN1	SH5DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **SH5DWN [7:0]**   Shading bank5 address setting for CCD. Unit is in 4k words**.**

It is also R-Channel shading bank1 address setting for CIS

Offset D6h …….…..…...…………...………..………..………..…..… **Default value = 8'h00**

SH6DWN7	SH6DWN6	SH6DWN5	SH6DWN4	SH6DWN3	SH6DWN2	SH6DWN1	SH6DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **SH6DWN [7:0]**   Shading bank6 address setting for CCD. Unit is in 4k words**.**

It is also G-Channel shading bank1 address setting for CIS

Offset D7h …….…..…...…………...………..………..………..…..… **Default value = 8'h00**

SH7DWN7	SH7DWN6	SH7DWN5	SH7DWN4	SH7DWN3	SH7DWN2	SH7DWN1	SH7DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **SH7DWN [7:0]**   Shading bank7 address setting for CCD. Unit is in 4k words**.**

It is also B-Channel shading bank1 address setting for CIS

Offset D8h …….…..…...…………...………..………..………..…..… **Default value = 8'h00**

SH8DWN7	SH8DWN6	SH8DWN5	SH8DWN4	SH8DWN3	SH8DWN2	SH8DWN1	SH8DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **SH8DWN [7:0]**   Shading bank8 address setting for CCD. Unit is in 4k words**.**

It is also Channel-4 shading bank1 address setting for CIS

Offset D9h …….…..…...…………...………..………..………..…..… **Default value = 8'h00**

SH9DWN7	SH9DWN6	SH9DWN5	SH9DWN4	SH9DWN3	SH9DWN2	SH9DWN1	SH9DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **SH9DWN [7:0]**   Shading bank9 address setting for CCD. Unit is in 4k words**.**

It is also Channel-5 shading bank1 address setting for CIS

Offset DAh …….…..…...…………...………..………..………..…..… **Default value = 8'h00**

PROTLN15	PROTLN14	PROTLN13	PROTLN12	PROTLN11	PROTLN10	PROTLN9	PROTLN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **PROTLN [15:8]**   Minimum scanning length protection setting for ADF operation

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Offset DBh …….……..…………….…....………..………..………….…..…..… **Default value = 8'h00**

PROTLN7	PROTLN6	PROTLN5	PROTLN4	PROTLN3	PROTLN2	PROTLN1	PROTLN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **PROTLN [7:0]**   Minimum scanning length protection setting for ADF operation

Offset DEh

ROMRD15	ROMRD14	ROMRD13	ROMRD12	ROMRD11	ROMRD10	ROMRD9	ROMRD8
-	-	-	-	-	-	-	-

7-0 ROMRD[15:8]   This port is for designers to read data to 93C46.

Offset DFh

ROMRD7	ROMRD6	ROMRD5	ROMRD4	ROMRD3	ROMRD2	ROMRD1	ROMRD0
-	-	-	-	-	-	-	-

7-0   ROMRD[7:0]   This port is for designers to read data to 93C46.

Offset E0h …….……..…………….…....………..………..………….…..…… **Default value = 8'h00**

R1DWN15	R1DWN14	R1DWN13	R1DWN12	R1DWN11	R1DWN10	R1DWN9	R1DWN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **R1DWN [15:8]**   Bit15~8 Registers setting for R-Channel ODD image buffer start-address.

When working on CIS mode, it is for ODD image buffer start-address setting.

Unit is in 1k words.

Offset E1h …….……..…………….…....………..………..………….…..…… **Default value = 8'h00**

R1DWN7	R1DWN6	R1DWN5	R1DWN4	R1DWN3	R1DWN2	R1DWN1	R1DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **R1DWN [7:0]**   Bit7~0 Registers setting for R-Channel ODD image buffer start-address.

When working on CIS mode, it is for ODD image buffer start-address setting.

Unit is in 1k words.

Offset E2h …….……..…………….…....………..………..………….…..…… **Default value = 8'h00**

R1UP15	R1UP14	R1UP13	R1UP12	R1UP11	R1UP10	R1UP9	R1UP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **R1UP[15:8]**   Bit15~8 Registers setting for R-Channel ODD image buffer end-address.

When working on CIS mode, it is for ODD image buffer end-address setting.

Unit is in 1k words.

Offset E3h …….…..…….…………....………..………..………….….…..… Default value = 8'h00

R1UP7	R1UP6	R1UP5	R1UP4	R1UP3	R1UP2	R1UP1	R1UP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0　R1UP [7:0]　　Bit7~0 Registers setting for R-Channel ODD image buffer end-address.

　　　　　　　　　　When working on CIS mode, it is for ODD image buffer end-address setting.

　　　　　　　　　　Unit is in 1k words.

Offset E4h …….…..…….…………....………..………..………….….…..… Default value = 8'h00

R2DWN15	R2DWN14	R2DWN13	R2DWN12	R2DWN11	R2DWN10	R2DWN9	R2DWN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0　R2DWN [15:8]　Bit15~8 Registers setting for R-Channel EVEN image buffer start-address.

　　　　　　　　　　When working on CIS mode, it is for EVEN image buffer start-address setting.

　　　　　　　　　　Unit is in 1k words.

Offset E5h …….…..…….…………....………..………..………….….…..… Default value = 8'h00

R2DWN7	R2DWN6	R2DWN5	R2DWN4	R2DWN3	R2DWN2	R2DWN1	R2DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0　R2DWN [7:0]　　Bit7~0 Registers setting for R-Channel EVEN image buffer start-address.

　　　　　　　　　　When working on CIS mode, it is for EVEN image buffer start-address setting.

　　　　　　　　　　Unit is in 1k words.

Offset E6h …….…..…….…………....………..………..………….….…..… Default value = 8'h00

R2UP15	R2UP14	R2UP13	R2UP12	R2UP11	R2UP10	R2UP9	R2UP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0　R2UP[15:8]　　Bit15~8 Registers setting for R-Channel EVEN image buffer end-address.

　　　　　　　　　　When working on CIS mode, it is for EVEN image buffer end-address setting.

　　　　　　　　　　Unit is in 1k words.

Offset E7h …….…..…….…………....………..………..………….….…..… Default value = 8'h00

R2UP7	R2UP6	R2UP5	R2UP4	R2UP3	R2UP2	R2UP1	R2UP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0　R2UP [7:0]　　Bit7~0 Registers setting for R-Channel EVEN image buffer end-address.

　　　　　　　　　　When working on CIS mode, it is for EVEN image buffer end-address setting.

　　　　　　　　　　Unit is in 1k words.

Offset E8h …….....………….…………….....…………....……….……...…………..…..…… **Default value = 8'h00**

G1DWN15	G1DWN14	G1DWN13	G1DWN12	G1DWN11	G1DWN10	G1DWN9	G1DWN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G1DWN [15:8]   Bit15~8 Registers setting for G-Channel ODD image buffer start-address. Unit is
in 1k words

Offset E9h …….....………….…………….....…………....……….……...…………..…..…… **Default value = 8'h00**

G1DWN7	G1DWN6	G1DWN5	G1DWN4	G1DWN3	G1DWN2	G1DWN1	G1DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G1DWN [7:0]   Bit7~0 Registers setting for G-Channel ODD image buffer start-address. Unit is in
1k words.

Offset EAh …….....…….…………….....…………....……….……...…………..…..…… **Default value = 8'h00**

G1UP15	G1UP14	G1UP13	G1UP12	G1UP11	G1UP10	G1UP9	G1UP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G1UP[15:8]   Bit15~8 Registers setting for G-Channel ODD image buffer end-address. Unit is
in 1k words.

Offset EBh …….....…….…………….....…………....……….……...…………..…..…… **Default value = 8'h00**

G1UP7	G1UP6	G1UP5	G1UP4	G1UP3	G1UP2	G1UP1	G1UP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G1UP [7:0]   Bit7~0 Registers setting for G-Channel ODD image buffer end-address. Unit is
in 1k words.

Offset ECh …….....…….…………….....…………....……….……...…………..…..…… **Default value = 8'h00**

G2DWN15	G2DWN14	G2DWN13	G2DWN12	G2DWN11	G2DWN10	G2DWN9	G2DWN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G2DWN [15:8]   Bit15~8 Registers setting for G-Channel EVEN image buffer start-address. Unit is
in 1k words

Offset EDh …….....…….…………….....…………....……….……...…………..…..…… **Default value = 8'h00**

G2DWN7	G2DWN6	G2DWN5	G2DWN4	G2DWN3	G2DWN2	G2DWN1	G2DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G2DWN [7:0]   Bit7~0 Registers setting for G-Channel EVEN image buffer start-address. Unit is in 1k words.

Offset EEh …….....…..………....……..………...……………...….…… **Default value = 8'h00**

G2UP15	G2UP14	G2UP13	G2UP12	G2UP11	G2UP10	G2UP9	G2UP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G2UP [15:8]   Bit15~8 Registers setting for G -Channel EVEN image buffer end-address. Unit is in 1k words

Offset EFh …….....…..………....……..………...……………...….…… **Default value = 8'h00**

G2UP7	G2UP6	G2UP5	G2UP4	G2UP3	G2UP2	G2UP1	G2UP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   G2UP [7:0]   Bit7~0 Registers setting for G -Channel EVEN image buffer end-address. Unit is in 1k words

Offset F0h …….....…..………....……..………...……………...….…… **Default value = 8'h00**

B1DWN15	B1DWN14	B1DWN13	B1DWN12	B1DWN11	B1DWN10	B1DWN9	B1DWN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   B1DWN [15:8]   Bit15~8 Registers setting for B-Channel ODD image buffer start-address. Unit is in 1k words.

Offset F1h …….....…..………....……..………...……………...….…… **Default value = 8'h00**

B1DWN7	B1DWN6	B1DWN5	B1DWN4	B1DWN3	B1DWN2	B1DWN1	B1DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   B1DWN [7:0]   Bit7~0 Registers setting for B-Channel ODD image buffer start-address. Unit is in 1k words.

Offset F2h …….....…..………....……..………...……………...….…… **Default value = 8'h00**

B1UP15	B1UP14	B1UP13	B1UP12	B1UP11	B1UP10	B1UP9	B1UP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   B1UP[15:8]   Bit15~8 Registers setting for B-Channel ODD image buffer end-address. Unit is in 1k words.

Offset F3h …….....…..………....……..………...……………...….…… **Default value = 8'h00**

B1UP7	B1UP6	B1UP5	B1UP4	B1UP3	B1UP2	B1UP1	B1UP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 B1UP [7:0]   Bit7~0 Registers setting for B-Channel ODD image buffer end-address. Unit is in 1k words.

Offset F4h …….…….……………...………..………..………….…..….. **Default value = 8'h00**

B2DWN15	B2DWN14	B2DWN13	B2DWN12	B2DWN11	B2DWN10	B2DWN9	B2DWN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 B2DWN [15:8]   Bit15~8 Registers setting for B-Channel EVEN image buffer start-address. Unit is in 1k words

Offset F5h …….…….……………...…...………..………..………….…..….. **Default value = 8'h00**

B2DWN7	B2DWN6	B2DWN5	B2DWN4	B2DWN3	B2DWN2	B2DWN1	B2DWN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 B2DWN [7:0]   Bit7~0 Registers setting for B-Channel EVEN image buffer start-address. Unit is in 1k words.

Offset F6h …….…….……………...………..………..………….…..….. **Default value = 8'h00**

B2UP15	B2UP14	B2UP13	B2UP12	B2UP11	B2UP10	B2UP9	B2UP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 B2UP [15:8]   Bit15~8 Registers setting for B-Channel EVEN image buffer end-address. Unit is in 1k words

Offset F7h …….…….……………...………..………..………….…..….. **Default value = 8'h00**

B2UP7	B2UP6	B2UP5	B2UP4	B2UP3	B2UP2	B2UP1	B2UP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0 B2UP [7:0]   Bit7~0 Registers setting for B-Channel EVEN image buffer end-address. Unit is in 1k words

Offset F8h …….…….……………...………..………..………….…..….. **Default value = 8'h00**

MAXSEL3	MAXSEL2	MAXSEL1	MAXSEL0	MINSEL3	MINSEL2	MINSEL1	MINSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-4 MAXSEL [3:0]   Define bank number of image buffer for buffer-full (for MAXWD)

3-0 MINSEL [3:0]   Define bank number of image buffer for buffer-empty

MAXSEL/MINSEL :

0➔ r_odd   1➔r_even

2➔ g_odd   3➔g_even

4➔ b_odd   5➔b_even

Offset FDh

MAINTSK3	MAINTSK2	MAINTSK1	MAINTSK0	SUBTSK3	SUBTSK2	SUBTSK1	SUBTSK0
R	R	R	R	R	R	R	R

7-4   **MAINTSK [3:0]**   To monitor internal flow control status of main task

3-0   **SUBTSK [3:0]**   To monitor internal flow control status of main task

Offset FEh …….…….…………….…………...………..…………..………….…..… Default value = 8'h00

MOTTGST3	MOTTGST2	MOTTGST1	MOTTGST0	AUTO_O3	AUTO_O2	AUTO_O1	AUTO_O0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-4   **MOTTGST [3:0]**   For debug usage

3-0   **AUTO_O [3:0]**   Auto pattern offset --> unit : $2^{auto\_o[3:0]}$

Offset FFh …….…….…………….…………...………..…………..………….…..… Default value = 8'h00

AUTO_S7	AUTO_S6	AUTO_S5	AUTO_S4	AUTO_S3	AUTO_S2	AUTO_S1	AUTO_S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7-0   **AUTO_S [7:0]**   Auto pattern High byte initial value

Low byte initial value=0

$$auto\_pattern[15:0] = AUTO\_S[7:0] << 8 + 2^{AUTO\_O[3:0]}$$

4.3 Motor Table

		Scanner Address[25:0]	AHB Address[31:0]
Motor Table (8K word/per table)	Table 1	0000000H~0001FFFH	0x1000_0000 – 0x100_3FFF
	Table 2	0002000H~0003FFFH	0x1000_4000 – 0x100_7FFF
	Table 3	0004000H~0005FFFH	0x1000_8000 – 0x100_BFFF
	Table 4	0006000H~0007FFFH	0x1000_C000 – 0x100_FFFF
	Table 5	0008000H~0009FFFH	0x1001_0000 – 0x101_3FFF

4.4 AHB address allocation

Address range	Size (Byte)	Mapping	Module
0x0000_0000 – 0x0FFF_FFFF	256M	On-chip register	APB bridge
0x1000_0000 – 0x17FF_FFFF	128M	SDRAM (16bits)	Scanner controller
0x2000_0000 – 0x2000_03FF	1K	32~8bits	Test Module
0x3000_0000 – 0x3000_0100	256	16bits	Two chip
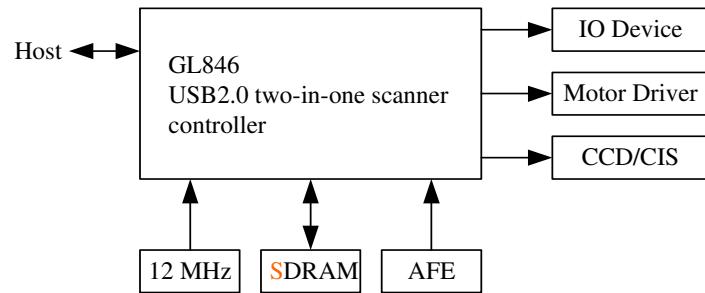
4.5 On-chip registers (APB) address allocation

Address range	Size (Byte)	Data width (bit)	Module
0x0000_0000 – 0x0000_01FF	512	8	Scanner register
0x0100_0000 – 0x0100_09FF	2560	16	Scanner gamma table
0x0100_0000 – 0x0100_01FF	512	16	gamma R (256x16)
0x0100_0200 – 0x0100_03FF	512	16	gamma G (256x16)
0x0100_0400 – 0x0100_05FF	512	16	gamma B (256x16)
0x0100_0A00– 0x0100_0A7F	128	16	motor phase table (64x14)
0x0110_0000 – 0x0110_007F	128	32	scan count ram(32x20)
0x0200_0000 – 0x0200_03FF		8	USB register
0x0300_0000 – 0x0300_03FF		16	SPI
0x0400_0000 – 0x0400_000F	16	8	APB delay register
0x0500_0000 – 0x0500_0000	4	32	RISC -->MCU Interrupt
0x0500_0000 – 0x0500_0004	4	32	MCU -->RISC Interrupt
0x0500_0000 – 0x0500_0008	4	32	MCU <-->RISC Register
0x0500_0000 – 0x0500_000C	4	32	RISC<-->MCU Register
0x0500_0000 – 0x0500_0010	4	32	Interrupt Pos/Neg edge
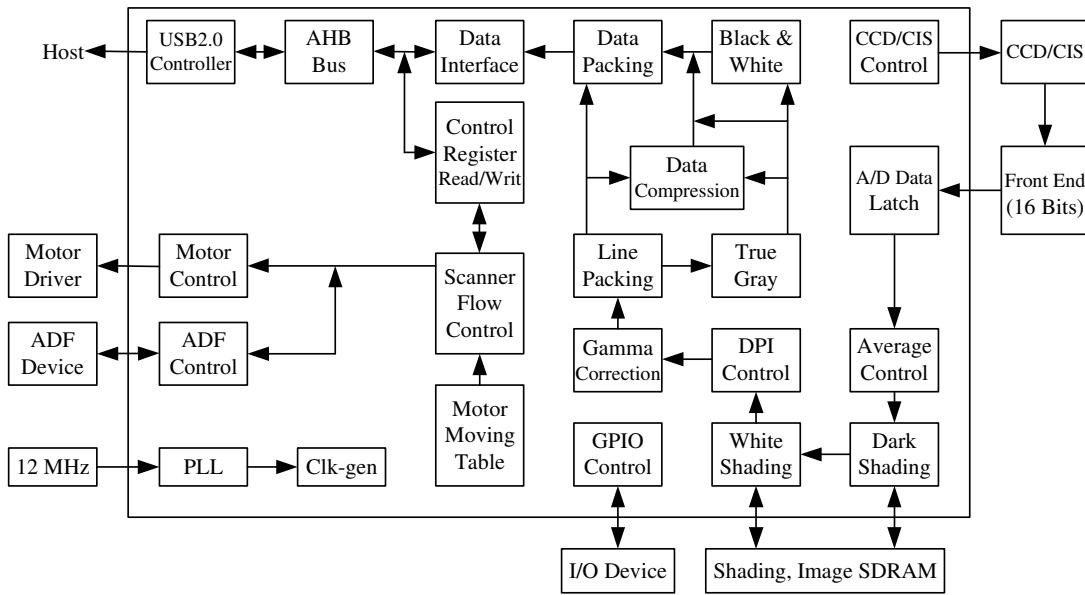
CHAPTER 5   BLOCK DIAGRAM

5.1 USB2.0 System Block Diagram

Figure 5.1 - USB2.0 System Block Diagram

5.2 Function Block Diagram

Figure 5.2 - Function Block Diagram

CHAPTER 6   FUNCTIONAL DESCRIPTION

1 System Clock

Internal PLL.

A. Input: 12MHz crystal.

B. Output: 12, 24, 30, 40, 48 or 60 MHz to scanner controller system.

2 Pixel Clock

A. Normal mode
   Scan mode 0:   a. 12 system clock/pixel.
                            b. Chunky color (three line in), gray or art scanning for CCD.
                            c. Planar color scan (one line in) or Monochrome scanning for CIS.

B. fast mode
   Scan mode 2:   a. 8 system clock/pixel.
                            b. fast gray or art scanning for CCD or CIS.
                            c. Planar color scan (one line in) or Monochrome scanning for CIS.

C. Scan mode 7
                            a. 16 system clock/pixel.
                            b. Chunky color (three line in), gray or line-art scanning for CCD.
                            c. Planar color scan (one line in) or Monochrome scanning for CIS.

D. Scan mode 6   a. 18 system clock/pixel
                            b. Chunky color (three line in), gray or art scanning for CCD.
                            c. Planar color scan (one line in) or Monochrome scan for CIS.

Note: Chunky Color is R1G1B1, R2G2B2, R3G3B3,………(three-line-in or pixel rate).
     Planar Color is R1, R2, R3,…..; G1, G2, G3,……; B1, B2, B3,……..(one-line-in or line rate).
     CCD: Chunky color or planar color.
     CIS: Planar color.

3 Scan Speed

A. System clock = 30MHz:
     a. Normal Mode: Chunky color, fine gray or fine line art scan.
        (scan mode 0)   12x33.333ns/pixel = 0.4us/pixel.
                         (1). 600dpi: 2.160ms/line, 15.163s/page.
                         (2). 1200dpi: 4.320ms/line, 60.653s/page.

B. System clock = 40MHz:
     a. Normal Mode: Chunky color, fine gray or fine line art scan.
                         12x25ns/pixel = 0.3us/pixel
                         (1). 600dpi: 1.620ms/line, 11.372s/page.
                         (2). 1200dpi: 3.240ms/line, 45.488s/page.

4 Fast Scan for Low Resolutions

Designers are allowed to increase CCD clock rates to up scanning speed in low resolutions,
such as 2, 4, 8, …times..

5 Scanning Type

GL846 supports three-line-in (parallel) for CCD and one-line-in for CIS.

A. CCD Type
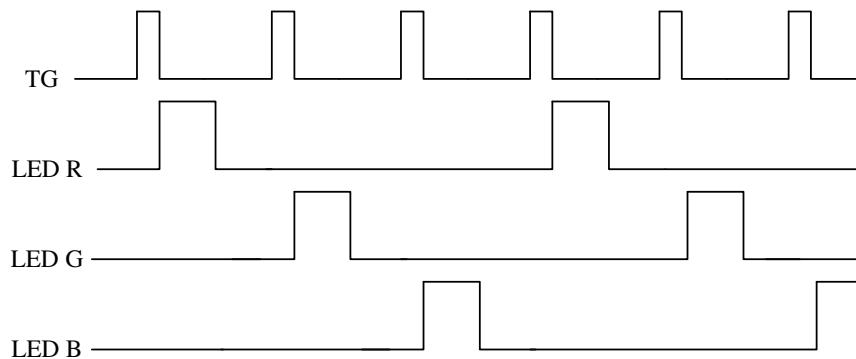
   CCD Exposure control:
   There are three modes to control CCD TG by TGMODE control bits.
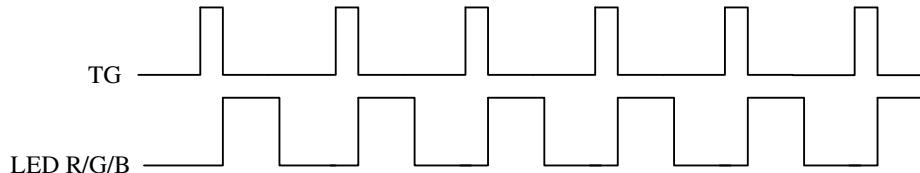
Mode 0: single exposure time for R, G and B channels.
Mode 1, 2: different exposure times for R, G and B channels .

B. CIS Type
   a. Color scan:

TG

LED R

LED G

LED B

  b. Gray scan:

TG

LED R/G/B

  c. True gray scan:

TG

LED R

LED G

LED B
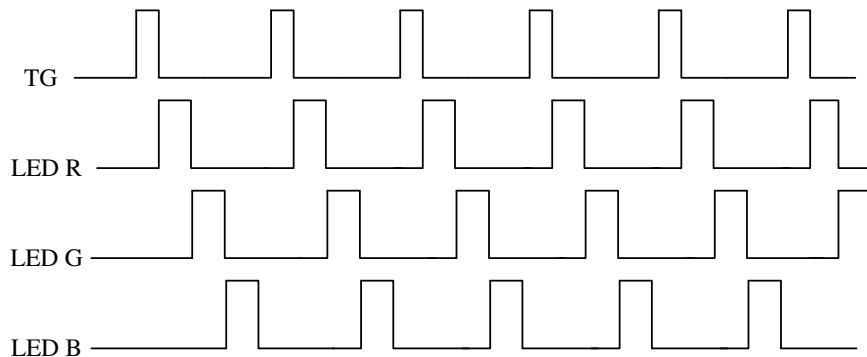
6 Image Sensor Timing

Image sensor timings can be programmed by S/W.

A. For CCD: Support 600, 1200, 2400, 3200, 3600 ,4800dpi ~ 9600dpi CCD such as NEC, TOSHIBA,
         Sony ……etc.

B. For CIS: Support 600, 1200, 2400, 3200, 3600,4800dpi ~ 9600dp CIS such as TOSHIBA, Canon ……etc

C. Supports Toshiba 4800dpi TCD2954 and 9600dpi TCD2962 CCDs.

7 Dummy Line

GL846 supports programmable dummy lines to resolve (overcome) start/stop problem.
Designers can insert dummy lines to reduce scanner start/stop events (buffer full).

A. Line base of dummy lines:

  The range of dummy lines is 0~30 lines.

B. Adjustable dummy line:

The range is from the minimum shift time of CCD/CIS up to 2096K pixel time, with 1 pixel time resolution.

8 Support Analog Front End Timing

GL846 supports external 16 bits front-end.
Wolfson: WM1645
Analog device: AD9826, …etc.

9 Image Type

A. Supports color, gray and line art scanning.
B. Supports color filters options (R, G or B channels) in gray or line art scanning.
C. Supports true gray with programmable R, G and B weightings.

10 Bits Depth

16*3 bits color, 16 bits gray level and 1 bit line art (Black & White).
Image data type: 16 bits, 8 bits and 1 bit.

11 Shading & Correction

a. White Shading & Dark Shading:

White shading and dark shading are pixel-by-pixel corrections with 16-bit solution and can be enabled or disabled by S/W. The white shading curve is calculated by S/W.

Data arrangement: three line in mode: dark R1, white R1, dark G1, white G1, dark B1, white B1,
dark R2, white R2, dark G2, white G2, dark B2, white B2,
dark R3, white R3, dark G3, white G3, dark B3, white B3,
one line in mode: dark R1, white R1, dark R2, white R2, dark R3, white R3…
dark G1, white G1, dark G2, white G2, dark G3, white G3…
dark B1, white B1, dark B2, white B2, dark B3, white B3…

White shading formula: $2000H * Target / (Wn-Dn) = White Gain data$ ----- for 8 times system
White shading formula: $4000H * Target / (Wn-Dn) = White Gain data$ ----- for 4 times system

For example: Target = 3FFFH,   Wn = 2FFFH,   Dn = 0040H and 8 times system operation
then White Gain = $2000H * 3FFFH / (2FFFH-0040H) = 2AE4H$ (1.34033 times)

b. Gamma Correction:

16-bit GAMMA correction table is programmed by S/W.
Range: 0 ~ 64k (16 bits) input mapping to 0 ~ 64k (16 bits) or 0 ~ 255 (8 bits) output.
Style: increment or decrement gamma curve
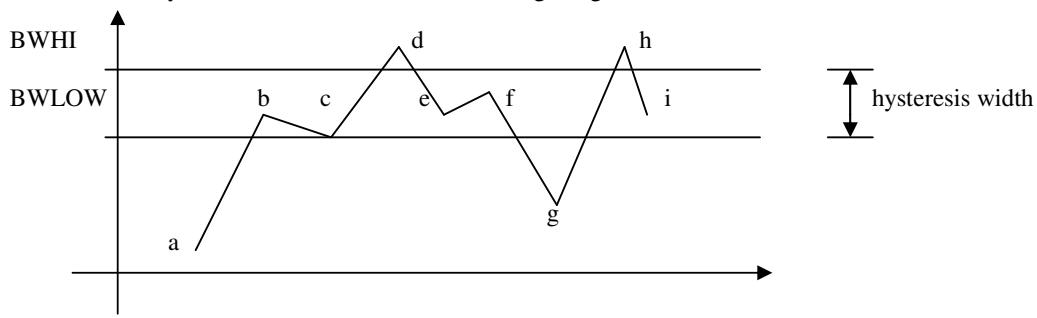
12 Threshold Setting for Line-Art

Threshold can be programmed by S/W.
Range: 0 ~ 255 adjustable.
The threshold with hysteresis characteristic is for reducing image noise.

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a,b,c,g : are black pixels
d,e,f,h,i : are white pixels

13 Exposure Time

Maximum: 2096k pixels time
Adjustment step: 1 pixel time.
For transparency scanning, the exposure time can be up to 2096k pixels time.

14 Scan Width control for Horizontal Line

a. Supports start and end pixels assignment in setting scan width.

b. Scanning width= end pixels - start pixels
   Maximum length: 128K pixels.
   Minimum length: 1 pixel.

15 Support built-in USB 2.0 Controller

2-in-1 USB2.0 controller + scanner controller.

16 SDRAM Timing

Supports 16M Bits (1M*16), 64M Bits (4M*16), 128M Bits (8M*16), 256M Bits (16M*16) and 512 M Bits (32M*16) SDRAM as image buffer and calibration buffer.

17 Horizontal Resolution Adjustable for DPI Function

A. Digital deletion type:
   Software adjustable resolutions range from 9600 to 1 dpi with 1 dpi decrement.

B. Digital average type:

   Supports 1/2, 1/3, 1/4, 1/5, 1/6, 1/8, 1/10, 1/12, 1/15 digital average function.
   For example, options for 1200dpi scanner are:

   1200dpi, 600dpi, 400dpi, 300dpi, 240dpi, 200dpi, 150dpi,120dpi, 100dpi, 80dpi by average function.

C. Support stagger CCD:

   Supports 1/2, 1/4, 1/8 resolutions, such as NEC Toshiba and Sony stagger CCD.

18 Vertical Resolution Adjustable for DPI Function

The resolution of motor moving is 16 bits wide and is flexibly controlled by motor tables.
The resolution can be up to 4800 dpi for 1200 dpi scanners, 9600 dpi for 2400 dpi scanners and 19200 dpi for 4800 dpi scanners.
Note: The resolution of vertical direction of quarter step can up to four times resolution.
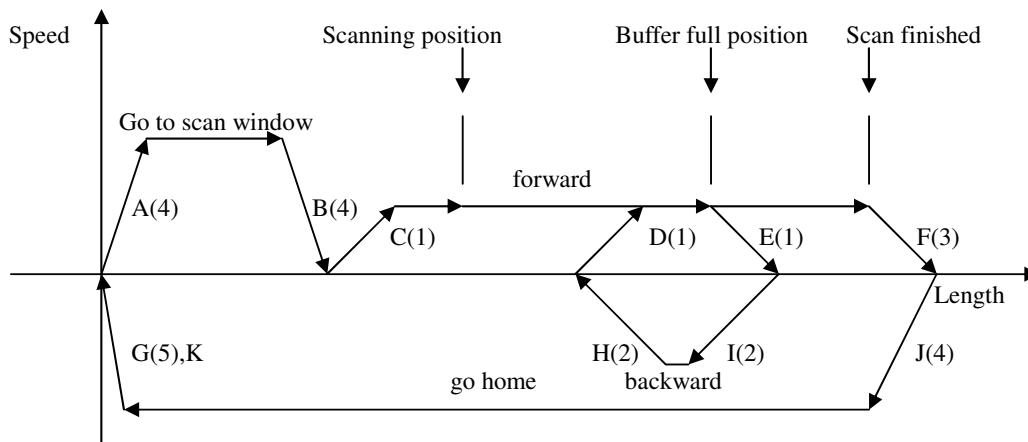
19 Five Acceleration/Deceleration Tables

The acceleration/deceleration tables are stored in internal SRAM and can be downloaded by S/W.
And the resolution is 16 bits in pixel-time. The number of table steps is from 1 to 1020 steps for arbitrary curves. There are five tables for motor moving. Three tables are for scanning and the others are for fast moving. The forward and backward steps can be programmed by S/W separately.
Note: "Fast move" means move back to home position or move forward to scan window in any position.
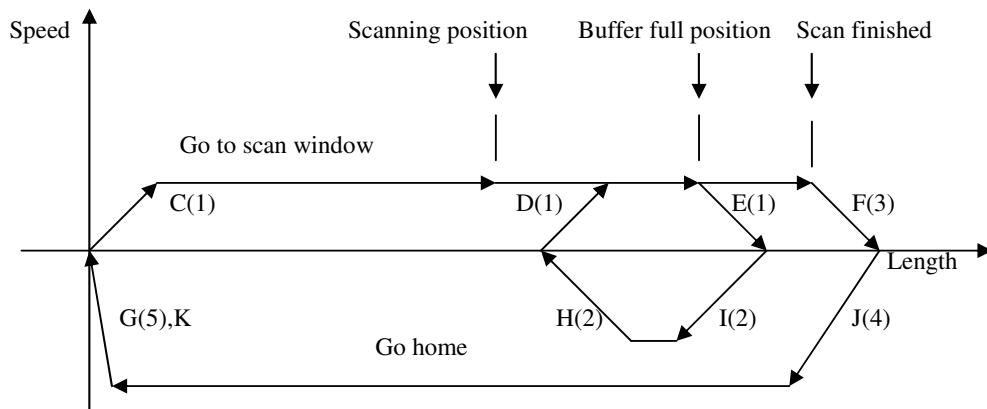
(1) Two tables type:

A,J : Acceleration curve in table four (slope four) for fast moving.
B : Deceleration curve in table four (slope four) for fast moving.
C,D : Acceleration curve in table one (slope one) for scanning.
E : Deceleration curve in table one (slope one) for scanning.
F : Deceleration curve in table three (slope three) for scanning finished to protect wall hitting.
I : Acceleration curve in table two (slope two) for back-track when image buffer full.
H : Deceleration curve in table two (slope two) for back-track when image buffer full.
G : Deceleration curve in table five (slope five) for go-home to protect wall hitting.
K : Touch home sensor deceleration curve for go-home.

(2) One tables type:

J : Acceleration curve in table four (slope four) for fast moving.
C,D : Acceleration curve in table one (slope one) for forward scanning.
E : Deceleration curve in table one (slope one) for scanning.
F : Deceleration curve in table three (slope three) for scanning finished to protect wall hitting.
I : Acceleration curve in table two (slope two) for back-track when image buffer full.
H : Deceleration curve in table two (slope two) for back-track when image buffer full.
G : Deceleration curve in table five (slope five) for go-home to protect wall hitting.
K : Touch home sensor deceleration curve for go-home.

20 Trigger Position Control

Designers can select to move motor first then capture image; or capture image first then move motor.

21 Stepping Motor Phase Control

There are 8 output control pins to control stepping motors:
MTR_PH 0~7 for bipolar motors   MTR_PH 0~3 for unipolar motors

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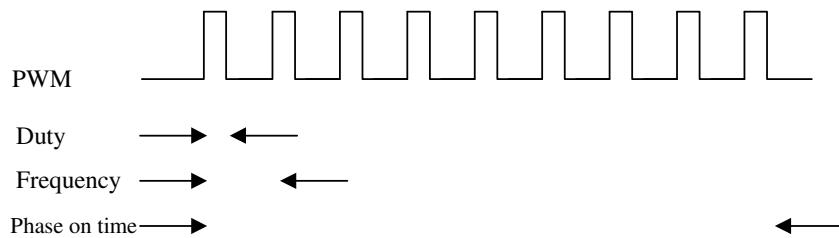
A. Bipolar motors:
    a. Supports 2916 motor driver timing and 2916 compatible driver IC, such as L6219.
       Include full, half and quarter steps control.
    b. Supports 3955 motor driver timing.
       Include full, half, quarter and eighth steps control.
    c. Supports 3967 motor driver timing.
       Include full, half, quarter and eighth steps control.
    d. Supports LB1939, 1940 motor driver timing.
       Include full and half steps control

B. Unipolar motors:
    a. Supports 2003 motor driver timing and 2003 compatible driver IC.
    b. Include full step two phases on, full step single phase on and half step.
    c. PWM control, include frequency and duty controls.

22 Watchdog Protection

This function can automatically reset the system to initial state when the system is hanged (no access signal) beyond the time limit. It can be enabled or disabled by S/W.
This function can protect motor power, lamp power and ASIC system.
Calculation formula: (30sec.) * (times setting) * (setting number.).

The range of setting number is from 1 to 15; the range of times setting is 0 or 1.

23 Lamp Time-out Control

This circuitry can automatically turn off the lamp power when this function is enabled. It can be enabled or disabled by S/W.
Calculation formula: (60sec.) * (times setting) * (setting number).
The range of setting number is from 1 to 7;the range of times setting is 0 to 3.

24 Lamp Power Control

These are two power control ports for lamp. One is for Flatbed and the other is for XPA (Transparency or film). These control ports have PWM function. According to the system clock, designers can flexibly adjust their frequency and duty by S/W. And the resolution of PWM is 16 bits.

25 Sensors

The system supports home sensor for flatbed; ADF sensor, document sensor and cover sensor for ADF module.

26 GPIO Ports

Designers can separately assign input or output direction for each GPIO pin of GPIO1~21 and GPIO27. Some GPIO can be designed for keypads, document sensor of sheetfed or motor power control…etc.
Designers can assign GPIO27 as general-purpose input/output port or as ADF sensor input.
Note : There are four pins for special function.

    GPIO9:   This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref3 for control
             Imax current.

GPIO13: This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref2 for control

Imax current.

GPIO12: 1. Pull up by resistor to indicate ASIC to turn on lamp power in power-on initial state.

2. Pull down by resistor to indicate ASIC to turn off lamp power in power-on initial state..

3. This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref1 for controlling

Imax current.

GPIO11: This pin can control bipolar motor driver IC (2916,6219,3955 or 3967) Vref0 for control

Imax current.

27 GPO28~33 Ports

GL846 provides 6 ports for general-purpose output. They exist in both 128 and 208 pins packages.

28 Power on Check

The default status of the PWRBIT control bit is reset. Programmers can set the PWRBIT control bit before controlling the ASIC. GL846 will keep the status until power is turn off. This operation is to check if the power had been turned off or not.

29 Extended GPIO

GPIO22~26 is only available in 208 pins QFP package.

30 LED Blinking
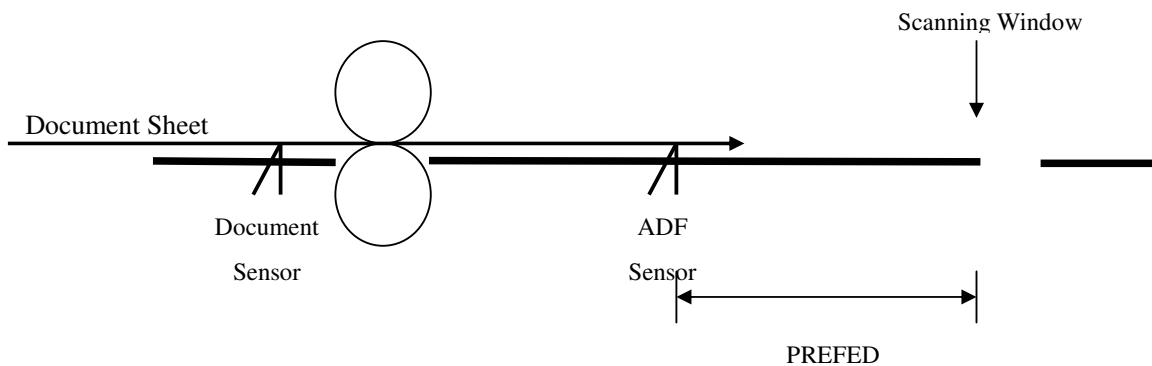
GL846 supports LED -blinking function. It is implemented in GPIO15~16 pins and GPIO21~26.

31 Support Back Scanning
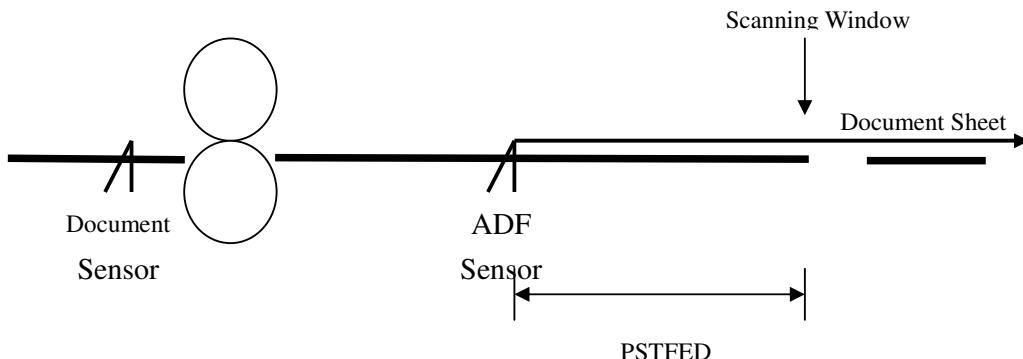
GL846 supports forward or backward scanning.

32 Supports ADF Function

GL846 supports ADF (Auto-document-feeder) function via internal logic circuitry. Programmers need to set

the ADFSEL control bit to logic '1'. GPIO6 controls the motor pulse trigger if the motor moving of ADF

module is implemented by trigger pulse, otherwise the motor moving is driven by motor phases. GPO28

controls the moving direction of motor if ADF module is necessary. GPIO16 is the cover sensor input,

GPIO27 is the ADF sensor input and HOME is document sensor input under ADF mode.

GL846 can feed document sheets automatically to scanning window. After sensing the present of document by document sensor, software should issue feed command to GL846 for paper feeding. After document sheet reaches ADF sensor, scanning process will be started after PREFED motor steps.

When document sheet keeps moving forward, after sensing the absent of document by ADF sensor, scanning process will be terminated after PSTFED scanning lines.

33 Supports RS232 Interface

GL846 supports RS232 interface via internal logic circuitry. Programmers need to set the RS232SEL control bit to logic '1'. GPIO6 transmits the data of RS232 and GPIO28 receives the data of RS232 under RS232 mode. The baud rate can be programmed to 2400,4800, 9600 and 19200 bps by S/W.

34 Supports EEPROM (93C46) Interface

GL846 supports EEPROM interface via internal logic circuitry. Programmers need to set the EPROMSEL control bit to logic '1'. GPIO1 controls SK of external EEPROM, GPIO2 controls DI/DO of EEPROM and GPIO17 controls CS of external EEPROM under EEPROM mode.

35 Supports External 24Kbytes flash ROM or Internal 24Kbyte mask ROM

Designers can use 24K bytes embedded mask ROM or external flash ROM. Firmware can be downloaded to flash ROM directly by PC S/W. It provides a flexible development environment to design the firmware.

36 "True gray" with R,G and B weightings

Designers can obtain the "true gray" image data by enabling "true gray" function. Image data is generated by R,G and B outputs and multiplied by weightings.
Formula of true gray value = $R*(TRUER [7:0]) + G*(TRUEG [7:0]) + B*(TRUEB [7:0])$

37 Lossless Data Compression

GL846 use Huffman coding method to implement the lossless data compression.

38 Lines Packing for Stagger CCD or R/G/B Line Differences

GL846 packs R, G and B lines together for CCD sensors by hardware. And it also packs the same color lines

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of stagger CCD together.

39 Fine CDS Sampling Adjustment

Designers can fine-tune the CDS sampling position to avoid the digital noise influence (8.33ns adjustment). The image noise may come from the digital noise of PCB.

40 Wall-Hitting Protection

Designers can use table five of motor moving to protect the wall hitting. The LONGCURV control bit has to be set to logic '1' to enable the long-curve function. The first several steps are used to decelerate the carriage moving; the other slower steps are focused on touching the home sensor.
Due to the special table five, designers can replace the photo-sensor by simple, cheaper mechanical-type sensors.

41 Motor Driver IC Setting

Designers add pull up/pull down   resistors on MTR_SEL0~2 will indicate ASIC to generate the timing of specified motor driver IC.

Motor type select : CCD_TGB   MTR_SEL2

                   CCD_TGG   MTR_SEL1

                   CCD_CK4X   MTR_SEL0

When designers select MTR_SEL0~2 to "111", MT_PH0~7 will output phase table which is stored in internal RAM.
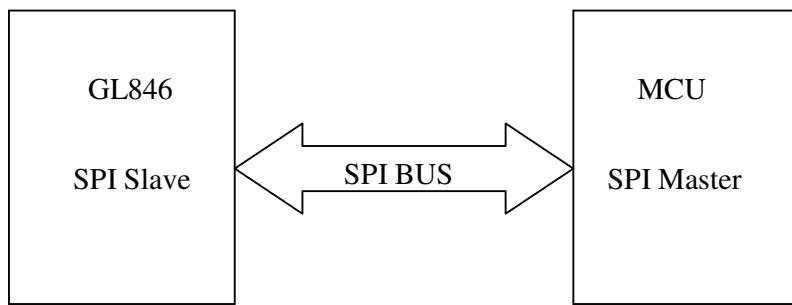
42 Operation Mode Setting

Designers add pull down   resistors on TSTSEL0~3 will indicate ASIC to work on normal mode.

ASIC mode select : CCD_CK3X   TSTSEL3

                  CCD_RSX   TSTSEL2

                  CCD_CK2X   TSTSEL1

   CCD_TGX   TSTSEL0
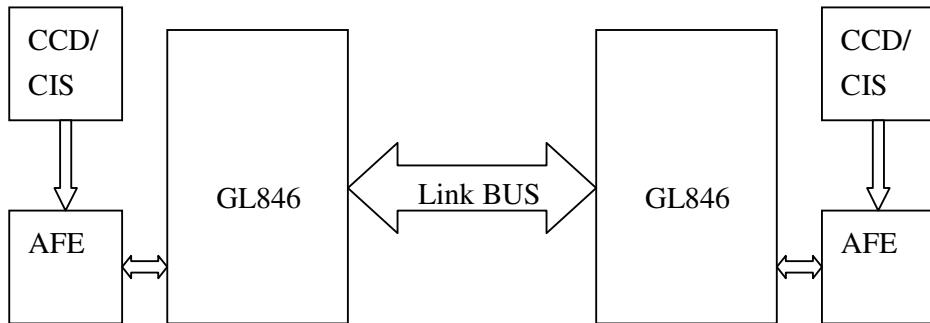
43 Support MCU with SPI interfaces for special application

GL846 can be as an external MCU SPI slave to receive any command and data from MCU which is as a SPI master.

```
┌──────────────┐                      ┌──────────────┐
│              │                      │              │
│   GL846      │      SPI BUS         │   MCU        │
│              │  <============>      │              │
│   SPI Slave  │                      │   SPI Master │
│              │                      │              │
└──────────────┘                      └──────────────┘
```

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44 Support two chips application for fast dual head scanning

GL846 supports two chips operation to provide fast dual head scanning for double side scanning.

CHAPTER 7   ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings (Voltage Referenced to GND)

Table 7.1 - Absolute Maximum Ratings (Voltage Referenced to GND)

Symbol	Description	Min	Max
DVCC1	DC supply voltage	-0.5V	2.5V
AVDD1~3	DC supply voltage	-0.5V	4.6V
VccCore1~4	DC supply voltage	-0.5V	2.5V
VccIO1~6	DC supply voltage	-0.5V	4.6V
V_I	Input Voltage	-0.5V	6V
V_O	Output Voltage	-0.5V	4.6V
$V_{AI/O}$	DC input voltage for USB D+/D- pins	-0.5V	4.6V
T_{OPT}	Operating Temperature	0°C	70°C
T_{OSTG}	Storage Temperature	-60°C	+125°C

7.2 DC Characteristics (Digital Pins): 1.8 V Logic Core and 3.3V Pads

Table 7.2 - DC Characteristics (Digital Pins): 1.8 V Logic Core and 3.3V Pads

SYMBOL	Description	Min	Typ.	Max	Unit
DVCC1	Power Supply Voltage	1.62	1.8	1.98	V
AVDD1~3	Power Supply Voltage	3.0	3.3	3.6	V
VccCore1~4	Power Supply Voltage	1.62	1.8	1.98	V
VccIO1~6	Power Supply Voltage 3.3V	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_T	Threshold point	1.45	1.58	1.74	V
V_{T+}	Schmitt trig. Low to High threshold point	1.44	1.50	1.56	V
V_{T-}	Schmitt trig. High to Low threshold point	0.89	0.94	0.99	V
V_J	Junction Temperature	0	25	125	°C
I_L	Input Leakage Current			±10	µA
I_{oz}	Tri-State output leakage current			±10	µA
R_{PU}	Pull-up Resistor	39K	65K	116K	Ω
R_{PD}	Pull-down Resistor	40K	56K	108K	Ω
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	2.4			V
I_{OL}	Low level output current @ V_{OL} =0.4V excluding D+/D-/VCC/GND	18.9	31.8	39.8	mA
I_{OH}	Low level output current @ V_{OH}=2.4V excluding D+/D-/VCC/GND	22	47.7	76	mA

7.3 DC Characteristics (D+/D-)
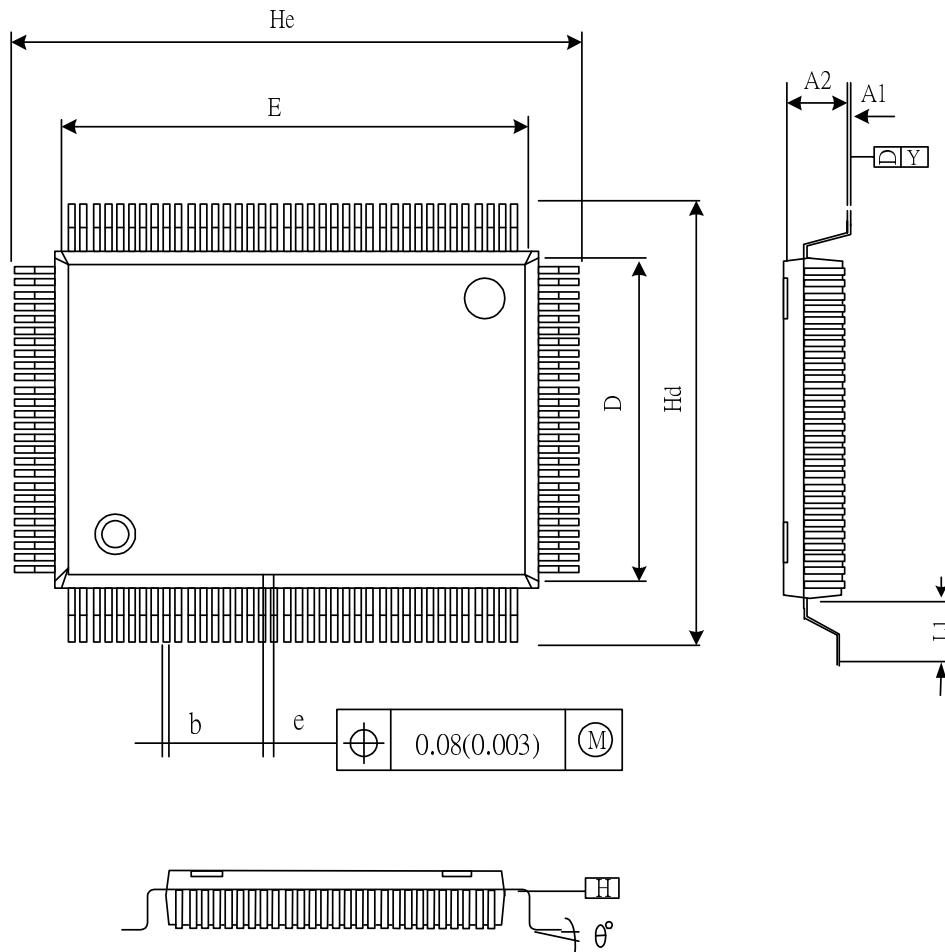
Table 7.3 - DC Characteristics (D+/D-)

SYMBOL	Description	Min	Typ.	Max	Unit
V_{OL}	D+/D- static output LOW(R_L of 1.5K to 3.6V)			0.3	V
V_{OH}	D+/D- static output HIGH (R_L of 15K to GND)	2.7		3.6	V
V_{DI}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold	0.2			V
C_{IN}	Transceiver capacitance			10	pF
I_{LO}	Hi-Z state data line leakage	-10		+10	µA
Z_{DRV}	Driver output resistance	40.5		49.5	Ω
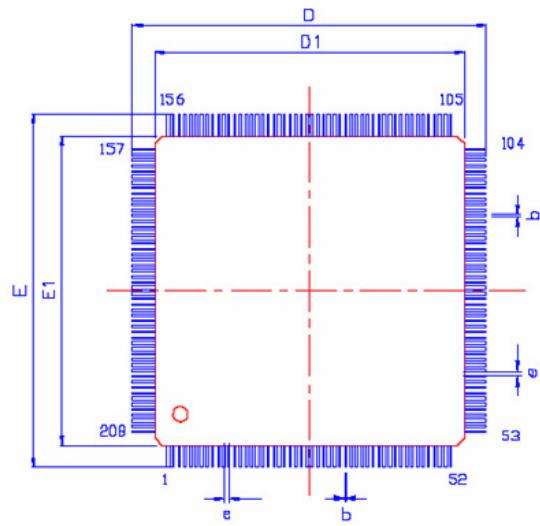
CHAPTER 8   PACKAGE DIMENSION

QFP-128L (14*20 mm, F/P: 3.2 mm):

SYMBOLS	MIN(mm)	NOM(mm)	MAX(mm)
A1	0.25	0.35	0.45
A2	2.57	2.72	2.87
b	0.10	0.20	0.30
C	0.10	0.15	0.20
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e	-	0.50	-
Hd	17.00	17.20	17.40
He	23.00	23.20	23.40
L	0.65	0.80	0.95
L1	-	1.60	-
Y	-	-	0.08
Θ	0	-	12
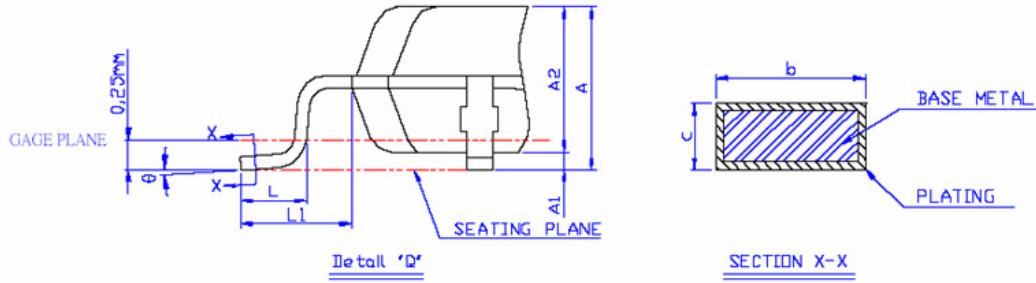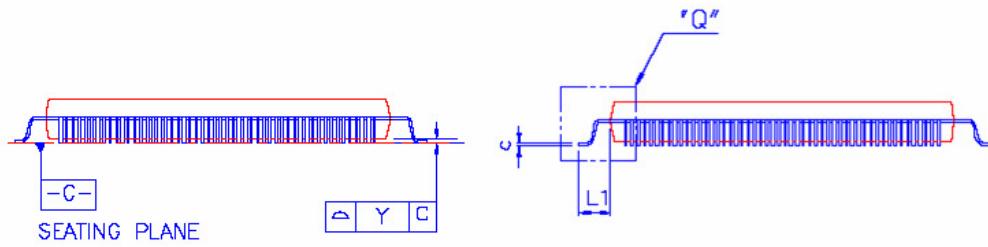
Figure 8.1 - GL846 128 Pin QFP Package

| SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	4.10 (161)
A1	0.25 (10)	---	---
A2	3.20 (126)	3.32 (131)	3.60 (142)
b	0.17 (7)	0.20 (8)	0.27 (11)
c	0.11 (4)	0.15 (6)	0.23 (9)
D	31.20 (1228) BSC		
D1	28.00 (1102) BSC		
E	31.20 (1228) BSC		
E1	28.00 (1102) BSC		
e	0.50 (20) BSC		
L	0.73 (29)	0.88 (35)	1.03 (41)
L1	1.60 (63) REF		
Y	---	---	0.10 (4)
θ	0°	---	7°

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

Figure 8.2- GL846 208 Pin QFP Package