

# MOS INTEGRATED CIRCUIT

## $\mu$ PD5205

### C-MOS ANALOG MULTIPLEXER

#### DESCRIPTION

The  $\mu$ PD5205 is 8-channel C-MOS analog multiplexer. A single-pole 8-position mode and double-pole 4-position mode are settable by 8/4 terminal. TTL/C-MOS compatible input threshold ( $\overline{EN}$ ,  $\overline{CS}$ ,  $\overline{WR}$ , RS) make the circuit directly driven by microprocessor. Further advantage each switch has low ON resistance, low leak current and wide analog input range. By these features, the  $\mu$ PD5205 is the optimum choice for data acquisition system.

#### TYPICAL CHARACTERISTICS

- Wide Supply Voltage: 44 V
- Low ON Resistance: 270  $\Omega$  TYP. ( $T_a = 25^\circ\text{C}$ )
- Low Source OFF Leak Current: 5 nA MAX. ( $T_a = 25^\circ\text{C}$ )
- Low Drain ON/OFF Leak Current: 20 nA MAX. ( $T_a = 25^\circ\text{C}$ )
- Guaranteed Break-Before-Make Operation

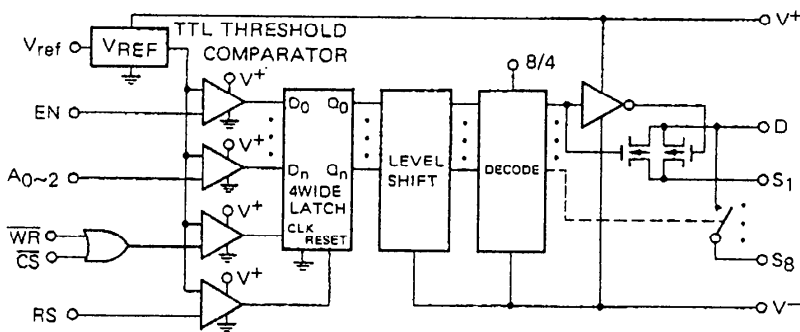
#### FEATURES

- A single-pole 8 position mode and double-pole 4 position mode are settable.
- TTL/C-MOS compatible digital input level. ( $\overline{EN}$ ,  $\overline{CS}$ ,  $\overline{WR}$ , RS)
- Analog input voltage range includes  $V^+$  and  $V^-$ .

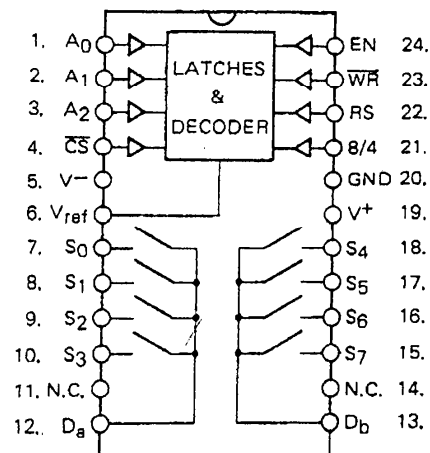
#### ORDERING INFORMATION

Part Number	Package
$\mu$ PD5205CA	24PIN PLASTIC SHRINK DIP (300 mil)
$\mu$ PD5205G	24PIN PLASTIC SOP (300 mil)

#### EQUIVALENT CIRCUIT



#### CONNECTION DIAGRAM (Top View)



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ABSOLUTE MAXIMUM RATINGS ( $T_a=25\text{ }^\circ\text{C}$ )

Supply Voltage between $V^+$ and $V^-$	$V^+ - V^-$	44	V
Supply Voltage between $V^+$ and GND	$V^+ - \text{GND}$	25	V
Supply Voltage between GND and $V^-$	$\text{GND} - V^-$	25	V
Input Current (Digital Input and S, D)		30	mA
Continuous Current between Source and Drain		20	mA
Peak Current between Source and Drain (Pulsed at 1 ms, 10 % Duty Cycle Max.)		40	mA
Power Dissipation	$P_t$	570	mW
Operating Temperature	$T_{opt}$	-20 to +85	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +125	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ( $T_a=25\text{ }^\circ\text{C}$ )

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{\pm}$	$\pm 8$	$\pm 15$	$\pm 16$	V
Low Level Logic Input Voltage (at $V_{\pm} = \pm 15\text{ V}$ )	$V_{INL}$			0.8	V
High Level Logic Input Voltage (at $V_{\pm} = \pm 15\text{ V}$ )	$V_{INH}$	2.4			V
Minimum Write Pulse Width ( $T_a = T_{opt}$ )	$t_{WW}$	300			ns
Data Settling Time ( $T_a = T_{opt}$ )	$t_{DW}$	100			ns
Data Hold Time ( $T_a = T_{opt}$ )	$t_{WD}$	180			ns
Minimum Reset Pulse Width ( $T_a = T_{opt}$ )	$t_{RS}$	500			ns

ELECTRICAL CHARACTERISTICS (V±=±15 V, GND=0)

CHARACTERISTIC	SYMBOL	TYP.	MAX.				UNIT	TEST CONDITIONS
		25 °C	-20 °C	25 °C	85 °C			
Analog Input Voltage	V <sub>ANALOG</sub>	±15		±15		±15	V	
Drain-Source ON Resistance	R <sub>DS(ON)</sub>	270 230	450	450	550	550	Ω	V <sub>D</sub> =10 V V <sub>D</sub> =-10 V V <sub>INL</sub> =0.8 V V <sub>INH</sub> =2.4 V I <sub>S</sub> =-200 μA
Drain-Source ON Resistance Matching (Between Channels)	ΔR <sub>DS(ON)</sub>	6					%	$\frac{R_{DS(ON) \text{ MAX.}} - R_{DS(ON) \text{ MIN.}}}{R_{DS(ON) \text{ AVERAGE}}}$ -10 V ≤ V <sub>S</sub> ≤ 10 V
Source OFF Leakage Current	I <sub>S(OFF)</sub>	-0.005 -0.005		±5	±50	±50	nA	V <sub>S</sub> =10 V V <sub>D</sub> =-10 V V <sub>S</sub> =-10 V V <sub>D</sub> =10 V V <sub>EN</sub> =0
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	-0.008 -0.008		±20	+100	+100	nA	V <sub>D</sub> =10 V V <sub>S</sub> =-10 V V <sub>D</sub> =-10 V V <sub>S</sub> =10 V
Drain ON Leakage Current	I <sub>D(ON)</sub>	-0.015 -0.015		±20	+100	+100	nA	V <sub>D</sub> =V <sub>S(all)</sub> =10 V V <sub>D</sub> =V <sub>S(all)</sub> =-10 V V <sub>INL</sub> =0.8 V V <sub>INH</sub> =2.4 V
High Level Logic Input Current	I <sub>INH</sub>	-0.002 0.006		-10	10	-30	μA	V <sub>IN</sub> =2.4 V V <sub>IN</sub> =15 V
Low Level Logic Input Current	I <sub>INL</sub>	-0.002		-10	-30	-30	μA	V <sub>IN</sub> =0 V
Switching Time of Multiplexer	t <sub>transition</sub>	0.6		1			μs	
Break Before Make Interval	t <sub>open</sub>	0.2		0.5			μs	
Turn ON Time (EN, $\overline{WR}$ , $\overline{CS}$ )	t <sub>ON</sub>	0.5		1			μs	
Turn OFF Time (EN, RS, $\overline{CS}$ )	t <sub>OFF</sub>	0.5		1			μs	
Charge Injection	Q	20					pC	
OFF Isolation	OIRR	68					dB	V <sub>EN</sub> =0, R <sub>L</sub> =1 K, C <sub>L</sub> =15 pF, V <sub>S</sub> =7 V <sub>r.m.s.</sub> , f=500 kHz
Logic Input Capacitance	C <sub>in</sub>	2.5					pF	
Source OFF Capacitance	C <sub>S(OFF)</sub>	5					pF	V <sub>S</sub> =0, V <sub>EN</sub> =0, $\overline{WR}$ =0, C <sub>S</sub> =0, f=140 kHz
Drain OFF Capacitance	C <sub>D(OFF)</sub>	12					pF	V <sub>D</sub> =0, V <sub>EN</sub> =0, $\overline{WR}$ =0, C <sub>S</sub> =0, f=140 kHz

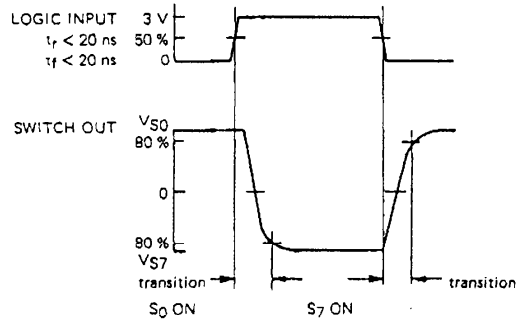
CHARACTERISTIC	SYMBOL	TYP.	MAX.			UNIT	TEST CONDITIONS
		25 °C	-20 °C	25 °C	85 °C		
Positive Supply Current	I <sup>+</sup>			2.5		mA	V <sub>EN</sub> =0, V <sub>AX</sub> =0
Negative Supply Current	I <sup>-</sup>			-1.5			V <sub>EN</sub> =0, V <sub>AX</sub> =0

Notes:

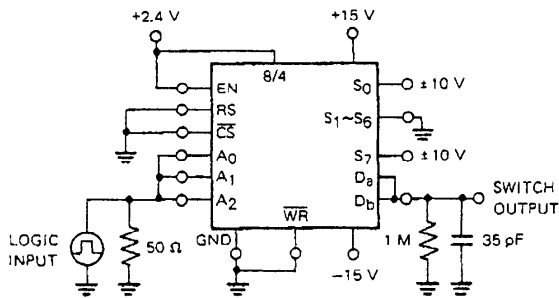
1. Please connect V<sup>-</sup> pin to the minimum voltage level and have a care that V<sup>-</sup> will not go to open or not go to higher than GND pin.
2. Please connect N.C. pin (11, 14 pin) to GND in order to improve Off Isolation.
3.  $\mu$ PD5205G has large chip size. Therefore we recommend hot plate belt conveyer type reflow soldering for mounting. Wave soldering or infrared rays type reflow soldering methods are not recommendable because of their hard heat shock.

MEASUREMENT CIRCUIT

Fig. 1 Switching Time of Multiplexer



Single-pole 8 position mode



Double-pole 4 position mode

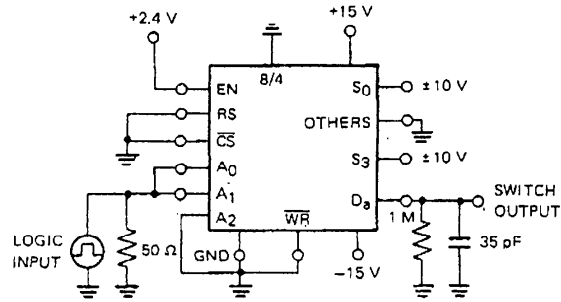


Fig. 2 Brake Before Make Interval

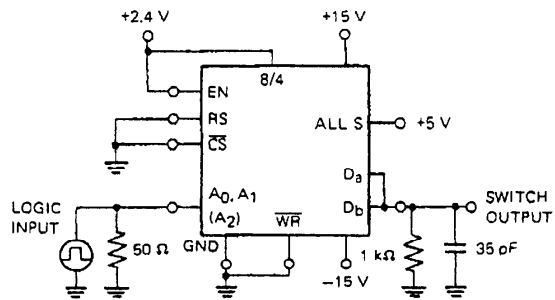
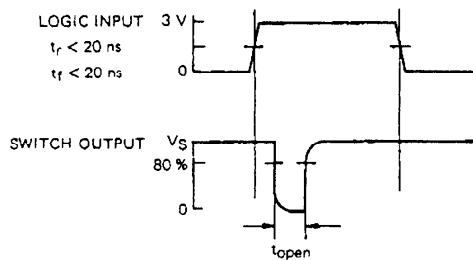


Fig. 3 Turn ON/OFF Time of EN

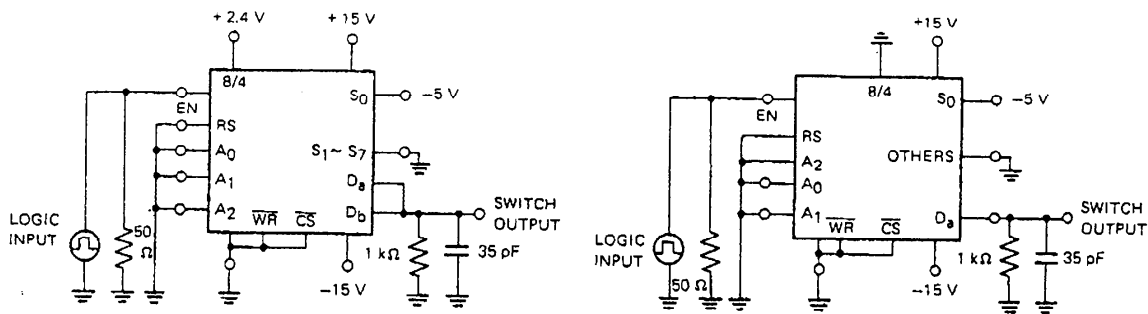
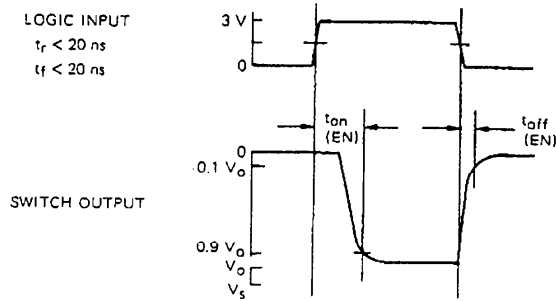


Fig. 4 Turn ON/OFF Time of  $\overline{\text{WR}}$

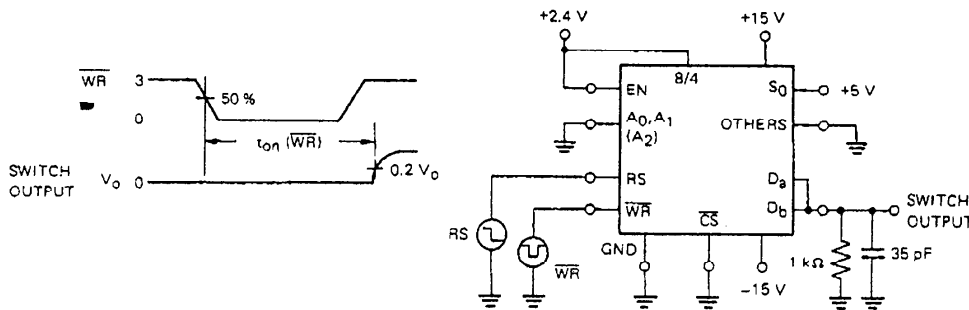


Fig. 5 Turn ON Time of RS

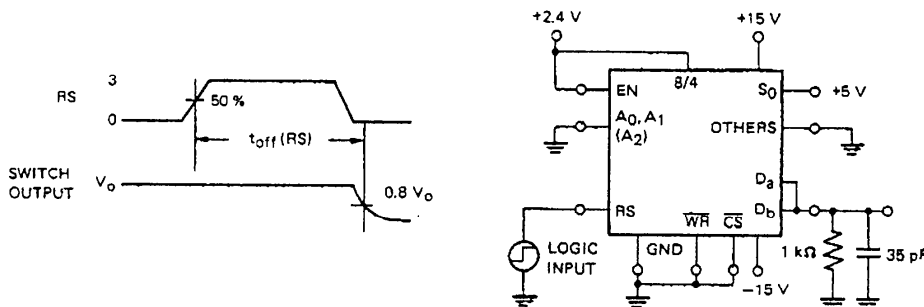


Fig. 6 Turn ON Time of  $\overline{CS}$

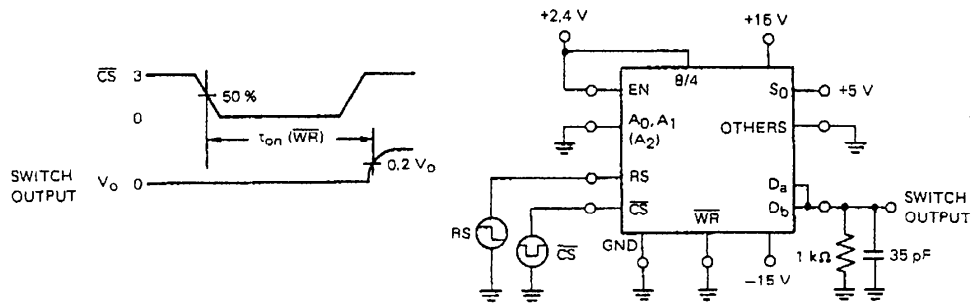
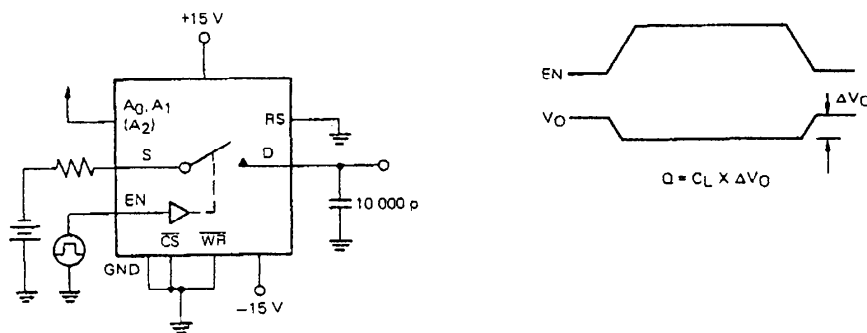


Fig. 7 Charge Injection



TIMMING CHART

Fig. 8 Data Settling/Hold Time

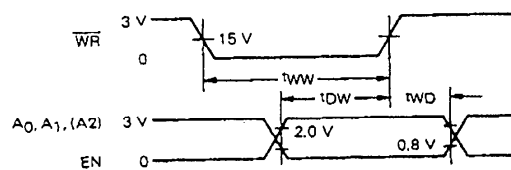
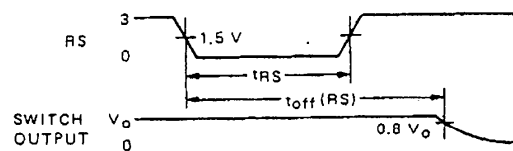


Fig. 9 Reset Pulse Width



## FUNCTION

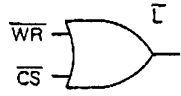
PIN	SYMBOL	FUNCTION
1	A <sub>0</sub>	SW Control Input
2	A <sub>1</sub>	SW Control Input
3	A <sub>2</sub>	SW Control Input
4	$\overline{CS}$	Chip Select. Active Low.
5	V <sup>-</sup>	Negative supply Voltage (-15 V)
6	V <sub>ref</sub>	Input threshold Level Control
7	S <sub>0</sub>	SW Input/Output
8	S <sub>1</sub>	SW Input/Output
9	S <sub>2</sub>	SW Input/Output
10	S <sub>3</sub>	SW Input/Output
11	N. C.	Non Connection (connect to GND)
12	D <sub>a</sub>	SW Input
13	D <sub>b</sub>	SW Input
14	N. C.	Non Connection (connect to GND)
15	S <sub>7</sub>	SW Input/Output
16	S <sub>6</sub>	SW Input/Output
17	S <sub>5</sub>	SW Input/Output
18	S <sub>4</sub>	SW Input/Output
19	V <sup>+</sup>	Positive Supply Voltage (+15 V)
20	GND	GND (0 V)
21	8/4	Mode Control ("H": 8channel, "L": 4channel)
22	RS	Reset
23	$\overline{WR}$	Write Request. Active Low.
24	EN	Enable



TRUTH TABLE

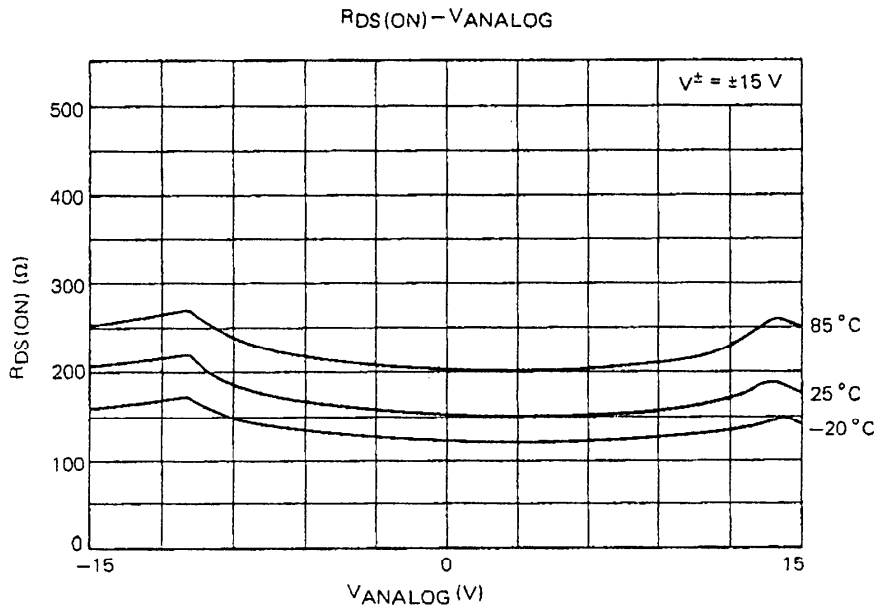
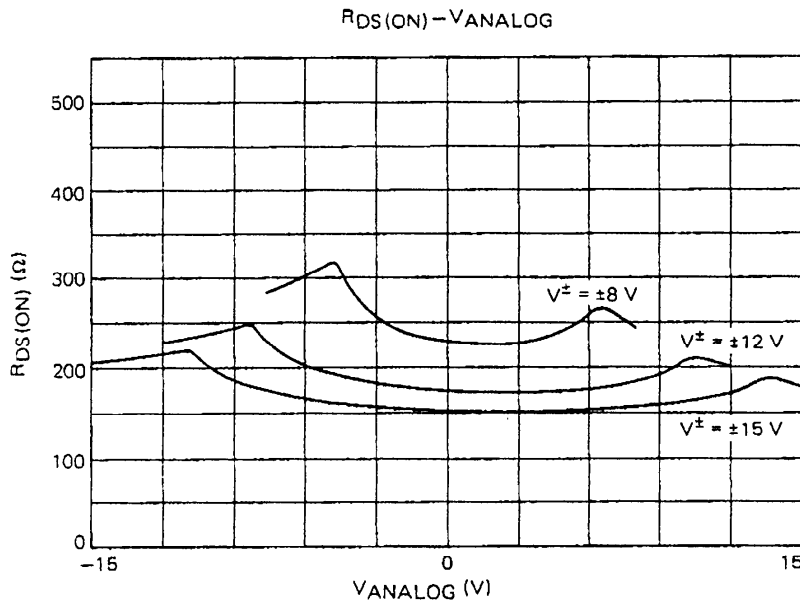
	EN	8/4	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	$\bar{L}$	RS	Ch 1				Ch 2				
								0	1	2	3	4	5	6	7	
	*	*	*	*	*		0	Latch								
	*	*	*	*	*	*	1	Latch Clear/SW OFF								
	0	*	*	*	*	0	0	SW OFF								
4 Ch * 2	1	0	*	0	0	0	0	ON				ON				
	1	0	*	0	1	0	0		ON				ON			
	1	0	*	1	0	0	0			ON				ON		
	1	0	*	1	1	0	0				ON					ON
8 Ch * 1	1	1	0	0	0	0	0	ON								
	1	1	0	0	1	0	0		ON							
	1	1	0	1	0	0	0			ON						
	1	1	0	1	1	0	0				ON					
	1	1	1	0	0	0	0					ON				
	1	1	1	0	1	0	0						ON			
	1	1	1	1	0	0	0							ON		
	1	1	1	1	1	0	0									ON

\* Don't Care



After reset, all switches remain off until chip select signal becomes active.

TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )



AC CHARACTERISTICS

Photo. 1 Switching Time of Multiplexer ( $V_{ANALOG} = \pm 10\text{ V}$ )

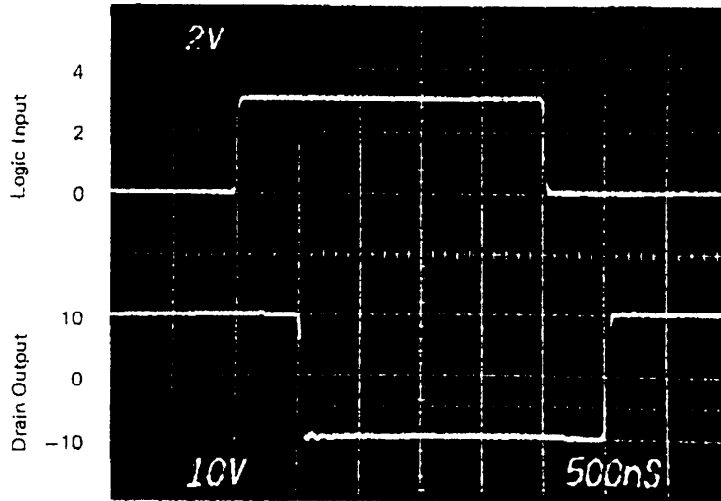


Photo. 2 Brake Before Make Interval ( $V_{ANALOG} = 5\text{ V}$ )

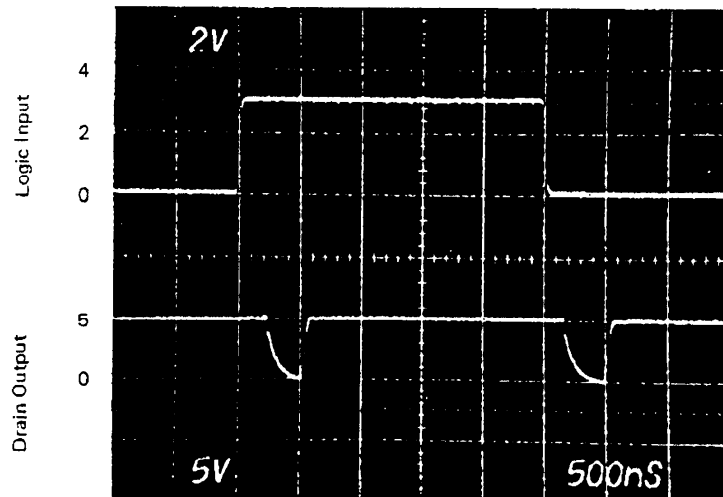


Photo. 3 Switch ON/OFF Time of EN ( $V_{ANALOG} = -5 V$ )

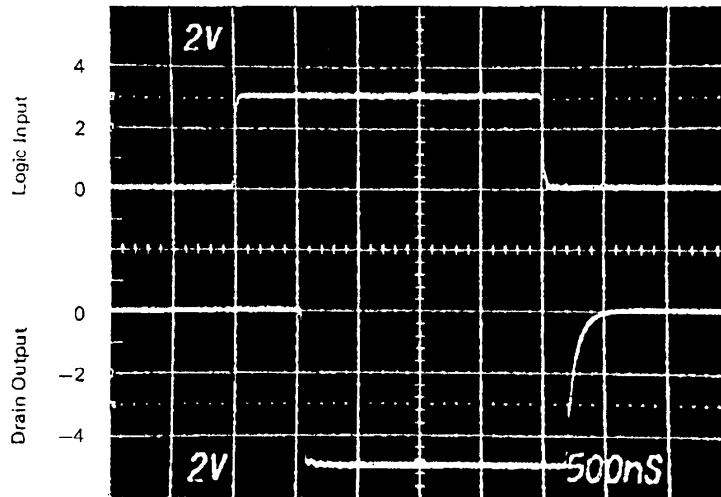


Photo. 4 Switch OFF Time of RS ( $V_{ANALOG} = 5 V$ )

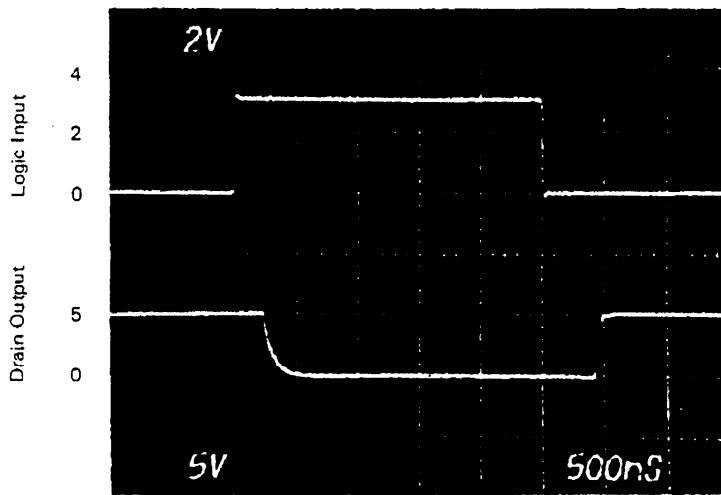
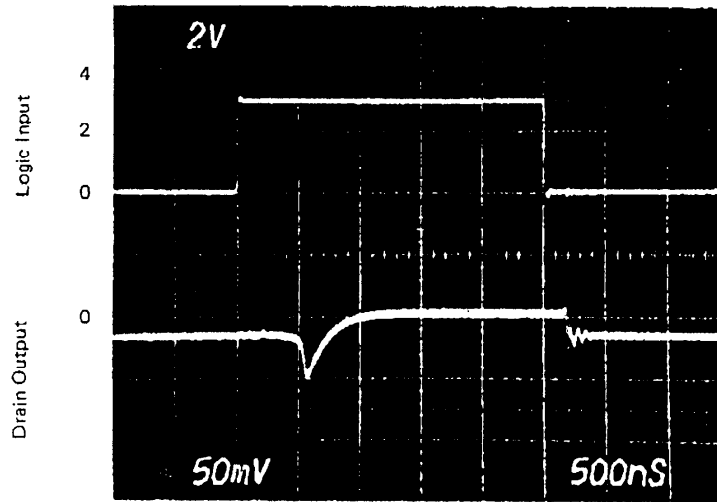
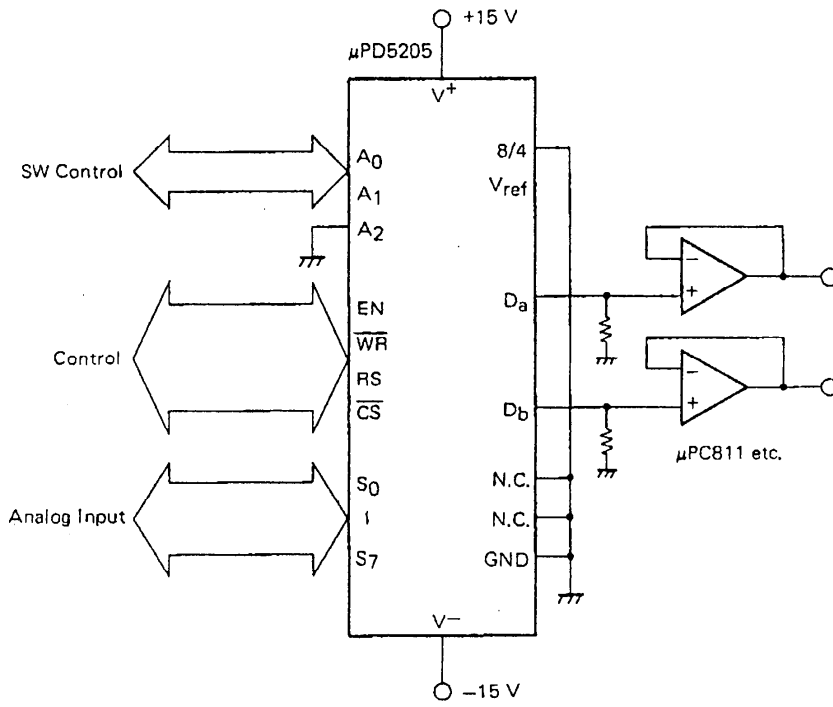


Photo. 5 Charge Injection

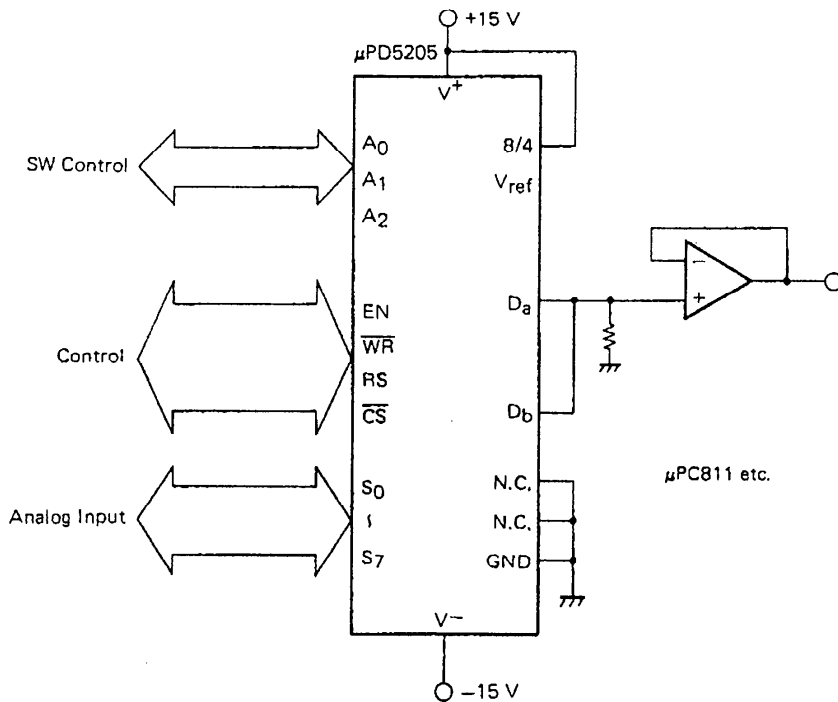


APPLICATION CIRCUIT

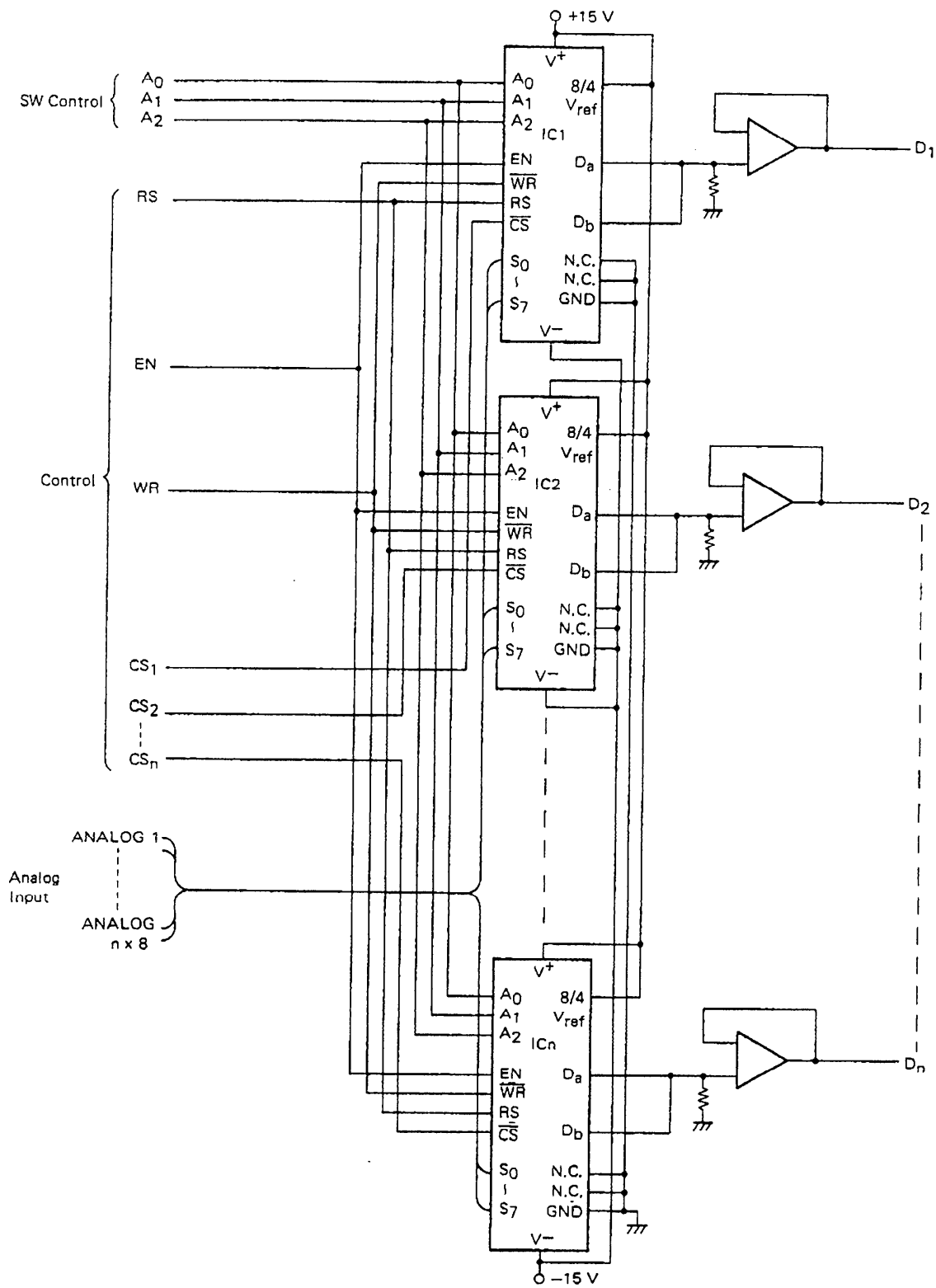
(1) Double-pole 4position mode



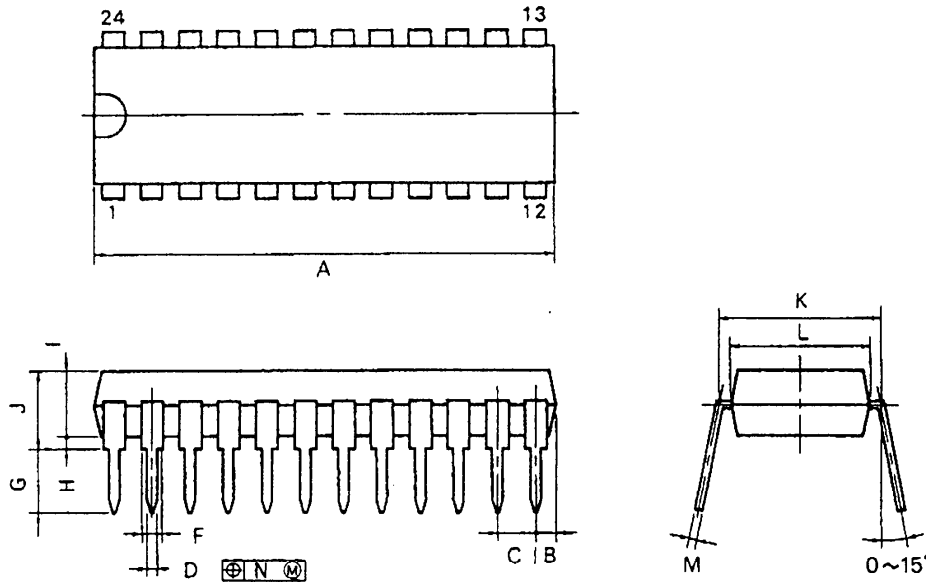
(2) Single-pole 8position mode



(3) Multi Connection



24PIN PLASTIC SHRINK DIP (300 mil)



S24C-70-3008

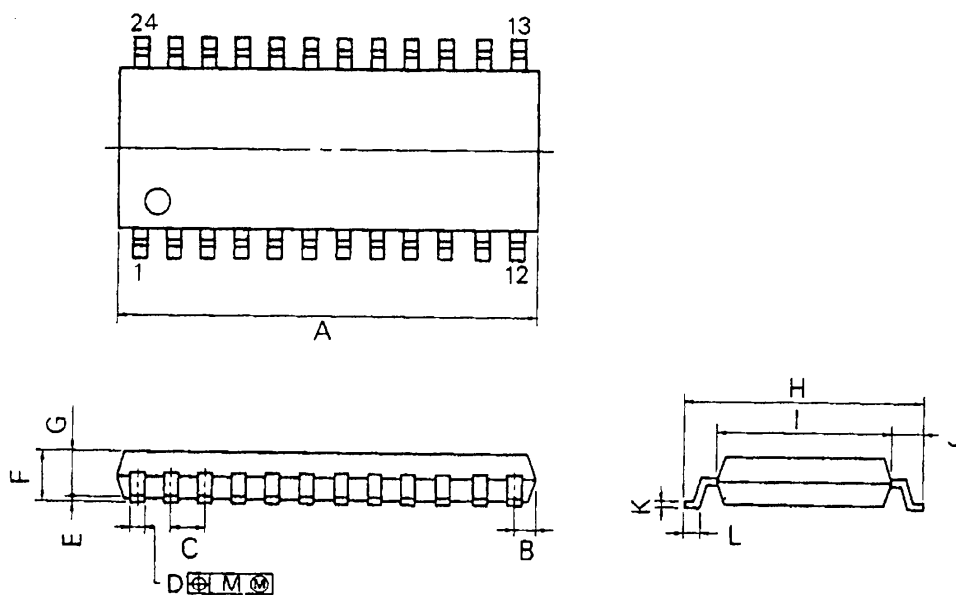
NOTES

- 1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ±0.10	0.020 ±0.004
F	0.85 MIN.	0.033 MIN.
G	3.2 ±0.3	0.126 ±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	0.25 ±0.08	0.010 ±0.003
N	0.17	0.007



24PIN PLASTIC SOP (300 mil)



P24GM-50-300B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 <sup>+0.10</sup> <sub>-0.08</sub>	0.016 <sup>+0.004</sup> <sub>-0.003</sub>
E	0.1 <sup>±0.1</sup>	0.004 <sup>±0.004</sup>
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 <sup>±0.3</sup>	0.303 <sup>±0.012</sup>
I	5.6	0.220
J	1.1	0.043
K	0.20 <sup>+0.10</sup> <sub>-0.08</sub>	0.008 <sup>+0.004</sup> <sub>-0.003</sub>
L	0.6 <sup>±0.2</sup>	0.024 <sup>+0.008</sup> <sub>-0.005</sub>
M	0.12	0.005

