G-LINK

GLT6400M16

Ultra Low Power 256k x 16 CMOS SRAM

Feb 2004(Rev. 1.2)

Features :

* Low-power consumption.
  -Active: 30mA Icc at 120ns.
  -Stand by :
  20 μA (CMOS input / output , LL)
  5 μA (CMOS input / output, SL)
* Single +2.3V to 2.7V Power Supply.
* Equal access and cycle time.
* 120 ns access time.
* Tri-state output.
* Automatic power-down when deselected.
* Multiple center power and ground pins for improved noise immunity.
* Individual byte controls for both Read and Write cycles.
* Industrial grade (-40°C ~ 85°C) available.
* Available in 48-fpBGA/44L TSOPII.
* CE2 pin available for fpBGA only.

Description :

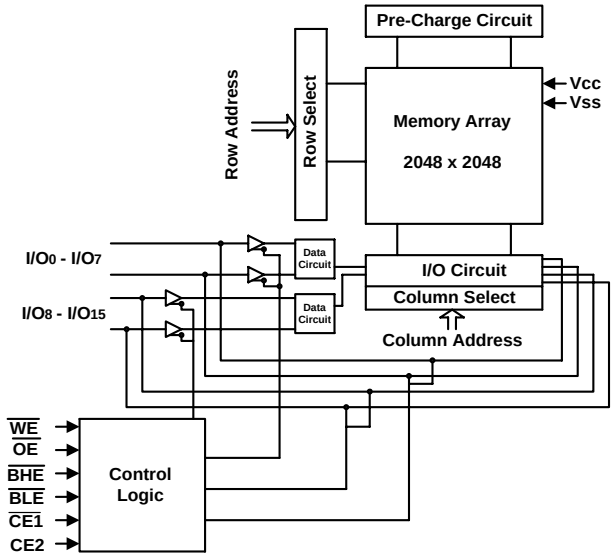
The GLT6400M16 is a low power CMOS Static RAM organized as 262,144 words by 16 bits. Easy memory expansion is provided by an active LOW **$\overline{CE1}$** and **$\overline{OE}$** pin and active HIGH CE2.

This device has an automatic power – down mode feature when deselected. Separate Byte Enable controls (**$\overline{BLE}$** and **$\overline{BHE}$**) allow individual bytes to be accessed. **$\overline{BLE}$** controls the lower bits I/O0 – I/O7. **$\overline{BHE}$** controls the upper bits I/O8 – I/O15.

Writing to these devices is performed by taking Chip Enable **$\overline{CE1}$** with Write Enable **$\overline{WE}$** and byte Enable (**$\overline{BLE}$** / **$\overline{BHE}$**) Low while CE2 remains HIGH.

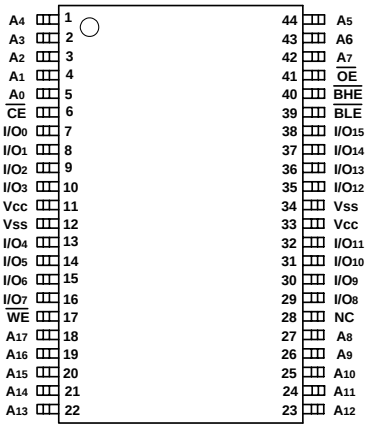
Reading from the device is performed by taking Chip Enable **$\overline{CE1}$** with Output enable **$\overline{OE}$** and byte Enable (**$\overline{BLE}$** / **$\overline{BHE}$**) Low while Write Enable **X \TO(WE)** and CE2 are held HIGH.

Function Block Diagram :

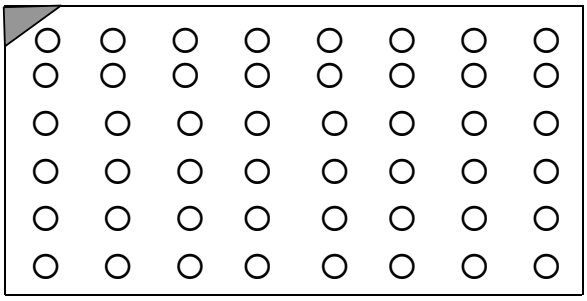


Pin Configurations :

GLT6400M16



48 Ball fpBGA :



	A	B	C	D	E	F	G	H
1	$\overline{\text{BLE}}$	I/O9	I/O10	Vss	Vcc	I/O15	I/O16	NC
2	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	I/O11	I/O12	I/O13	I/O14	NC	A8
3	A0	A3	A5	A17	NC	A14	A12	A9
4	A1	A4	A6	A7	A16	A15	A13	A10
5	A2	$\overline{\text{CE1}}$	I/O2	I/O4	I/O5	I/O6	$\overline{\text{WE}}$	A11
6	CE2	I/O1	I/O3	Vcc	Vss	I/O7	I/O8	NC

Note：NC means no Ball.

Pin Descriptions:

Name	Function
$A_0 – A_{17}$	Address Inputs
$\overline{CE}_1$ and CE_2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$I/O_0 – I/O_{15}$	Data Input and Data Output
V_{CC}	2.5V Power Supply
$\overline{BLE}$	Lower Byte Enable Input (I/O_0 to I/O_7)
$\overline{BHE}$	Higher Byte Enable Input (I/O_8 to I/O_{15})
GND	Ground
NC	No Connection

Truth Table:

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O0-I/O7	I/O8-I/O15	Power	Mode
H	X	X	X	X	X	High-Z	High-Z	Standby	Deselected
X	L	X	X	X	X	High-Z	High-Z	Standby	Deselected
X	X	X	X	H	H	High-Z	High-Z	Standby	Deselected
L	H	H	H	L	X	High-Z	High-Z	Active	Output Disabled
L	H	H	H	X	L	High-Z	High-Z	Active	Output Disabled
L	H	L	H	L	H	Data Out	High-Z	Active	Lower Byte Read
L	H	L	H	H	L	High-Z	Data Out	Active	Upper Byte Read
L	H	L	H	L	L	Data Out	Data Out	Active	Word Read
L	H	X	L	L	H	Data In	High-Z	Active	Lower Byte Write
L	H	X	L	H	L	High-Z	Data In	Active	Upper Byte Write
L	H	X	L	L	L	Data In	Data In	Active	Word Write

Note ; X means don care. (Must be low or high state).

Absolute Maximum Ratings*

Parameter	Symbol	Minimum	Maximum	Unit
Voltage on Any Pin Relative to Gnd	Vt	-0.5	Vcc + 0.5	V
Power Dissipation	P_T	-	1.0	W
Storage Temperature (Plastic)	Tstg	-55	+150	°C
Temperature Under Bias	Tbias	-25	+85	°C

*Note : Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions (TA = -25°C to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.3	2.5	2.7	V
	Gnd	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.0	-	V_{CC}+0.2	V
	V_{IL}	-0.2*	-	0.6	V

* V_{IL} min = -2.0V for pulse width less than $t_{RC}/2$.

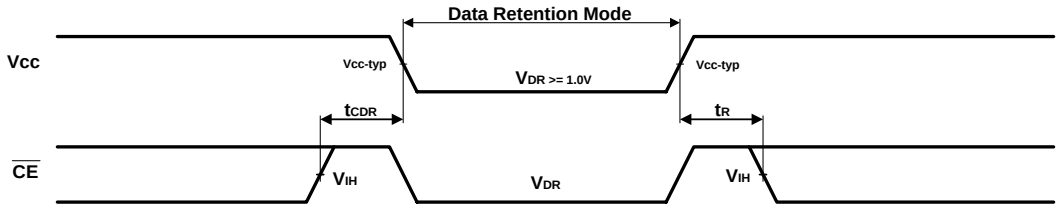
DC Operating Characteristics (Vcc=2.3 to 2.7V, T_A = -25°C to 85°C)

Parameter	Sym.	Test Conditions		120		Unit
				Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, Vin = Gnd to V_{CC}		-	1	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CE}$ =V_{IH} or V_{CC} = Max, V_{OUT} = Gnd to V_{CC}		-	1	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}$ =V_{IL} ,V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0		-	5	mA
Average Operating Current	I_{CC1}	I_{OUT} = 0mA, Min Cycle, 100% Duty		-	30	mA
	I_{CC2}	$\overline{CE}$ ≤ 0.2V I_{OUT} = 0mA, Cycle Time=1µs, 100% = Duty		-	5	mA
Standby Power Supply Current(TTL Level)	I_{SB}	$\overline{CE}$ =V_{IH}		-	0.3	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE}$ ≥ V_{CC}-0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC}-0.2V	GLT6400M16LL	-	20	µA
			GLT6400M16SL	-	5	µA
Output Low Voltage	V_{OL}	I_{OL} = 0.5 mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA		2.0	-	V

Data Retention

Parameter	Sym.	Test Conditions	Min.	Max.	Unit
V_{CC} for Data retention	V_{DR}	$\overline{CE}$ ≥ V_{CC} -0.2V	1.0	-	V
Data Retention Current	I_{CCDR}	CE2 ≤ +0.2V	-	4	µA
Chip Deselect to Data Retention Time	t_{CDR}	V_{IN} ≥ V_{CC} -0.2V or	0	-	ns
Operating Recovery Time[2]	t_R	V_{IN} ≤ 0.2V	t_{RC}	-	ns

Data Retention Waveform (TA = -25°C to +85°C)

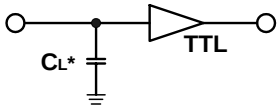


AC Test Conditions

Input Pulse Levels	0.4V to 2.2V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.1V

Output Load Condition
C_L = 30pf + 1TTL Load

AC Test Loads and Waveforms

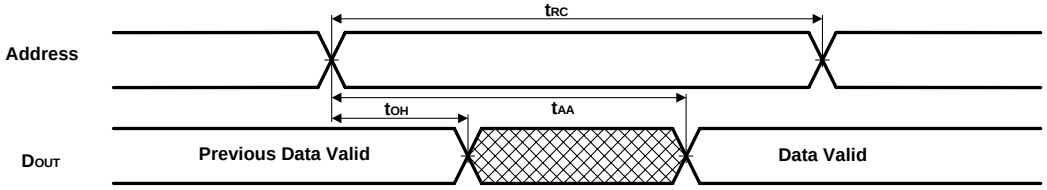


*Including Scope and Jig Capacitance

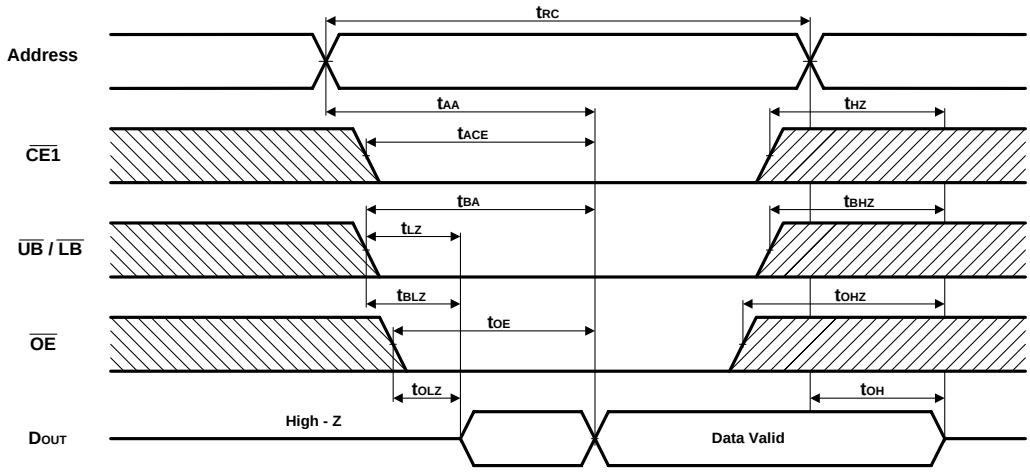
Read Cycle [9](Vcc=2.3V to 2.7V, T_A = -25°C to 85°C)

Parameter	Symbol	120		Unit	Note
		Min	Max		
Read Cycle Time	t_{RC}	120	-	ns	
Address Access Time	t_{AA}	-	120	ns	
Chip Enable Access Time	t_{ACE}	-	120	ns	
Output Enable Access Time	t_{OE}	-	60	ns	
Output Hold from address Change	t_{OH}	15	-	ns	
Chip Enable to Output in Low-Z	t_{LZ}	20	-	ns	4,5
Chip Disable to Output in High-Z	t_{HZ}	0	35	ns	3,4,5
Output Enable to Output in Low-Z	t_{OLZ}	20	-	ns	
Output Disable to Output in High-Z	t_{OHZ}	0	35	ns	
$\overline{BLE}$, $\overline{BHE}$ Enable to Output in Low-Z	t_{BLZ}	20	-	ns	4,5
$\overline{BLE}$, $\overline{BHE}$ Disable to Output in High-Z	t_{BHZ}	0	35	ns	3,4,5
$\overline{BLE}$, $\overline{BHE}$ Access Time	t_{BA}	-	60	ns	

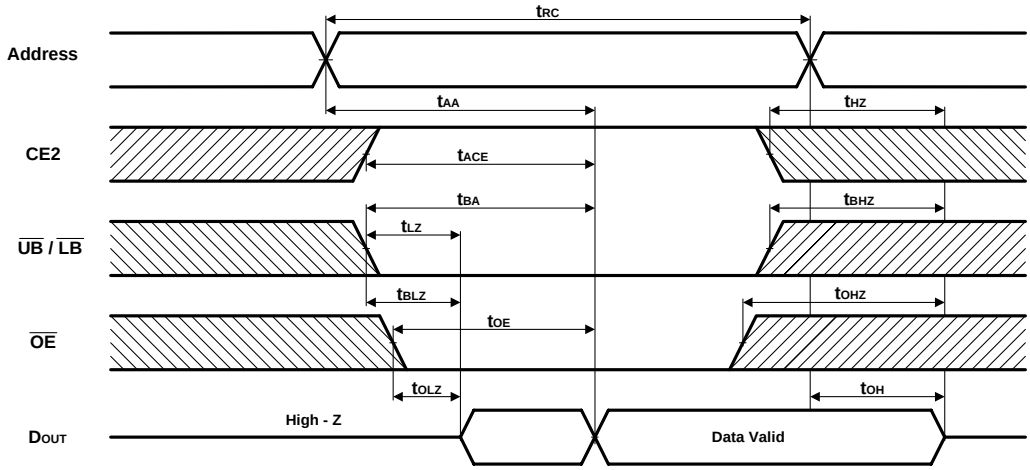
Timing Waveform of Read Cycle 1 (Address Controlled)



Timing Waveform of Read Cycle 2 (3~5)



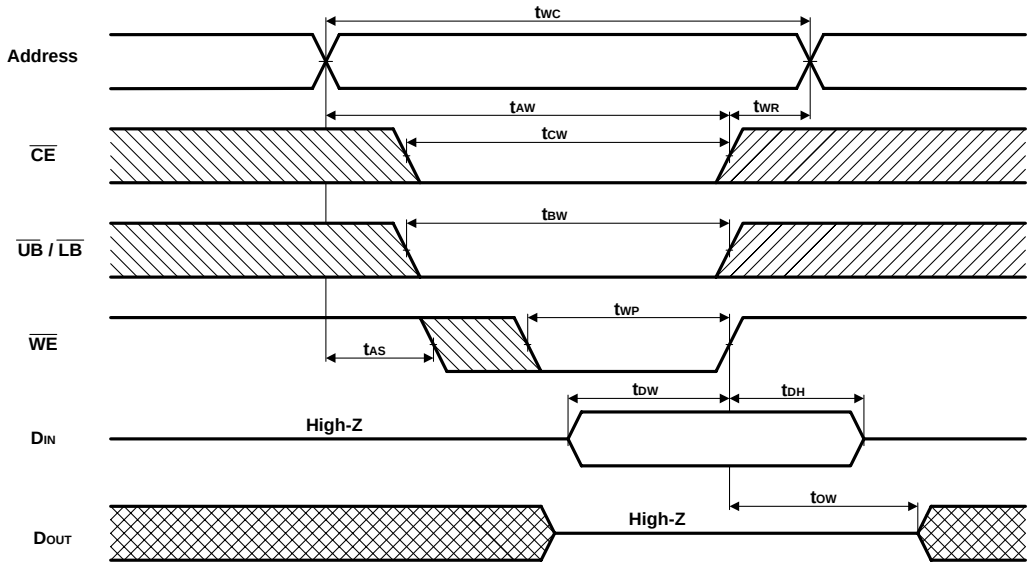
Timing Waveform of Read Cycle 3 (3~5)



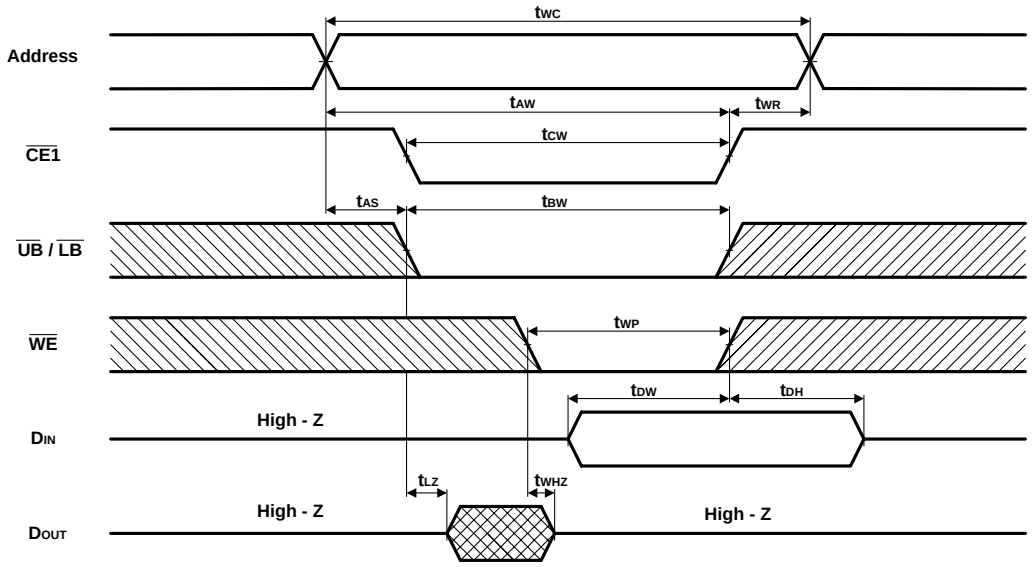
Write Cycle [11](Vcc=2.3 to 2.7V, T_A = -25°C to 85°C)

Parameter	Symbol	120		Unit	Note
		Min	Max		
Write Cycle Time	t_{WC}	120	-	ns	
Chip Enable to Write End	t_{CW}	100	-	ns	
Address Setup to Write End	t_{AW}	100	-	ns	
Address Setup Time	t_{AS}	0	-	ns	
Write Pulse Width	t_{WP}	80	-	ns	
Write Recovery Time	t_{WR}	0	-	ns	
Data Valid to Write End	t_{DW}	50	-	ns	
Data Hold Time	t_{DH}	0	-	ns	
Write Enable to Output in High-Z	t_{WHZ}	0	35	ns	
Output Active from Write End	t_{OW}	5	-	ns	
$\overline{BLE}$, $\overline{BHE}$ Setup to Write End	t_{BW}	100	-	ns	

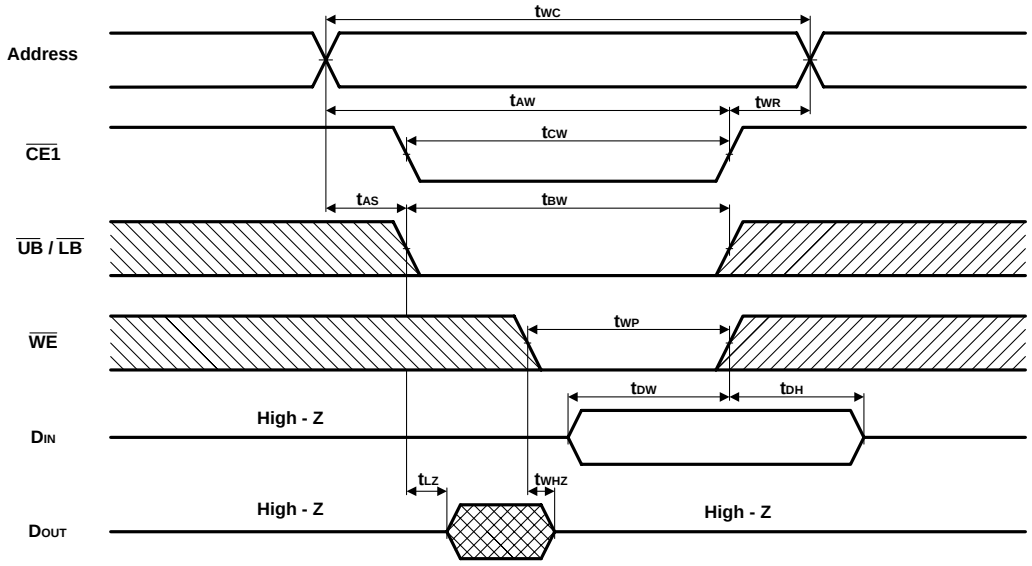
Timing Waveform of Write Cycle 1 (Address Controlled)[2~6,8]



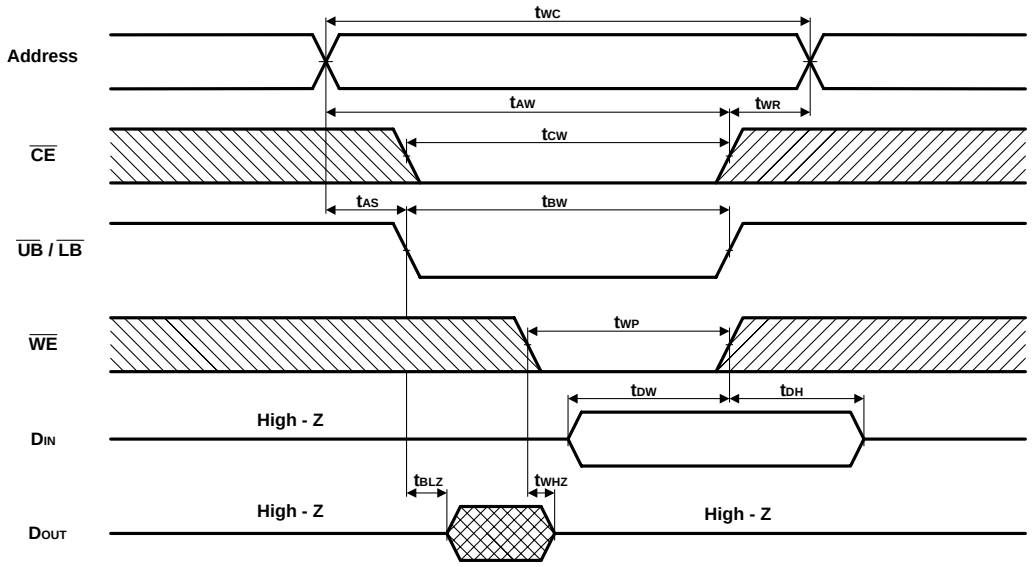
Timing Waveform of Write Cycle 2 ($\overline{CE}$ Controlled)(2~6,8)



Timing Waveform of Write Cycle 3 (CE2 Controlled)(2~6,8)



Timing Waveform of Write Cycle 4 ($\overline{UB}$ / $\overline{LB}$ Controlled)[2~6,8]



Notes :

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see AC Test Condition.
4. This parameter is tested with CL = 5pF. Transition is measured ± 500mV from steady – state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{CE1}$ transition LOW or CE2 transition HIGH.
9. All read cycle timings are referenced from the last valid address to the first transition address.
10. $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 must be LOW during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

Ordering Information

Part Number	*SPEED*	*POWER*	*PACKAGE*
GLT6400M16LL-120TC	120ns	Normal	TSOPII 44L
GLT6400M16SL-120TC	120ns	Normal	TSOPII 44L
GLT6400M16LLI-120TC	120ns	Normal	TSOPII 44L
GLT6400M16SLI-120TC	120ns	Normal	TSOPII 44L

Parts Numbers (Top Mark) Definition :

GLT 6 400 M 16 LL I - 120 TC

4 : DRAM
5 : Synchronous DRAM
6 : Standard SRAM /Pseudo SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM
9 : SGRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M
200 : 2M
400 : 4M

-DRAM
10 : 1M(C/EDO)
11 : 1M(C/FPM)
12 : 1M(H/EDO)
13 : 1M(H/FPM)
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
160 : 16M(EDO)
161 : 16M(FPM)
640 : 64M(EDO)
641 : 64M(FPM)

-SDRAM
40 : 4M
160 : 16M
320 : 32M,4Bank
640 : 64M
1280 : 128M

-PSEUDO SDRAM
020 – 2M
160 – 16M
320 – 32M

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

VOLTAGE
Blank : 5V
L : 3.3V
M : 2.5V
N : 2.0V

POWER
Blank : Standard
L : Low Power
LL : Low Low Power
SL : Super Low Power

SPEED
-SRAM/PSEUDO SRAM
12 : 12ns
15 : 15ns
20 : 20ns
55 : 55ns
70 : 70ns
85 : 85ns
120 : 120ns

-DRAM
25 : 25ns
28 : 28ns
30 : 30ns
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns
70 : 70ns
80 : 80ns
100 : 100ns

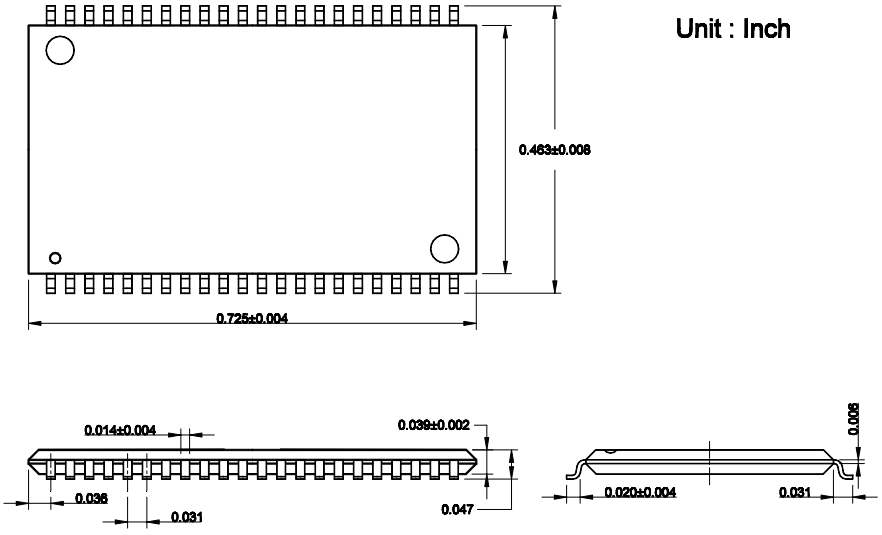
-SDRAM
5 : 5ns/200 MHZ
5.5 : 5.5ns/183 MHZ
6 : 6ns/166 MHZ
7 : 7ns/143 MHZ
8 : 8ns/125 MHZ
10 : 10ns/100 MHZ

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
ST : sTSOP(Type I)
TC : TSOPII (40/44)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP
FG : 48Pin BGA 9x12
FH : 48Pin BGA 8x10
FI : 48Pin BGA 6x8
FJ : 60Ball VFBGA

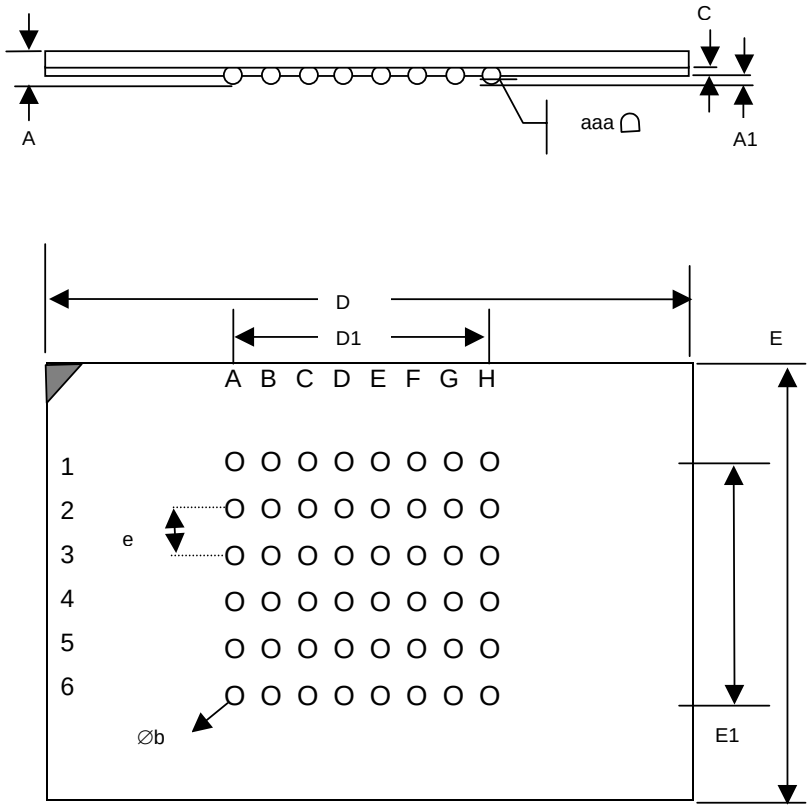
Temperature Range
E : Extended Temperature
II : Industrial Temperature
Blank : Commercial Temperature
P : Pb – free part

Package Information

44 pin Small Outline J-form Package (TSOPII)



GLT6400M16 fpBGA



PACKAGE OUTLINE DWG.

SYMBOL	UNIT : MM
A	1.10±0.1
A1	0.22±0.05
∅b	0.35
C	0.32TYP
D	10.00±0.10
D1	5.25
E	8.00±0.10
E1	3.75
e	0.75TYP
aaa	0.10