Application Considerations for Silicon Carbide MOSFETs

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Introduction

The silicon carbide (SiC) MOSFET has unique capabilities that make it a superior switch when compared to its silicon counterparts. The advantages of SiC MOSFETs have been documented extensively in the literature [1]. However, there are some unique operating characteristics that need to be understood so that the device can be used to its full potential.

Discussion

The key to successfully applying the SiC MOSFET requires an understanding of the device's unique operating characteristics. In this section, the characteristics of Cree's 1200V 80mΩ SiC MOSFET (CMF20120D) will be discussed. Comparisons will be made with other similar silicon devices along with application implications. The intention of this comparison is to illustrate the differences in operating characteristics, not to pick the best device. The comparison silicon devices are as follows:

- 900V, 0.12 Ω Si super junction MOSFET (SJMOSFET) Infineon IPW90R120C3 [2]
- 1.2 kV, 20 A trench/field stop (TFS) Si IGBT Fairchild FGA20N120FGD [3]
- 1.2 kV, 20 A non-punch though (NPT) Si IGBT International Rectifier IRGP20B120U [4]
- 1.2 kV, 0.30 Ω Si MOSFET (Si MOS8) Microsemi APT34M120J [5]

The devices selected for comparison are representative of commercially available Si IGBTs and MOSFETs with voltage and current ratings similar to the CMF20120D. The TFS IGBT is representative of a low on-voltage device and the NPT IGBT is representative of a low turn-off loss device. The Si MOS8 is representative of a commercially available 1.2kV Si MOSFET. Lastly, although not a 1.2kV device, the 900V SJMOSFET data was included for comparison purposes. All comparisons were made with measured data except in the case of the SJMOSFET. Data sheet values were used.

Consider the output characteristics of a typical Cree CMF20120D and the Si TFS IGBT shown in Figure 1. For the CMF20120D, the transition from triode (ohmic) to saturation (constant current) regions is not as clearly defined as it is for the Si TFS IGBT. This is a result of the modest transconductance of the device. The modest amount of transconductance causes the transition from triode to saturation to be spread over a wider range of drain current. The result is that the CMF20120D behaves more like a voltage controlled resistance than a voltage controlled current source.

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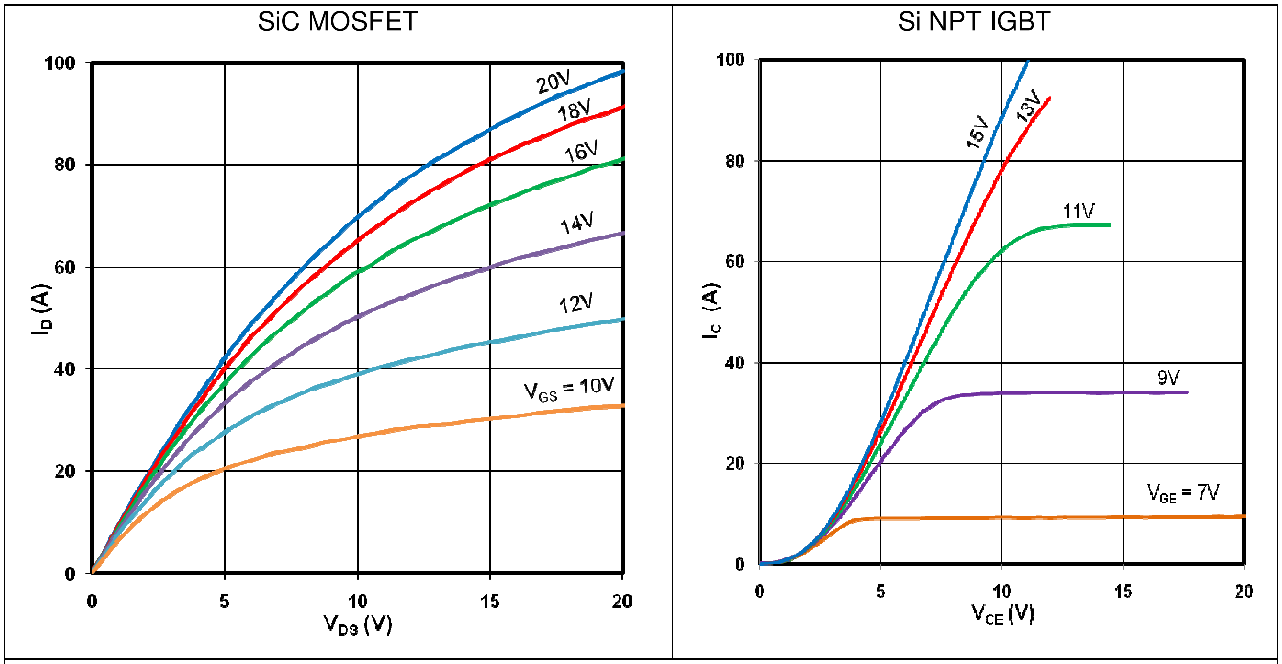

Figure 1: Output characteristics comparison (T_J = 150 ℃)

The modest transconductance and short-channel effects are important to consider when applying the device. The CMF20120D needs to be driven with a higher gate voltage swing than what is customary with SJMOSFETS or IGBTs. Presently, a +20V and -2V to -5V negative bias gate drive is recommended for the CMF20120D. Care needs to be taken not to exceed -5V in the negative direction. The rate of rise of gate voltage will have a greater effect on the rate of rise of the drain current due to the lower transconductance. Therefore, the gate drive needs to supply a fast rise and fall time gate pulse to maximize switching speed. The CMF20120D also has a threshold voltage similar to the Si SJMOSFET (2V nominal). Like the Si SJMOSFET, considerations need to be made for the lower threshold voltage, especially at high temperatures.

The rather large triode region can have an impact on certain types of fault detection schemes, chiefly the active de-saturation circuits. Some of these designs assume that the switching device enters a fairly high impedance constant current and/or transconductance saturation region during over-current faults. For the CMF20120D , the output impedance is lower and the device does not go into a clean constant current region during this type of over-current fault, especially under moderate over-currents. Therefore, the drain to source voltage will not increase as much. These characteristics of the SiC MOSFET need to be carefully considered in fault protection schemes.

The forward conduction characteristics of the CMF20120D along with the Si SJMOSFET, TFS, and NPT IGBTs are presented in Figure 2. The Si SJMOSFET's relatively high positive temperature coefficient of $R_{DS(on)}$ has a considerable effect on its conduction losses. At 25 ℃, the Si SJMOSFET and CMF20120D were somewhat similar. At 150 ℃, the $R_{DS(on)}$ of the CMF20120D increases by only about 20% from 25 ℃ to 150 ℃, whereas both the Si SJMOSFET and Si MOS8 devices increase by 250%. This has a significant effect on system thermal design. The obvious advantage is that a smaller device can be used at higher operating temperatures.

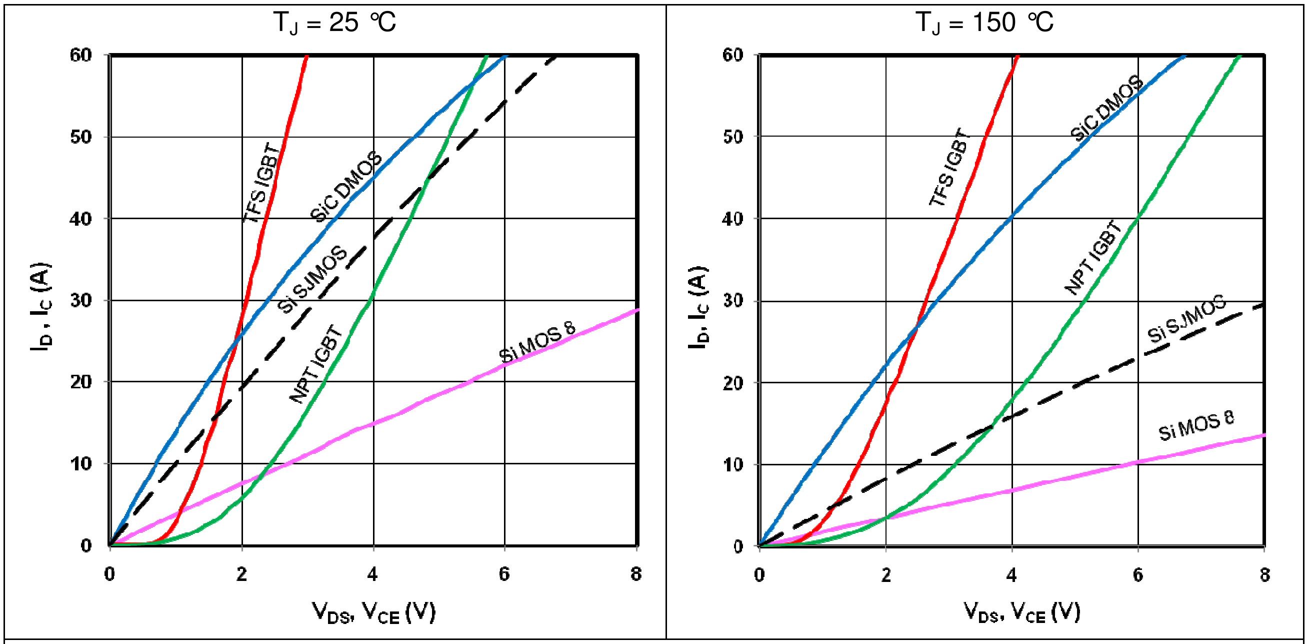

Figure 2: Forward conduction characteristics comparison (V_{GS} = 20V, V_{GE} = 15V)

One of the key advantages to SiC is the high temperature capability afforded by the wide bandgap. This is clearly reflected in the leakage current comparison at elevated temperature shown in Figure 3. The CMF20120D has about 20x lower leakage current at 150 °C. At 200 °C, the Si comparison parts leakage current increases dramatically, to the point where the device fails due to excess power dissipation. The CMF20120D leakage current is still acceptable at this temperature and is over 100x lower than the Si devices.

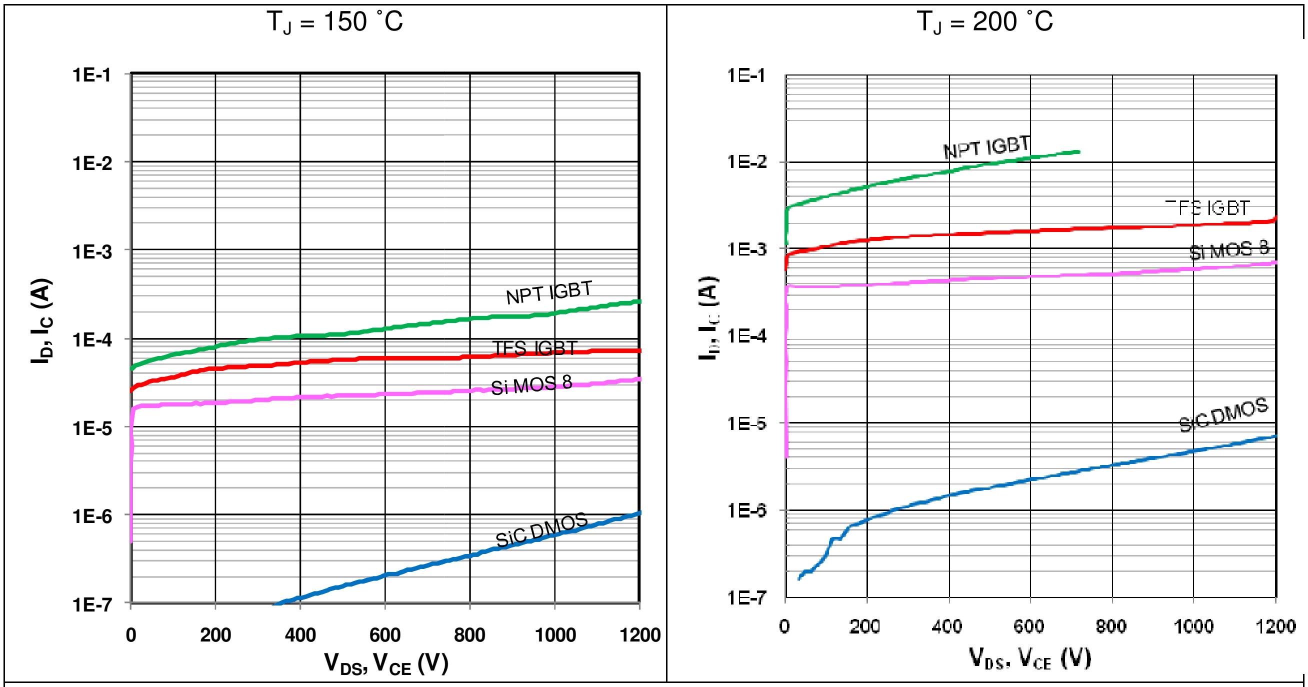

Figure 3: High temperature leakage current comparison

As previously mentioned, the recommended gate drive voltage for the CMF20120D is +20V and -2V to -5V negative bias. However, the amount of gate charge required to switch the device is low. The ramifications of the modestly higher gate voltage and lower gate charge can be reconciled by using the product of gate charge and gate voltage as a metric of gate energy. The gate charge and gate energy comparison is shown in Figure 4. Even though the operating conditions are not exactly matched, the results of this comparison show that the CMF20120D gate energy is comparable to or lower than the other devices. Therefore, the higher voltage swing does not adversely affect gate drive power requirements. The CMF20120D V_{GS} versus gate charge characteristics are somewhat different from what is usually experienced with other gate controlled silicon devices. The Miller plateau is not as flat as observed in typical silicon MOSFETs and IGBTs. Once again, this is primarily due the modest amount of transconductance.

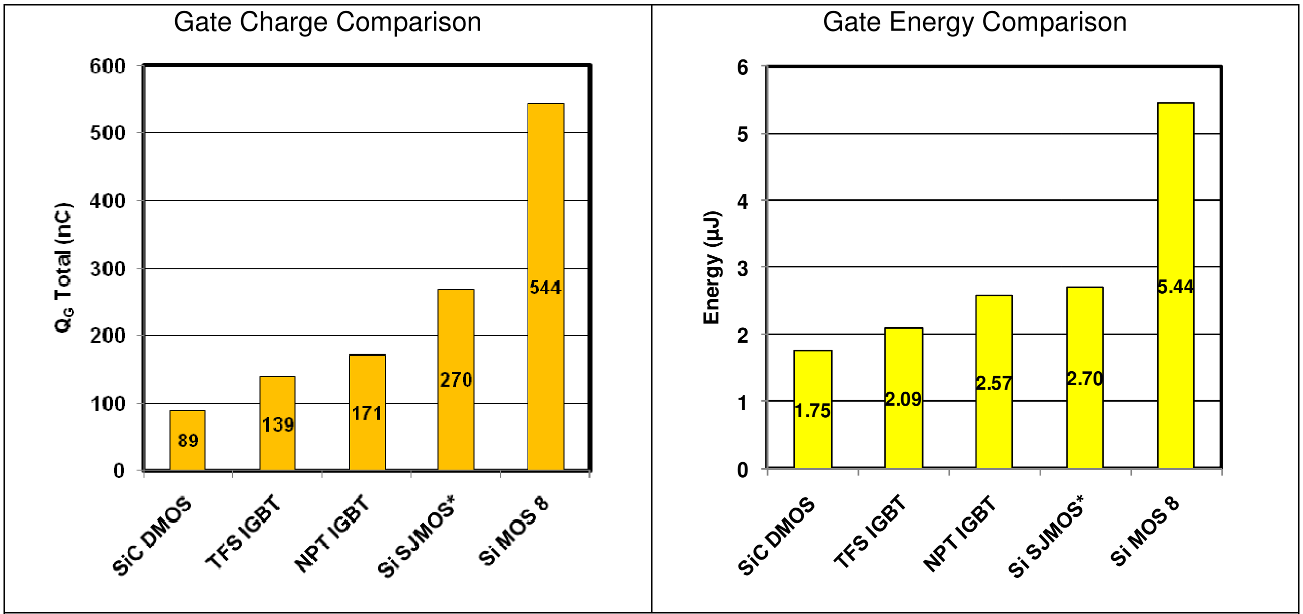

Figure 4: Gate charge and energy comparison

A popular figure of merit when comparing MOSFETs is the product of $R_{DS(on)}$ and total gate charge [6]. Minimization of the figure of merit is an indicator of the superior part. A comparison between the CMF20120D and the other Si MOSFETs is shown in Figure 5. The Si SJMOSFET has a figure of merit of 32.4 Ω*nC. The figure of merit of the CMF20120D is 7.12 Ω*nC. Furthermore, the CMF20120D is a 1.2 kV part whereas the Si SJMOSFET is rated at only 900 V.

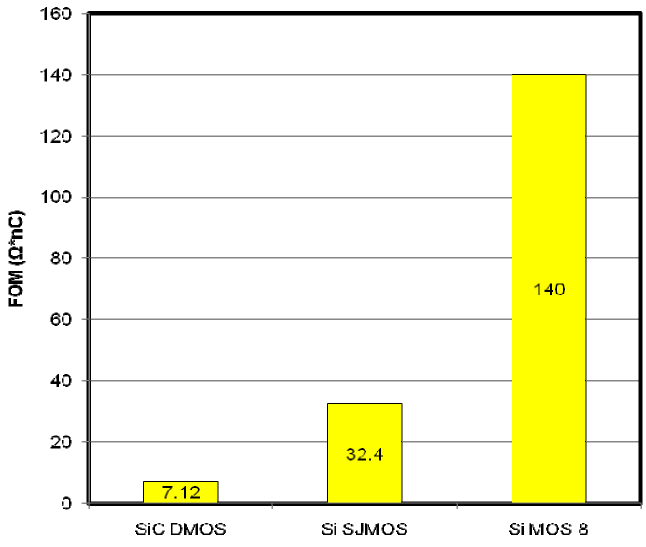

Figure 5: $Qg*R_{DS(on)}$ Figure of Merit Comparison

The inductive turn-off losses versus temperature of the CMF20120D compared with the TFS and NPT IGBTs are shown in Figure 6. The freewheeling diode used with all devices was a 1.2 kV, 10A SiC Schottky diode. The turn-off losses of the IGBTs are significantly higher than the CMF20120D and strongly increase with temperature. This is due to the tail loss inherent with IGBTs. The NPT IGBT is significantly better than the TFS IGBT. However, the NPT IGBT conduction losses are much higher than the CMF20102D. The TFS IGBT conduction loss is lower than the NPT IGBT, but the switching loss is the highest of the three.

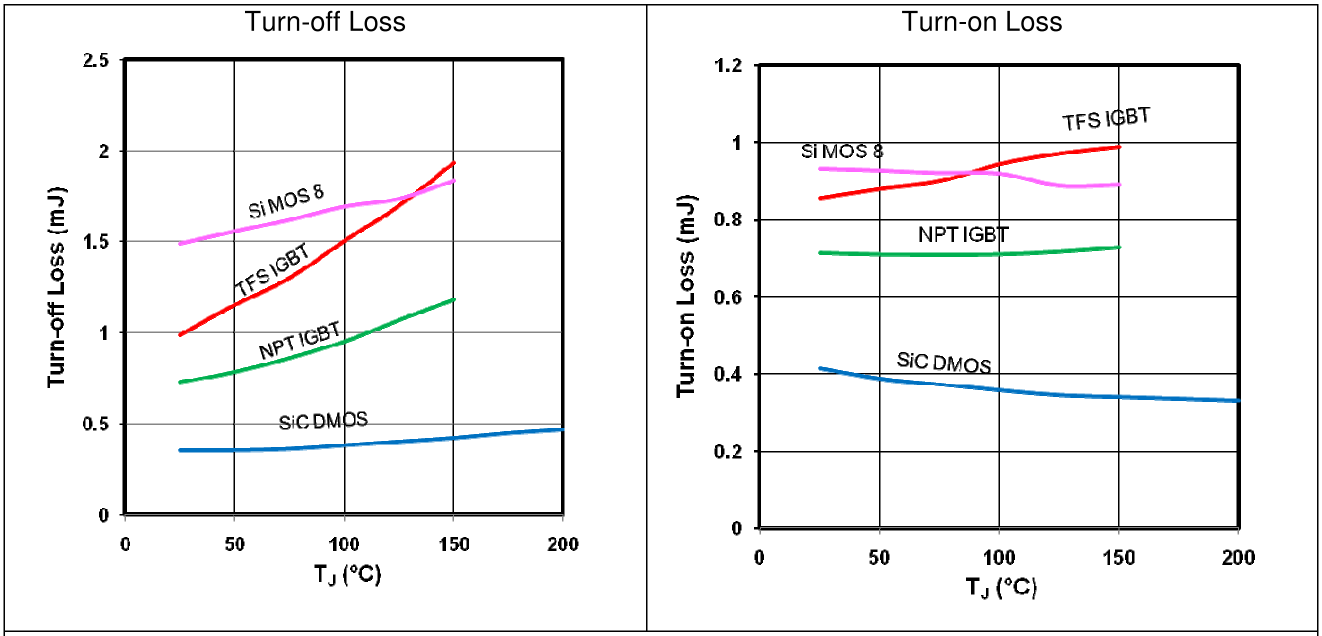

Figure 6: Switching loss vs. temperature comparison ($V_{DD} = V_{CC} = 800V$, $I_D = I_C = 20A$, $R_G = 10\Omega$)

To achieve fast switching time, the gate drive interconnections need to have minimum parasitics, especially inductance. This requires the gate driver to be located as close as possible to the CMF20120D. Care should be exercised to minimize or eliminate ringing in the gate drive circuit. This can be achieved by selecting an appropriate external gate resistor. The silicon IGBT current tail provides a certain amount of turn-off snubbing that reduces voltage overshoot and ringing. As with any majority carrier device, the CMF20120D has no tail, so the amount of drain voltage overshoot and parasitic ringing is noticeably higher. The higher ringing is of concern because the lower transconductance and low threshold voltage of the CMF20120D reduces gate noise immunity. The high level of drain current di/dt can couple back to the gate circuit through any common gate/source inductance. A Kelvin connection for the gate drive is recommended, especially if the gate driver cannot be located close to the CMF20120D. Ferrite beads (nickel-zinc recommended) in lieu of or in addition to an external gate resistor are helpful to minimize ringing while maintaining fast switching time. It is also recommended to connect a high value resistor (10kΩ) between gate and source in order to prevent excessive floating of the gate during system power up propagation delays.

Like any other power MOSFET, the CMF20102D has a body diode. The body diode is a SiC PN diode that has a 2.5 – 2.7 V built-in voltage, but a substantially lower reverse recovery charge when compared to a Si SJMOSFET. Use of this diode is not recommended due to its high forward drop. An external SiC Schottky diode is suggested. Cree's C2D10120A is the recommended device until such time that a TO-247 single co-packaged part is released.

Summary

The CMF20120D has definite system advantages over competing Si switching devices. However, its unique operating characteristics need to be carefully considered to fully realize these advantages. The gate driver needs to be capable of providing +20V and -2V to -5V negative bias with minimum output impedance and high current capability. The parasitics between the gate driver and the CMF20120D need to be minimized (close location, separate source return, etc.) to assure that the gate pulse has a fast rise and fall time with good fidelity. The fast switching speed of the CMF20120D can result in higher ringing and voltage overshoots. The effects of parasitics in the high current paths need to be carefully assessed.

References:

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