NEC
NEC Electronics Inc.

µPD4364
8192 x 8-BIT STATIC CMOS RAM

Description

The µPD4364 is a high-speed, 8192-word by 8-bit static RAM. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the µPD4364 a very low-power device that requires no clock or refreshing to operate.

Two chip enable pins are provided for battery backup application, and an output enable pin is provided for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 V (-xxL and -xxLL versions).

The µPD4364 is packaged in standard and slim 28-pin plastic DIP, as well as plastic miniflat packages that are plug-in compatible with 2764-type EPROMs.

Features

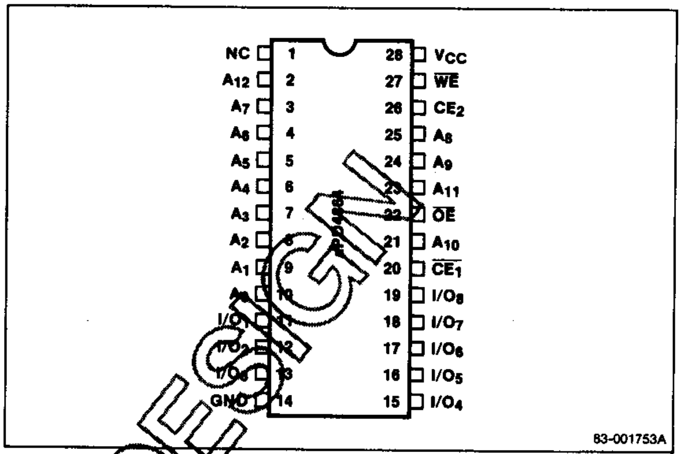
- ☐ Single +5-volt power supply
- ☐ Fully static operation—no clock or refreshing required
- ☐ TTL-compatible—all inputs and outputs
- ☐ Common I/O using three-state outputs
- ☐ One output enable and two chip enable pins for easy application
- ☐ Data retention voltage: 2 V min for -xxL and -xxLL versions
- ☐ Plug-in compatible with 2764-type EPROMs
- ☐ Standard 28-pin plastic DIP
- ☐ 28-pin 300 mil plastic slim DIP
- ☐ 28-pin plastic miniflat package

Pin Identification

Name	Function
A_0-A_{12}	Address input
I/O_1-I/O_8	Data input/output
$\overline{CE_1}$	Chip enable input, active low
CE_2	Chip enable input, active high
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

28-Pin Plastic DIP or Miniflat



Ordering Information

Part Number (Notes 1, 2, 3)	Standby Current (max)	Access Time (max)	Package
µPD4364C-xx	2 mA	(Notes 1,4)	28-pin DIP
C-xxL	100 µA		
C-xxLL	50 µA		
CX-xx	2 mA	(Notes 1,5)	28-pin slim DIP
CX-xxL	100 µA		
µPD4364G-xx	2 mA	(Notes 1,4)	28-pin miniflat
G-xxL	100 µA		
G-xxLL	50 µA		

Notes:

(1) The symbol "xx" in the part number denotes access time.

xx	Access Time (max)
10	100 ns
12	120 ns
15	150 ns
20	200 ns

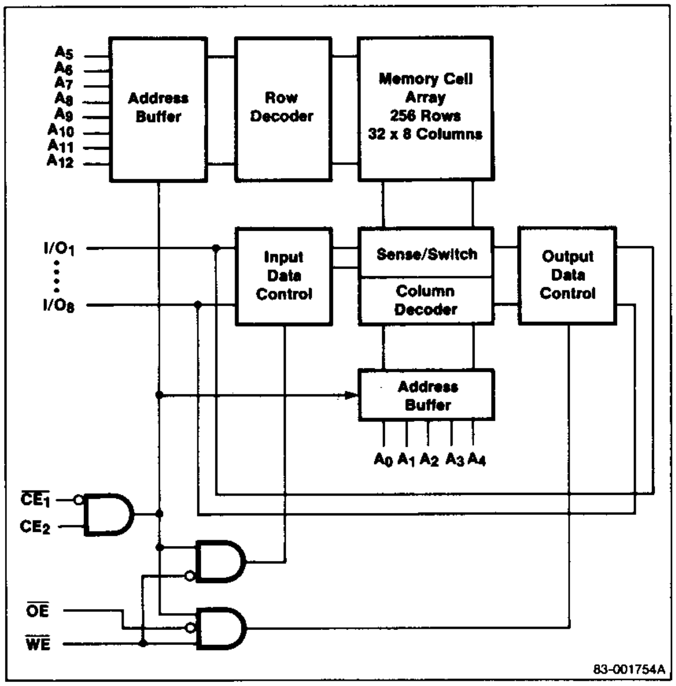
(2) The symbol C, CX, or G in the part number denotes a 28-pin plastic package.
C = 600-mil DIP
CX = 300-mil slim DIP
G = Miniflat

(3) Part number example: µPD4364CX-12L denotes a 300-mil DIP package, 120-ns maximum access time, and 100-µA maximum standby current.

(4) Contact your NEC sales representative for availability of a -10LL version.

(5) A 200-ns access time is not available in the CX package.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	–0.5 to 7.0 V
Input voltage, V_{IN} (Note 1)	–0.5 V to V_{CC} + 0.5 V
Output voltage, V_{OUT} (Note 1)	–0.5 V to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	–55 to 125°C
Power dissipation, P_D	1.0 W

Notes:

(1) –3.0 V min (pulse width of 50 ns max)

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under Recommended DC Operating Conditions.

Capacitance

T_A = 25°C; f = 1.0 MHz

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_I			(1)	pF	$V_I = 0$ V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

Notes:

(1) Maximum input capacitance
CX package: 5 pF
C or G package, 100-ns version: 5 pF
C or G package, except 100-ns version: 6 pF

Recommended DC Operating Conditions

T_A = 0 to +70°C

		Limits			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	–0.3 (Note 1)		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V

Notes:

(1) –3.0 V min (pulse width 50 ns max)

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0$ V to V_{CC}
Output leakage current	I_{LO}			1	μA	$V_{I/O} = 0$ V to V_{CC} $\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}			(1)	mA	$\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, Min cycle
	I_{CCA2}		5	10	mA	$\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, DC current
	I_{CCA3}		3	5	mA	$\overline{CE_1} \leq 0.2$ V, $CE_2 \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, f = 1 MHz, $I_{I/O} = 0$
Standby supply current	I_{SB}			(2)	mA	$\overline{CE_1} \geq V_{IH}$ or $CE_2 = V_{IL}$
	I_{SB1}			(3)	mA	$\overline{CE_1} \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
	I_{SB2}			(3)	mA	$CE_2 \leq 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –1.0 mA

Notes:

(1) μPD4364-10/10L: 45 mA max
μPD4364-12/12L/12LL: 40 mA max
μPD4364-15/15L/15LL: 40 mA max
μPD4364-20/20L/20LL: 35 mA max

(2) μPD4364-xx: 5 mA max
μPD4364-xxL: 3 mA max
μPD4364-xxLL: 3 mA max

(3) μPD4364-xx: 2 mA max
μPD4364-xxL: 100 μA max
μPD4364-xxLL: 50 μA max

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

		Limits								
		μPD4364 -10/10L		μPD4364 -12/12L/12LL		μPD4364 -15/15L/15LL		μPD4364 -20/20L/20LL		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read Cycle										
Read cycle time	t_{RC}	100		120		150		200		ns
Address access time	t_{AA}		100		120		150		200	ns
$\overline{CE}_1$ access time	t_{CO1}		100		120		150		200	ns
CE_2 access time	t_{CO2}		100		120		150		200	ns
Output enable to output valid	t_{OE}		50		60		70		100	ns
Output hold from address change	t_{OH}	10		10		15		15		ns
Chip enable ($\overline{CE}_1$) to output in low-Z	t_{LZ1}	10		10		15		15		ns
Chip enable (CE_2) to output in low-Z	t_{LZ2}	10		10		15		15		ns
Output enable to output in low-Z	t_{OLZ}	5		5		5		5		ns
Chip enable ($\overline{CE}_1$) to output in high-Z	t_{HZ1}		35		40		50		100	ns
Chip enable (CE_2) to output in high-Z	t_{HZ2}		35		40		50		100	ns
Output enable to output in high-Z	t_{OHZ}		35		40		50		80	ns
Write Cycle										
Write cycle time	t_{WC}	100		120		150		200		ns
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	80		85		100		180		ns
Chip enable (CE_2) to end of write	t_{CW2}	80		85		100		180		ns
Address valid to end of write	t_{AW}	80		85		100		180		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	60		70		90		140		ns
Write recovery time	t_{WR}	5		5		5		5		ns
Data valid to end of write	t_{DW}	40		50		60		80		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write enable to output in high-Z	t_{WHZ}		35		40		50		100	ns
Output active from end of write	t_{OW}	5		5		10		10		ns

Notes:

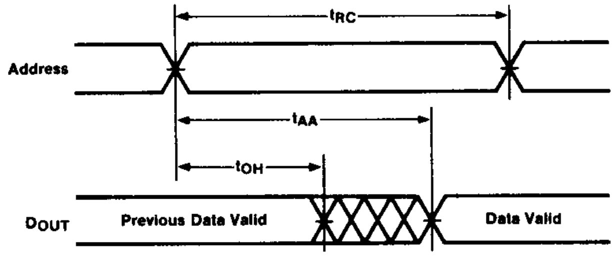
(1) Input pulse levels: 0.8 to 2.4 V
Input pulse rise and fall times: 5 ns
Timing reference levels: 1.5 V
Output load: 1 TTL gate and C_L = 100 pF

Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	D_{OUT} disable	High-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Timing Waveforms

Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The device is continuously selected; $\overline{CE}_1 = \overline{OE} = V_{IL}$, $CE_2 = V_{IH}$.

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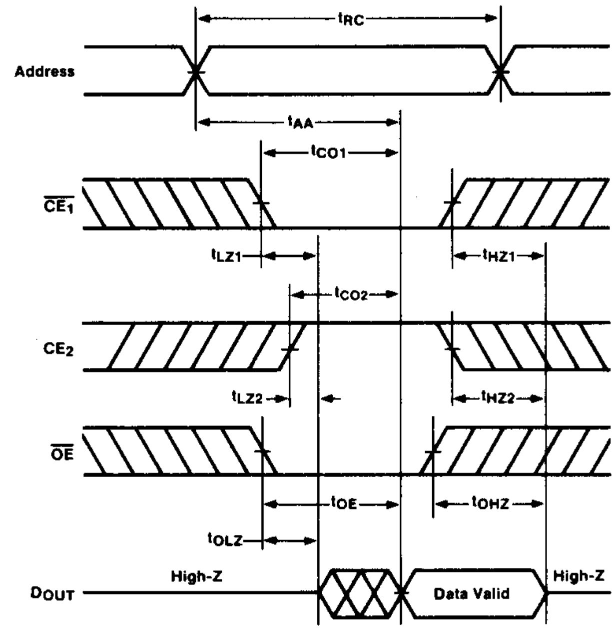
Read Cycle No. 2 (Chip Enable Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The address inputs are valid prior to or coincident with the $\overline{CE}_1$ transition low and the CE_2 transition high.

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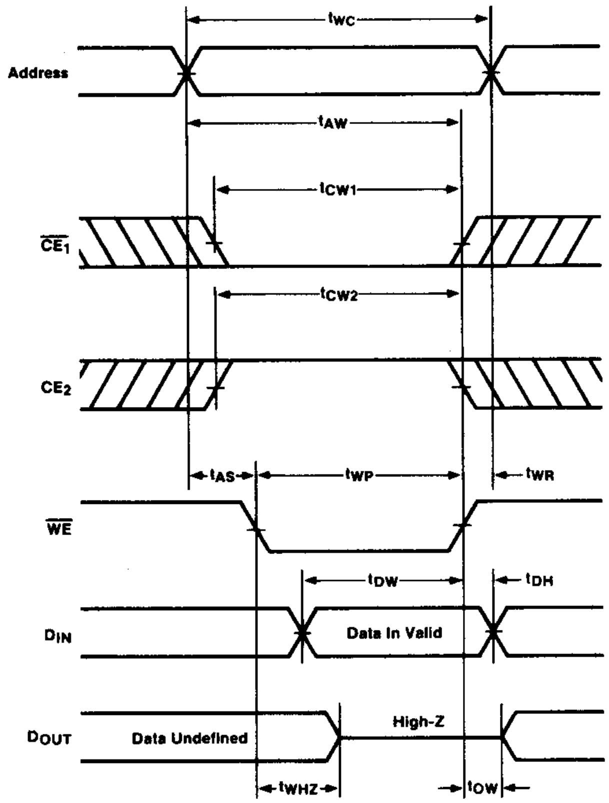
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:
[1] A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.
[3] If $\overline{OE}$ is high the I/O pins remain in a high impedance state.

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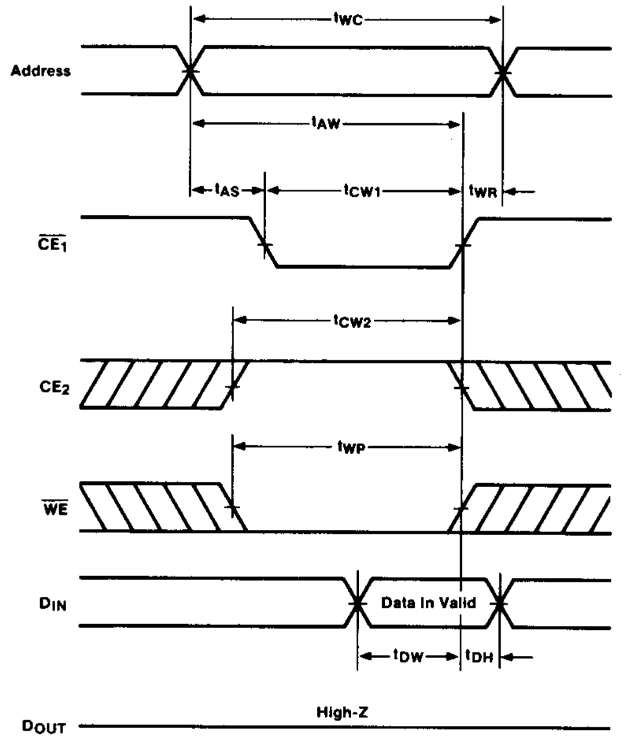
Timing Waveforms (cont)

Write Cycle No. 2 ($\overline{CE_1}$ Controlled)



Note:

[1] A write occurs during the overlap of a low $\overline{CE_1}$ and a high CE2 and a low $\overline{WE}$.

[2] $\overline{CE_1}$ or $\overline{WE}$ [or CE2] must be high [low] during any address transition.

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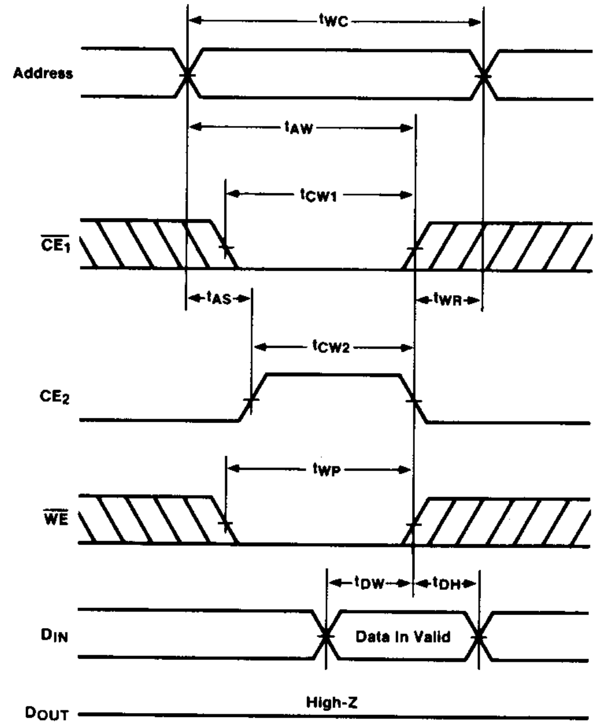
Write Cycle No. 3 (CE2 Controlled)



Note:

[1] A write occurs during the overlap of a low $\overline{CE_1}$ and a high CE2 and a low $\overline{WE}$.

[2] $\overline{CE_1}$ or $\overline{WE}$ [or CE2] must be high [low] during any address transition.

83-001759A

Low V_{CC} Data Retention Characteristics

T_A = 0 to +70°C

Parameter	Symbol	Limits				
		Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2.0		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
	V_{CCDR2}	2.0		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		1	(2)	μA	$V_{CC} = 3.0$ V $\overline{CE}_1 \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
	I_{CCDR2}		1	(2)	μA	$V_{CC} = 3.0$ V $CE_2 \leq 0.2$ V
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC} Note 3			ns	

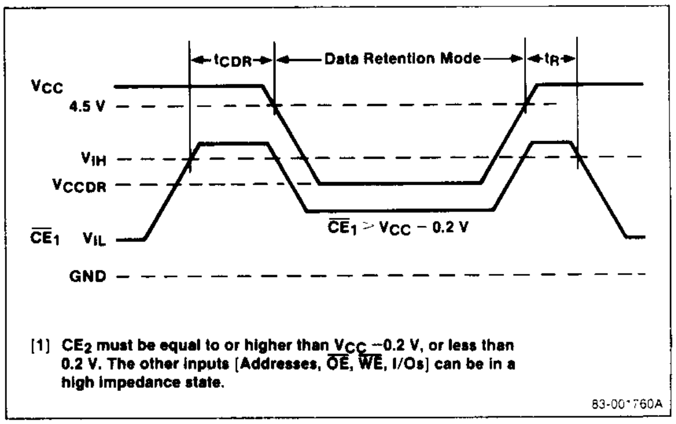
Notes:

(1) This table is applicable to μPD4364-xxL and -xxLL only.

(2) μPD4364-xxL: 50 μA max; 15 μA (0 to 40°C)
μPD4364-xxLL: 20 μA max; 5 μA (0 to 40°C)

(3) t_{RC} is read cycle time.

Data Retention ($\overline{CE}_1$ Controlled)



[1] CE_2 must be equal to or higher than V_{CC} −0.2 V, or less than 0.2 V. The other inputs [Addresses, $\overline{OE}$, $\overline{WE}$, I/Os] can be in a high impedance state.

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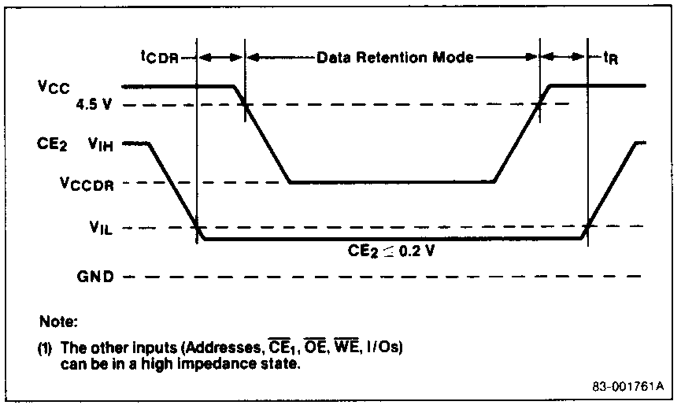
Data Retention (CE_2 Controlled)



Note:

(1) The other inputs (Addresses, $\overline{CE}_1$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

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