ARIZONA MICROTEK, INC.

AZ100LVEL16VR

ECL/PECL Oscillator Gain Stage & Buffer with Selectable Enable

FEATURES

- Green and RoHS Compliant / Lead (Pb) Free Packages Available
- Enhanced Enable Operation
- High Bandwidth for ≥1GHz
- Similar Operation as AZ100EL16VO
- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS/TTL or PECL)
- Available in a MLP 16 or MLP 8 Package
- S–Parameter (.s2p) and IBIS Model Files Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING	NOTES
MLP 16 (3x3)	AZ100LVEL16VRL	AZM 16R <Date Code>	1,2
MLP 16 (3x3) RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VRL+	AZM+ 16R <Date Code>	1,2
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZ100LVEL16VRNEG	R5G <Date Code>	1,2
DIE	AZ100LVEL16VRXP	N/A	3
DIE	AZ100LVEL16VRXR	N/A	4

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" for year followed by "WW" for week.
3 Waffle Pack. Die thickness 14 mils.
4 Die on 7 inch Tape & Reel, 3k parts per reel. Die thickness 14 mils.

DESCRIPTION

The AZ100LVEL16VR is a specialized oscillator gain stage with high gain output buffer including an enable function. The $Q_{HG}/\overline{Q}_{HG}$ outputs have voltage gain several times greater than the $Q/\overline{Q}$ outputs.

MLP 16, 3x3 mm Package (VRL) or DIE (VRX)

The AZ100LVEL16VR provides a selectable $Q_{HG}/\overline{Q}_{HG}$ enable that allows continuous oscillator operation via the $Q/\overline{Q}$ outputs. The enable truth table on the next page shows the operating modes. Leaving EN-SEL open (NC) selects PECL/ECL operation for the EN pad/pin. In this mode the $Q_{HG}/\overline{Q}_{HG}$ outputs are enabled when EN is left open (NC) or set to a PECL/ECL low.

Connecting EN-SEL to V_{CC}, V_{EE} or V_{BB} selects CMOS operation for the EN pad/pin. When EN-SEL is tied to V_{EE}, the $Q_{HG}/\overline{Q}_{HG}$ outputs are disabled when EN is left open (NC). When EN-SEL is tied to V_{CC} or V_{BB}, the $Q_{HG}/\overline{Q}_{HG}$ outputs are enabled when EN is left open.[1] This default logic condition can be overridden by a ≤20kΩ resistor connected to the opposite supply.

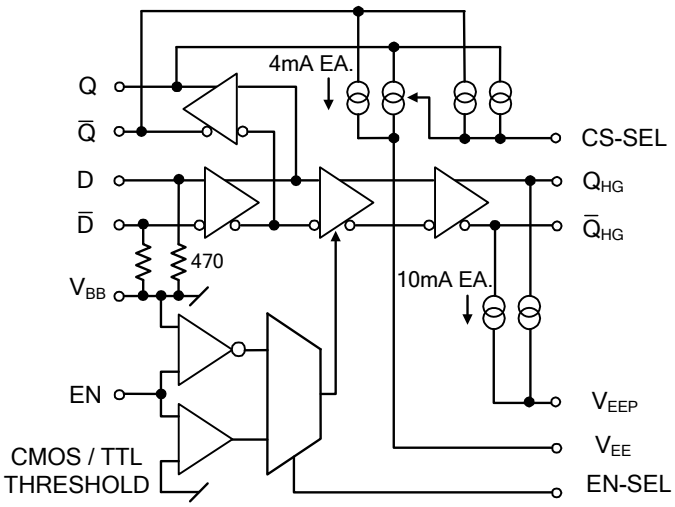
The AZ100LVEL16VR also provides a V_{BB} and 470Ω internal bias resistors from D to V_{BB} and $\overline{D}$ to V_{BB}. The V_{BB} pin supports 1.5mA sink/source current. V_{BB} should be bypassed to ground or V_{CC} with a 0.01 μF capacitor.

Outputs $Q/\overline{Q}$ each have a selectable on-chip pull-down current source. See the current source truth table on the next page for the supported values. External resistors may also be used to increase pull-down current to a maximum total of 25mA for the $Q/\overline{Q}$ outputs.

Each of the $Q_{HG}/\overline{Q}_{HG}$ outputs has an optional on-chip pull-down current source of 10 mA. When pad/pin V_{EEP} is left open (NC), the output current sources are disabled and the $Q_{HG}/\overline{Q}_{HG}$ operate as standard PECL/ECL. When V_{EEP} is connected to V_{EE}, the current sources are activated. The $Q_{HG}/\overline{Q}_{HG}$ pull-down current can be decreased by using a resistor between V_{EEP} and V_{EE}.

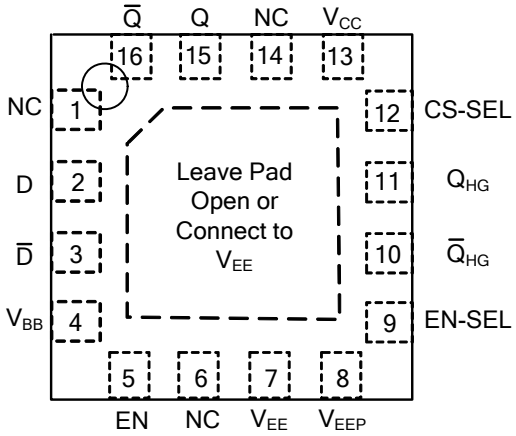
[1]This operational mode (EN-SEL to V_{CC} or V_{BB}) is not supported for date codes prior to 0428 (July 2004). EN-SEL to V_{EE} is supported for all date codes.

MLP 16 (VRL) AND DIE (VRX)



AZ100LVEL16VRL, VRX

AZ100LVEL16VRL
MLP 16



TOP VIEW

ENABLE TRUTH TABLE

EN-SEL	EN	Q/Q̄	Q_{HG}	$\bar{Q}_{HG}$
NC	PECL Low, V_{EE} or NC	Data	Data	Data
NC	PECL High or V_{CC}	Data	Low	High
V_{EE}[1]	CMOS Low, V_{EE} or NC	Data	Low	High
V_{EE}[1]	CMOS High or V_{CC}	Data	Data	Data
V_{CC} or V_{BB}[1,2]	CMOS Low or V_{EE}	Data	Low	High
V_{CC} or V_{BB}[1,2]	CMOS High, V_{CC} or NC	Data	Data	Data

[1] EN-SEL connections must be ≤1Ω.
[2] Date codes prior to 0428 do not support this operating mode.

CURRENT SOURCE TRUTH TABLE

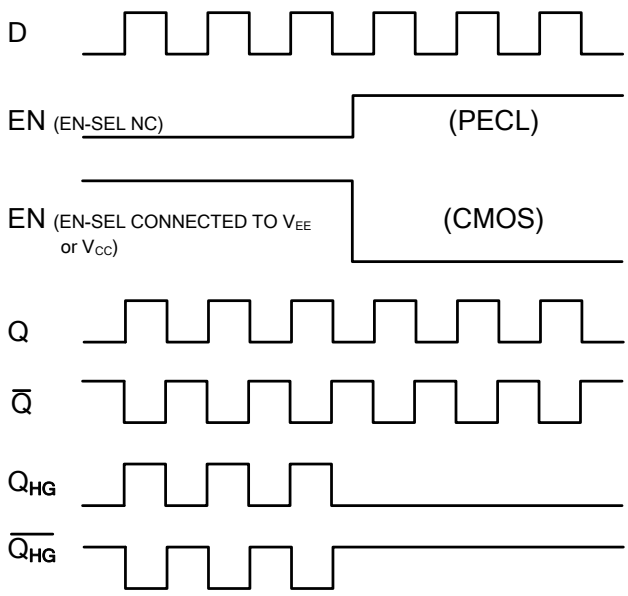
CS-SEL	Q	Q̄
NC	4mA typ.	4mA typ.
V_{EE}[1]	8mA typ.	8mA typ.
V_{CC}[1]	0	4mA typ.

[1]Connections to V_{CC} or V_{EE} must be ≤1Ω.

PIN DESCRIPTION

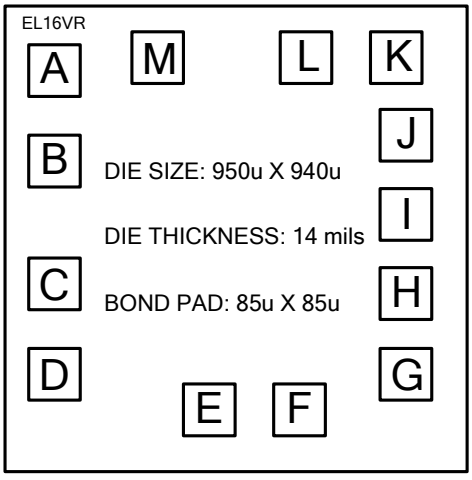
PIN	FUNCTION
D/D̄	Data Inputs
Q/Q̄	Data Outputs
$Q_{HG}/\bar{Q}_{HG}$	Data Outputs w/High Gain
V_{BB}	Reference Voltage Output
EN-SEL	Enable Logic Select
EN	Enable Input
CS-SEL	Selects Q and Q̄ Current Source Magnitude
V_{EEP}	Optional Q_{HG} and $\bar{Q}_{HG}$ Current Sources
V_{EE}	Negative Supply
V_{CC}	Positive Supply

MLP 16 (VRL) AND DIE (VRX)



TIMING DIAGRAM

DIE PAD COORDINATES



NAME	SIGNAL	X (Microns)	Y (Microns)
A	D	-342.5	312.5
B	$\overline{D}$	-342.5	144.5
C	V_{BB}	-342.5	-87.0
D	EN	-342.5	-255.0
E	V_{EE}	-33.5	-312.5
F	V_{EEP}	126.5	-312.5
G	EN-SEL	312.5	-248.5
H	$\overline{Q}_{HG}$	312.5	-98.5
I	Q_{HG}	312.5	51.5
J	CS-SEL	312.5	201.5
K	V_{CC}	302.5	342.5
L	Q	142.5	342.5
M	$\overline{Q}$	-140.5	342.5

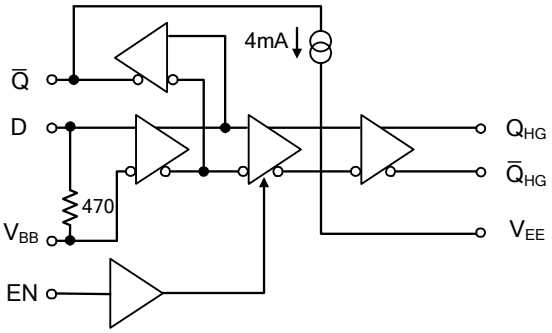
Notes:
1. Other die thicknesses available. Contact factory for further information.
2. The die backside may be left open or connected to V_{EE}.

MLP 8, 2x2 mm Package (VRNE)

A CMOS enable input (EN) allows continuous oscillator operation. When the EN input is HIGH or left open (NC), the $\overline{Q}$ and $Q_{HG}/\overline{Q}_{HG}$ outputs follow the data input. When EN is LOW, the Q_{HG} output is forced high and the $\overline{Q}_{HG}$ output is forced low while $\overline{Q}$ continues to follow the data input. The $\overline{Q}$ output has an internal 4 mA current source to V_{EE}, in most cases eliminating the need for an external pull-down resistor.

The data input D is tied to the V_{BB} pin through a 470 Ω internal bias resistor while the inverting input $\overline{D}$ is connected directly to V_{BB}. Bypassing V_{BB} to ground with a 0.01 µF capacitor is recommended.

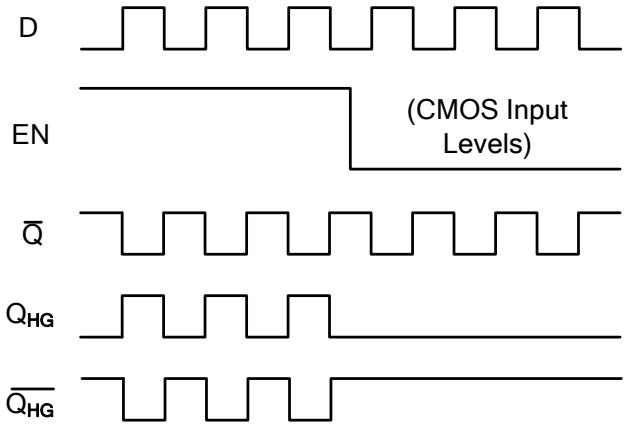
NOTE: The specifications in the ECL/PECL tables are valid when thermal equilibrium has been established.



AZ100LVEL16VRNE

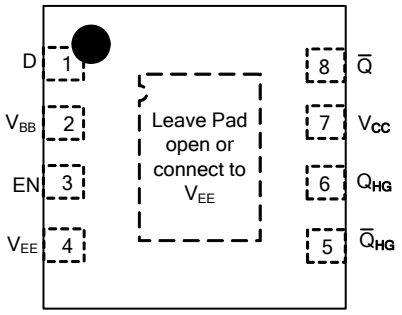
PIN DESCRIPTION

PIN	FUNCTION
D	Data Input
$\overline{Q}$	Data Output
$Q_{HG}/\overline{Q}_{HG}$	Data Outputs w/High Gain
V_{BB}	Reference Voltage Output
EN	Enable Input
V_{EE}	Negative Supply
V_{CC}	Positive Supply



TIMING DIAGRAM

AZ100LVEL16VRNE
MLP 8, 2x2 mm



TOP VIEW

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic		Rating	Unit
V_{CC}	PECL Power Supply	(V_{EE} = 0V)	0 to +6.0	Vdc
$V_{D/\bar{D}}$	PECL D/$\bar{D}$ Input Voltage	(V_{EE} = 0V)	±0.75 with respect to V_{BB}	Vdc
V_{EN}	PECL EN Input Voltage	(V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply	(V_{CC} = 0V)	-6.0 to 0	Vdc
$V_{D/\bar{D}}$	ECL D/$\bar{D}$ Input Voltage	(V_{CC} = 0V)	±0.75 with respect to V_{BB}	Vdc
V_{EN}	ECL EN Input Voltage	(V_{CC} = 0V)	-6.0 to 0	Vdc
I_{OUT}	Output Current, Q/$\bar{Q}$	— Continuous — Surge	25 50	mA
I_{HGOUT}	Output Current, $Q_{HG}/\bar{Q}_{HG}$	— Continuous — Surge	50 100	mA
T_A	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V_{OL}	Output LOW Voltage[1]	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{IH}	Input HIGH Voltage D/$\bar{D}$, EN (ECL)[2] EN (CMOS)[3]	 -1165 V_{EE}+2000	 -740 V_{CC}	 -1165 V_{EE}+2000	 -740 V_{CC}	 -1165 V_{EE}+2000	 -740 V_{CC}	 -1165 V_{EE}+2000	 -740 V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\bar{D}$, EN (ECL)[2] EN (CMOS)[3]	 -1900 V_{EE}	 -1475 V_{EE} + 800	 -1900 V_{EE}	 -1475 V_{EE} + 800	 -1900 V_{EE}	 -1475 V_{EE} + 800	 -1900 V_{EE}	 -1475 V_{EE} + 800	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)[2] EN (CMOS)[3]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[1]		48		48		48		54	mA

1. Specified with V_{EEP} and CS-SEL NC, $Q_{HG}/\bar{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
2. EN-SEL = NC.
3. EN-SEL = V_{CC} or V_{EE}.

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage[1,2]	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage[1] D/$\bar{D}$, EN (PECL)[3] EN (CMOS)[4]	 2135 2000	 2560 V_{CC}	 2135 2000	 2560 V_{CC}	 2135 2000	 2560 V_{CC}	 2135 2000	 2560 V_{CC}	mV
V_{IL}	Input LOW Voltage[1] D/$\bar{D}$, EN (PECL)[3] EN (CMOS)[4]	 1400 GND	 1825 800	 1400 GND	 1825 800	 1400 GND	 1825 800	 1400 GND	 1825 800	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (PECL)[3] EN (CMOS)[4]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[2]		48		48		48		54	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with V_{EEP} and CS-SEL NC, $Q_{HG}/\bar{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL = NC.
4. EN-SEL = V_{CC} or V_{EE}.

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage[1,2]	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 3835 2000	 4260 V_{CC}	 3835 2000	 4260 V_{CC}	 3835 2000	 4260 V_{CC}	 3835 2000	 4260 V_{CC}	mV
V_{IL}	Input LOW Voltage[1] D/$\overline{D}$, EN (PECL)[3] EN (CMOS)[4]	 3100 GND	 3525 800	 3100 GND	 3525 800	 3100 GND	 3525 800	 3100 GND	 3525 800	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (PECL)[3] EN (CMOS)[4]	 0.5 -150		 0.5 -150		 0.5 -150		 0.5 -150		µA
I_{EE}	Power Supply Current[2]		48		48		48		54	mA

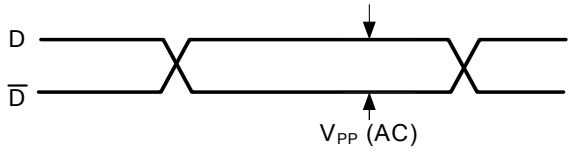
1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with V_{EEP} and CS-SEL NC, $Q_{HG}/\overline{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL = NC.
4. EN-SEL = V_{CC} or V_{EE}.

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC} = GND or V_{EE} = GND; V_{CC} = +3.0V to +5.5V)

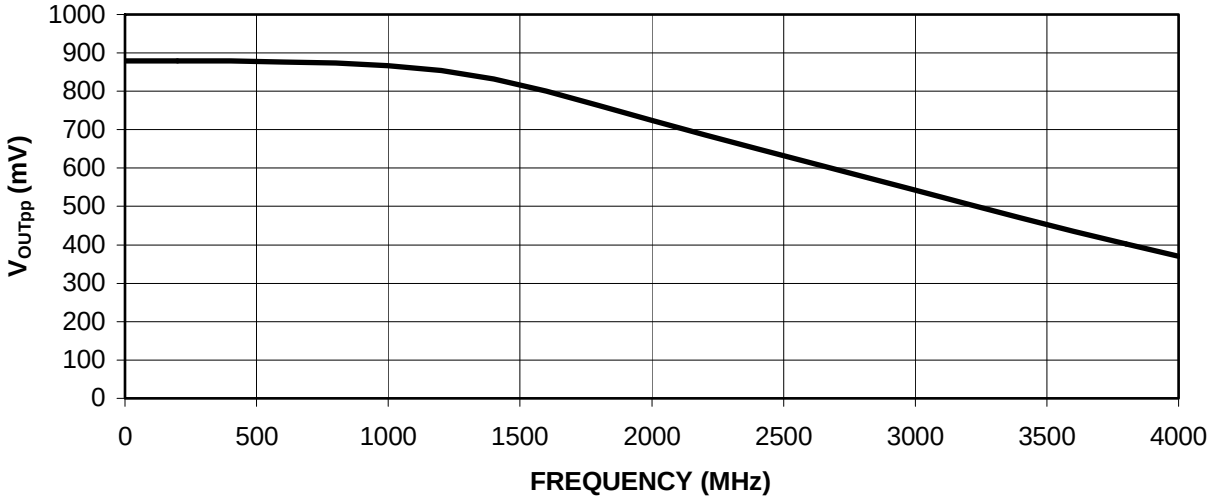
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Propagation Delay D to Q/$\overline{Q}$ Outputs[1] (SE) D to $Q_{HG}/\overline{Q}_{HG}$ Outputs[2] (SE)	 	 	 400 450	 	 	 400 450	 	 	 400 450	 	 	 400 450	ps
t_{SKEW}	Duty Cycle Skew[4] (SE)		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Differential Input Swing[5]	80		1000	80		1000	80		1000	80		1000	mV
t_r / t_f	Output Rise/Fall[1,2] (20% - 80%)	100		240	100		240	100		240	100		240	ps

1. Specified with CS-SEL connected to V_{EE}, Q/$\overline{Q}$ terminated with an AC coupled 50Ω load.
2. Specified with V_{EEP} NC, $Q_{HG}/\overline{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
3. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
4. The peak-to-peak differential input swing is the range for which AC parameters are guaranteed. V_D and V_D must remain within the range of ± 750 mV with respect to V_{BB}. The device has a voltage gain of ≈ 20 to the Q/$\overline{Q}$ outputs and a voltage gain of ≈ 100 to the $Q_{HG}/\overline{Q}_{HG}$ outputs.

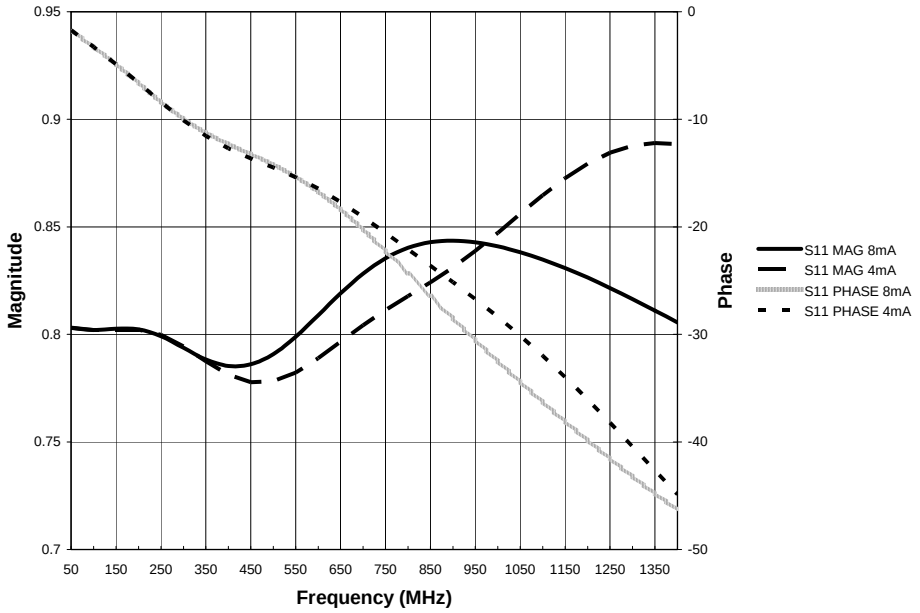
AC PP INPUT



Typical Large Signal Outputs, $Q_{HG}/\overline{Q}_{HG}$

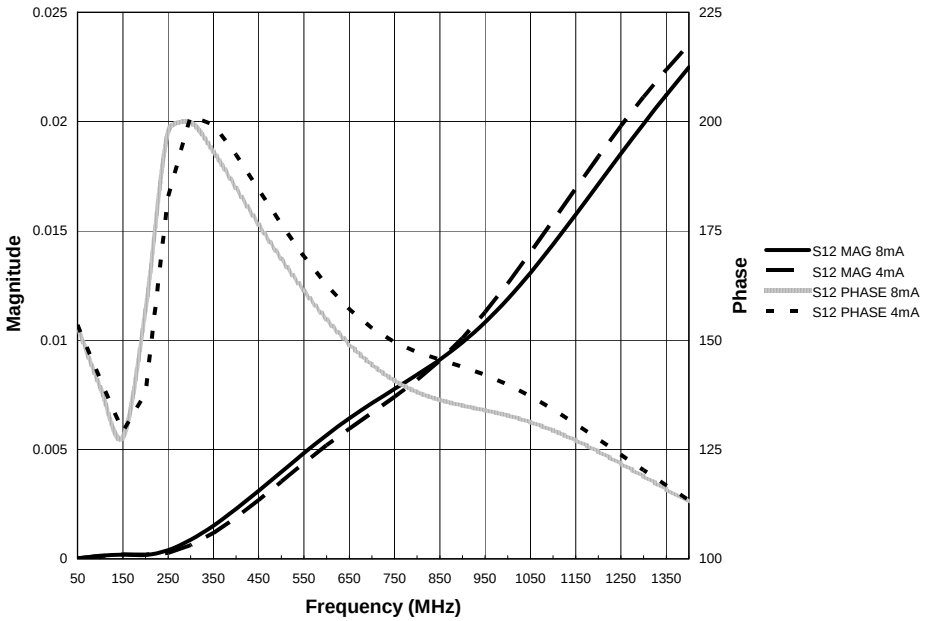


Measured with 750mv differential input, V_{EEP} NC, $Q_{HG}/\overline{Q}_{HG}$ each terminated to V_{CC}-2V via 50 Ω resistors.



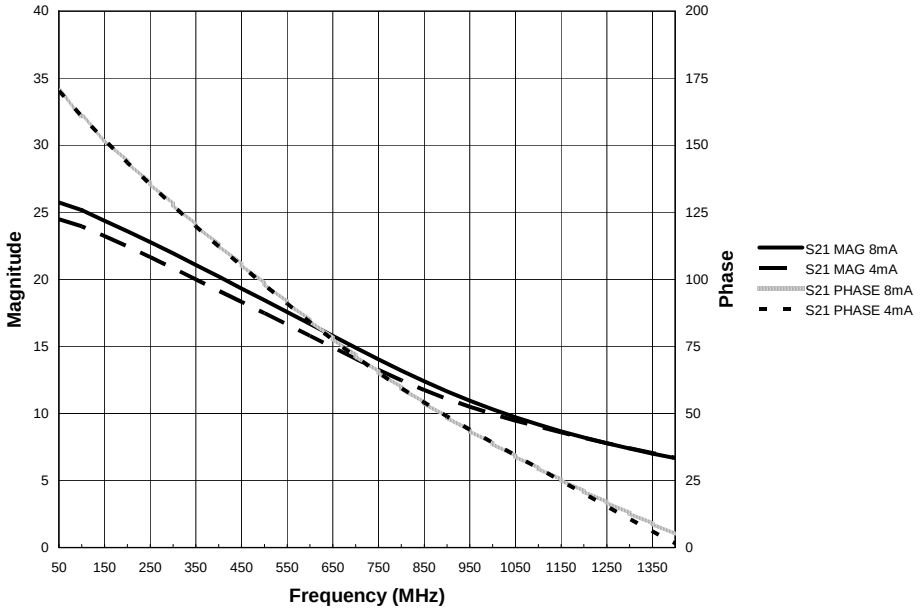
S11, D to $\bar{Q}$

(50 Ω external AC, 4 & 8mA internal DC Load on $\bar{Q}$)



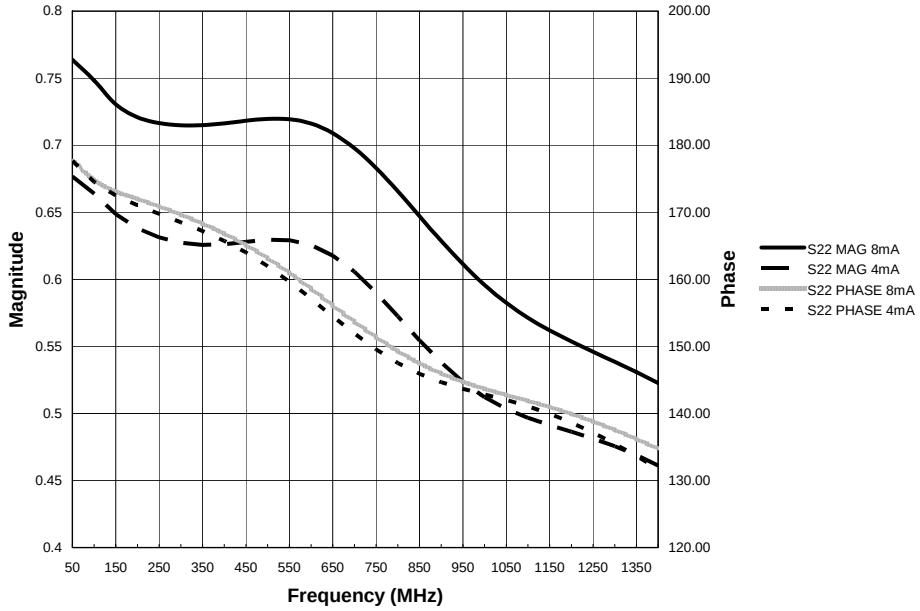
S12, D to $\bar{Q}$

(50 Ω external AC, 4 & 8mA internal DC Load on $\bar{Q}$)



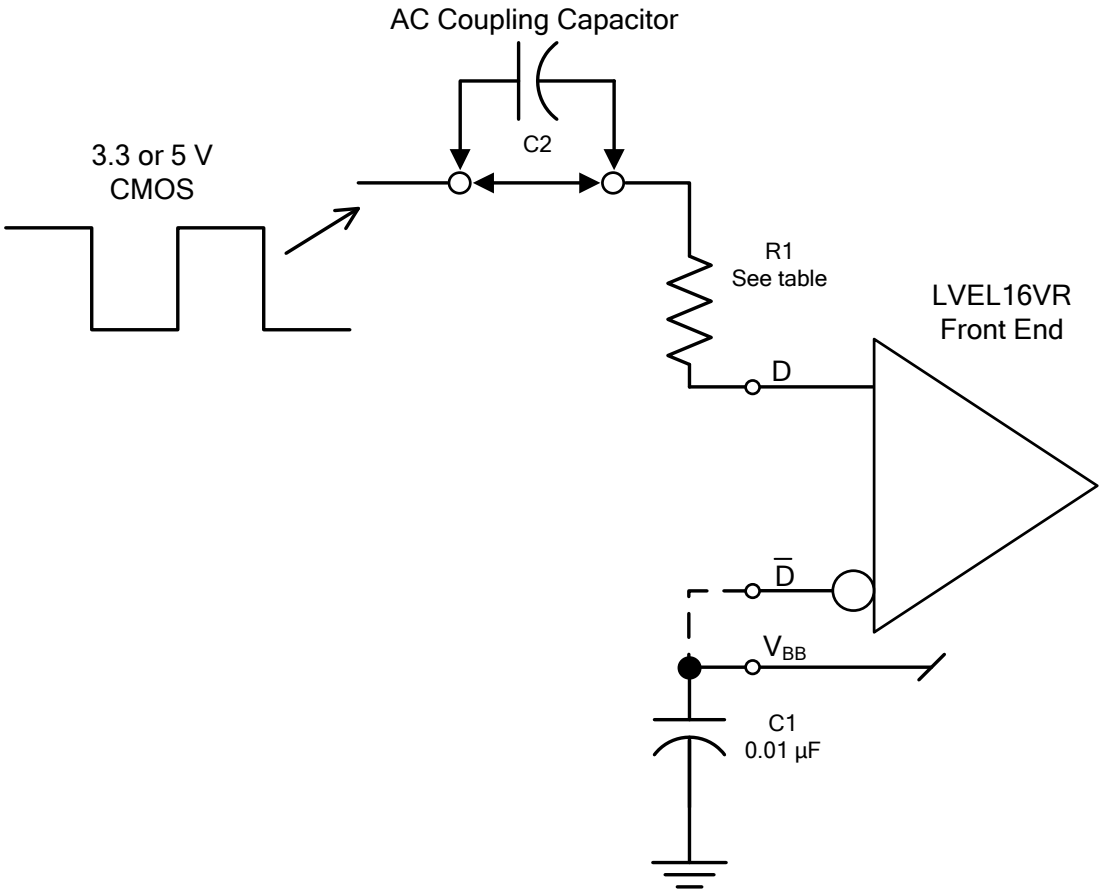
S21, D to $\bar{Q}$

(50 Ω external AC, 4 & 8mA internal DC Load on $\bar{Q}$)



S22, D to $\bar{Q}$

(50 Ω external AC, 4 & 8mA internal DC Load on $\bar{Q}$)



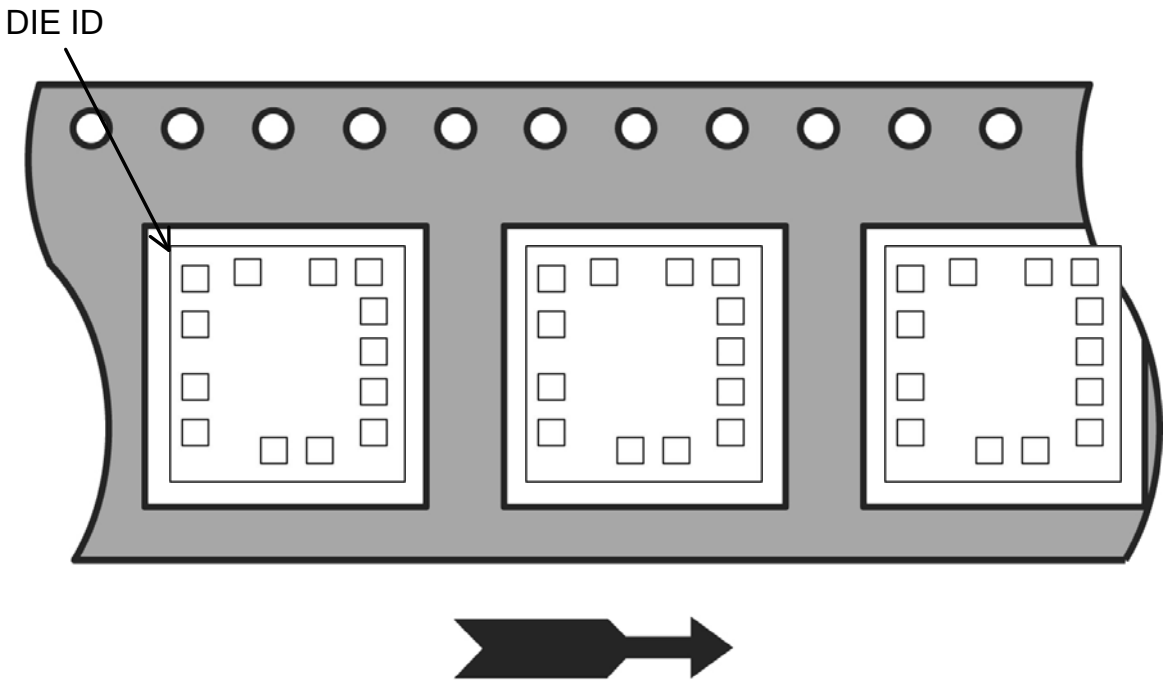
Application Circuit for CMOS Inputs

Input Type	R1[1]	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3 V CMOS	1.1 kΩ	2.0 kΩ
5 V CMOS	1.6 kΩ	3.3 kΩ

[1] R1 should be chosen so that the input swing on the D input with respect to $\overline{D}$ is in the range of ±80 to ±1000 mV, per the AC Characteristics table and the D input is < ±750 mV with respect to V_{BB}.

Recommended Component Values for CMOS Single Ended Inputs

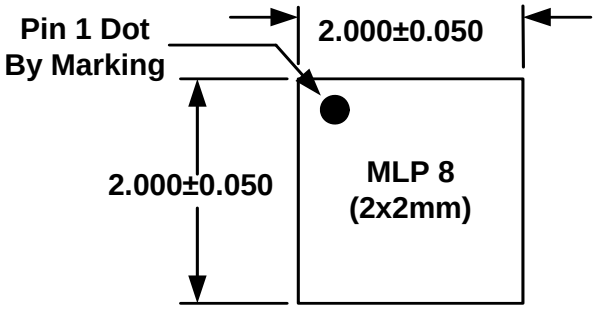
DIE ON TAPE OREINTATION



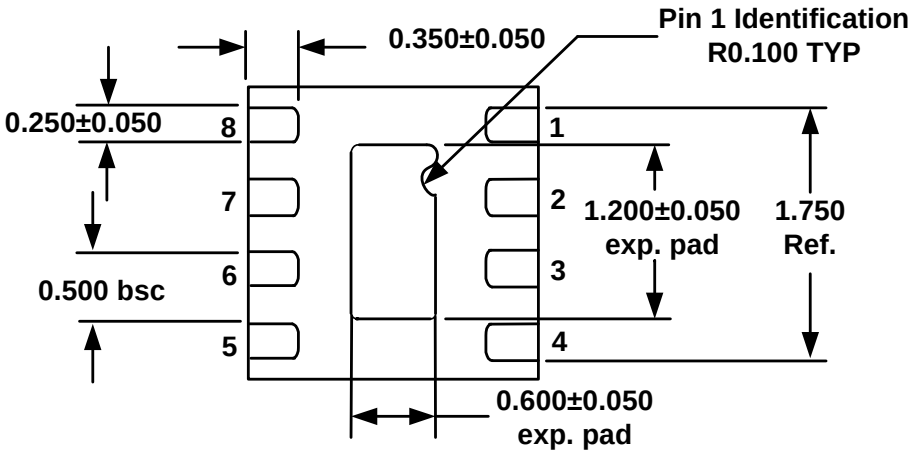
Direction of Feed

Package	Suffix	Reel Diameter	Quantity	Carrier Tape Width	Carrier Tape Pitch
X (Die)	R	7”	3000	8mm	4mm

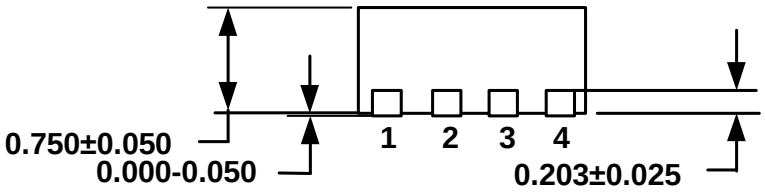
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



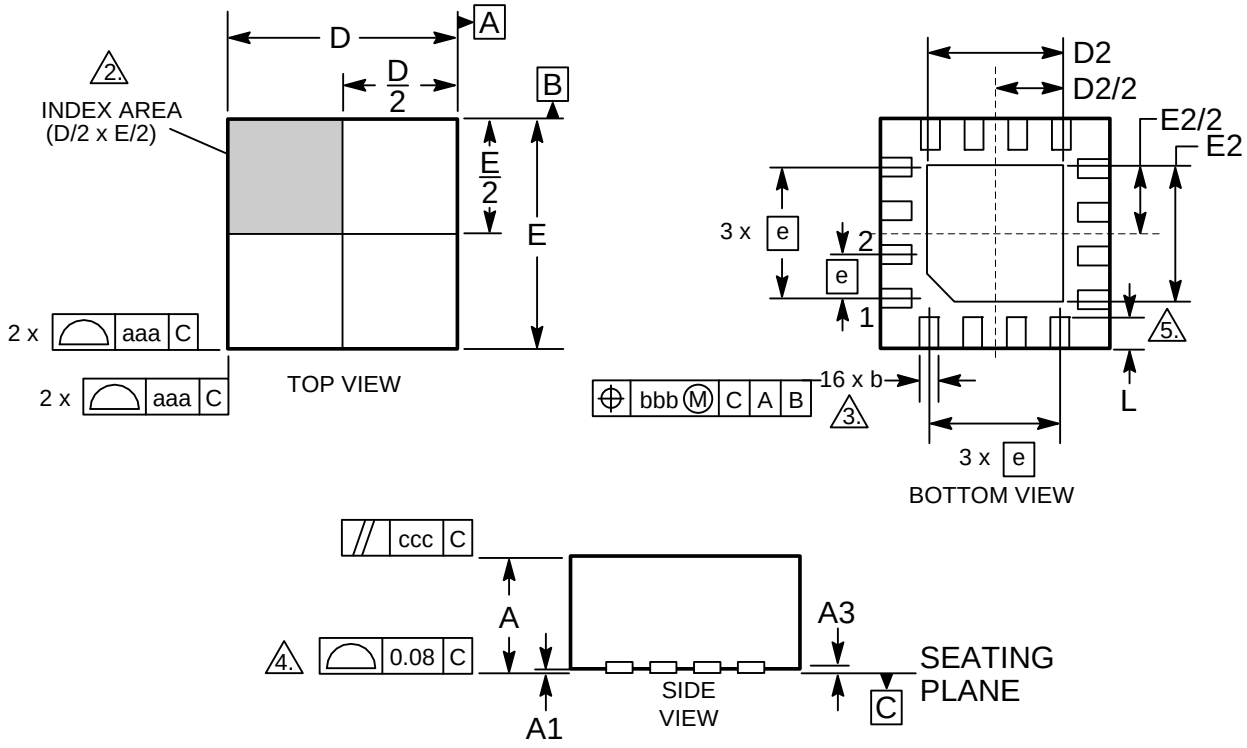
BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm

PACKAGE DIAGRAM
MLP 16



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. INSIDE CORNERS OF METALLIZED PAD MAY BE SQUARE OR ROUNDED

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	