

AZ10ELT20

AZ100ELT20

CMOS/TTL to Differential PECL Translator

FEATURES

- 0.5ns Typical Propagation Delay
- Differential PECL Outputs
- Flow Through Pinouts
- Operating Range of +3.0V to +5.5V
- Direct Replacement for ON Semi MC10ELT20, MC100ELT20, MC100LVELT20 & Micrel SY89329V
- Available in 2x2 mm MLP Package
- IBIS Model Files Available on Arizona Microtek Website

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2x0.75)	AZ100ELT20N	TC <Date Code>	1,2
MLP 8 (2x2x0.75) Green / RoHS Compliant / Lead (Pb) Free	AZ100ELT20NG	TCG <Date Code>	1,2
SOIC 8	AZ10ELT20D	AZM10 ELT20	1,2,3
SOIC 8	AZ100ELT20D	AZM100 ELT20	1,2,3
SOIC 8 Green / RoHS Compliant / Lead (Pb) Free	AZ100ELT20DG	AZM100G ELT20	1,2,3
TSSOP 8 Green / RoHS Compliant / Lead (Pb) Free	AZ100ELT20TG	AZHG LT20	1,2,3
DIE	AZ10/100ELT20XP	N/A	4
DIE	AZ10/100ELT20XR	N/A	5

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" or "YY" for year followed by "WW" for week.
- 3 Date code "YWW" or "YYWW" on underside of part.
- 4 Waffle Pack. Die thickness 14 mils
- 5 Die on 7 inch Tape & Reel. 3k parts per reel. Die thickness 14 mils.

DESCRIPTION

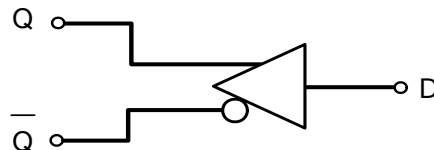
The AZ10/100ELT20 is a CMOS/TTL to differential PECL translator. It operates with a single power supply of +3.0 to +5.5 volts, making it ideal for both LVCMOS/LVTTL and CMOS/TTL applications. The extremely small MLP 8 2x2 mm package makes it ideal for those applications where space, performance and low power are at a premium.

When the D input is left floating, the Q output is forced HIGH, and the Q output is forced LOW.

The ELT20 is available in both PECL standards: the AZ10ELT20 is compatible with PECL 10K logic levels while the AZ100ELT20 is compatible with PECL 100K logic levels.

NOTE: Specifications in the PECL tables are valid when thermal equilibrium is established.

BLOCK DIAGRAM



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Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	0 to +8.0	V
V _{IN}	Input Voltage	0 to +6.0	V
I _{OUT}	Current Applied to Output in Low Output State — Continuous — Surge	50 100	mA
T _A	Operating Temperature Range (In Free-Air)	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

TTL/CMOS INPUT DC CHARACTERISTICS (GND = 0.0V, V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I _{IH}	Input HIGH Current			15	μA	V _{IN} = 2.7V
I _{IHH}	Input HIGH Current			20	μA	V _{IN} = V _{CC}
I _{IL}	Input LOW Current			-0.1	mA	V _{IN} = 0.5V
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18mA
V _{IH}	Input HIGH Voltage	2.0			V	
V _{IL}	Input LOW Voltage			0.8	V	

10K LVPECL DC Characteristics (GND = 0.0V, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2220		2410	2280		2460	2320		2490	2390		2580	mV
V _{OL}	Output LOW Voltage ^{1,2}	1350		1650	1350		1670	1350		1670	1350		1705	mV
I _{CC}	Power Supply Current ³			16			16			16			16	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

10K PECL DC Characteristics (GND = 0.0V, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3920		4110	3980		4160	4020		4190	4090		4280	mV
V _{OL}	Output LOW Voltage ^{1,2}	3050		3350	3050		3370	3050		3370	3050		3405	mV
I _{CC}	Power Supply Current ³			16			16			16			16	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

100K LVPECL DC Characteristics (GND = 0.0V, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	2220		2420	2275		2420	2275		2420	2275		2420	mV
V _{OL}	Output LOW Voltage ^{1,2}	1400		1750	1400		1680	1400		1680	1400		1680	mV
I _{CC}	Power Supply Current ³			16			16			16			16	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

100K PECL DC Characteristics (GND = 0.0V, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ^{1,2}	3920		4120	3975		4120	3975		4120	3975		4120	mV
V _{OL}	Output LOW Voltage ^{1,2}	3100		3450	3100		3380	3100		3380	3100		3380	mV
I _{CC}	Power Supply Current ³			16			16			16			16	mA

- Output parameters vary 1:1 with V_{CC}.
- Each output is terminated through a 50Ω resistor to V_{CC} - 2V.
- I_{CC} measurements must be done with outputs open.

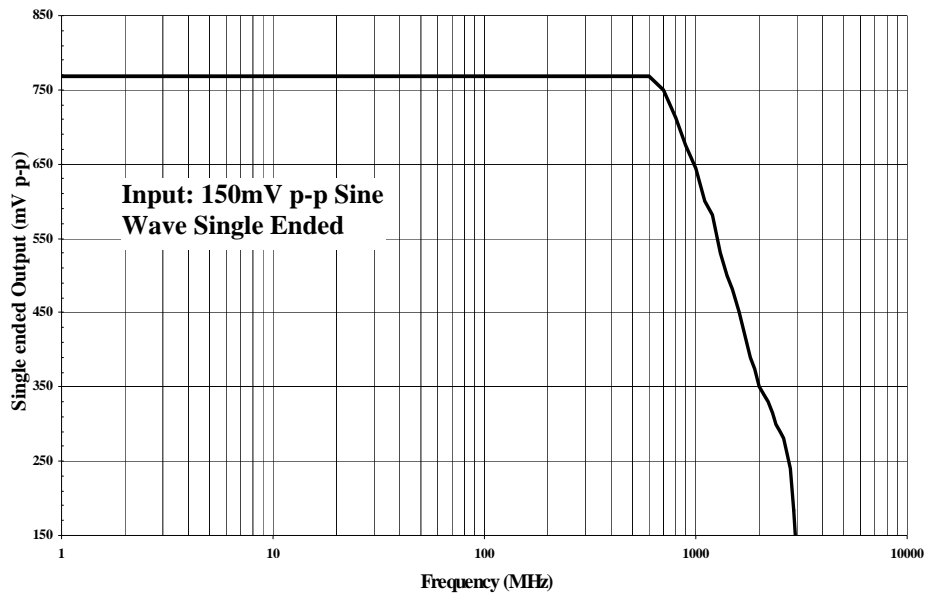
AZ10ELT20

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AC CHARACTERISTICS (GND = 0.0V, V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40°C		0°C		25°C			85°C		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
t _{PLH} /t _{PHL}	Propagation Delay ¹	100	550	100	500	100		450	100	600	ps	
t _r /t _f	Output Rise/Fall Time	80	250	80	250	80		250	80	250	ps	20-80%
f _{MAX}	Maximum Frequency ²	800		800		800			800		MHz	

1. Propagation delay is measured from +1.5V on the input to 50% of the PECL output swing. Input rise/fall times are < 1ns/V.
2. Output at -3 dB.



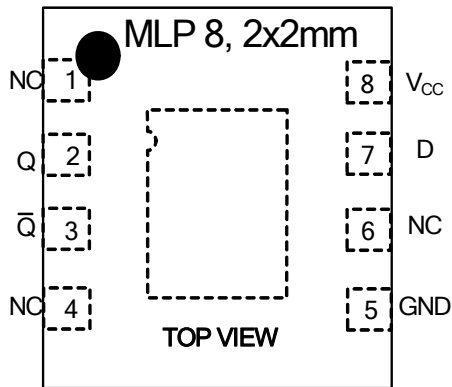
Large Signal Bandwidth

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PIN DESCRIPTION

PIN	FUNCTION
Q, Q	Differential PECL Outputs
D	TTL/CMOS Input
GND	Ground
V _{CC}	Positive Supply
NC	No Connect, Leave Open Except as Noted
10K	10K/100K Mode Select

AZ100ELT20N



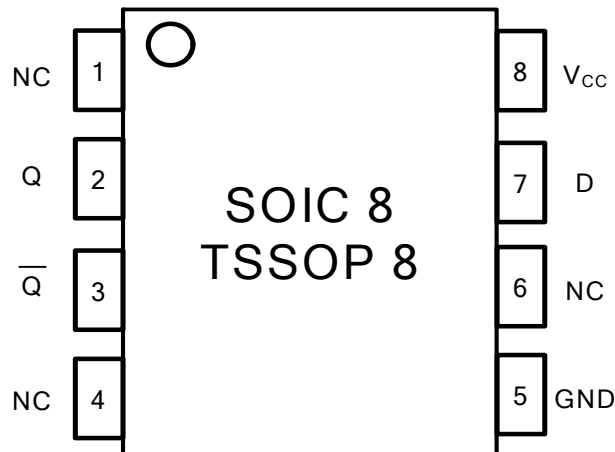
DIE (XP, XR) 10K/100K Selection

Connect pin/pad 10K to GND to select 10K operation. Float (NC) pin/pad 10K to select 100K operation. GND connection must be less than 1Ω.

Pin 8 of the MLP 16 package may be connected to pin 7 (GND) with no effect on the circuit.

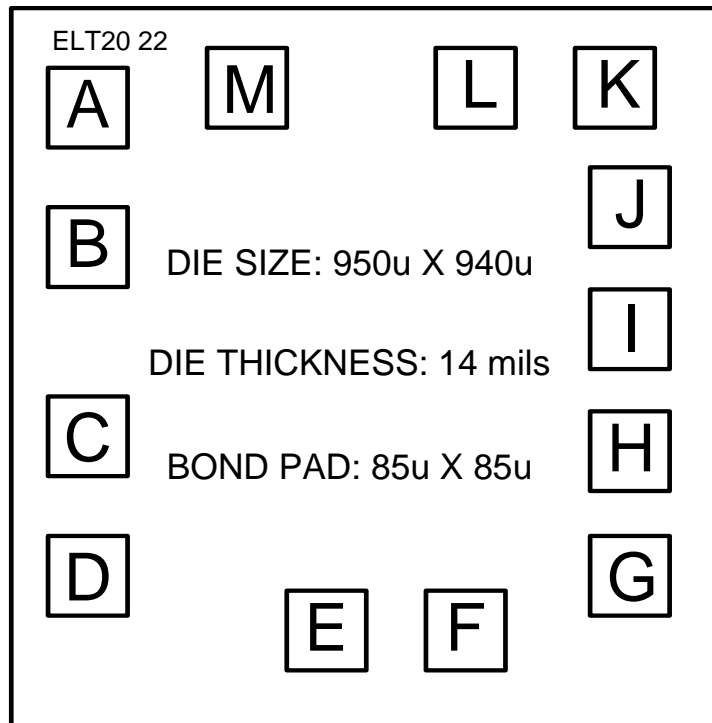
Leave Center Bottom Pad open or connect to GND.

AZ10ELT20D
AZ100ELT20D
AZ100ELT20T



DIE PAD COORDINATES

AZ10/100ELT20 DIE:



**Note: Other die thicknesses available. Contact factory for further information.
The die backside may be left open or connected to GND.**

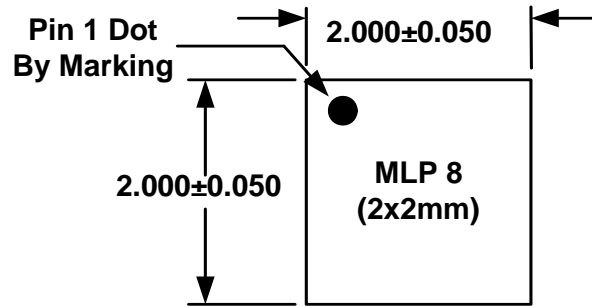
PAD CENTER COORDINATES

NAME	PAD DESIGNATION	X(Microns)	Y(Microns)
A	NC	-342.5	312.5
B	NC	-342.5	144.5
C	D	-342.5	-87.0
D	NC	-342.5	-255.0
E	V _{CC}	-33.5	-312.5
F	V _{CC}	126.5	-312.5
G	Q	312.5	-248.5
H	Q	312.5	-98.5
I	NC	312.5	51.5
J	NC	312.5	201.5
K	NC	302.5	342.5
L	10K	142.5	342.5
M	GND	-140.5	342.5

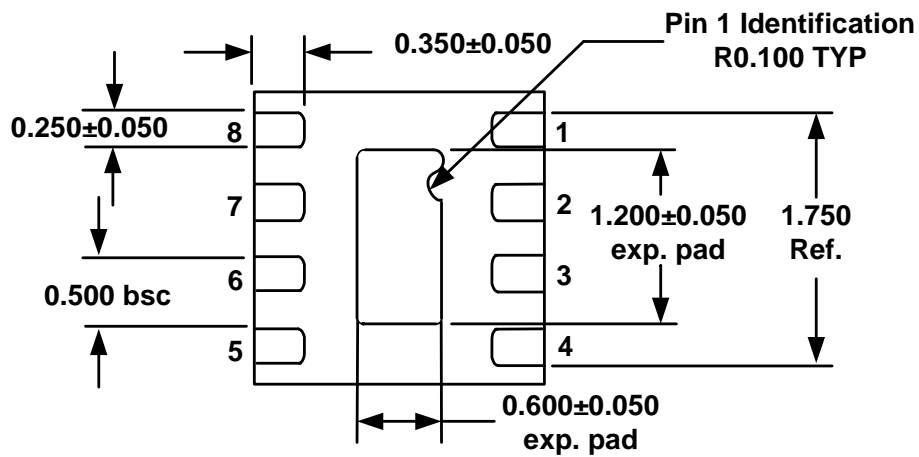
NC = No connect, leave open.

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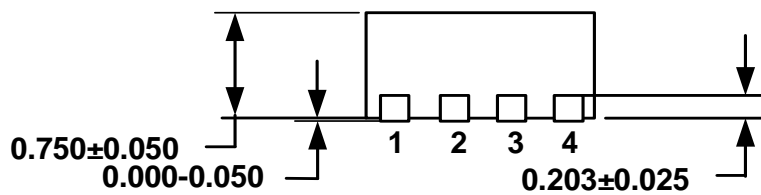
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



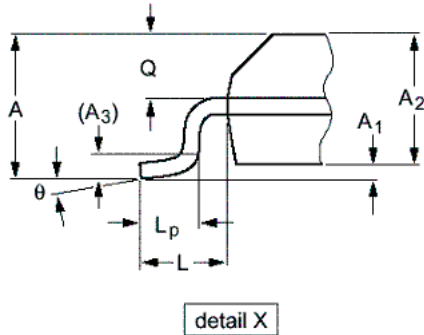
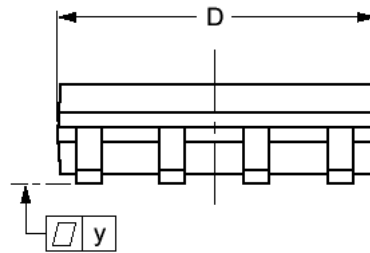
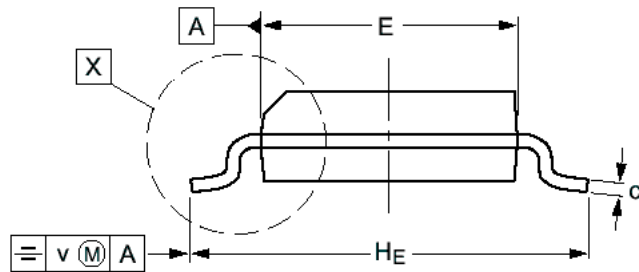
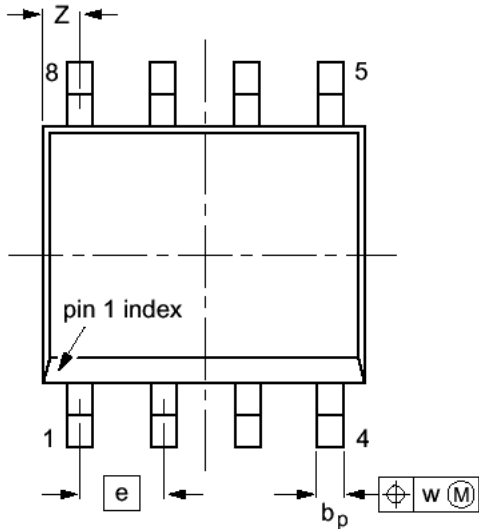
BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm

**PACKAGE DIAGRAM
SOIC 8**



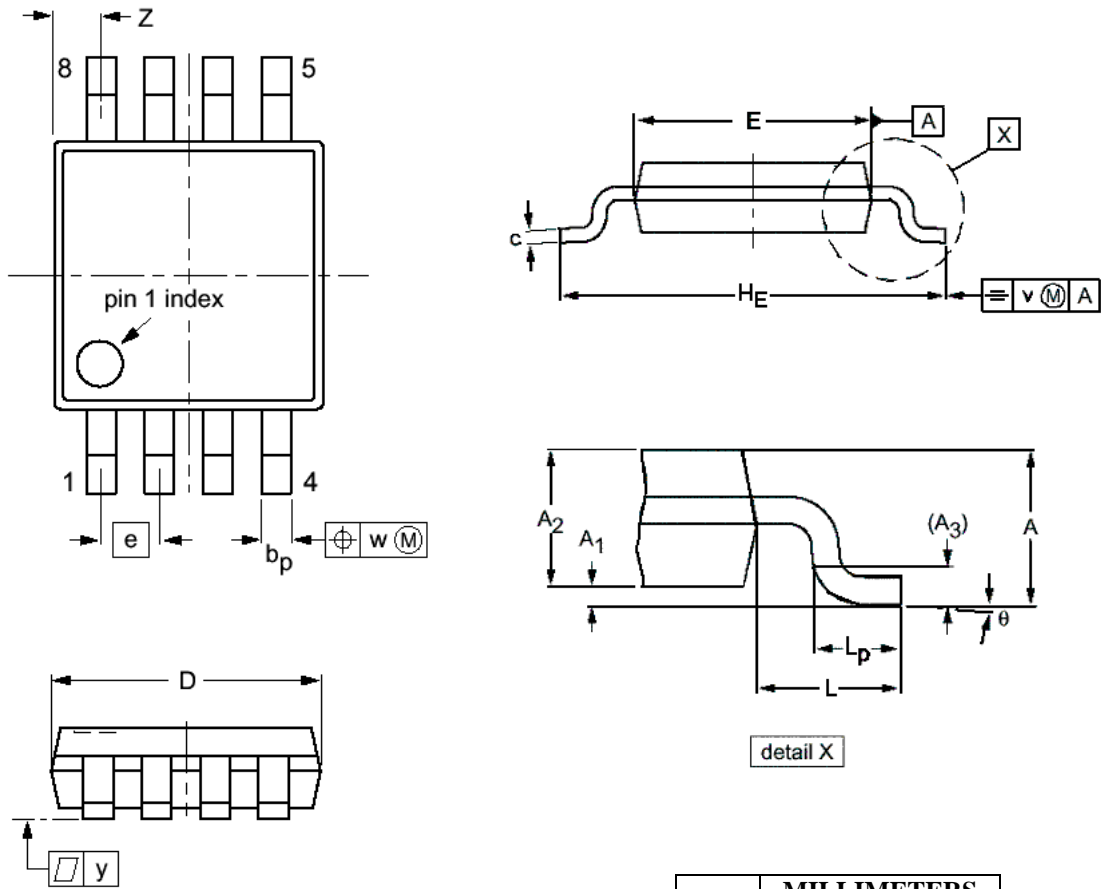
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.053	0.069
A ₁	0.10	0.25	0.004	0.010
A ₂	1.28	1.57	0.050	0.062
A ₃	0.25		0.01	
b _p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.80	5.00	0.19	0.20
E	3.80	4.00	0.15	0.16
e	1.27		0.050	
H _E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L _p	0.40	1.27	0.016	0.050
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

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PACKAGE DIAGRAM
TSSOP 8



NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.75	0.95
A ₃	0.25	
b _p	0.22	0.40
c	0.13	0.23
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.75	5.05
L	0.95	
L _p	0.40	0.70
v	0.10	
w	0.08	
y	0.10	
Z	0.38	0.64
θ	0°	6°

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