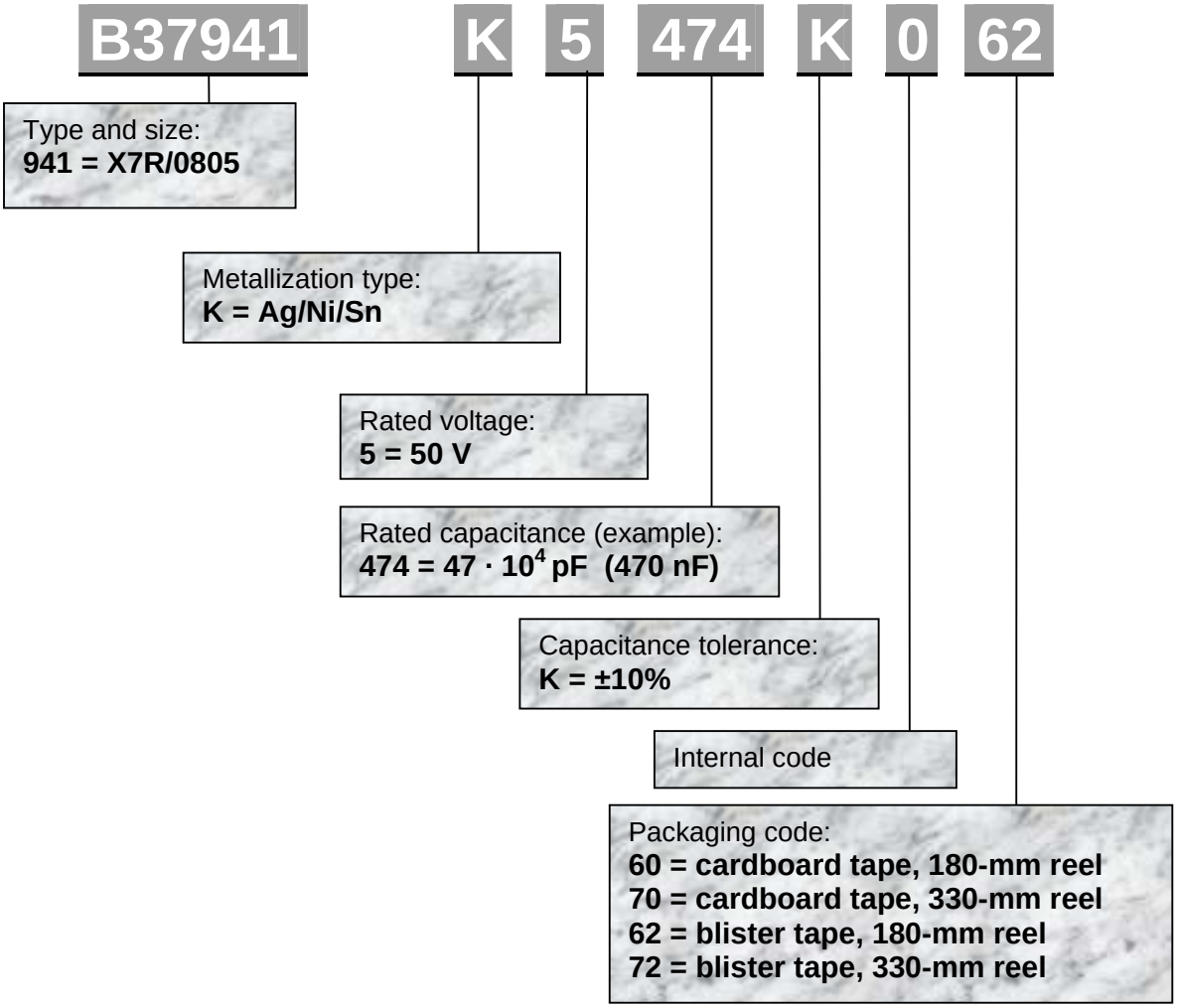
Multilayer ceramic capacitor

HighCV, X7R 0805 50 V

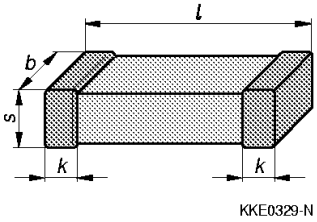
Series/Type: **Chip**
Ordering code: **B37941K5***K0****

Date: 25.10.2005
Version: 2

Ordering code



Dimensional drawing



Size [inch / mm]	l [mm]	b [mm]	s [mm]	k [mm]
0805 / 2012	2.0 ±0.20	1.25 ±0.15	1.35 max.	0.13 – 0.75

see also “Ordering codes and chip thickness”, dimensions in accordance to CECC 32101-801

Electrical data

Temperature characteristic:	X7R
Climatic category (IEC 60068-1):	55/125/56
Standard:	EIA
Dielectric:	Class 2
Rated voltage:	50 V
Capacitance[1)] test conditions	
Test frequency:	(1.0 ±0.2) kHz
Test voltage:	(1.0 ±0.2) V_{RMS}
Max. relative capacitance change:	±15%
Dissipation factor tanδ (limit value):	$< 25 \cdot 10^{-3}$
Time constant τ at +25 °C:	> 500 s
Operating temperature range:	–55 °C ... +125 °C
Capacitance value:	**220 … 470 nF**

[1)] Subject to aging, please see “General Technical Information” at www.epcos.com/ceramic_capacitors or the databook “Multilayer Ceramic Capacitors”.

Ordering codes and chip thickness

Size [inch]	C_R [nF]	Ordering code	Thickness [mm]	Packing quantity ∅ 180-mm reel [pcs]	Packing quantity ∅ 330-mm reel [pcs]
0805	220	B37941K5224K060*	0.80 ±0.1	4000	16000
	470	B37941K5474K062**	1.25 ±0.1	3000	12000

* Ordering code example — Standard tolerance: ±10%; Standard packaging: Cardboard, 180-mm reel

** Ordering code example — Standard tolerance: ±10%; Standard packaging: Blister tape, 180-mm reel

Further information

Please see General Technical Information at www.epcos.com/ceramic_capacitors or the data book "Multilayer Ceramic Capacitors" for further information on:

- Soldering directions
- Taping and packing
- Surface mounting instructions
- Effects of mechanical stress

Cautions and warnings

- Derating: A "state of the art" application design is essential to achieve failures rates at ppb level. Do not use designs based on 100% of specified rated values.
- AC applications may damage MLCC on a much lower level than DC voltage due to power dissipation losses.
- Mechanical stress - Please note EPCOS "General Technical Information", "Surface mounting instructions" and information about the effect of mechanical stress.
- ESD - EPCOS recommends the use of varistors.
- Further processing - care must be taken using moulding processes.
- Combined stresses - the total stress (e.g. DC voltage, AC ripple, pulses and temperature) has to be taken into account to estimate reliability of MLCC.

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