4-Pin µP Voltage Supervisor with Manual Reset

The IMP811/IMP812 are low-power supervisors designed to monitor voltage levels of 3.0V, 3.3V and 5.0V power supplies in low-power microprocessor (µP), microcontroller (µC) and digital systems. Each features a debounced manual reset input. The IMP811/812 are improved drop-in replacements for the Maxim MAX811/812 with extended temperature specifications to 105°C.

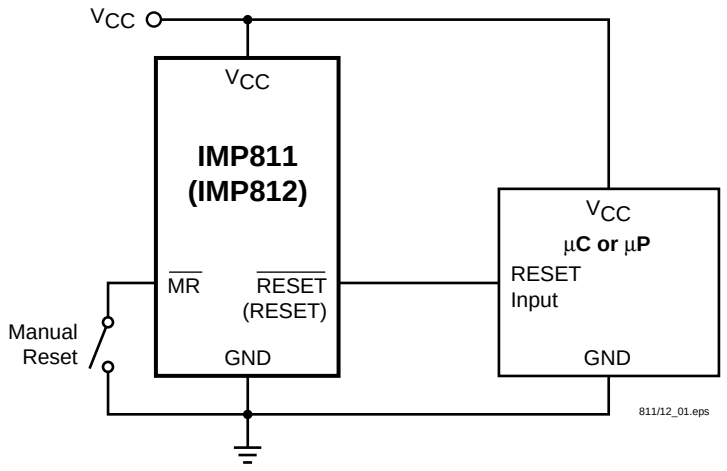
A reset signal is issued if the power supply voltage drops below a preset threshold and is asserted for at least 140ms after the supply has risen above the reset threshold. The IMP811 has an active-low output $\overline{\text{RESET}}$ that is guaranteed to be in the correct state for V_{CC} down to 1.1V. The IMP812 has an active-high output RESET. The reset comparator is designed to ignore fast transients on V_{CC} .

Low power consumption makes the IMP811/IMP812 ideal for use in portable and battery-operated equipment. Available in a compact 4-pin SOT143 package, the devices use minimal board space.

Six voltage thresholds are available to support 3V to 5V systems:

Reset Threshold	
Suffix	Voltage (V)
L	4.63
M	4.38
J	4.00
T	3.08
S	2.93
R	2.63

Block Diagrams



Key Features

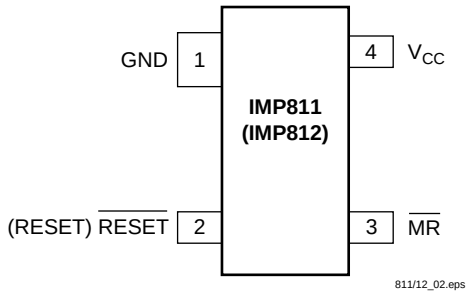
- Improved Maxim MAX811/MAX812 replacement
  - Specified to 105°C
  - New 4.0V threshold option
- 6µA supply current
- Monitor 5V, 3.3V and 3V supplies
- Manual reset input
- 140ms min. reset pulse width
- Guaranteed over temperature
- Active-LOW reset valid with 1.1V supply (IMP811)
- Small 4-pin SOT-143 package
- No external components
- Power-supply transient-immune design

Applications

- Computers and controllers
- Embedded controllers
- Battery operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

Pin Configuration

SOT143



Ordering Information

Part Number [1]	Reset Threshold (V)	Temperature Range	Pin-Package	Package Marking[2] (XX Lot Code)
IMP811 Active LOW Reset with Active LOW Manual Reset				
IMP811LEUS-T	4.63	–40°C to +105°C	4-SOT143	AMXX
IMP811MEUS-T	4.38	–40°C to +105°C	4-SOT143	ANXX
IMP811JEUS-T	4.00	–40°C to +105°C	4-SOT143	AOXX
IMP811TEUS-T	3.08	–40°C to +105°C	4-SOT143	APXX
IMP811SEUS-T	2.93	–40°C to +105°C	4-SOT143	AQXX
IMP811REUS-T	2.63	–40°C to +105°C	4-SOT143	ARXX
IMP812 Active HIGH Reset with Active LOW Manual Reset				
IMP812LEUS-T	4.63	–40°C to +105°C	4-SOT143	ASXX
IMP812MEUS-T	4.38	–40°C to +105°C	4-SOT143	ATXX
IMP812JEUS-T	4.00	–40°C to +105°C	4-SOT143	AUXX
IMP812TEUS-T	3.08	–40°C to +105°C	4-SOT143	AVXX
IMP812SEUS-T	2.93	–40°C to +105°C	4-SOT143	AWXX
IMP812REUS-T	2.63	–40°C to +105°C	4-SOT143	AXXX

Notes: *1. Tape and Reel packaging is indicated by the -T designation.*
2. Devices may also be marked with full part number: 811L, 812M etc. XX refers to lot.

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground

V_{CC} . . . . . –0.3V to 6.0V
RESET, $\overline{RESET}$ and $\overline{MR}$ . . . . . –0.3V to (V_{CC} + 0.3V)
Input Current at V_{CC} and $\overline{MR}$ 20mA
Output Current: RESET or $\overline{RESET}$ 20mA
Rate of Rise at V_{CC} 100V/µs

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability

Power Dissipation (T_A = 70°C) 320mW
(Derate SOT-143 4mW/°C above 70°C)
Operating Temperature Range . . . . . –40°C to 105°C
Storage Temperature Range . . . . . –65°C to 160°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

Electrical Characteristics

Unless otherwise noted V_{CC} is over the full voltage range, T_A = –40°C to 105°C.
Typical values at T_A = 25°C, V_{CC} = 5V for L/M/J devices, V_{CC} = 3.3V for T/S devices and V_{CC} = 3V for R devices.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Voltage (V_{CC}) Range	V_{CC}	T_A = 0°C to 70°C T_A = –40°C to 105°C		1.1 1.2		5.5 5.5	V
Supply Current (Unloaded)	I_{CC}	T_A = –40°C to 85°C T_A = –40°C to 85°C T_A = 85°C to 105°C T_A = 85°C to 105°C	V_{CC} < 5.5V, L/M/J V_{CC} < 3.6V, R/S/T V_{CC} < 5.5V, L/M/J V_{CC} < 3.6V, R/S/T		6 5	15 10 25 20	µA
Reset Threshold	V_{TH}	L devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	4.56 4.50 4.40	4.63	4.70 4.75 4.86	V
		M devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	4.31 4.25 4.16	4.38	4.45 4.50 4.56	
		J devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	3.93 3.89 3.80	4.00	4.06 4.10 4.20	
		T devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	3.04 3.00 2.92	3.08	3.11 3.15 3.23	
		S devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	2.89 2.85 2.78	2.93	2.96 3.00 3.08	
		R devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	2.59 2.55 2.50	2.63	2.66 2.70 2.76	
Reset Threshold Temp. Coefficient	TC_{VTH}				30		ppm/°C
V_{CC} to Reset Delay		V_{CC} = V_{TH} to (V_{TH} - 125mV), L/M/J devices			40		µs
		V_{CC} = V_{TH} to (V_{TH} - 125mV), R/S/T devices			20		
Reset Active Timeout Period	V_{OL}	T_A = 0°C to 70°C		140		560	ms
		T_A = –40°C to 105°C		100		840	
$\overline{MR}$ Minimum Pulse Width	t_{MR}			10			µs
$\overline{MR}$ Glitch Immunity		Note 3			100		ns
$\overline{MR}$ to RESET Propagation Delay	t_{MD}	Note 2			0.5		µs
$\overline{MR}$ Input Threshold	V_{IH}	V_{CC} > $V_{TH\ (MAX)}$, IMP811/812L/M/J		2.3			V
	V_{IL}					0.8	
	V_{IH}	V_{CC} > $V_{TH\ (MAX)}$, IMP811/812R/S/T		0.7V_{CC}			
	V_{IL}					0.25V_{CC}	
$\overline{MR}$ Pull-up Resistance				10	20	30	kΩ
Low $\overline{RESET}$ Output Voltage (IMP811)	V_{OL}	V_{CC} = V_{TH} min., I_{SINK} = 1.2mA, IMP811R/S/T				0.3	V
		V_{CC} = V_{TH} min., I_{SINK} = 3.2mA, IMP811L/M/J				0.4	
		V_{CC} > 1.1V, I_{SINK} = 50µA				0.3	
High $\overline{RESET}$ Output Voltage (IMP811)	V_{OH}	V_{CC} > V_{TH} max., I_{SOURCE} = 500µA, IMP811R/S/T		0.8V_{CC}			V
		V_{CC} > V_{TH} max., I_{SOURCE} = 800µA, IMP811L/M/J		V_{CC} -1.5			
Low RESET Output Voltage (IMP812)	V_{OL}	V_{CC} = V_{TH} max., I_{SINK} = 1.2mA, IMP812R/S/T				0.3	V
		V_{CC} = V_{TH} max., I_{SINK} = 3.2mA, IMP812L/M/J				0.4	
High RESET Output Voltage (IMP812)	V_{OH}	1.8V < V_{CC} < V_{TH} min., I_{SOURCE} = 150µA		0.8V_{CC}			V

Notes: *1. Production testing done at T_A = 25°C. Over temperature specifications guaranteed by design only using six sigma design limits.*
2. $\overline{RESET}$ output is active LOW for the IMP811 and RESET output is active HIGH for the IMP812.
3. Glitches of 100ns or less typically will not generate a reset pulse.

Pin Descriptions

Pin Number	Name	Function
1	GND	Ground
2 (IMP811)	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is asserted LOW if V_{CC} falls below the reset threshold and remains LOW for the 140ms minimum after the reset conditions are removed. In addition, $\overline{\text{RESET}}$ is active LOW as long as the manual reset is low.
2 (IMP812)	RESET	RESET is asserted HIGH if V_{CC} falls below the reset threshold and remains HIGH for the 140ms minimum after the reset conditions are removed. In addition, RESET is active HIGH as long as the manual reset is low.
3	$\overline{\text{MR}}$	Manual Reset Input. A logic LOW on $\overline{\text{MR}}$ asserts RESET. RESET remains active as long as $\overline{\text{MR}}$ is LOW and for 180ms after $\overline{\text{MR}}$ returns HIGH. The active low input has an internal 20kΩ pull-up resistor. The input should be left open if not used. It can be driven by TTL or CMOS logic or shorted to ground by a switch..
4	V_{CC}	Power supply input voltage (3.0V, 3.3V, 5.0V)

Related Products

	IMP809	IMP810	IMP811	IMP812
Max. Supply Current	15µA	15µA	15µA	15µA
Package Pins	3	3	4	4
Manual RESET input			■	■
Package Type	SOT-23	SOT-23	SOT-143	SOT-143
Active-HIGH RESET output		■		■
Active-LOW RESET output	■		■	

Detailed Description

Reset Timing and Manual Reset ($\overline{MR}$)

The reset signal is asserted–LOW for the IMP811 and HIGH for the IMP812 – when the V_{CC} signal falls below the threshold trip voltage and remains asserted for 140ms minimum after the V_{CC} has risen above the threshold.

A logic low on $\overline{MR}$ asserts $\overline{RESET}$ LOW on the IMP811 and HIGH on the IMP812. $\overline{MR}$ is internally pulled high through a 20kΩ resistor and can be driven by TTL/CMOS gates or with open collector/drain outputs. $\overline{MR}$ can be left open if not used.

$\overline{MR}$ may be connected to a normally-open switch connected to ground without an external debounce circuit.

For added noise rejection, a 0.1µF capacitor from $\overline{MR}$ to Ground can be added.

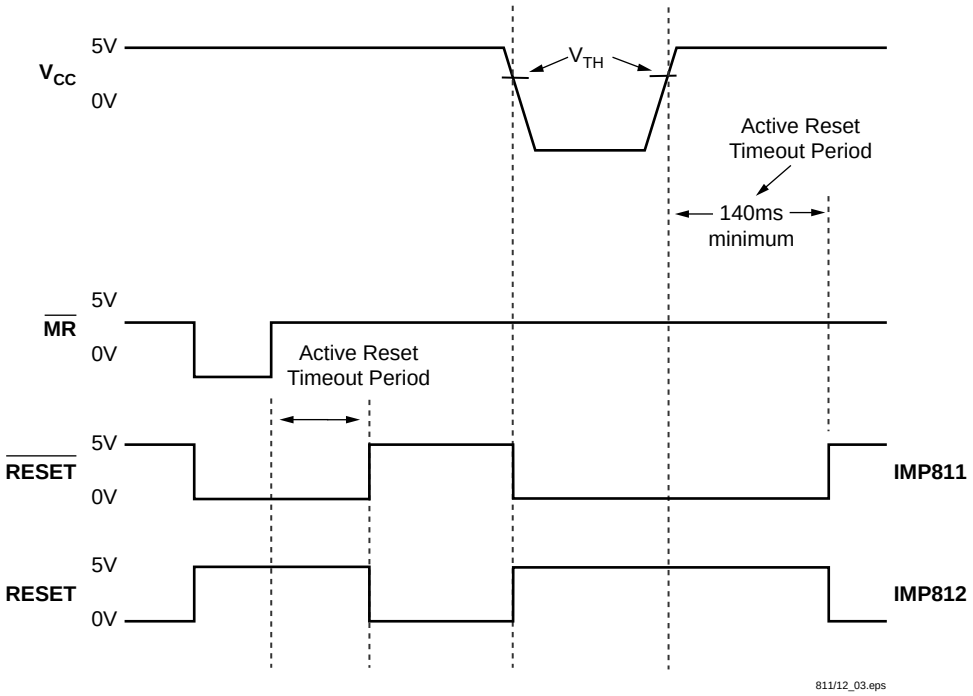


Figure 1. Reset Timing and Manual Reset (MR)

Application Information

RESET Output Operation

In µP/µC systems it is important to have the processor begin operation from a known state or be able to return the system to a known state. A RESET output to a processor is provided to prevent improper operation during power supply sequencing or low voltage – brownout – conditions.

The IMP811/812 are designed to monitor the system power supply voltages and issue a RESET signal when levels are out of range. RESET outputs are guaranteed to be active for V_{CC} above 1.1V. When V_{CC} exceeds the reset threshold, an internal timer keeps RESET active for the reset timeout period, after which RESET becomes inactive (HIGH for the IMP811 and LOW for the IMP812).

If V_{CC} drops below the reset threshold, RESET automatically becomes active. Alternatively, external circuitry or a human operator can initiate this condition using the Manual Reset ($\overline{MR}$) pin. There is an internal pullup on $\overline{MR}$ so it can be left open if it is not used. $\overline{MR}$ can be driven by TTL/CMOS logic or even an external switch, since it is already debounced. If the switch is at the end of a long cable, it might require a bypass (100nF) at the pin if noise pickup is a problem.

Six voltage thresholds are available to support 3V and 5V systems:

Reset Threshold	
Suffix	Voltage (V)
L	4.63
M	4.38
J	4.00
T	3.08
S	2.93
R	2.63

Valid Reset with V_{CC} under 1.1V

To ensure that logic inputs connected to the IMP811 $\overline{RESET}$ pin are in a known state when V_{CC} is under 1.1V, a 100kΩ pull-down resistor at $\overline{RESET}$ is needed. The value is not critical.

A similar pull-up resistor to V_{CC} is needed with the IMP812.

Negative V_{CC} Transients

Typically short duration transients of 100mV amplitude and 20µs duration do not cause a false RESET. A 0.1µF capacitor at V_{CC} increases transient immunity.

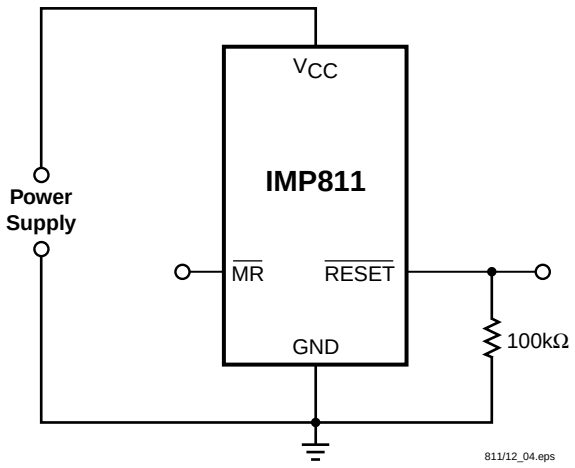


Figure 2. RESET Valid with V_{CC} Under 1.1V

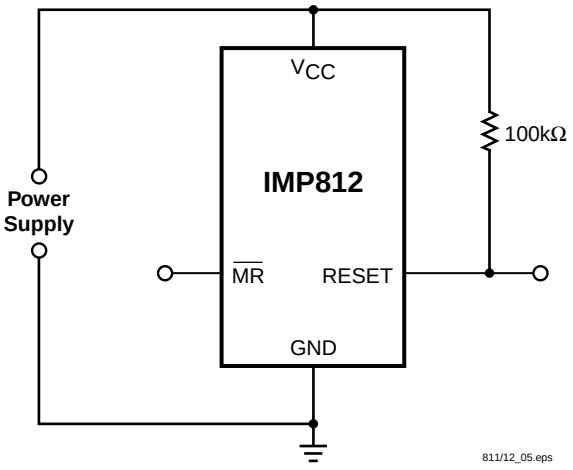


Figure 3. RESET Valid with V_{CC} Under 1.1V

Bi-directional Reset Pin Interfacing

The IMP811/812 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the IMP809/810 reset output and the µP/µC bi-directional reset pin.

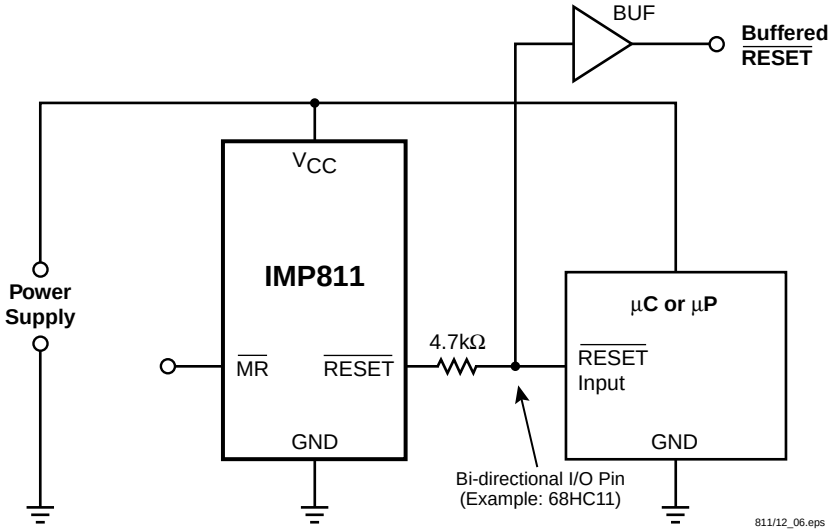
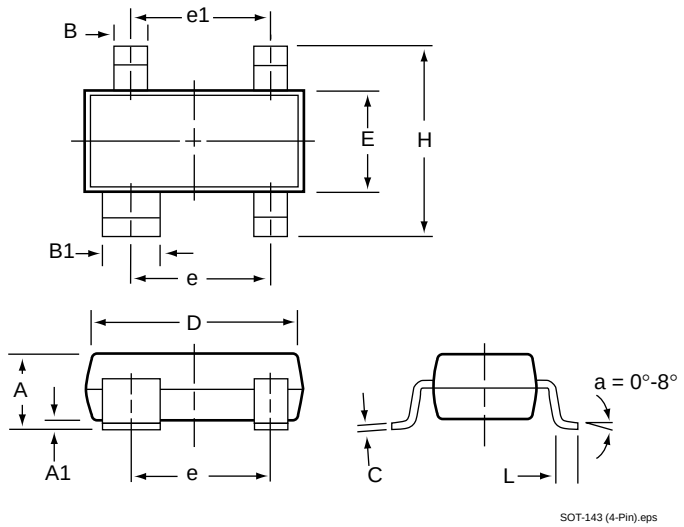


Figure 4. Bi-directional Reset Pin Interface

Package Dimensions

Plastic SOT-143 (4-Pin)



	Inches		Millimeters	
	Min	Max	Min	Max
Plastic SOT-143 (4-Pin)				
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
B1	0.030	0.038	0.762	0.965
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
e1	0.071	0.079	1.803	2.007
H	0.082	0.098	2.083	2.489
I	0.004	0.012	0.102	0.305

ISO 9001 Registered

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