DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAC-9630
CMOS IMAGE SENSOR

126 (H) X 98 (V)
Ultra Sensitive Global Shutter 580 fps Monochrome CIS

September 2004
Revision 1.1

KAC-9630 126(H)x98(V), 580 fps Ultra Sensitive Monochrome CMOS Image Sensor

General Description

The KAC-9630 is a high performance, low power, CMOS Active Pixel Image Sensor capable of capturing grey-scale images at 580 frames per second.

In addition to the active pixel array, an on-chip 8 bit A/D convertor, fixed pattern noise elimination circuits and a video gain amplifier are provided.

The integrated programmable timing and control circuit allows the user maximum flexibility in adjusting integration time and frame rate. Furthermore, a fast read out circuit is provided allowing a full frame to read out on a single 8-bit digital data bus in less than 2ms.

The sensor utilizes a patented pixel design that incorporates an integrated electronic shutter. This together with its ultra high sensitivity makes the KAC-9630 an ideal choice for low light imaging applications or applications where images of fast moving objects need to be captured with minimum motion blur.

Applications

- High Speed Motion Detection
- IR Imaging
- Low Light Imaging Applications

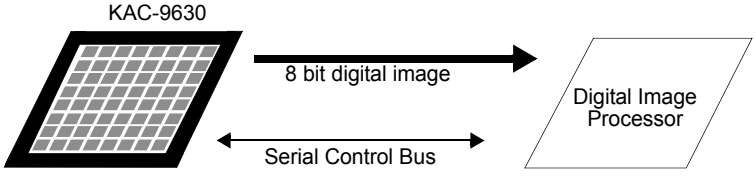
Features

- Electronic shutter with pixel exposure.
- Programmable analog video gain.
- Integrated 8 bit analog to digital conversion.
- Programmable integration time.
- Programmable frame rate.
- Master and slave mode of operation
- On chip black level compensation.
- Power down and low power modes.
- I^2C compatible serial interface.
- 10 bit digital video port (8 data, vertical & horizontal sync).
- Power on reset with hardware and software override.

Key Specifications

Array Format Total Active	 128H x 101V 126H x 98 V
Effective Image Area Total Active	 2.56 mm x 2.00 mm 2.52 mm x 1.96 mm
Pixel Size	20μm x 20μm
Video Outputs	8 Bit Digital
Sensitivity	22 Volt/lux.s
Dark Level	< 10 LSBs
Read Noise	< 1 LSB
Frame Rate	580 frames / sec
Read Out Time	2 ms
Integration Time	10μs - 20ms in steps of 10 μs
Idle Time	10μs - 20ms in steps of 10 μs
Wake up time	10 msec
Package	32 CLCC
Single Supply	3.0V to 3.3V
Power Consumption	<130 mW in low power mode < 1mW in sleep mode
Operating Temp	-40°C to 85°C

System Block Diagram



Chip Block Diagram

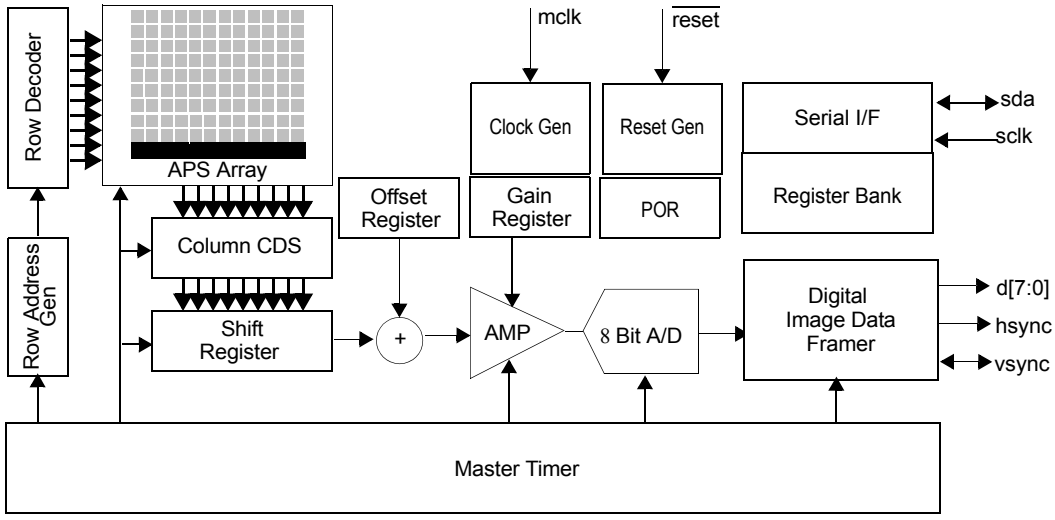


Figure 1: Chip Block **Diagram**

Chip Pin Out

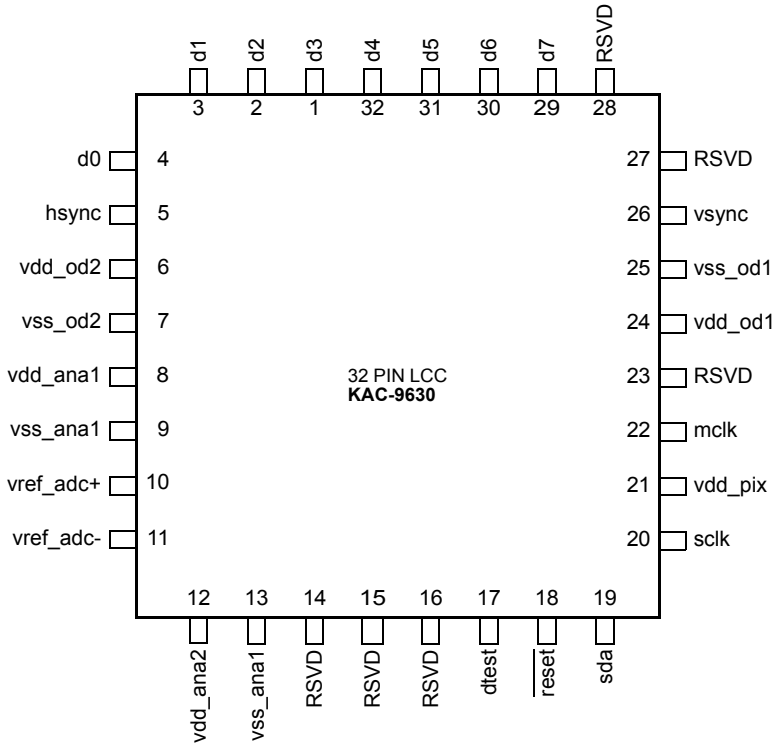


Figure 2: Pin Out Diagram (top view)

Ordering Information

KAC-9630 32 LCC parts	KAC-9630TBD
A small PCB that houses KAC-9630 sensor together with all discrete components.	KAC-9630HEADBOARD

Typical Application Circuit

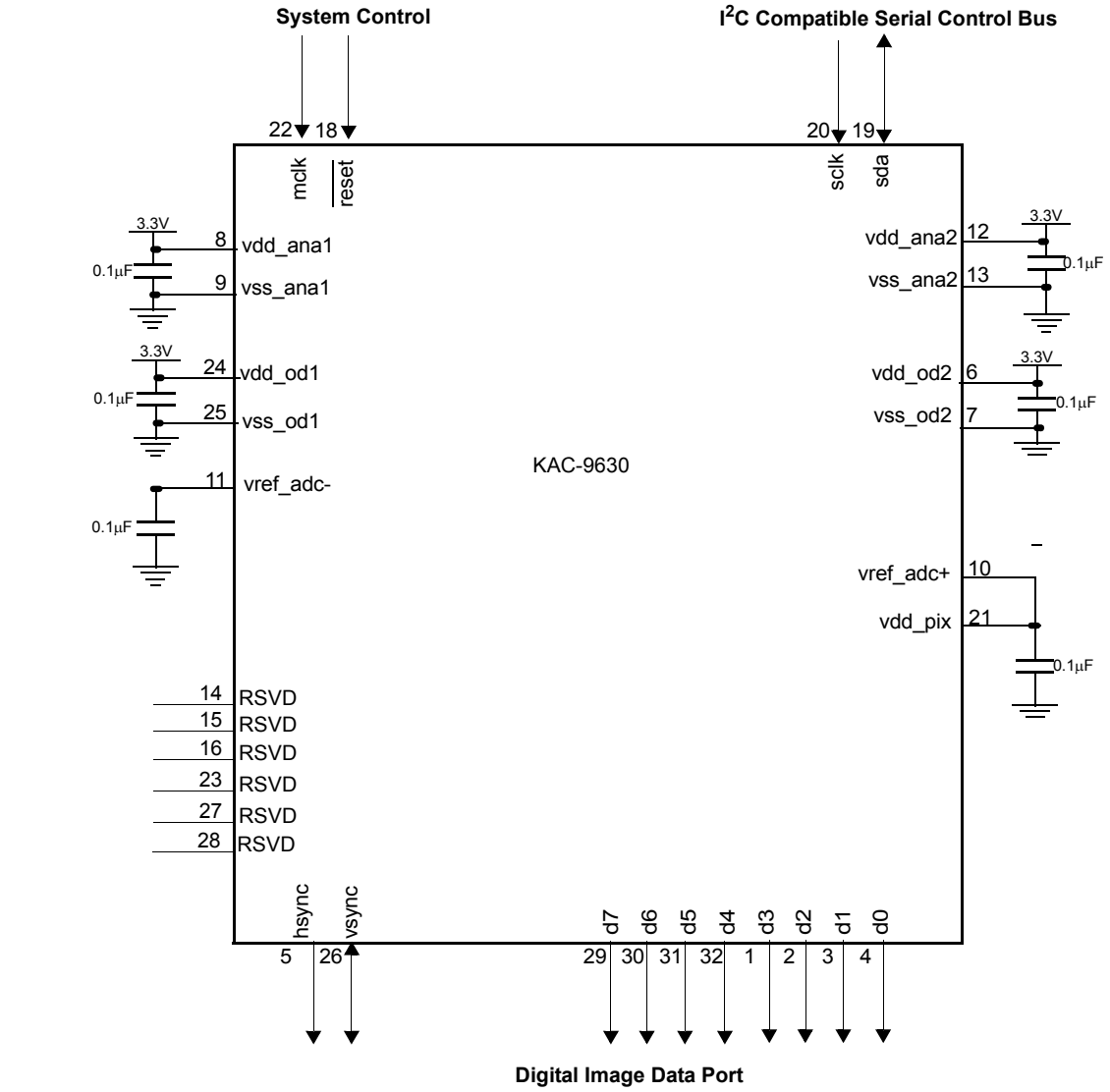


Figure 3: Typical Application Circuit Diagram

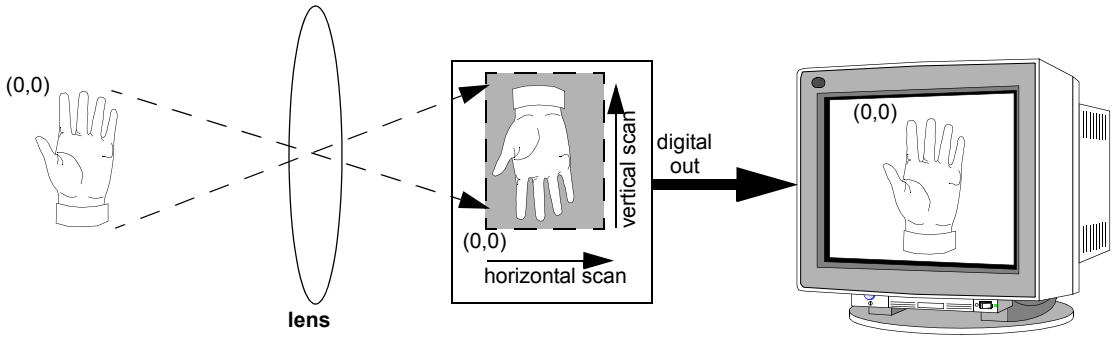


Figure 4: Scan directions and position of origin in imaging system

Pin Descriptions

LCC Pin	Name	I/O	Typ	Description
1	d3	O	D	Digital output. Bit 3 of the digital video output bus.
2	d2	O	D	Digital output. Bit 2 of the digital video output bus.
3	d1	O	D	Digital output. Bit 1 of the digital video output bus.
4	d0	O	D	Digital output. Bit 0 of the digital video output bus. This pin is also the serial pixel out pin.
5	hsync	O	D	Digital output. This pin is the horizontal synchronization signal.
6	vdd_od2	I	P	3.3 volt supply for the digital IO buffers.
7	vss_od2	I	P	0 volt supply for the digital IO buffers
8	vdd_ana1	I	P	3.3 volt supply for analog circuits.
9	vss_ana1	I	P	0 volt supply for analog circuits.
10	vref_adc+	I	A	Reference ladder input for ADC. Note this pin should always be tied to vdd_pix+ pin and bypassed with a 0.1μf capacitor.
11	vref_adc-	I	A	Reference ladder input for ADC. Bypass with 0.1uF capacitor to ground.
12	vdd_ana2	I	P	3.3 volt supply for analog circuits.
13	vss_ana2	I	P	0 volt supply for analog circuits.
14	RSVD			Reserved, do not connected.
15	RSVD			Reserved, do not connected.
16	RSVD			Reserved, do not connected.
17	dtest	I	D	Factory test pin, do not connect.
18	$\overline{\text{reset}}$	I	D	Digital input with pull up resistor. Active low system reset pin.
19	sda	IO	D	I^2C compatible serial interface data bus. The output stage of this pin has an open drain driver.
20	sclk	I	D	I^2C compatible serial interface clock.
21	vdd_pix	I	P	3.0 Volt supply for the pixel array. Note this pin should always be tied to vref_adc+ pin and bypassed with a 0.1μf capacitor.
22	mclk	I	D	Digital input. This pin is the 10 MHz master clock.
23	RSVD			Reserved, do not connect.
24	vdd_od1	I	P	3.3 volt supply for the digital IO buffers.
25	vss_od1	I	P	0 volt supply for the digital IO buffers
26	vsync	IO	D	Digital Bidirectional with pull down resistor. This pin is an output in video mode and is the vertical synchronization signal. In snapshot mode the pin is an input and is the external frame trigger.
27	RSVD			Reserved, do not connect.
28	RSVD			Reserved, do not connect.
29	d7	O	D	Digital output. Bit 7 of the digital video output bus.
30	d6	O	D	Digital output. Bit 6 of the digital video output bus.
31	d5	O	D	Digital output. Bit 5 of the digital video output bus.
32	d4	O	D	Digital output. Bit 4 of the digital video output bus.

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog).

Absolute Maximum Ratings (Notes 1 & 2)

Any Positive Supply Voltage	4.2V
Voltage On Any Input or Output Pin	-0.3V to 4.2V
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Machine Model	200V
Storage Temperature	-40°C to 150°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range (Note 10)	$-40°C \leq T_A \leq +85°C$
All Supply Voltages	+3.0V to +3.6V

DC and Logic Level Specifications

The following specifications apply for supplies= +3.3V, C_L = 10pF, and M_{CLK} = 10 MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
Digital Input Characteristics						
VIH	Logical “1” Input Voltage		**2.0**			V
VIL	Logical “0” Input Voltage				**1.0**	V
IIH	Logical “1” Input Current	VIH = vdd_od, Digital inputs except Reset		100		nA
		VIH = vdd_od, Reset (internal pull-down resistor)		400		µA
IIL	Logical “0” Input Current	VIL = vss_dig		-100		nA
Digital Output Characteristics						
VOH	Logical “1” Output Voltage	vdd_od = 3.6V, Iout = -0.5mA vdd_od = 3.0V, Iout = -0.5mA	**2.5** **2.3**			V
VOL	Logical “0” Output Voltage	vdd_od = 3.6V, Iout = 1.6mA vdd_od = 3.0V, Iout = 1.6mA			**0.4** **0.4**	V
IOS	Output Short Circuit Current			30		mA
Power Supply Characteristics						
IA	Analog Supply Current			42		mA
ID	Digital Supply Current			1		mA

Power Dissipation Specifications

The following specifications apply for supplies= +3.3V, C_L = 10pF, and M_{CLK} = 10MHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C)

Symbol	Parameter	Conditions	Min (note 9)	Typical (note 8)	Max (note 9)	Units
PWR	Average Power Dissipation	Full operational mode @ 3.3V		130		mW
		Power down mode @3.3V		2		mW

Video Amplifier Specifications

The following specifications apply for supply= +3.3V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Steps	Range
G	Video Amplifier Nominal Gain	32 Logarithmic steps	1-28.1

AC Electrical Characteristics

The following specifications apply for supply= +3.3V. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
mclk	Input Clock Frequency		**8**		**10**	MHz
T_{ch}	Clock High Time	@ $mclk_{max}$	**45**			ns
T_{cl}	Clock Low Time	@ $mclk_{max}$	**45**			ns
	Clock Duty Cycle	@ $mclk_{max}$	**45**		**55**	
T_{rc}, T_{fc}	Clock Input Rise and Fall Time			3		ns

CMOS Active Pixel Array Specifications

Parameter	Value	Units
Number of pixels (row, column)	101 x 128	Pixels
Array size (x,y Dimensions)	2.56 x 2.00	mm
Pixel Pitch	20	µ

Image Sensor Specifications

The following specifications apply for supply= +3.3V.

Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
Optical Sensitivity	White Light 2850°K, 700nm IR cutoff filter & Unity gain		22		V/(lux.s)
Shutter Light RejectionRatio[1]	@ All gain settings	**52**			dB
Dark Signal[2]	@ digital output of sensor in dark with 1ms integration time and unity gain. @ digital output of sensor in dark with 0.1 ms integration time and 10X gain.[5]			**10** **10**	LSBs
Read Noise[3]	@ unity gain @ 10 x gain[5]		<1.0 <2.0	**1** **3**	LSBs
Offset FPN[4]	RMS% of full scale at unity gain RMS% of full scale at 10X gain		0.5 5	**3** **20**	%
Sensitivity FPN[5]	RMS deviation in%		1.3	**3**	%

1 The ratio of the sensitivity of the sensor when the shutter is open to when it is closed.
2 The signal at the output of the ADC due to the dark current of the photo diode inside the pixel. This does not include any offset components which can be cancelled by the on-chip offset compensation DAC
3 The read noise is the RMS temporal black readout noise of a single pixel measured at the output of the ADC and averaged over all pixels in the array. The dynamic range can be calculated from the read noise as the ratio between the maximum ADC output code and the read noise expressed in dB.
3 Offset FPN is the RMS spatial noise in a random-noise free image taken at zero illumination.
4 Sensitivity FPN is the RMS percentage mismatch of the sensitivity between the individual pixels in the array.
5. It is not recomended to operate the sensor above 10X gain if these specs are to be maintained.

Sensor Response Curves

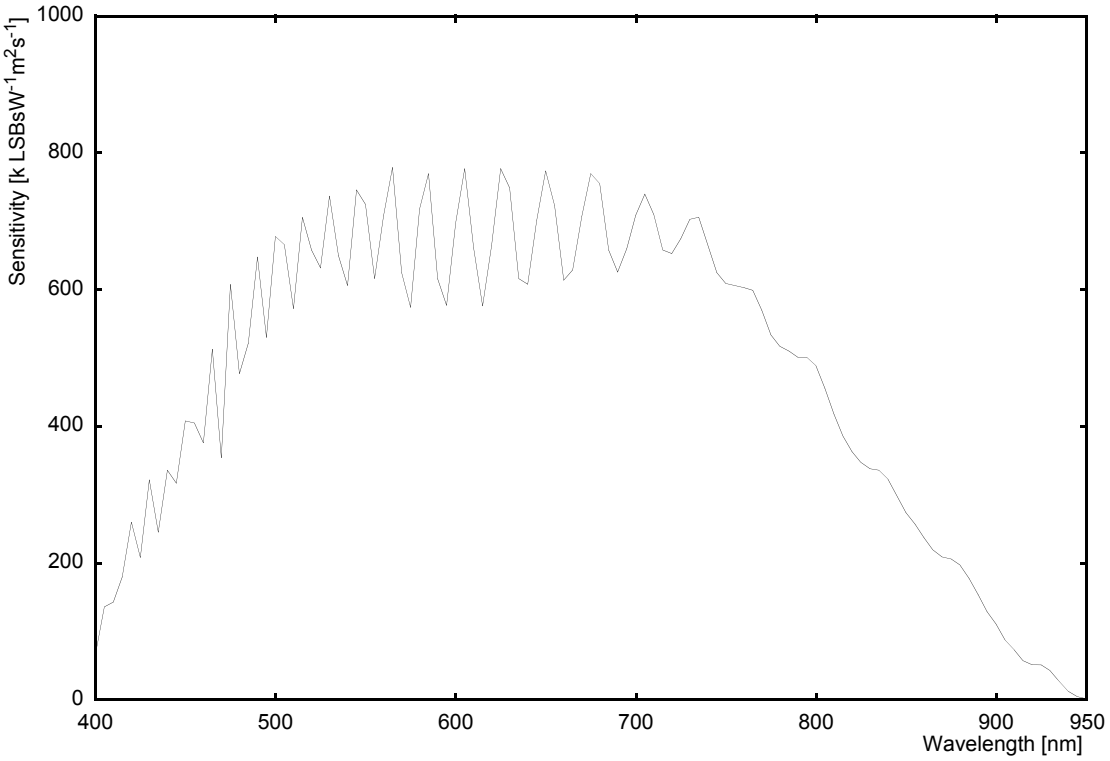


Figure 5: Spectrum Response Curve

General System Overview

Light Capture and Conversion

The KAC-9630 contains a CMOS active pixel array consisting of 101 rows by 128 columns. The last row in the array consists of optically shielded (black) pixels as shown in figure below.

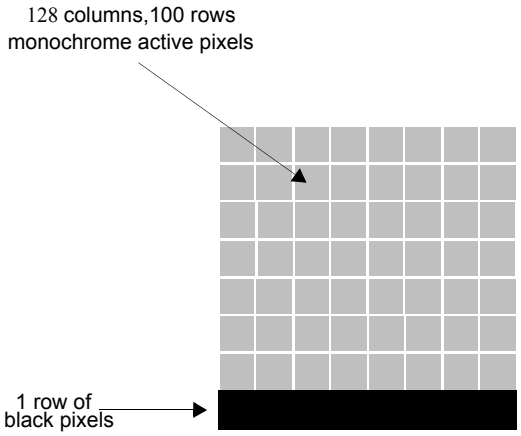


Figure 6: CMOS APS region of the KAC-9630

At the beginning of a given integration time the on-board timing and control circuit will reset every pixel in the array simultaneously.

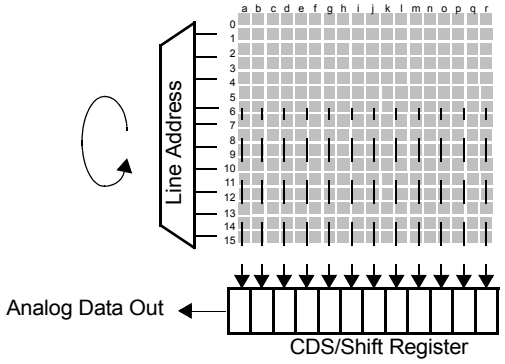


Figure 7: CMOS APS Row and Column addressing scheme

At the end of the integration time, the timing and control circuit will stop the integration time of every pixel in the array simultaneously.

There is no delay between the beginning of the integration period for the first and last pixels of a given frame.

At the end of the integration time, the timing and control circuit will address each row and simultaneously transfer the integrated value of the pixel to a correlated double sampling circuit and then to a shift register as shown in figure 7.

Once the correlated double sampled data has been loaded into the shift register, the timing and control circuit will shift them out one pixel at a time starting with column “a”.

The pixel data is then fed into an analog video amplifier, where a user programmed gain can be applied.

After gain adjustment the analog value of each pixel is converted to 8 bit digital data as shown in figure 8.

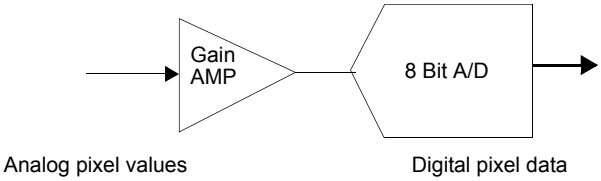


Figure 8: Analog Signals In, Digital Data Out.

Program and Control Interfaces

The programming, control and status monitoring of the KAC-9630 is achieved through a four wire serial bus. (see figure 9).

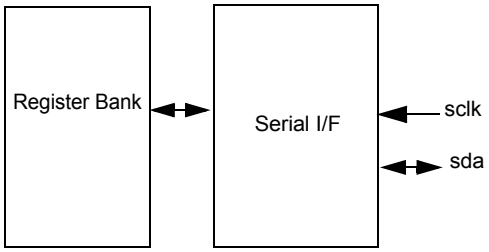


Figure 9: Control Interface to the KAC-9630.

Readout

The row of black pixels is always read out first, one pixel at a time, starting with the left most pixel. This is followed by the consecutive reading out of every pixel in every row of the active pixel array, one pixel at a time, starting with the left most pixel in the top most row. Hence, for the example shown in figure 10, the read out order will be *a0,b0,...,r0* then *a1,b1,...,r1* and so on until pixel *r20* is read out.

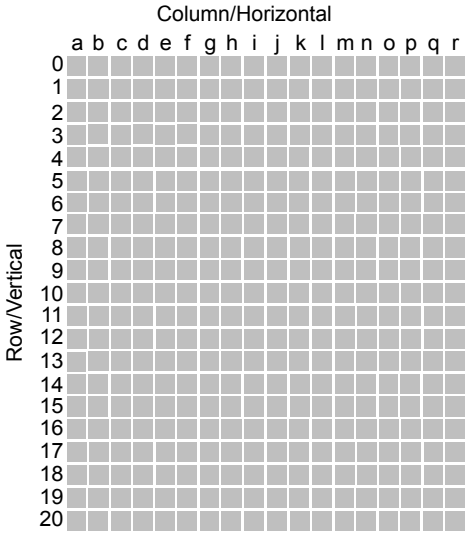


Figure 10: Array Readout

System Reset

The KAC-9630 is equipped with an integrated power on reset block that will ensure that all configuration registers will power up with their respective default values.

An external reset pin, $\overline{reset}$, is provided so that the chip can be reset at any time after power up without the need to power down and power up.

This is a synchronous reset so a clock must be running on the *mclk* pin. It takes one *mclk* clock cycle for the reset to take effect.

In addition to the external $\overline{reset}$ pin it is possible to reset the sensor by writing to the rest bit (*res)* in the *Main Configuration Register* (MFGC). The timing and control circuit will automatically clear this bit upon completion of the reset.

Power Management

Power Up and Down

The KAC-9630 is equipped with an on-board power management system allowing the analog and digital circuitry to be switched off (power down) and on (power up) at any time.

The sensor can be put into power down mode by writing to the power down bit (*PwrDown*) in the *Main Configuration Register* (MCFG).

The digital master clock will be internally switched off. A clock must be running at the *mclk* pin before power up can be achieved.

When the power down bit is asserted during frame integration or readout time, the sensor will enter power down state after the frame has been read out completely.

Advanced Power Mode

In addition to the power up/power down feature, the analog video amplifier can be powered down and its input signal can be connected directly to the A/D as illustrated in figure 11.

This flexibility allows power dissipation to be traded of with signal gain as shown in the table below:

PGA Amp	Power Saving
on	0mW
off	25mW

The video gain amplifier can be powered down and bypassed by writing to the (*PwdAmp*) & (*BypassAmp*) bits in the *Main configuration Register* (MFCG)

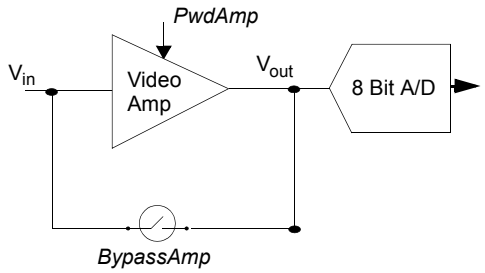


Figure 11: Advance Power Mode

Analog Gain

The analog signal out of the active pixel array can be amplified up to 28.1 times in 32 logarithmic steps. The gain can be calculated as follows:

$$Gain = 1.11^{VidGain}$$

Where:

VidGain is the programmed value in the *Video Gain Register* (VGAIN).

The gain setting can be programmed at any time, the internal timing and control circuit will only update the gain setting during the horizontal blanking time.

Video and Snapshot Mode

The image sensor can be operated in two modes, video and snapshot.

Video Mode

In video mode the sensor will continually capture and read out images at the programmed frame rate.

Snapshot Mode

In snapshot mode the sensor is externally triggered to capture and read out a single frame.

Upon reset the senor will operate in snapshot mode. To operate the sensor in video mode, bit 0 of the *Main Configuration Register* (MCFG) must be set to a logic 0.

Frame Rate Programming

General Operation

A frame is defined as the time it takes to reset every pixel in the array, integrate the incident light, convert it to digital data and present it on the digital video port. Figure 12 shows the sensor's Master Timer FSM.

For correct operation all frame rate programming registers should only be updated during array read out.

Integration Time

The integration time is user programmable and is given by:

$$T_{integration} = (100 * N_{int}) * P_{mclk}$$

Where:

N_{int} is a user programmable delay. This delay is held in the *Integration Time Registers* (ITIMEH & ITIMEL)

P_{mclk} is the period of the master clock *mclk*.

Idle Time

The Idle time is the time from the beginning of a frame to the point that all pixels in the array are reset and the shutter is opened and as is given by:

$$T_{idle} = (100 * N_{idle} + 2) * P_{mclk}$$

Where:

N_{idle} is a user programmable delay. This delay is held in the *Idle Time Register* (IDLE).

P_{mclk} is the period of the master clock *mclk*.

Idle time is only used in video mode.

Read Out Time

The time it will take to readout a complete frame including the row of black pixels is given by:

$$T_{readout} = (128 * \sigma + 40) * 101 * P_{mclk}$$

Where:

σ is 1 when the digital image data port is operating in parallel mode and 8 when the digital image data port is operating in serial mode.

The horizontal blanking time is 40 clocks.

Frame Rate

The frame rate in frames per second is given by:

$$F_{rate} = \frac{1}{T_{idle} + T_{integration} + T_{readout}}$$

Note: Integration (N_{int}) and Idle (N_{idle}) delays can be programmed at any time but will not take effect until the next frame.

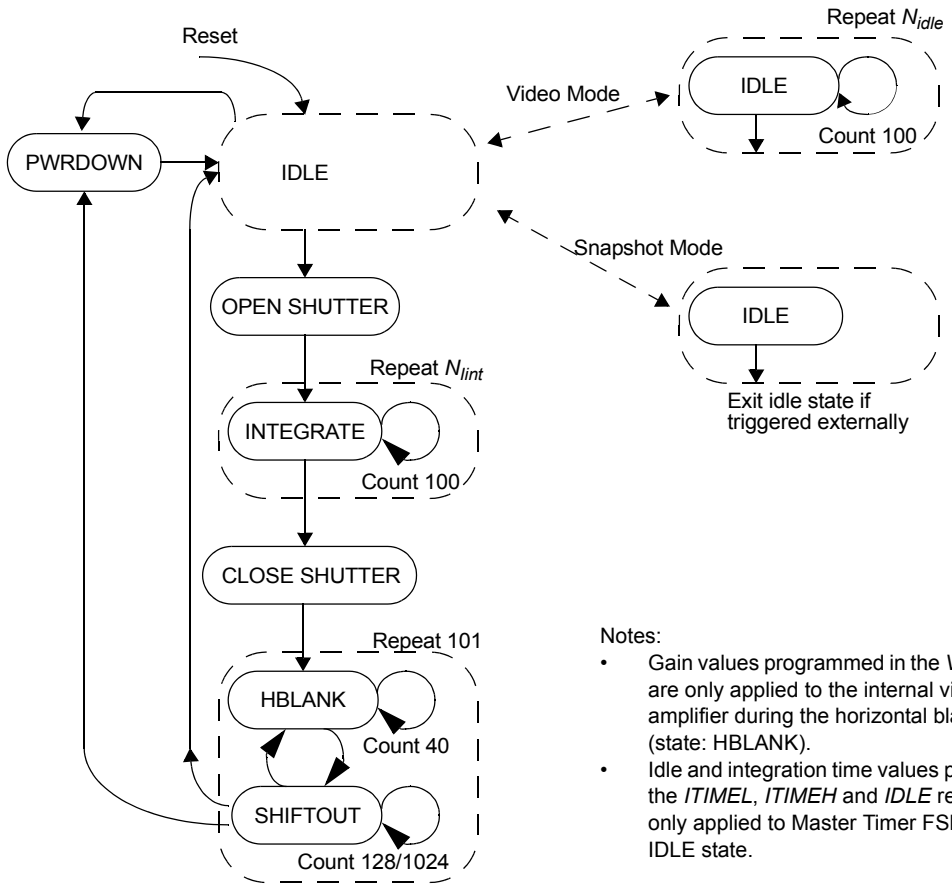


Figure 12: Master Timer FSM

Notes:

- Gain values programmed in the *VGAIN* register are only applied to the internal video gain amplifier during the horizontal blanking period (state: HBLANK).
- Idle and integration time values programmed in the *ITIMEL*, *ITIMEH* and *IDLE* registers are only applied to Master Timer FSM during the IDLE state.

I²C Compatible Serial Interface

The serial bus interface consists of the *sda* (serial data) and the *sclk* (serial clock). The KAC-9630 can operate only as a slave.

The *sclk* pin is an input only and clocks the serial interface data *sclk*. It is synchronised to *mclk*. A clock must be running at the *mclk* pin in order to communicate with the serial control port. Note *mclk* must be at least 10X *sclk*.

It is possible to communicate with the sensor via this port when in power down mode.

General Definitions

Start/Stop Conditions

The serial bus will recognize a logic 1 to logic 0 transition on the *sda* pin while the *sclk* pin is at logic 1 as the ***start*** condition. A logic 0 to logic 1 transition on the *sda* pin, while the *sclk* pin is at logic 1, is interrupted as the ***stop*** condition as shown in figure 13.

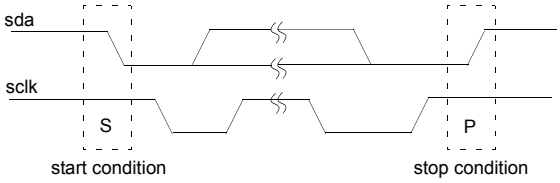


Figure 13: Start/Stop Conditions

Device Address

The serial bus *Device Address* of the KAC-9630 is set to 1000100.

Acknowledgment

The KAC-9630 will hold the value of the *sda* pin to a logic 0 during the logic 1 state of the *Acknowledge* clock pulse on *sclk* as shown in figure 14.

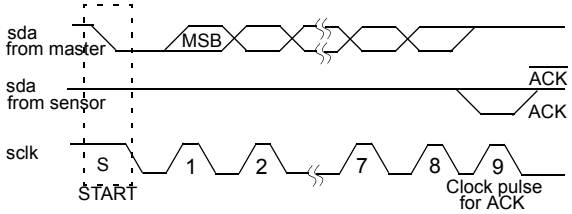


Figure 14: Acknowledge

Data Valid

The master must ensure that data is stable during the logic 1 state of the *sclk* pin. All transitions on the *sda* pin can only occur when the logic level on the sclk pin is “0” as shown in figure 15.

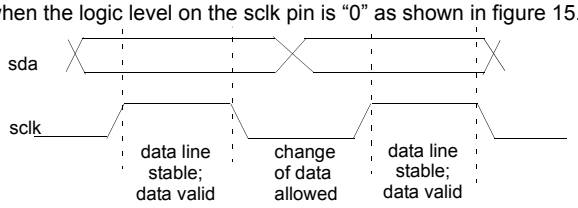


Figure 15: Data Validity

Byte Format

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an *Acknowledge* except for the last byte. The most significant bit of the byte is should always be transmitted first. See figure 16.

Write Operation

A write operation is initiated by the master with a *Start Condition* followed by the sensor’s *Device Address* and *Write* bit. After the master receives an *Acknowledge* from the sensor it must transmit 8 bit internal register address. The sensor will respond with a second *Acknowledge* signaling the master to start transmitting data bytes. Each byte successfully received will be acknowledged by the sensor with an *Acknowledge*.

The write operation is completed when the master asserts a *Stop Condition* or a repeated *Start Condition*. See figure 17.

Read Operation

A read operation is initiated by the master with a *Start Condition* followed by the sensor’s *Device Address* and *Write* bit. After the master receives an *Acknowledge* from the sensor it must transmit the internal *Register Address* byte. The sensor will respond with a second *Acknowledge*. The master must then issue a repeated *Start Condition* followed by the sensor’s *Device Address* and *read* bit. The sensor will respond with an *Acknowledge* followed by the first *Read Data* byte. Each read data byte must be acknowledged by the master.

The read operation is finished when the master asserts a *Not Acknowledge* (instead of an *Acknowledge*) followed by *Stop Condition* or a repeated *Start Condition*.See figure 18.

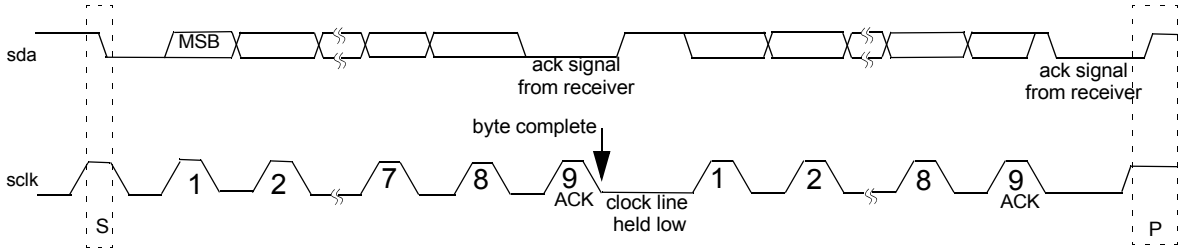
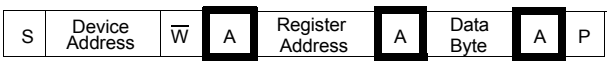


Figure 16: Serial Bus Byte Format



bold **sensor action**

Figure 17: Serial Bus Write Byte Operation

bold **sensor action**

Figure 18: Serial Bus Read Byte Operation

Parallel Digital Image Data Port

By default the captured image is placed onto an 10-bit digital image data port as shown in figure 19. The digital image data port consists of an 8-bit digital data out bus (*d[7:0]*) and two synchronisation signals (*hsync & vsync)*.

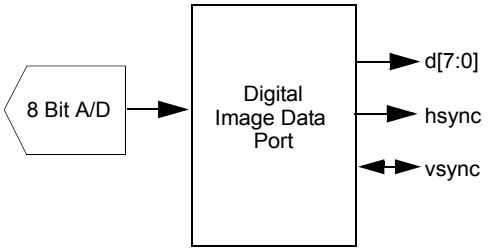


Figure 19: Digital Video Port

The following sections provide a detailed description of the timing of the digital image data port.

Digital Image Data Out Bus (d[7:0])

Pixel data is output on an 8-bit digital video bus and is synchronized to the positive edge of *mclk*.

Synchronisation Signals

Two synchronisation outputs are provided:

hsync is the horizontal synchronisation output signal.
vsync is the vertical synchronisation output signal in video mode and the external frame trigger input in snapshot mode.

Horizontal Synchronisation Output Pin (hsync)

The horizontal synchronisation output pin, *hsync*, is used as an indicator for row data.

The *hsync* output pin will go high at the start of each row and remain at that level until the last pixel of that row is read out on *d[7:0]* as shown in figure 20.

The *hsync* signal is synchronized to the positive edge of *mclk*.

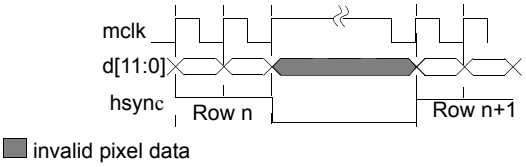


Figure 20: *hsync* Timing

Vertical Synchronisation Pin in Video Mode (vsync)

The vertical synchronisation pin, *vsync,* in video mode is an output and is used as an indicator for pixel data within a frame.

*T*he *vsync* pin will go high at the start of each frame and remain at that level until the last pixel of that row in the frame is placed on *d[7:0]* as shown in figure 21.

The *vsync* signal is synchronized to the positive edge of *mclk*.

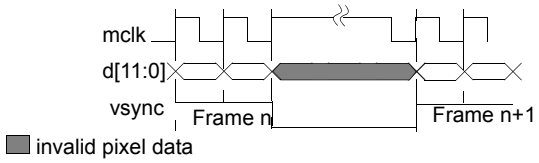


Figure 21: vsync Timing in Video Mode.

Vertical Synchronisation Pin in Snapshot Mode (vsync)

The vertical synchronisation pin, *vsync,* in snapshot mode is an input and is used as an external trigger to start the capture of a single frame.

The *vsync* pin must be forced high for at least two "*mclk*" cycles during the idle state of the sensor to trigger a single frame as shown in figure 23.

The sensor can only be externally triggered when it is in the idle state.

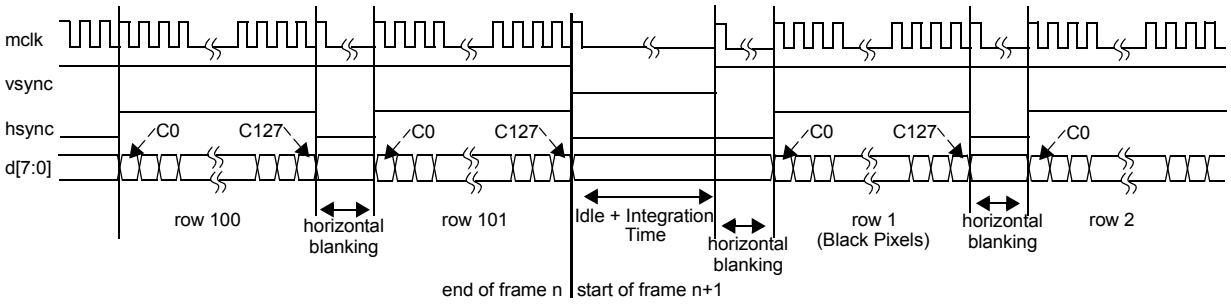


Figure 22: Parallel Digital Image Data Port Timing Diagram In Video Mode

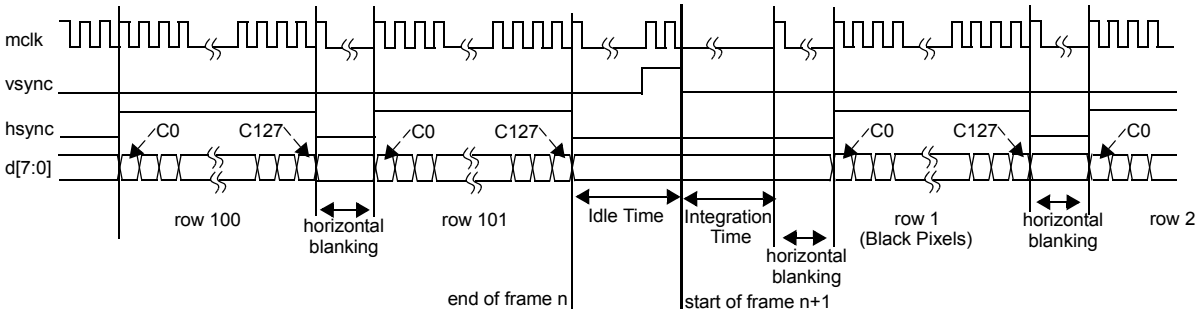


Figure 23: Parallel Digital Image Data Port Timing Diagram in Snapshot Mode

Serial Digital Image Data Port

The sensor can be programmed so that the captured image is placed onto a 4 bit serial digital image data port as shown in figure 24. The serial digital image data port consists of a single data out pin (*d[0]*) and three synchronisation signals (*d[1]*, *hsync & vsync)*.

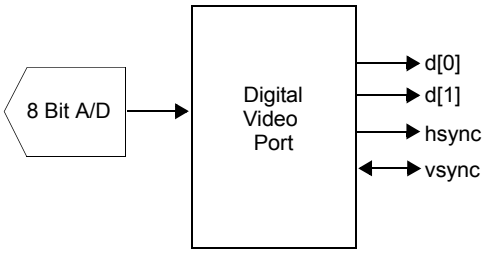


Figure 24: Serial Digital Image Data Port

When the sensor is programmed to work in this mode, all optical and analog specifications will not be guaranteed. Pins d[2:7] will be tri-stated.

The following sections provide a detailed description of the timing of the serial digital image data port.

Digital image data Data Out (d[0])

Pixel data is output on a single digital image data pin, d[0] and is synchronized to the positive edge of *mclk*. The MSB of every pixel byte will be transmitted first.

Synchronisation Signals

The integrated timing and control block controls the flow of data onto the 8-bit digital port, three synchronisation outputs are provided:

d[1]	is the bit synchronisation signal and will go high for one clock cycle indicating the first bit (MSB) of every pixel.
hsync	is the horizontal synchronisation output signal.
vsync	is the vertical synchronisation output signal in video mode and the external frame trigger input in snapshot mode.

Bit Synchronisation Output Pin (d[1]

The bit synchronisation output pin, *d[1]*, is used as an indicator for pixel data.

The *d[1]* output is synchronized to the positive edge of *mclk* and will go high at the start of each pixel byte and remain high for one *mclk* clock cycle as shown in figure 25.

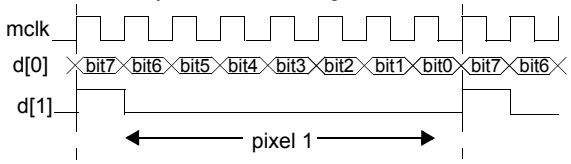


Figure 25: d[1] timing diagram

Horizontal Synchronisation Output Pin (hsync)

The horizontal synchronisation output pin, *hsync*, is used as an indicator for row data.

The *hsync* output pin is synchronized to the positive edge of *mclk* and will go high at the start of each row and remain at that level until the last pixel of that row is read out on *d[0]* as shown in figure 20.

Vertical Synchronisation Pin in Video Mode (vsync)

The vertical synchronisation pin, *vsync,* in video mode is an output and is used as an indicator for pixel data within a frame.

The *vsync* pin is synchronized to the positive edge of *mclk* and will go high at the start of each frame and remain at that level until the last pixel of that row in the frame is placed on *d[0]* as shown in figure 21.

Vertical Synchronisation Pin in Snapshot Mode (vsync)

The vertical synchronisation pin, *vsync,* in snapshot mode is an input and is used as an external trigger to start the capture of a single frame.

The *vsync* pin must be forced high for at least two "*mclk*" cycles during the idle state of the sensor to trigger a single frame as shown in figure 23. The sensor can only be externally triggered when it is in the idle state.

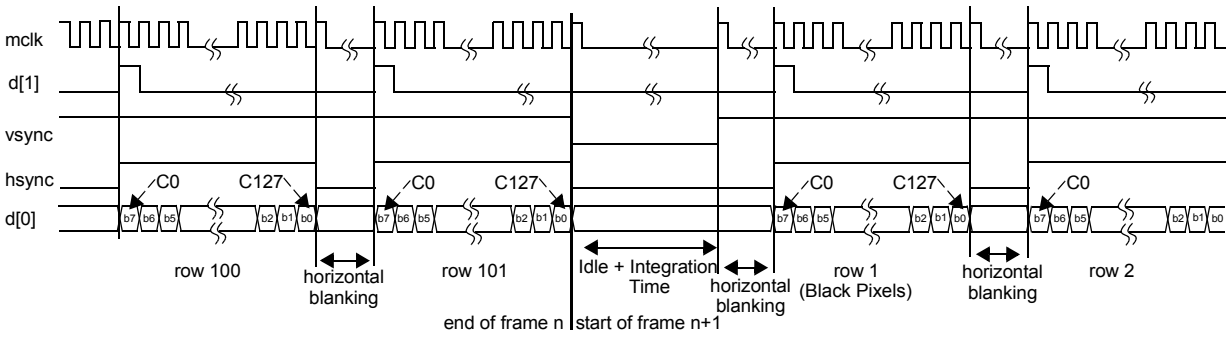


Figure 26: Serial Digital Image Data Port Timing Diagram In Video Mode

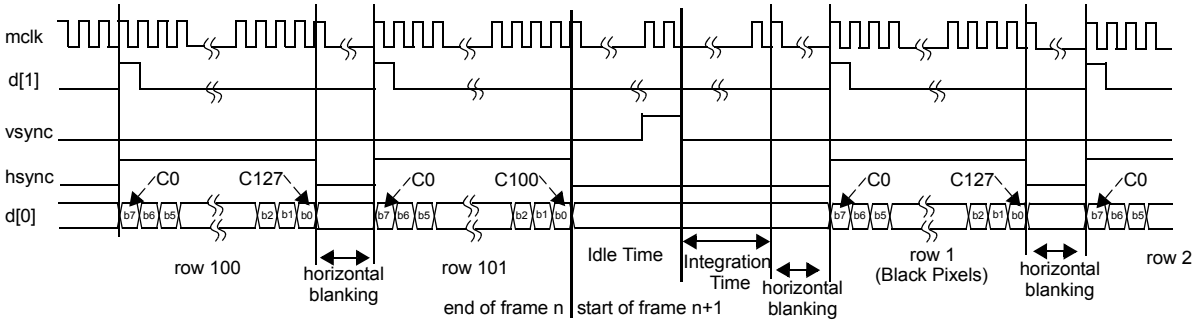


Figure 27: Serial Digital Image Data Port Timing in Snapshot Mode

MEMORY MAP

ADDR	Register	Reset Value	Description
00h	REV	00h	Silicon Revision & Bank Enable Register
01h	MCFG	00h	Main Configuration Register.
02h	VGAIN	00h	Video Gain Register
03h	ITIMEL	0Ah	Integration Time Low Register
04h	IDLE	00h	Idle Time Register
05h	ITIMEH	00h	Integration Time High Register
06h	POWSET		Power Setting Register
07h			Reserved
08h	OFFSET	00h	Offset Adjustment Register

Register Set

The following section describes all available registers in the KAC-9630 register bank and their function.

Register Name **Silicon Rev & Bank Enable Register**
Mnemonic **REV**
Address **00 Hex**
Type **Read/Write.**

Bit	Bit Symbol	Description
7	OffsetBnkEn	Assert to switch on the offset adjustment bank. Note that the *OffsetDacEn* bit must also be enabled. This bit also enables the user to access the POWSET register. (Default setting is logic 0)
6:3		Reserved
4:0	SiRev	Read only bits The silicon revision register.

Main Configuration

Register Name **Main Configuration 0**
Address **01 Hex**
Mnemonic **MCFG**
Type: **Read/Write**
Reset Value **01 Hex**

Bit	Bit Symbol	Description
7		Reserved
6	DVBmode	Assert to configure the digital image data port to operate in serial mode. Clear (the default) to configure the digital image data port to operate in parallel mode. Note: When this bit is set, pins d[2:7] are tri-stated.
5	PwrDown	Assert to power down the sensor. Clear (the default) this bit to power up the sensor.
4	PwdAmp	Assert to power down the programmable video gain amplifier. Clear (the default) to power up the video gain amplifier.
3	ByPassAmp	Assert to route the analog video signal from the output of the pixel core to the input of the 8 bit A/D. Clear (the default) to route the signal to the video gain amplifier.
2	Res	Assert to activate a system reset. The integrated timing and control circuit will automatically clear this bit. (Default setting is logic 0).
1	TriDVP	Assert to tristate the *digital video port*, clear (the default) enable *sdo*.
0	Mode	Asset (the default) to operate the sensor in snapshot mode, clear to operate the sensor in video mode.

Register Set (continued)

Video Gain Programming Register

Register Name **Video Gain Register**
Address **02 Hex**
Mnemonic **VGAIN**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7		Reserved
6	Offset-DacEn	Assert to switch on the offset adjustment bank. Note that the *OffsetBnkEn* bit must also be enabled. (Default setting is logic 0)
5		Reserved
4:0	VidGain	Use to program the overall video gain.

Integration Time Programming Registers

Register Name **Integration Time Low Register**
Address **03 Hex**
Mnemonic **ITIMEL**
Type **Read/Write**
Reset Value **0A Hex.**

Bit	Bit Symbol	Description
7:0	Nint[7:0]	Program to set the integration time of the array.

Idle Time Programming Register

Register Name **Integration Time High Register**
Address **04 Hex**
Mnemonic **IDLE**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:0	Nidle[7:0]	Program to set the idle time of the array. The minimum value that can be programmed in this register is 01 hex.

Register Name **Integration Time High Register**
Address **05 Hex**
Mnemonic **ITIMEH**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:6		Reserved
5:3	Nidle[10:8]	Program to set the idle time of the array.
2:0	Nint[10:8]	Program to set the integration time of the array.

Register Name **Power Setting Register**
Address **06 Hex**
Mnemonic **POWSET**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:4	SetPower	Program to increase or decrease the sensor's bias currents from the default as follows SetPower / Power 1111 / +6.7mA 0000 / 0 mA 1110 / - 6.7mA This should be programed once after system reset. Note that the OffsetBnkEn must be set to enable this register.
3:0		Reserved

Offset Adjustment Register

Register Name **Offset Adjustment Register**
Address **08 Hex**
Mnemonic **OFFSET**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7	OffSign	Sign of the offset adjust value. When set to a logic 1, OffValue will be positive. When set to a logic 0 OffValue will be negative. note both *OffsetBnk* and *Offset-DacEn* bits must be set to 1 before this register can be used.
6		Reserved
5:0	OffValue	Offset adjustment value. A positive offset is added when OffSign is set to a logic 1. A negative offset is added when OffSign is set to a logic 0. note both *OffsetBnk* and *Offset-DacEn* bits must be set to 1 before this register can be used.

Digital Image Data Port Timing

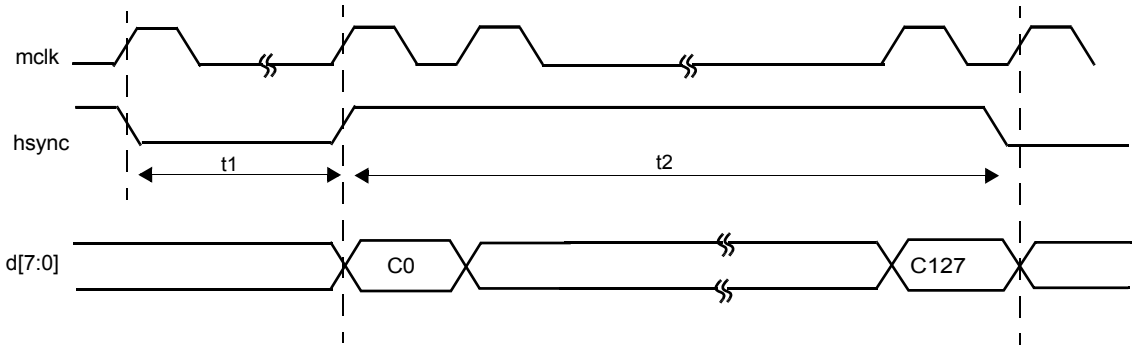


Figure 28: Row Timing Diagram

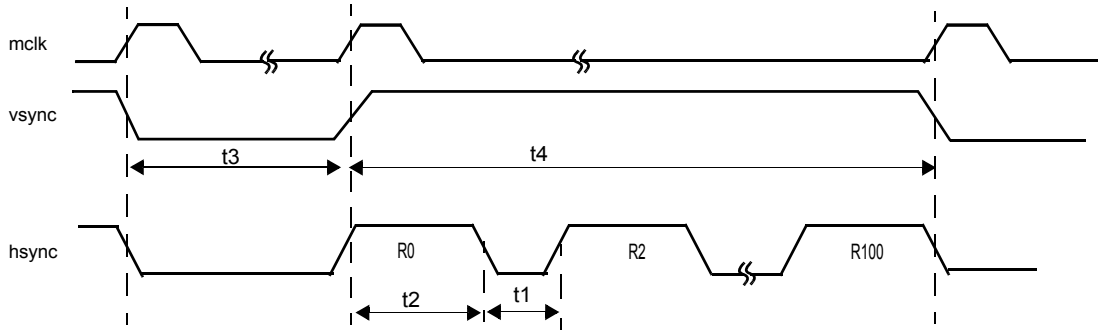


Figure 29: Frame Timing Diagram

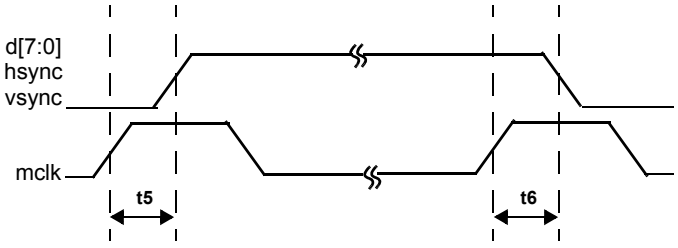
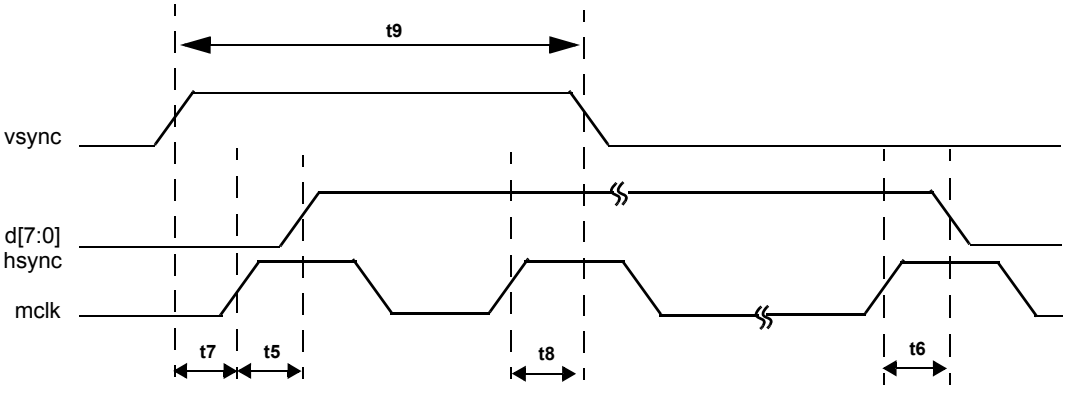


Figure 30: *d[7:0]*, *hsync* & *vsync* to active high *mclk* timing in video mode.



only valid when sensor is in idle state

Figure 31: d[7:0], hsync & vsync to active high mclk timing in snapshot mode

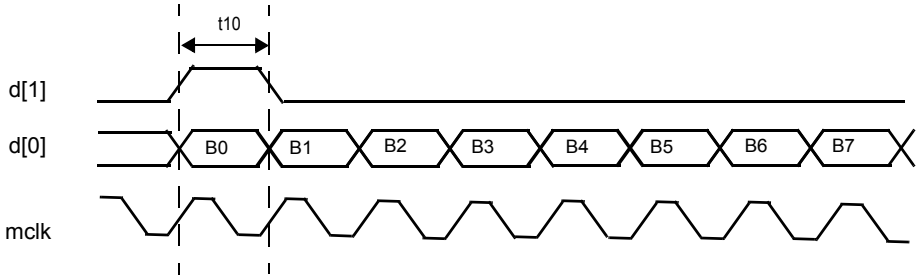


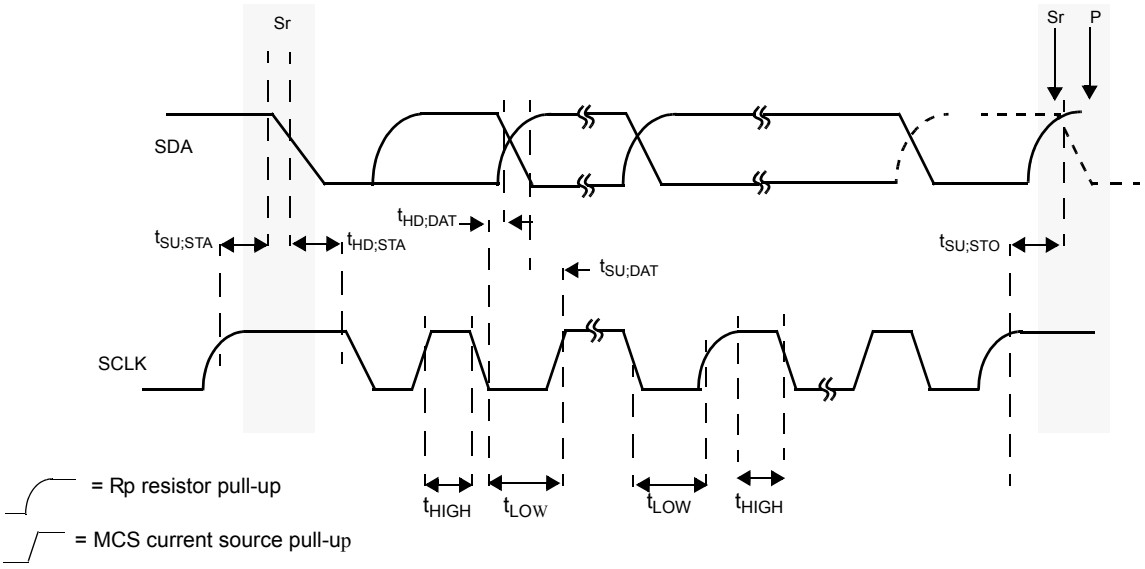
Figure 33: d[1] Timing for Serial Digital Image Data Port.

Label	Descriptions	Value
t1	Horizontal Blanking Time	40 * *mclk*
t2	Time to read out a single row	128 * *mclk* in parallel mode 1024 * *mclk* in serial mode
t3	Idle Time (T_{idle})	see T_{idle} in the Frame Rate Programming section.
t4	Time to read out a single frame	T_{idle} + $T_{integration}$ + $T_{readout}$ See the Frame Rate Programming section.
t9	Minimum *vsync* pulse width	2 * *mclk*
t10	d[1] pulse for the serial digital image data port	1 * *mclk*

The following specifications apply for all supply pins = +3.3V and C_L = 10pF unless otherwise noted. Boldface limits apply for TA = T_{MIN} to T_{MAX}: all other limits T_A = 25°C (Note 7)

Label	Descriptions	Min	Typ	Max
t5	Time from rising edge of *mclk* to rising edge of *vsync*, *hsync* or *d[7:0]*	10ns		25ns
t6	Time from rising edge of *mclk* to falling edge of *vsync*, *hsync* or *d[7:0]*	10ns		25ns
t7	Set up time from rising edge of *vsync* to rising edge of *mclk*.	0ns		
t8	Hold time from rising edge of *mclk* to falling edge of *vsync*.	7ns		

Serial Interface Timing



(1) Rising edge of the first SCLK pulse after an acknowledge bit.

Figure 34: I²C compatible serial bus timing.

The following specifications apply for all supply pins = +3.3V, C_L = 10pF, and *sclk* = 400KHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

PARAMETER	SYMBOL	MIN	MAX	UNIT
sclk clock frequency	f_{SCLH}	0	400	KHz
Set-up time (repeated) START condition	$t_{SU;STA}$	0.6	-	µS
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	-	µS
LOW period of the *sclk* clock	t_{LOW}	1.3	-	µS
HIGH period of the *sclk* clock	t_{HIGH}	0.6	-	µS
Data set-up time	$t_{SU;DAT}$	100	-	nS
Data hold time	$t_{HD;DAT}$	0	0.9	µS
Set-up time for STOP condition	$t_{SU;STO}$	0.6		µS
Capacitive load for *sda* and *sclk* lines	C_b		400	pF

Test Circuitry

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND = 0V, unless otherwise specified.

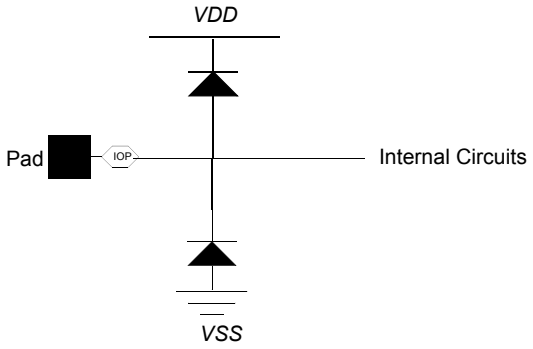
Note 3: When the voltage at any pin exceeds the power supplies (VIN < GND or VIN > vdd_ana or vdd_od), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA to two.

Note 4: The absolute maximum junction temperature (TJmax) for this device is 125^{o}C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (Θ_{JA}), and the ambient temperature (TA), and can be calculated using the formula PDMAX = (TJmax - TA)/Θ_{JA}. In the 32-pin LCC, Θ_{JA} is 41.6^{o}C/W, so PDMAX = 2.4W at 25^{o}C and 1.8W at the maximum operating ambient temperature of 50^{o}C. Note that the power dissipation of this device under normal operation will typically be about 130 mW. The values for maximum power dissipation listed above will be reached only when the KAC-9630 is operated in a severe fault condition.

Note 5: Human body model is 100pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220pF discharged through ZERO Ohms.

Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The analog inputs are protected as shown below. Input voltage magnitude up to 500mV beyond the supply rails will not damage this device. However, input errors will be generated If the input goes above vdd_ana and below AGND.

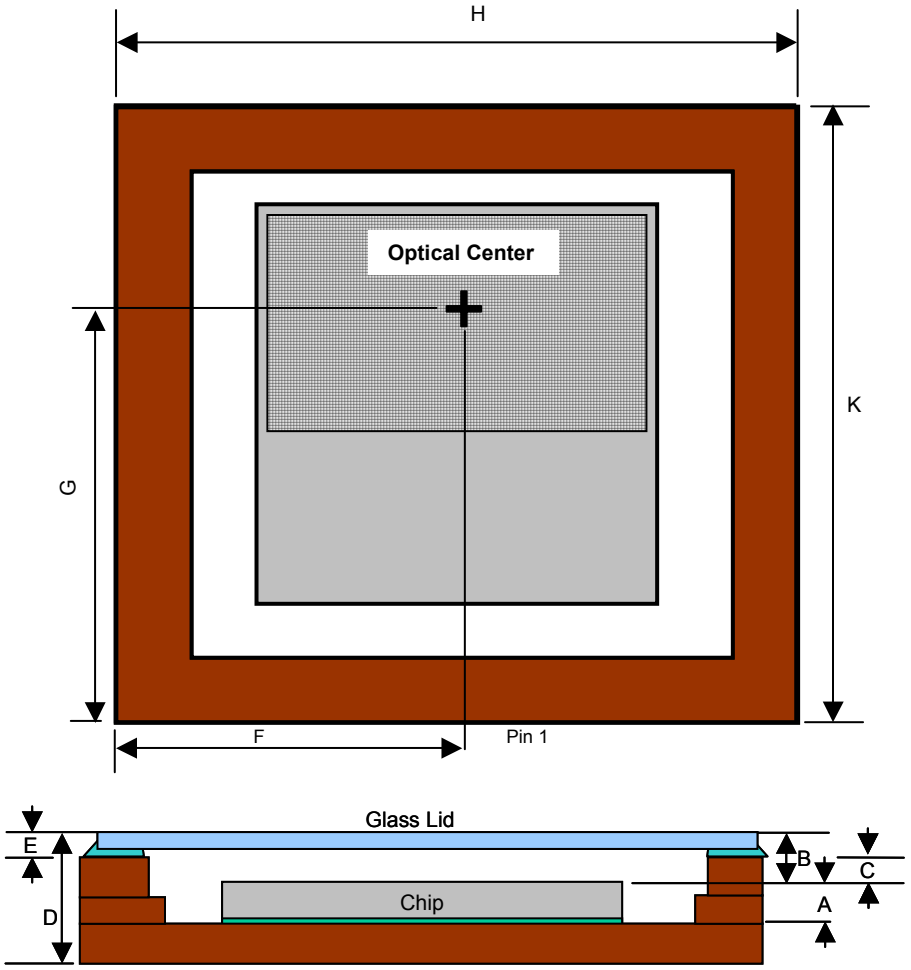


Note 8: Typical figures are at TJ = 25^{o}C, and represent most likely parametric norms

Note 9: Test limits are guaranteed to AOQL (Average Outgoing Quality Level).

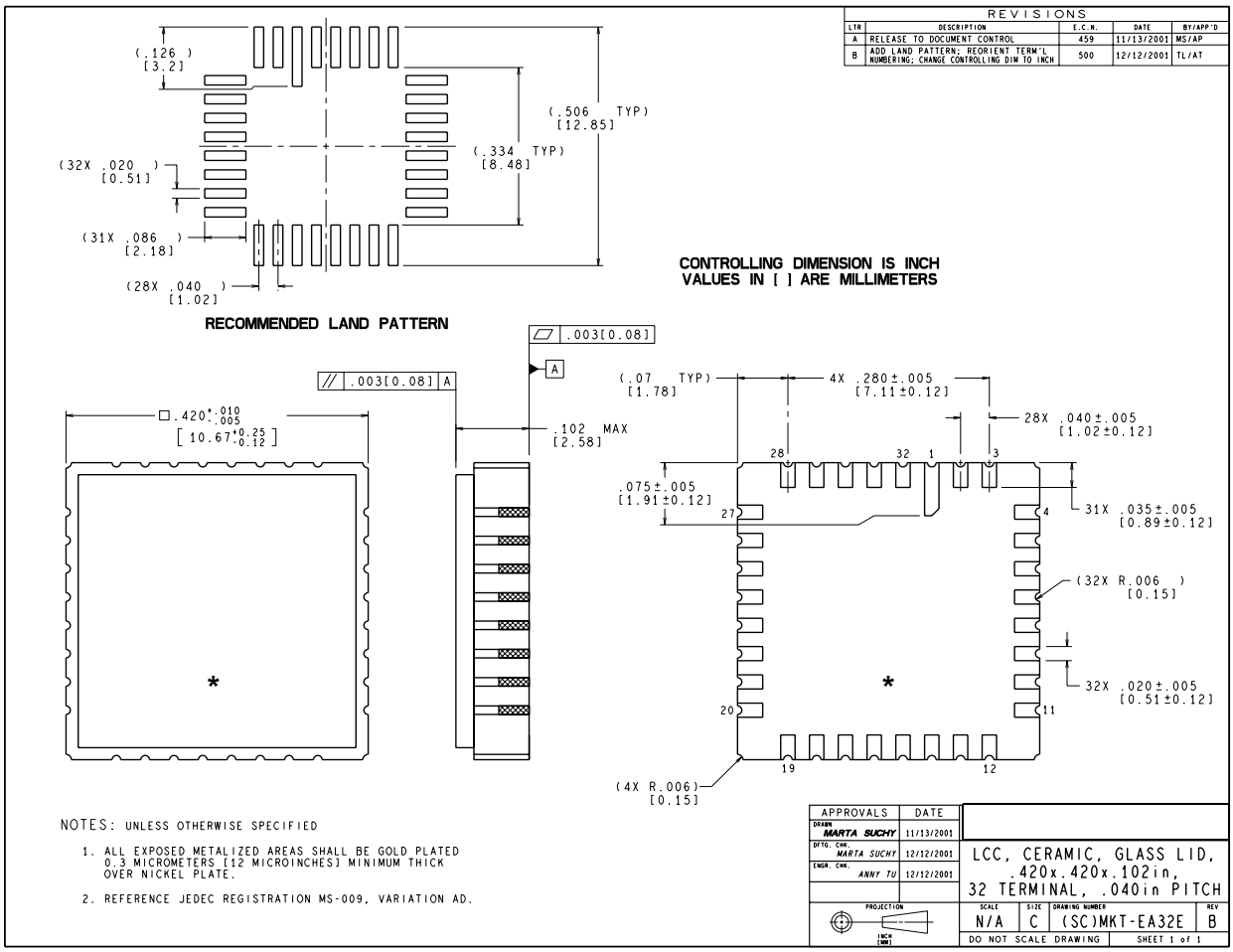
Note 10: The dew point temperature (the temperature below which there is a possibility of moisture condensation forming inside the package) of the package is rated at -10^{o}C. Suitable precautions should be taken to avoid dew formation when operating the sensor between -40^{o}C and -10^{0}C.

Mechanical Information



Dimension	Description	min (mm)	typ (mm)	max (mm)
A	Distance from top of die to bottom of cavity	0.788	0.820	0.852
B	Top of die to top of glass lid	0.690	0.970	1.250
C	Top of package to top of glass lid	0.250	0.420	0.590
D	Max total thickness of die	N/A	N/A	2.580
E	Thickness of lid	0.530	0.640	0.750
F	X-Coordinate of optical center (nom)	N/A	5.302	N/A
G	Y-Coordinate of optical center (nom)	N/A	6.070	N/A
H	X-Dimension of Package	10.540	10.670	10.970
K	Y-Dimension of Package	10.540	10.670	10.970

Package Information



* For Optical Center information see Mechanical Information on Page 20