DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAC-9628
CMOS IMAGE SENSOR

648 (H) X 488 (V)
High Dynamic Range 30 fps
Color CIS

January 2007
Revision 2.2

KAC-9628 Color High Dynamic Range CMOS Image Sensor VGA 30 FPS

General Description

The KAC-9628 is a high performance, low power, 1/3" VGA CMOS Active Pixel Sensor capable of capturing color digital still or motion images and converting them to a digital data stream.

In addition to the active pixel array, an on-chip 12 bit A/D convertor, fixed pattern noise elimination circuits, a video gain and separate color gain amplifier are provided. Furthermore, an integrated programmable smart timing and control circuit allows the user maximum flexibility in adjusting integration time, active window size, gain and frame rate. Various control, timing and power modes are also provided.

The excellent linear dynamic range of the sensor can be extended to above 100dB by programming a non linear response curve that matches the response of the human eye.

Features

- Video or snapshot operations
- Programmable pixel clock, inter-frame and inter-line delays.
- Programmable partial or full frame integration
- Programmable gain and individual color gain adjustment
- Horizontal & vertical sub-sampling (2:1 & 4:2)
- Programmable digital video response curve
- Windowing
- External snapshot trigger & event synchronisation signals
- Auto black level compensation
- Flexible digital video read-out supporting programmable:
  - polarity for synchronisation and pixel clock signals
  - leading edge adjustment for horizontal synchronization
- Programmable via 2 wire I^2C compatible serial interface
- Power on reset & power down mode

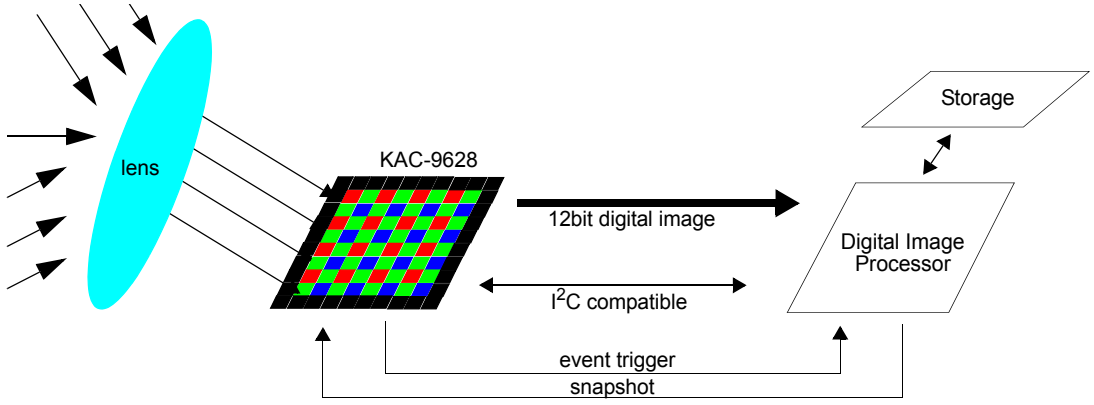
Applications

- Dual Mode Camera
- Digital Still Camera
- Security Cameras
- Machine Vision
- Automotive

Key Specifications

Array Format	Total: 664H x 504V Active: 648H x 488V
Effective Image Area	Total: 4.98mm x 3.78 mm Active: 4.86 mm x 3.66 mm
Optical Format	1/3"
Pixel Size	7.5µm x 7.5µm
Video Outputs	8,10 & 12 Bit Digital
Frame Rate	30 frames per second
Dynamic Range	62dB in linear mode 110dB in non linear mode
Electronic Shutter	Rolling reset
FPN	0.1%
PRNU	1.5%
Sensitivity	2.7 V/lux.s
Quantum Efficiency	27%
Fill Factor	47%
Color Mosaic	Bayer pattern
Package	48 CLCC
Single Supply	3.3 V +/-10%
Power Consumption	168 mW
Operating Temp	-40 to 85°C

System Block Diagram



Overall Chip Block Diagram

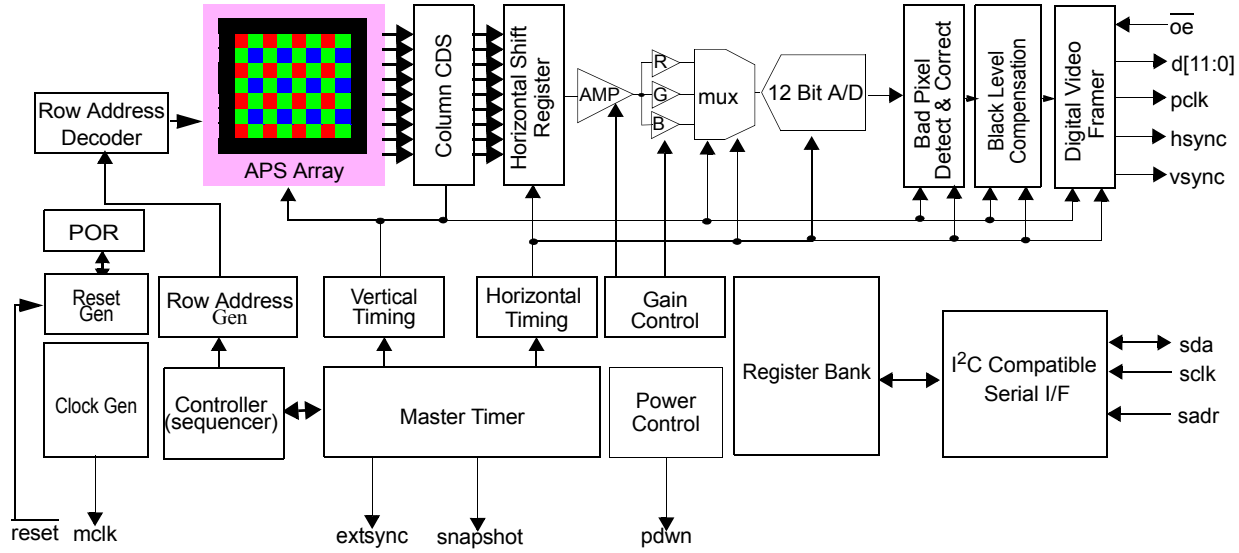
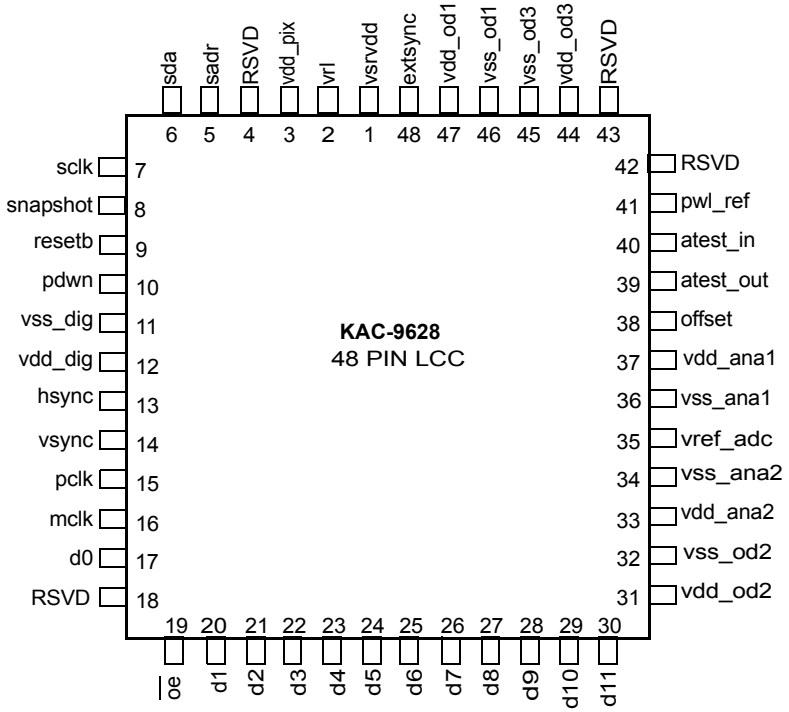


Figure 1. Chip Block Diagram

Connection Diagram



Ordering Information

Catalog Number	Product Name	Description
4H0716	KAC-9628-CBA-FB-AA	Standard Grade in Tray

Typical Application Circuit

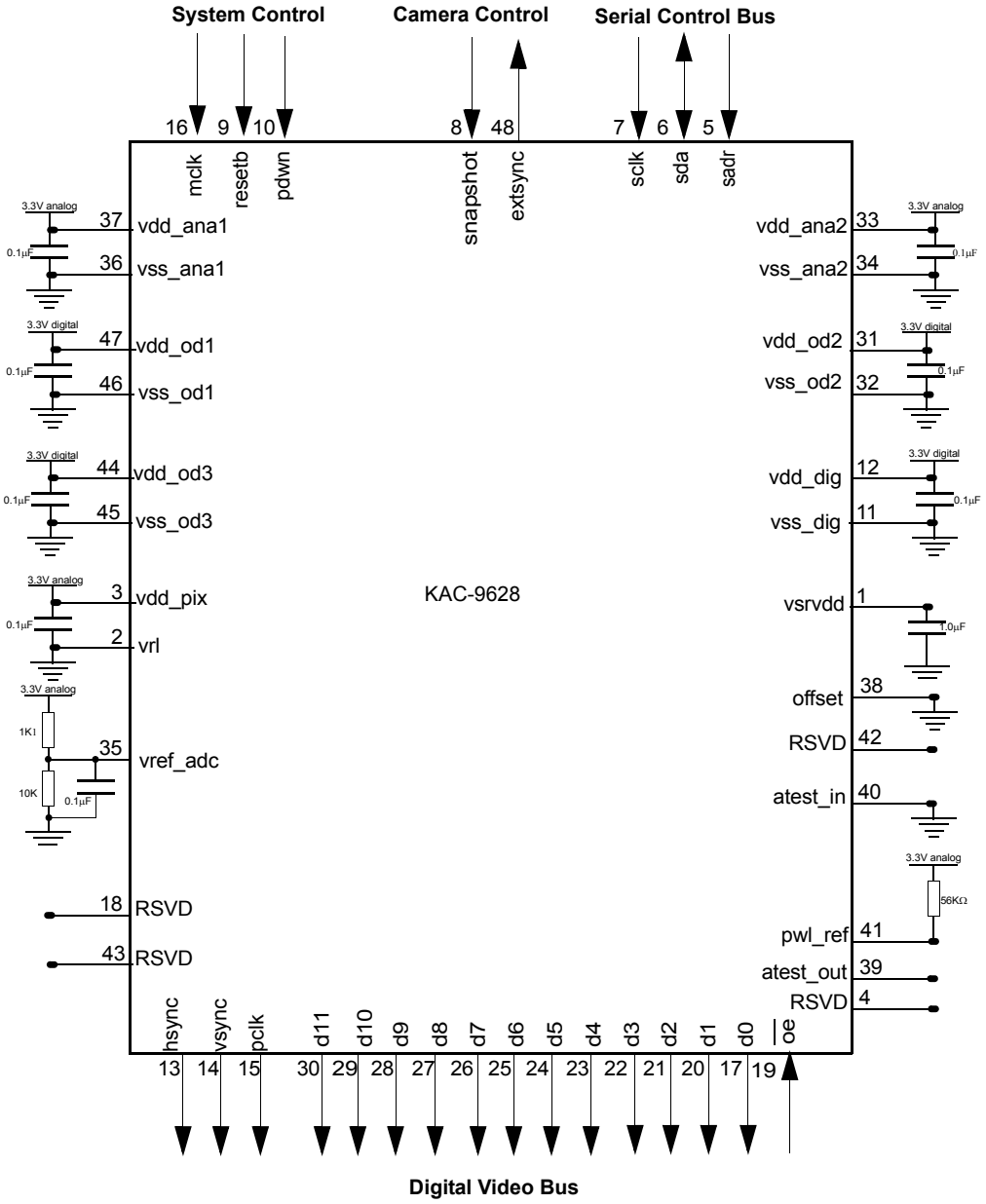


Figure 2. Typical Application Diagram

Scan Read Out Direction

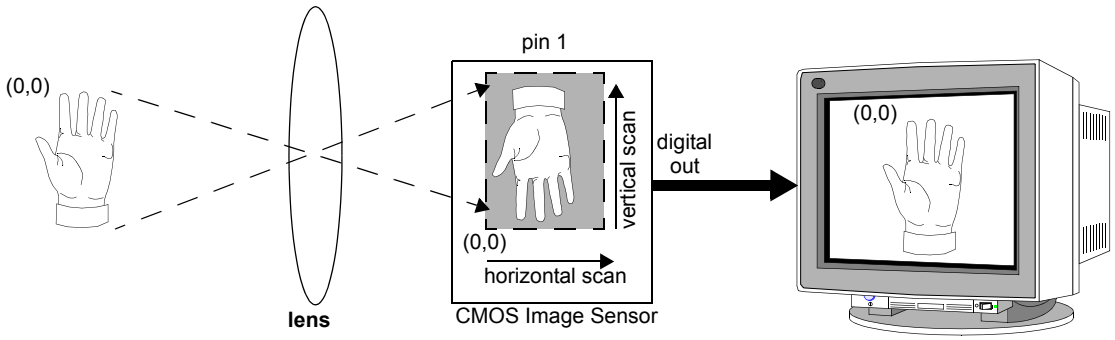


Figure 3. Scan directions and position of origin in imaging system

Pin Descriptions

Pin	Name	I/O	Typ	Description
1	vsrvdd	0	P	Charge pump output, connect to ground via a1.0μf capacitor.
2	vrl	I	A	Anti blooming pin. This pin is normally tied to ground.
3	vdd_pix	I	P	3.3 volt supply for the pixel array.
4	RSVD			This pin is reserved for future use, do not connect.
5	sadr	I	D	Digital input with pull down resistor. This pin is used to program different slave addresses for the sensor in an I^2C compatible system.
6	sda	IO	D	I^2C compatible serial interface data bus. The output stage of this pin has an open drain driver.
7	sclk	I	D	I^2C compatible serial interface clock.
8	snapshot	I	D	Digital input with pull down resistor used to activate (trigger) a snapshot sequence.
9	resetb	I	D	Digital input with pull up resistor. When forced to a logic 0 the sensor is reset to its default power up state. The *resetb* signal is internally synchronized to *mclk* which must be running for a reset to occur.
10	pdwn	I	D	Digital input with pull down resistor. When forced to a logic 1 the sensor is put into power down mode.
11	vss_dig	I	P	0 volt power supply for the digital circuits.
12	vdd_dig	I	P	3.3 volt power supply for the digital circuits.
13	hsync	IO	D	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, (the default), this pin is an output and is the horizontal synchronization pulse. When the sensor's digital video port is configured to be a slave, this pin is an input and is the row trigger.
14	vsync	IO	D	Digital Bidirectional. This is a dual mode pin. When the sensor's digital video port is configured to be a master, (the default), this pin is an output and is the vertical synchronization pulse. When the sensor's digital video port is configured to be a slave, this pin is an input and is the frame trigger.
15	pclk	IO	D	Digital output. The pixel clock.
16	mclk	I	D	Digital input. The sensor's master clock input.
17	d0	O	D	Digital output. Bit 0 of 11 of the digital video output bus. This output can be put into tri-state mode.
18	RSVD			This pin is reserved for future use, do not connect.
19	$\overline{oe}$	I	D	Digital input with pull down resistor. When forced to a logic 1 the sensor's digital video port d[11:0], vsync & hsync will be tri-stated.
20	d1	O	D	Digital output. Bit 1 of 11 of the digital video output bus. This output can be put into tri-state mode.
21	d2	O	D	Digital output. Bit 2 of 11 of the digital video output bus. This output can be put into tri-state mode.
22	d3	O	D	Digital output. Bit 3 of 11 of the digital video output bus. This output can be put into tri-state mode.
23	d4	O	D	Digital output. Bit 4 of 11 of the digital video output bus. This output can be put into tri-state mode.

Pin Descriptions (Continued)

Pin	Name	I/O	Typ	Description
24	d5	O	D	Digital output. Bit 5 of 11 of the digital video output bus. This output can be put into tri-state mode.
25	d6	O	D	Digital output. Bit 6 of 11 of the digital video output bus. This output can be put into tri-state mode.
26	d7	O	D	Digital output. Bit 7 of 11 of the digital video output bus. This output can be put into tri-state mode.
27	d8	O	D	Digital output. Bit 8 of 11 of the digital video output bus. This output can be put into tri-state mode.
28	d9	O	D	Digital output. Bit 9 of 11 of the digital video output bus. This output can be put into tri-state mode.
29	d10	O	D	Digital output. Bit 10 of 11 of the digital video output bus. This output can be put into tri-state mode.
30	d11	O	D	Digital output. Bit 11 of 11 of the digital video output bus. This output can be put into tri-state mode.
31	vdd_od2	I	P	3.3 volt supply for the digital IO buffers.
32	vss_od2	I	P	0 volt supply for the digital IO buffers
33	vdd_ana2	I	P	3.3 volt supply for analog circuits.
34	vss_ana2	I	P	0 volt supply for analog circuits.
35	vref_adc	I	A	A/D reference resistor ladder high voltage. Internal resistor to gnd 530Ω resistor.
36	vss_ana1	I	P	0 volt supply for analog circuits.
37	vdd_ana1	I	P	3.3 volt supply for analog circuits.
38	offset	I	A	Analog input used to manually adjust the offset of the sensor. This pin should be tied to ground.
39	atest_out	A	O	Analog test output for factory use only. This pin should not be connected.
40	atest_in	A	I	Analog test input for factory use only. This pin should be tied to ground.
41	pwl_ref	A	I	Analog input used to control the position of the piecewise linear breakpoints. This pin should be connected to vdd_ana1 via a 56KΩ resistor.
42	RSVD			This pin is reserved for future use, do not connect.
43	RSVD			This pin is reserved for future use, do not connect.
44	vdd_od3	I	P	3.3 volt supply for the sensor.
45	vss_od3	I	P	0 volt supply for the sensor.
46	vss_od1	I	P	0 volt supply for the digital IO buffers
47	vdd_od1	I	P	3.3 volt supply for the digital IO buffers.
48	extsync	O	D	Digital output. The external event synchronization signal is used to synchronize external events in snapshot mode.

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog).

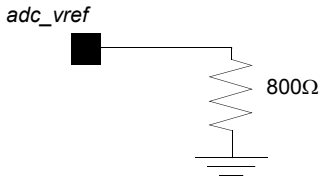


Figure 4. Equivalent Circuits For *adc_ref* pin

Absolute Maximum Ratings (Notes 1 & 2)

Any Positive Supply Voltage	6.5V
Voltage On Any Input or Output Pin	-0.5V to 6.5V
Input Current at any pin (Note 3)	±25mA
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Machine Model	200V
Package Input Current (Note 3)	±50mA
Package Power Dissipation @ T_A(Note 4)	2.5W
Soldering Temperature Infrared, 10 seconds (Note 6)	220°C
Storage Temperature	-40°C to 125°C

Operating Ratings (Notes 1 & 2)

Operating Temperature Range (Note 10)	-40°C≤T≤+85°C
All VDD Supply Voltages	+3.0V to +3.6V
Voltage on *vref_adc* pin	+1.1V

DC and logic level specifications

The following specifications apply for all VDD pins= +3.3V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
sclk, sda, sadr, Digital Input/Output Characteristics (Note: sadr has a pulldown resistor)						
VIH	Logical “1” Input Voltage		0.7*vdd_od		vdd_od+0.5	V
VIL	Logical “0” Input Voltage		-0.5		0.3*vdd_od	V
VOL	Logical “0” Output Voltage	vdd_od = +3.15V, Iout=3.0mA			0.5	V
V_{hys}	Hysteresis *(SCLK pin only)*	vdd_od = +3.15V	0.05*vdd_od			V
I_{leak}	Input Leakage Current (without pulldown resistor)	Vin=vss_od		-1		µA
mclk, snapshot, pdwn, reset, hsync, vsync, oe Digital Input Characteristics (Note: snapshot, pdwn, oe have pulldown resistors and reset has a pullup resistor)						
VIH	Logical “1” Input Voltage	vdd_dig = +3.6V	2.0			V
VIL	Logical “0” Input Voltage	vdd_dig = +3.15V			0.8	V
IIH	Logical “1” Input Current (without pulldown resistor)	VIH = vdd_dig		0.1		µA
IIL	Logical “0” Input Current (without pullup resistor)	VIL = vss_dig		-1		µA
d0 - d11, pclk, hsync, vsync, extsync, Digital Output Characteristics						
VOH	Logical “1” Output Voltage	vdd_od=3.15V, Iout=-1.6mA	2.2			V
VOL	Logical “0” Output Voltage	vdd_od=3.15V, Iout =-1.6mA			0.5	V
IOZ	TRI-STATE Output Current	VOUT = vss_od VOUT = vdd_od		-0.1 0.1		µA µA
IOS	Output Short Circuit Current			+/-17		mA
Power Supply Characteristics						
IA	Analog Supply Current	Power down mode, no clock. Operational mode in dark		0.45 35.0		mA mA
ID	Digital Supply Current	Power down mode, no clock. Operational mode in dark		0.15 16.0		mA mA

Power Dissipation Specifications

The following specifications apply for All VDD pins = +3.3V, *mclk* = 48MHz, Hclk = 12MHz, frame rate = 30Hz, *vref* = 1.1 volt. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
P_{dwn}	Power Down	no clock running		1.98		mW
PWR	Average Power Dissipation	in dark		168		mW

Video Amplifier Specifications

The following specifications apply for all VDD pins= +3.3V. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
V_{gain}	Video Amplifier Nominal Gain	64 linear steps		0-15		dB
C_{gain}	Color Amplifiers Nominal Gain	128 linear steps	0	0-14		dB

AC Electrical Characteristics

The following specifications apply for All VDD pins = +3.3V. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C

Symbol	Parameter	Conditions	Min note 9	Typical note 8	Max note 9	Units
F_{mclk}	Input Clock Frequency		**12**		**48**	MHz
T_{ch}	Clock High Time	@ CLK_{max}	**10**		**45**	ns
T_{cl}	Clock Low Time	@ CLK_{max}	**10**		**45**	ns
	Clock Duty Cycle	@ CLK_{max}	**45/55**		**55/45**	min/max
T_{rc}, T_{fc}	Clock Input Rise and Fall Time					ns
F_{hclk}	Internal System Clock Frequency		**1.0**		**14.0**	MHz
T_{reset}	Reset pulse width		**1.0**			µs
FRM_{rate}	Frame Rate		**1**		**30**	fps

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to VSS = vss_ana = vss_od = vss_dig = 0V, unless otherwise specified.

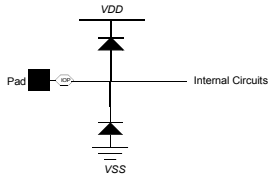
Note 3: When the voltage at any pin exceeds the power supplies (VIN < VSS or VIN > VDD), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25mA.

Note 4: The absolute maximum junction temperature (TJmax) for this device is 125°C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (ΘJA), and the ambient temperature (T_A), and can be calculated using the formula PDMAX = (TJmax - T_A)/ΘJA. In the 48-pin LCC, ΘJA is 38.5°C/W, so PDMAX = 2.5W at 25°C and 1.94W at the maximum operating ambient temperature of 50°C. Note that the power dissipation of this device under normal operation will be well under the PDMAX of the package.

Note 5: Human body model is 100pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220pF discharged through ZERO Ohms.

Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The analog inputs are protected as shown below. Input voltage magnitude up to 500mV beyond the supply rails will not damage this device. However, input errors will be generated If the input goes above AV+ and below AGND.



Note 8: Typical figures are at TJ = 25°C, and represent most likely parametric norms.

Note 9: Test limits are guaranteed to AOQL (Average Outgoing Quality Level).

Note 10: The dew point temperature (the temperature below which there is a possibility of moisture condensation forming inside the package) of the package is rated at -20°C. Suitable precautions should be taken to avoid dew formation when operating the sensor between -40°C and -20°C.

CMOS Active Pixel Array Specifications

Parameter	Value	Units
Number of pixels (row, column) Total Active	 664 x 504 648 x 488	 pixels pixels
Array size (x,y Dimensions) Total Active	 4.98 x 3.78 4.86 x 3.66	 mm mm
Pixel Pitch	**7.5**	µm
Fill Factor without micro-lens	**47**	%

Image Sensor Specifications

The following specifications apply for All VDD pins = +3.3V, T_A = 25°C, Illumination Color Temperature = 2500°K, IR cutoff filter at 700nm, *mclk* = 48MHz, Hclk = 12MHz, frame rate = 30Hz, *vref* = 1.1 volt, video gain 0dB.

Parameter	Description	Min note 9	Typical note 8	Max note 9	Units
Optical Sensitivity[1,2] red green blue	Measured at the input of the A/D		2.7 1.4 0.9		Volt/lux.s
Dark Signal	The pixel output signal due to dark current.		**130**		LSBs/s
Read Noise[2]	The RMS temporal noise of the pixel output signal in the dark averaged over all pixels in the array.		4		LSBs
Dynamic Range[2,3]	The ratio of the saturation pixel output signal and the read noise expressed in dB.		62		dB
FPN	Fixed Pattern Noise: the RMS spatial noise in the dark excluding the effect of read noise.		0.1		%
PRNU	Photo Response Non Uniformity: the RMS variation of pixel sensitivities as a percentage of the average optical sensitivity.		1.5		%

1 The optical sensitivity at the A/D output, in units of LSBs/lux.s, can be calculated using: $\frac{4096}{vref} \cdot$ Optical Sensitivity

2. For effect of clock frequency on Sensitivity, Read Noise and Dynamic range see KAC-9628 Application note 1.
3. For effect of sensor operation in piecewise linear mode on Dynamic range see KAC-9628 Application note 2.

Blemish Specifications

Due to random process deviations, not all pixels in an image sensor array will react in the same way to a given light condition. These variations are known as blemishes.

Eastman Kodak tests the KAC-9628 CMOS image sensor under both dark and illuminated conditions. These two tests are referred to as “Dark Tests” and “Standard Light Tests” respectively.

For full documentation of the KAC-9628 blemish specification and test conditions please refer to the “KAC-9628 Blemish Specification” document.

Sensor Response Curves

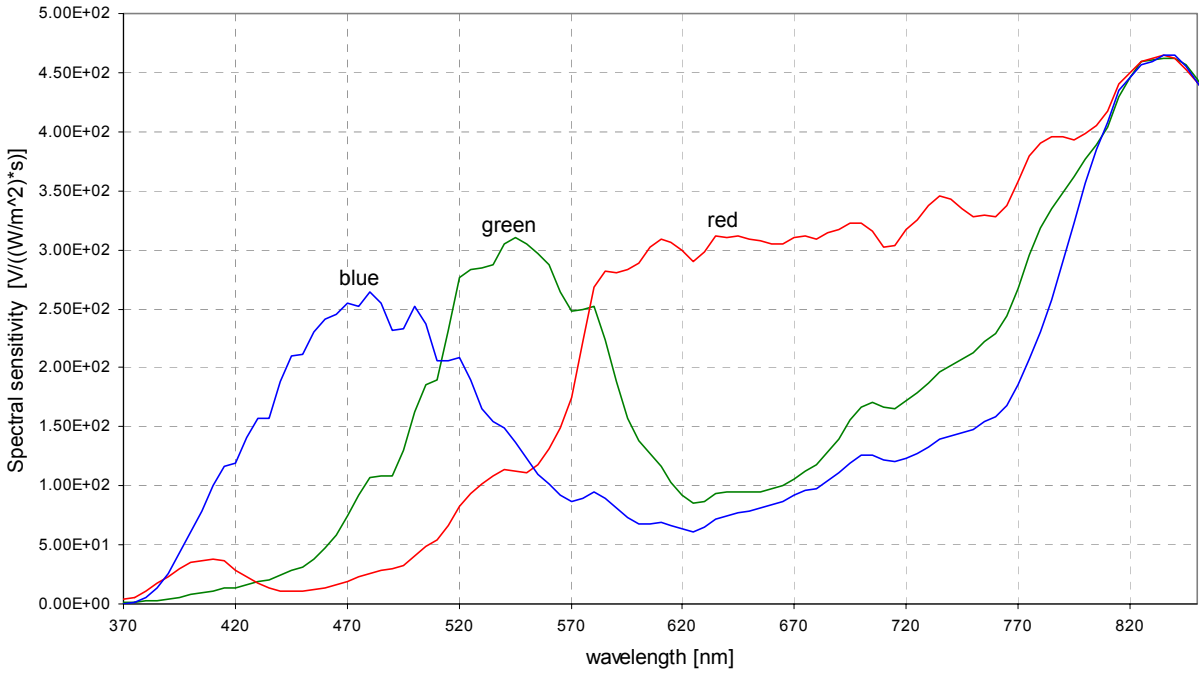
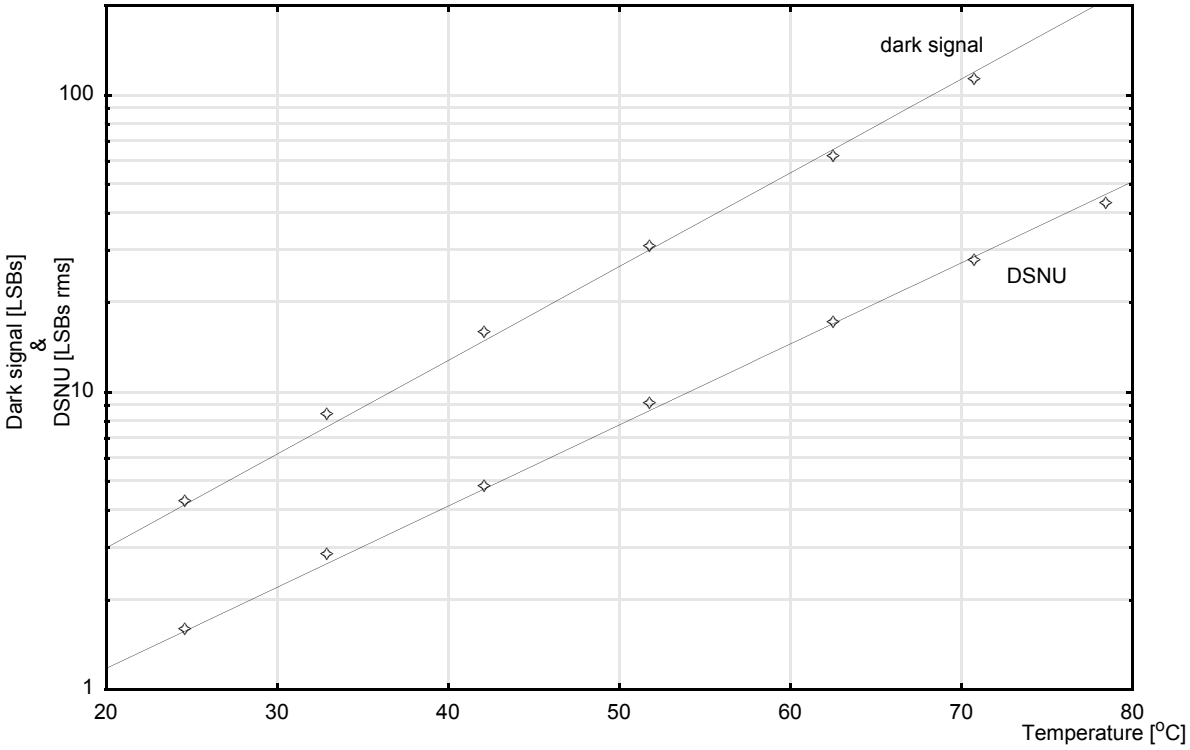


Figure 5. Spectral Response Curve



notes:

1) The dark signal and DSNU both increase linearly with integration time. The results in the graph were measured at 33 ms integration time.
2) At any temperature, the total spatial noise in the dark can be found by quadratically adding the offset FPN from the 'Image Sensor Specifications' table and the DSNU from this graph.

Figure 6. Dark signal and Dark Signal Non-Uniformity @ 30 FPS versus Temperature

Functional Description

1.0 OVERVIEW

1.1 Light Capture and Conversion

The KAC-9628 contains a CMOS active pixel array consisting of 488 rows by 648 columns. This active region is surrounded by 8 columns and 8 rows of optically shielded (black) pixels as shown in Figure7.

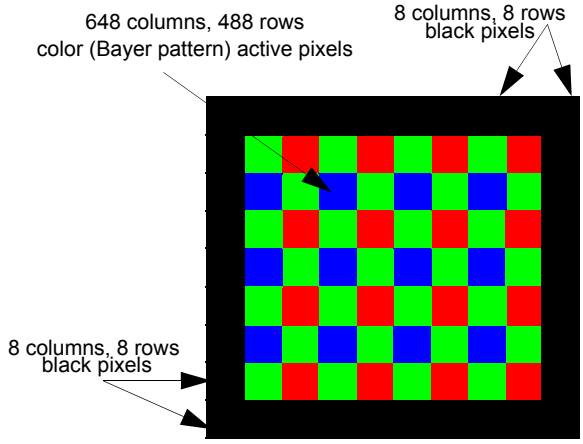


Figure 7: CMOS APS region of the KAC-9628

The color filters are Bayer pattern coded starting at row 8 and column 8. (rows 0 to 7 & columns 0 to 7 are black). The color coding is green, red, green, red until the end of row 8, then blue, green, blue, green until the end or row 9 and so on (see Figure 7).

At the beginning of a given integration time the on-board timing and control circuit will reset every pixel in the array one row at a time as shown in Figure 8

Note that all pixels in the same row are simultaneously reset, but not all pixels in the array

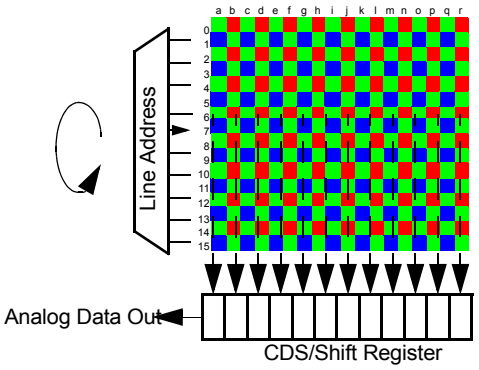


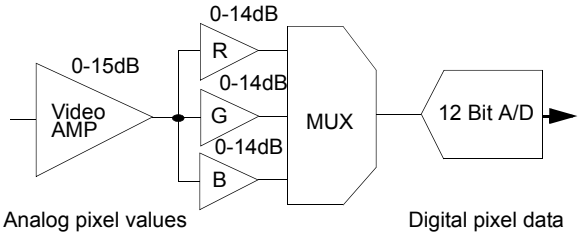
Figure 8. Sensor Addressing Scheme

At the end of the integration time, the timing and control circuit will address each row and simultaneously transfer the integrated value of the pixel to a correlated double sampling circuit and then to a shift register as shown in Figure 8.

Once the correlated double sampled data has been loaded into the shift register, the timing and control circuit will shift them out one pixel at a time starting with column “a”.

The pixel data is then fed into an analog video amplifier, where a user programmed gain is applied, then to the color amplifiers (red, green, blue), where each color gain can be individually adjusted (see Figure).

After gain and color gain adjustment the analog value of each pixel is converted to 12 bit digital data as shown in Figure .



Analog Signals Conditioning & Conversion to Digital

The digital pixel data is further processed to:

- remove defects due to bad pixels,
- compensate black level, before being framed and presented on the digital output port. (see Figure 9).

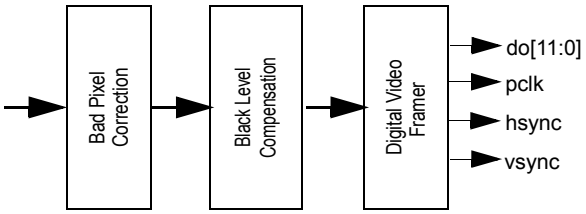


Figure 9. Digital Pixel Processing.

1.2 Program and Control Interfaces

The programming, control and status monitoring of the KAC-9628 is achieved through a two wire I^2C compatible serial bus. In addition, a slave address pin is provided (see Figure 10).

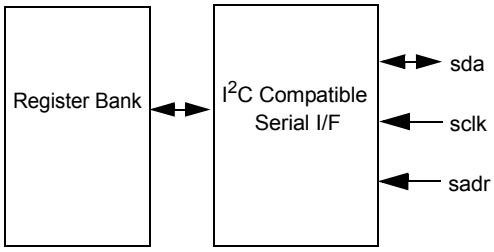


Figure 10. Control Interface to the KAC-9628.

Additional control and status pins: snapshot and external event synchronization are provided allowing the latency of the serial control port to be bypassed during single frame capture. An interrupt request pin is also available allowing complex snapshot operations to be controlled via an external micro-processor (see Figure 11).

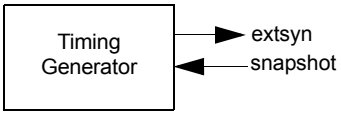


Figure 11. Snapshot & External Event Trigger Signals

Functional Description (continued)

2.0 WINDOWING

The integrated timing and control circuit allows any size window in any position within the active region of the array to be read out with a 1x1 pixel resolution. The window read out is called the "*Display Window*".

A "*Scan Window*" must be defined first, by programing the start and end row addresses as shown in Figure 12. Four coordinates (start row address, start column address, end row address & end column address) are programmed to define the size and location of the "*Display Window*" to be read out (*see Figure 12*).

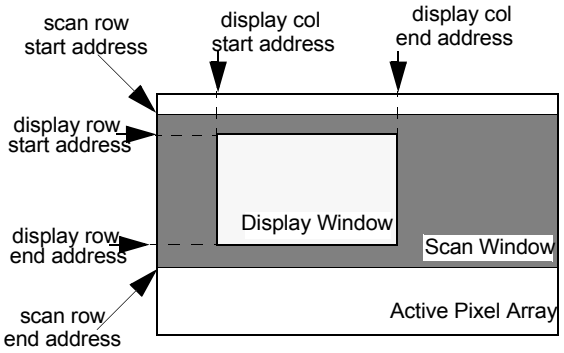


Figure 12. Windowing

Notes:

Note a: The "*Display Window*" must always be defined within the "*Scan Window*".
Note b: By default the "*Display Window*" is the complete array.
Note c: The end column address of the "Display Window" cannot be smaller than 3F hex (63 Decimal).
Note d: New "*Scan Window*" coordinates only take effect at the beginning of the first frame after the *UpdateSettings* bit is set in the UPDATE register.

2.1 Programming the scan window (mode a, default)

Two registers (SROWS & SROWE) are provided to program the size of the *scan window.* The start and end row address of the *scan window* is given by:

scan row start address = (2 SwStartRow) + SwLsb*
scan row end address = (2 SwEndRow) + 1 + SwLsb*

Where:

SwStartRow
is the contents of the *Scan Window* start row register (SROWS)
SwEndROW
is the contents of the *Scan Window* end row register (SROWE)
SwLsb
is bit 6 of the *Display Window* LSB register (DWLSB)

This mode is provided for backward compatibility with the KAC-9627 and KAC-9617 CMOS image sensors.

2.2 Programming the scan window (mode b)

To programme the scan window in mode b, bit 0 of the Scan Window LSB Register (SROWLSB). In this mode the binary value of scan window start and end row addresses are given by

scan row start address (bin) = [SwStartRow, SwStartRowLsb]
scan row end address (bin) = [SwEndRow, SwEndRowLsb]

Where:

SwStartRow
is the contents of the *Scan Window* start row register (SROWS)
SwEndRow
is the contents of the *Scan Window* end row register (SROWE)
SwStartRowLsb
is the contents of bit 7 of the *Scan Window Row LSB* register (SROWLSB)
SwEndRowLsb
is the contents of bit 6 of the *Scan Window Row LSB* register (SROWLSB)

2.3 Updating the Scan Window

After the "*Scan Window*" coordinates have been programmed, the *UpdateSettings* bit in the UPDATE register should be set. The timing and control circuit will set the new "*Scan Window*" at beginning of the next frame and reset the *UpdateSettings* bit in the UPDATE register.

2.4 Programming the Display Window

Five register (DROWS, DROWE, DCOLS, DCOLE and DWLSB) are provided to program the display window as described in the register section of this datasheet.

3.0 READ OUT MODES

3.1 Progressive Scan Readout Mode

In progressive scan readout mode, every pixel in every row in the display window is consecutively read out, one pixel at a time, starting with the left most pixel in the top most row. Hence, for the example shown in Figure 13, the read out order will be *a0,b0,...,r0* then *a1,b1,...,r1* and so on until pixel *r20* is read out.

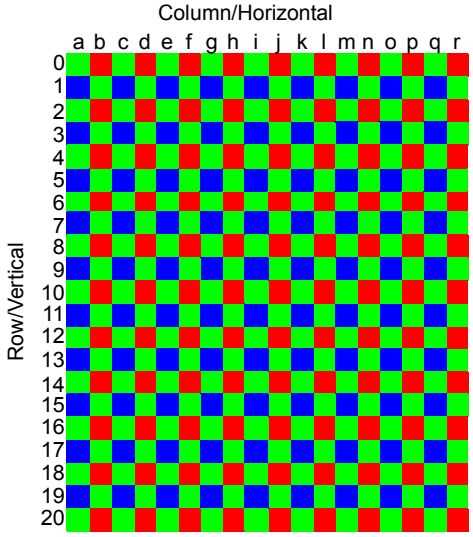


Figure 13. Progressive Scan Read Out Mode

Functional Description (continued)

3.2 Interlaced Readout Mode

In interlaced readout mode, pixels are read out in two fields, an *Odd Field* followed by an *Even Field*.

The *Odd Field,* consisting of all odd row pairs contained within the display window, is read out first. Each pixel in the "*Odd Field*" is consecutively read out, one pixel at a time, starting with the top left most pixel.

The *Even Field,* consisting of all even row pairs contained within the display window, is then read out. Each pixel in the "*Even Field*" is consecutively read out, one pixel at a time, starting with the top left most pixel.

Notes:

Note a: When using a color sensor in interlace mode, the *ScanMode* bit in the MCFG1 register should be set to a logic one.

Note b: If a *Scan Window* is defined with an odd number of rows, the timing and control circuit will automatically append an additional row. The is only true when the *ScanMode* bit in the MCFG1 register is set to a logic one.

The following are examples of how programming different scan window sizes effect the interlace read out:

Example 1, figure 14 shows a "*Scan Window*" of 20 rows and a "*Display Window*" of 20 rows and 18 columns. This is broken up into two fields:

- The odd field is read out first. The odd field will consist of pixels *a0,b0,...,r0*; *a1,b1,...,r1*; ... ; *a17,b17,...r17* as shown in figure 14.
- The even field is then read out. The even field will consist of pixels a2,b2,...,r2 ; a3,b3,...,r3 ; ... ; a19,b19,...,r19 as shown in figure 14.

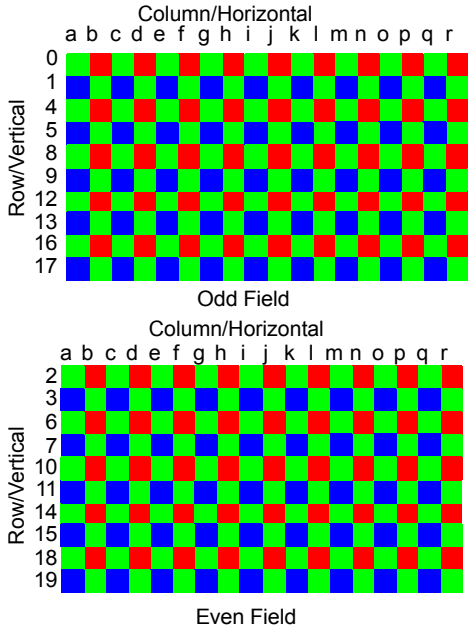


Figure 14. Interlace Read Out Mode Example 1

Example 2, figure 15 shows an interlace read out when a "*Scan Window*" of 5 or 6 rows and a "*Display Window*" of 5 or 6 row and 18 columns is programmed.

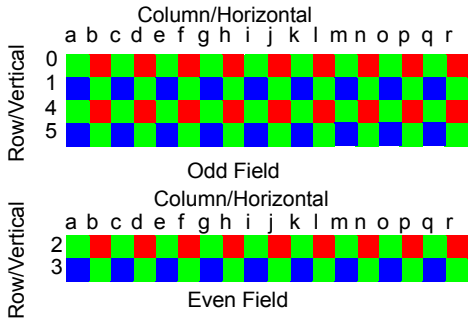


Figure 15. Interlace Read Out Example 1

Example 3, figure 16 shows an interlace readout when a "*Scan Window*" of 9 or 10 rows and a "*Display Window*" of 9 or 10 row and 18 columns is programmed.

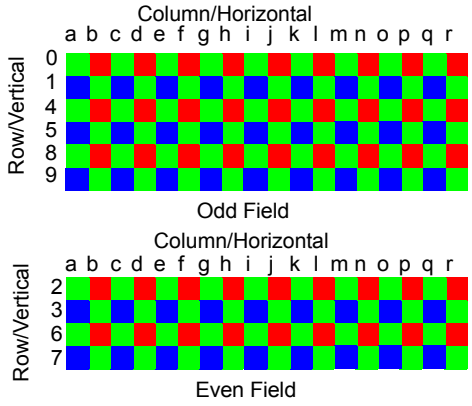


Figure 16. Interlace Read Out Example 2

Example 4, Figure shows an interlace readout when a "*Scan Window*" of 3 or 4 rows and a "*Display Window*" of 3 or 4 row and 18 columns is programmed.

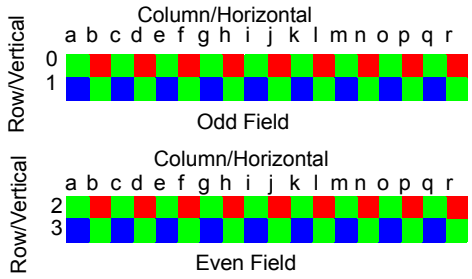


Figure 17. Interlace Read Out Example 3

Functional Description (continued)

4.0 SUB-SAMPLING MODES

4.1 2:1 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the display window vertically, horizontally or both, with an aspect ratio of 2:1 as illustrated in figure 18.

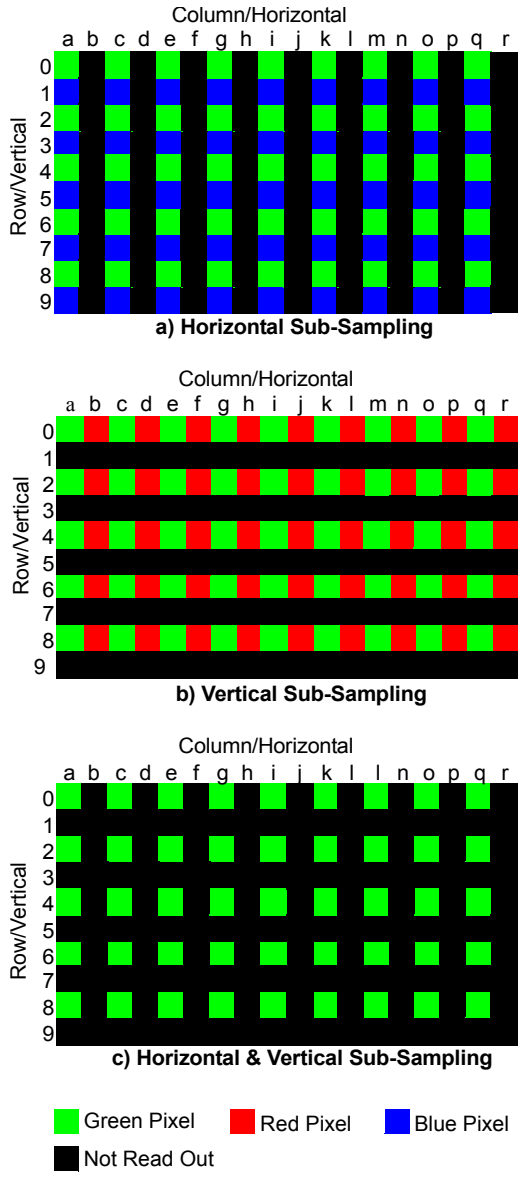


Figure 18. 2:1 Horizontal and Vertical Sub-Sampling

Notes:

Note a: To program the sensor in 2:1 Sub-sampling the *HSubSamEn* bit in the MCFG1 register should to be set to a logic one.

Note b: Setting the *HSubSamEn* bit in the MCFG1 to a logic one will switch on the horizontal sub-sampling, while setting the *VSubSamEn* bit in the MCFG1 register will switch on the vertical sub-sampling.

Note c: Sub-sampling cannot be used with interlace readout mode.

Note d: When using horizontal sub-sampling Pclk is divided by 2. The active time of Hsync is the same in sub-sampled and non sub-sampled mode. Horizontal sub-sampling does not increase frame rate.

4.2 4:2 Sub-Sampling

The timing and control circuit can be programmed to sub-sample pixels in the display window vertically, horizontally or both, with an aspect ratio of 4:2 as illustrated in figure 19

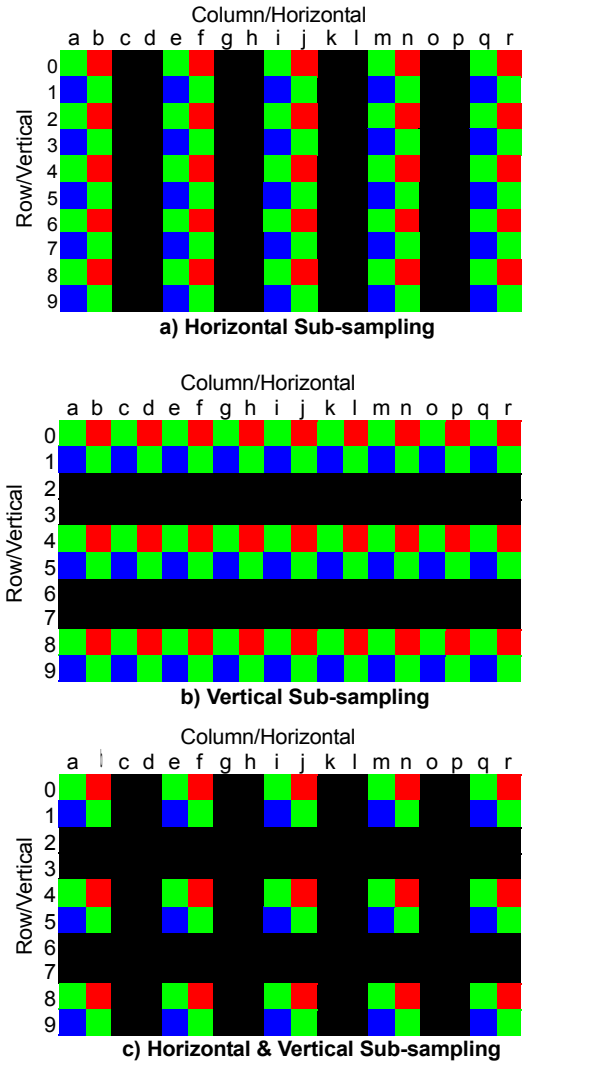


Figure 19. 4:2 Horizontal and Vertical Sub-Sampling

Notes:

Note a: To program the sensor in 4:2 Sub-sampling the *HSubSamEn* bit in the MCFG1 register should be set to a logic zero.

Note b: Setting the *HSubSamEn* bit in the MCFG1 to a logic one will switch on the horizontal sub-sampling, while setting the *VSubSamEn* bit in the MCFG1 register will switch on the vertical sub-sampling.

Note c: Sub-sampling cannot be used with interlace readout mode.

Note d: When using horizontal sub-sampling Pclk is divided by 2. The active time of Hsync is the same in sub-sampled and non sub-sampled mode. Horizontal sub-sampling does not increase frame rate.

Functional Description (continued)

5.0 FRAME RATE & EXPOSURE CONTROL

5.1 Introduction

A frame is defined as the time it takes to reset every pixel in the array, integrate the incident light, convert it to digital data and present it on the digital video port. This is not a concurrent process and is characterized in a series of events each needing a certain amount of time as shown in Figure 20.

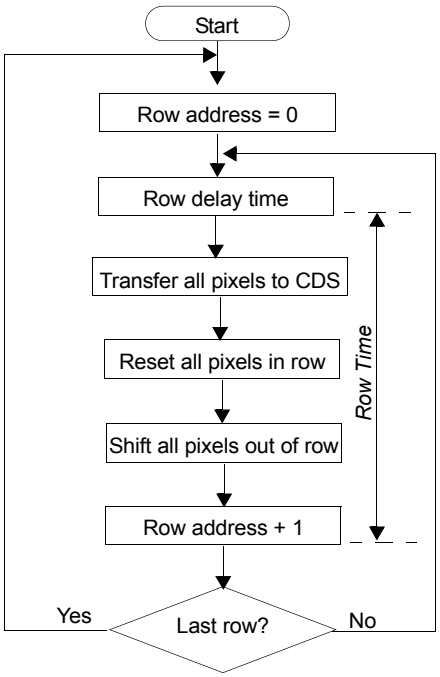


Figure 20. Frame Readout Flow Diagram

The following factors effect frame rate, the:

- frequency of *Hclk*
- size of the "*Scan Window*"
- sub sampling mode
- programmed row delay
- programmed frame delay.

The following factors effect exposure but not frame rate

- analog gain
- integration time
- modification of the sensor's linear response.

This section describes how to program the frame rate and exposure time.

5.2 Analog Gain and Color Gain

There are two analog gain stages built into the sensor before the A/D allowing the video and separate color gains to be programmed.

The video gain is given by:

$$V_{gain} = 1 + 0.07032 * VidGain$$

Where:

VidGain is the six bit video gain step programmed in the VGAIN register

The red gain is given by:

$$R_{gain} = 1 + 0.03125 * RGain$$

Where:

RGain is the six bit video gain step programmed in the RGAIN register

The green gain is given by:

$$G_{gain} = 1 + 0.03125 * GGain$$

Where:

GGain is the six bit video gain step programmed in the GGAIN register

The blue gain is given by:

$$B_{gain} = 1 + 0.03125 * BGain$$

Where:

BGain is the six bit video gain step programmed in the BGAIN register

Functional Description (continued)

5.3 Clock Generation

The KAC-9628 contains a clock generation module (figure 21) that will create three clocks as follows:

Hclk, the horizontal clock. This is an internal system clock and can be programmed to be the input clock *(mclk)* or *mclk* divided by any number between 1 and 31. All exposure times are in multiples of this clock.

To set the frequency of this clock the *HclkGen* bits in the VCLKGEN register should be programed.For the new frequency to take effect the *UpdateSettings* bit in the UPDATE register should be set. The timing and control circuit will set the new *Hclk* frequency at beginning of the next frame and reset the *UpdateSettings* bit in the UPDATE register.

pclk the pixel clock. This is the external pixel clock that appears at the digital video port. **pclk** is always equal to *Hclk* except when the sensor is programmed to work sub-sampling mode in which case **pclk** will be equal to *Hclk* divided by 2. This clock cannot be programed.

Aclk the array clock. This is an internal clock used by the pixel array.Its frequency does not effect the exposure time.

To set the frequency of this clock the *AclkGen* bits in the VCLKGEN register should be programed. For the new frequency to take effect the *UpdateSettings* bit in the UPDATE register should be set. The timing and control circuit will set the new *Hclk* frequency at beginning of the next frame and reset the *UpdateSettings* bit in the UPDATE register.

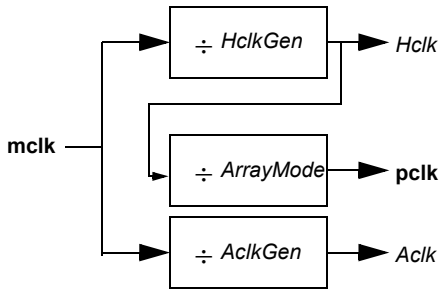


Figure 21. Clock Generation Module

5.4 Full Frame Integration

Full frame integration is when each pixel in the array integrates light incident on it for the duration of a frame (see Figure 22).

The number of *Hclk* clock cycles required to process & shift out one row of pixels is given by:

$$RN_{Hclk} = R_{opcycle} + R_{delay}$$

Where:

$R_{opcycle}$ is a fixed integer value of 780 representing the *Row Operation Cycle Time* in multiples of *Hclk* clock cycles. It is the time required to carry out all fixed row operations outlined in Figure 20.

R_{delay} a programmable value between 0 & 2047 representing the *Row Delay Time* in multiples of *Hclk*. This parameter allows the *Row Operation Cycle* time to be extended. (See the Row Delay High and Row Delay Low registers).

New R_{delay} values only take effect at the beginning of the first frame after the *UpdateSettings* bit is set in the UPDATE register.

The number of rows in a scan window is given by:

$$SWN_{rows} = (RAD_{end} - RAD_{start}) + 1$$

Where:

RAD_{end} is the end row address of the defined scan window. (See section 2.0)

RAD_{start} is the start row address of the defined scan window. (Scan section 2.0).

The number of *Hclk* clocks required to process a full frame is given by:

$$FN_{Hclk} = [(M_{factor} * SWN_{rows}) + F_{delay}] * RN_{Hclk}$$

Where:

M_{factor} is a Mode Factor which must be applied. It is dependent on the selected mode of operation as shown in the table below:

Progressive Scan	1
Vertical Sub-sampling or Interlace	0.5

SWN_{rows} is the *Number of Rows in Selected Scan Window.*

F_{delay} a programmable value between 0 & 4096 representing the *Inter Frame Delay* in multiples of RN_{Hclk}. This parameter allows the frame time to be extended. (See the Frame Delay High and Frame Delay Low registers).

New F_{delay} values only take effect at the beginning of the first frame after the *UpdateSettings* bit is set in the UPDATE register.

The frame rate is given by:

$$Frame\ Rate = \frac{Hclk}{FN_{Hclk}}$$

Functional Description (continued)

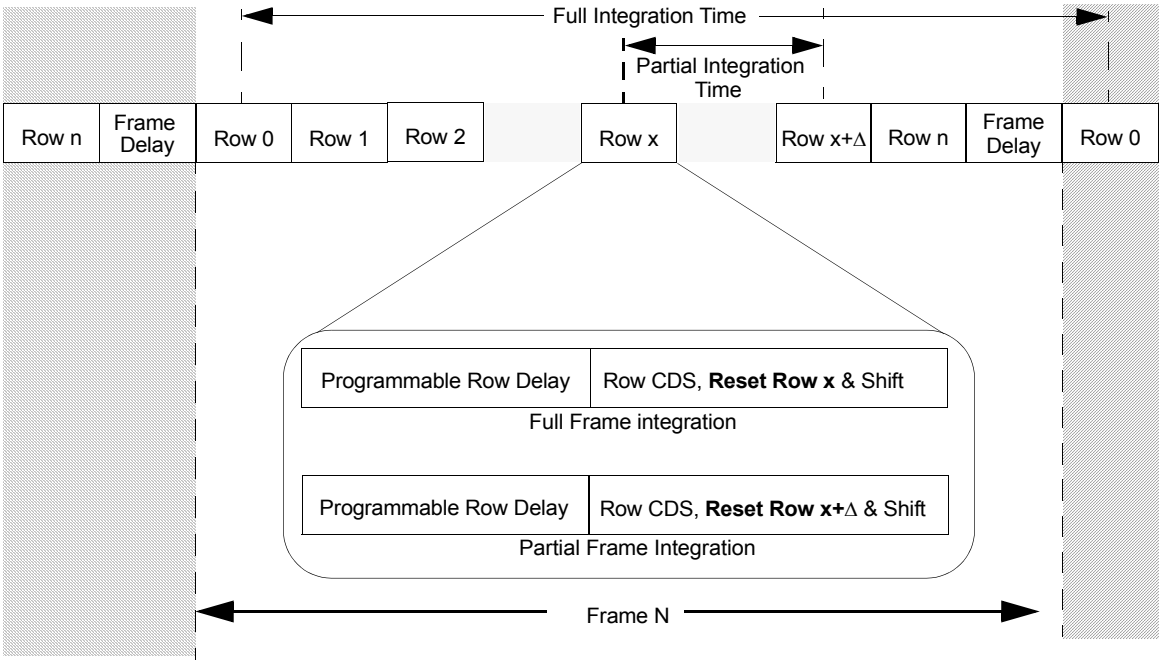


Figure 22. Partial and Full Frame Integration

5.5 Partial Frame Integration

In some cases it is desirable to reduce the time during which the pixels in the array are allowed to integrate incident light without changing the frame rate.

This is known as *Partial Fame Integration* and can be achieved by resetting pixels in a given row ahead of the row being selected for readout as shown in Figure 22. The number of *Hclk* clocks required to process a partial frame is given by:

$$FP_{Hclk} = RN_{Hclk} * I_{time}$$

Where:

RN_{Hclk} is the number of *Hclk* clock cycles required to process & shift out one row of pixels.

I_{time} is the number of rows ahead of the current row to be reset. (See the Integration Time High and Low registers).

New I_{time} values only take effect at the beginning of the first frame after the *UpdateSettings* bit is set in the UPDATE register.

The Integration time is subject to the following limits:

Mode	Limit
Progressive Scan	$I_{time} <= SWN_{rows} + F_{delay}$
Interlace	$I_{time} <= 2* (SWN_{rows} + F_{delay})$
Sub-Sampled	$I_{time} <= 0.5 * (SWN_{rows} + F_{delay})$

5.6 Modification of Linear Response Curve

The electro-optic transfer curve of the pixel array is linear. While a linear response is satisfactory for capturing images containing similar brightness levels, it is not always satisfactory for capturing images with a large variation of brightness levels.

For a fixed integration time, pixels capturing bright areas of a scene will saturate much faster than pixels capturing darker regions. When there is a large variation in the light intensities between the dark and light regions it is not possible to simultaneously capture the detail in both regions. One would have to be sacrificed.

Since the response of the human eye to light is non-linear, a non- linear response such as that shown with the dashed curve in figure 23 would allow the detail in both the light and dark regions of the image to be captured and seen.

The timing and control circuit built into the KAC-9628 allows the linear response of the electro-optic response to be modified into a piece-wise linear response (approximate gamma)

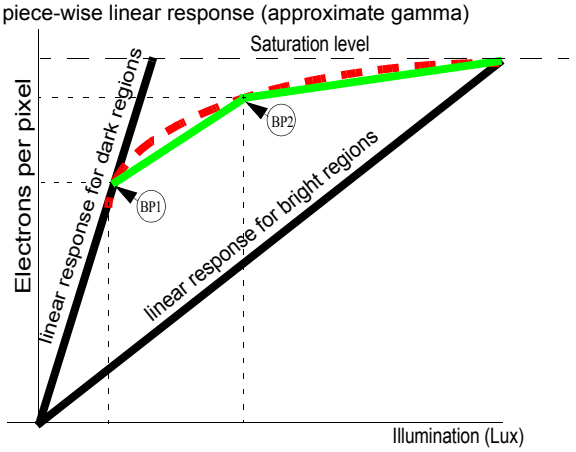


Figure 23. Linear & Non Linear Transfer Responses

Functional Description (continued)

The KAC-9628 integrated timing and control circuit allows up to two break points to be programmed such that a piecewise linear response can be achieved as shown with the green lines in figure 23.

To operate the sensor in piecewise linear mode a 56k ohm resistor must be connected to pin 41 and the following sequence must be written after system reset:

Address (Hex)	Value
03Hex	set bit 3 to a logic 1
32Hex	40Hex
30Hex	40Hex
03Hex	set bit 3 to a logic 0

Two registers are provided to define each break point. The *Level* register and the *Sensitivity* register.

The sensitivity of the first branch, (slope 0 in figure 24), is determined by the time settings and the image sensor characteristics. The sensitivity (slope), of the other branches is determined by the value programmed in the *Sensitivity* registers. The levels at which the piecewise linear curve switches from one slope to another are determined by the values programmed in the *Level* registers.

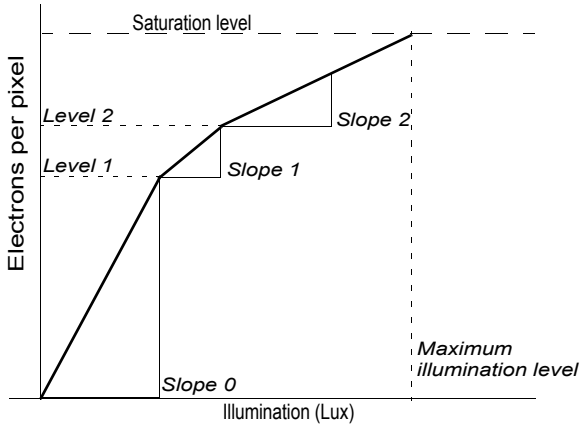


Figure 24. Break Points Programming

The maximum illumination level (see figure 24) that can be detected by the sensor is determined by the settings of the level and slope registers.

For a full explanation of how to use the KAC-9628 in piecewise linear mode refer to KAC-9618/28 Application note 2.

5.7 Frame Rate Programming Guide

The table bellow can be used as a guide for programming the sensor. Note that it is assumed that the sensor is being driven with a 48MHz clock. All programmed values are given in decimal.

register	vclkgen	rdelayh	rdelayl	fdelayh	fdelayl	srows	srowe	dwlsb
address	05hex	15hex	16hex	17hex	18hex	0Bhex	0Chex	12hex
fps		[10:8]	[7:0]	[11:8]	[7:0]	[8:1]	[8:1]	
30	4	0	0	0	9	0	251	50
15	4	0	0	2	40	0	251	50
7.5	4	0	0	6	12	0	251	50
3.75	4	3	12	6	12	0	251	50
25	4	0	172	0	0	0	251	50
12.5	5	0	0	1	226	0	251	50
6.25	5	0	0	5	188	0	251	50
3.125	4	0	156	14	14	0	251	50
5	4	2	255	4	23	0	251	50
4	5	0	0	10	12	0	251	50
3	5	0	0	14	14	0	251	50
2	6	0	200	13	248	0	251	50
1	6	3	241	15	126	0	251	50

Functional Description (continued)

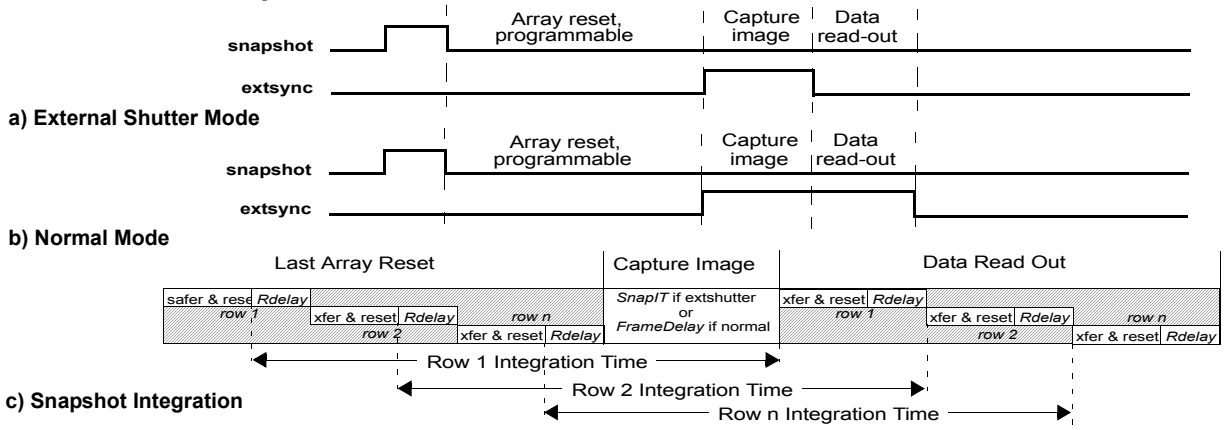


Figure 25. Timing Diagram in the SNAP State

6.0 SNAPSHOT MODE

6.1 Introduction

Two dedicated pins are provided on the KAC-9628, **snapshot**, and **extsync** allowing the sensor to be externally controlled to capture a single image.

The **snapshot** input pin is used to trigger a snapshot, while the **extsync** output pin is used to synchronize a light source, strobe or mechanical shutter.

6.2 Taking a Snapshot

By default the sensor will operate in the **VIDEO** state (see figure 26). To take a snapshot, the snapshot mode must be enabled by setting the *SnapEnable* bit in the SNAPSHOTMODE register to a logic 1. This will cause the sensor to enter the **FREEZE** state at the end of the current frame. In the **FREEZE** state the sensor is idle.

The sensor will leave the **FREEZE** state and return to **VIDEO** state when the snapshot mode is disabled (*SnapEnable* bit in the SNAPSHOTMODE register set to a logic 0)

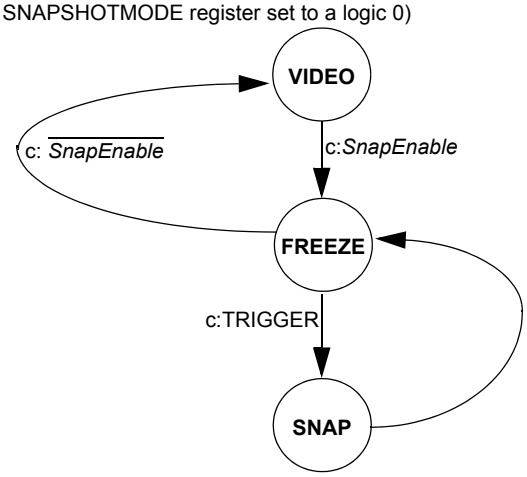


Figure 26. Snapshot Mode

Alternatively, when an active snapshot signal is applied to the snapshot input pin an internal trigger signal, *TRIGGER*, is generated as shown in figure 27. The trigger generation circuit will create two types of TRIGGER as follows:

- **Pulse Trigger** (*SnapshotMode* bit of the SNAPSHOTMODE register is cleared). In this mode (the default) a single TRIGGER pulse will be generated.
- **Level Trigger (***SnapshotMode* bit of the SNAPSHOTMODE register is set). In this mode the TRIGGER will remain high as long as an active level is held on the **snapshot** pin.

When a TRIGGER is generated, the sensor will enter the SNAP state as shown in figure 26.

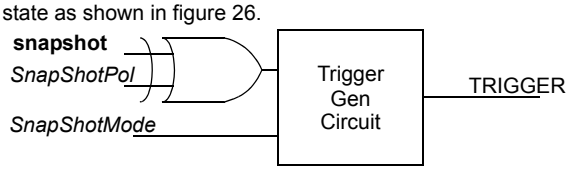


Figure 27. TRIGGER Generation Logic

6.3 The SNAP State in External Shutter Mode

To take a snapshot in external shutter mode, the *ShutterMode* bit of the SNAPSHOTMODE register must be set.

In this mode three consecutive operations will be carried out in the SNAP state as follows (see figure 25a):

- **Array Reset**, during which the **extsync** pin is kept in-active and the array is reset one row at a time. The number of times the array is reset is programmable from 1-3 frames, (see the *SsFrames* bits in the SNAPSHOTMODE register).
- **Image Capture**, the **extsync** pin will activate. The width of the extsync signal can be programed from 1 to 2047 lines by programming the integration time registers, ITMEH and ITIMEL.
- **Array Read Out**, the third and final operation reads the image data out one row at a time.

6.4 The SNAP State in Normal Mode (default)

To take a snapshot in normal mode, the *ShutterMode* bit of the SNAPSHOTMODE register must be cleared. In this case the following consecutive operations will be carried out in the **SNAP** state (see figure 26b):

- **Array Reset**, during which the **extsync** pin is kept in-active and the array is reset one row at a time. The number of times the array is reset is programmable from 1-3 frames, (see the *SsFrames* bits in the SNAPSHOTMODE register).
- **Image Capture**, the **extsync** pin will activate and remain active for the duration of the capture time. The width of the image capture can be extended by programming FDELAYH and FDELAYL, which will increase integration time.
- **Array Read Out**, the image data is read out one row at a time. During this operation the extsync pin remains active.

6.5 Return to the FREEZE State

When read out is complete the sensor will return to the **FREEZE** state.

6.6 Return to the VIDEO state

If the snapshot mode is disabled before readout is complete (*SnapEnable* bit in the SNAPSHOTMODE register is set to a logic 0), then at the end of readout the sensor will return to the **VIDEO** state.

Functional Description (continued)

7.0 SIGNAL PROCESSING

7.1 Bad Pixel Detection & Correction

The KAC-9628 has a built-in bad pixel detection and correction block that operates on the fly. This block can be switched off by the user.

7.2 Black Level Compensation

In addition to the programmable gain the KAC-9628 has a built in black level compensation block as illustrated in Figure 28. This block can be switched off.

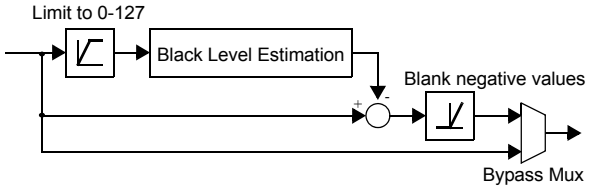


Figure 28. Digital Black Level Compensation.

The black level compensation block subtracts the estimated average black level from the digital video output to compensate for the temperature and integration time dependent dark signal level of the pixels. Figure illustrates the black level estimation circuit built into the KAC-9618

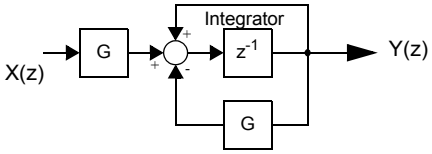


Figure 29. Black Level Estimation Circuit

After optional clipping (the *Clip* parameter in the BLCOEFF register) of the MSB (used to remove the signal level of hot pixel noise, the block estimates the average of the black signal level by means of a low-pass filter that is applied to the series of black pixel signals of the black pixels that are included in the scan window. This low-pass filter features a programmable time-constant. The estimated average black level value is then subtracted from the pixel data. During readout of active pixels, the running average is frozen and not updated.

The transfer function (in Z-domain) of the low-pass filter in the black level estimation block is given by:

$$Y(z) = X(z)\frac{G}{z-(1-G)}$$

where the gain G is programmable through α:

$$G = 2^{-(7+\alpha)}$$

An increased value of α (the *Alpha* parameter in the BLCOEFF register) increases the loop gain and therefore increases its time-constant, resulting in a slower update of the integrator.

The actual black pixels used for the black level estimation is dependent on the user defined scan window as illustrated in figure 30. In all cases only the inner 4 rows and columns are used.

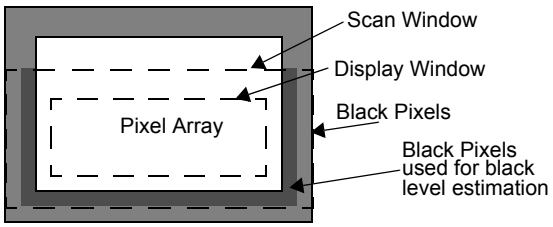


Figure 30. Black Pixels Used For Black Level Estimation

8.0 POWER MANAGMENT

8.1 Power Up and Down

The KAC-9628 is equipped with an on-board power management system allowing the analog and digital circuitry to be switched off (power down) and on (power up) at any time.

The sensor can be put into power down mode by asserting a logic one on the "*pdwn*" pin or by writing to the power down bit in the main configuration register via the I^2C compatible serial interface.

To power up the sensor a logic zero can be asserted on the "*pdwn*" pin or write to the power down bit in the main configuration register via the I^2C compatible serial interface.

It will take a few milliseconds for all the circuits to power up. The power management register contains a bit indicating when the sensor is ready for use. During this time the sensor cannot be used for capturing images. A status bit in the power management register will indicate when the sensor is ready for use.

9.0 OFFSET ADJUSTMENT

The level of the offset voltage determines the black level of the image and has a direct impact on the image quality. Too high an offset results in a white washed or hazy looking image, while too low of an offset results in a dark image with low contrast even though the light conditions are good.

For maximum image quality over a wide range of light conditions it is necessary to set an appropriate offset voltage before using the sensor to capture images.
The offset of each part can be adjusted by programming the offset control register (OCR) via the I^2C compatible serial interface.

To calibrate the offset of a given part the following procedure should be followed:

- Disable the black level compensation block by writing a logic 1 to bit 4 of the **Main Configuration Register 0** (MCFG0: address 02Hex).
- Set the sensor's gain to 1 by writing 00Hex to registers VGAIN, GGAIN, BGAIN, RGAIN.
- Calculate the average black level by reading a full frame and calculating the average black level ($BL_{average}$) of the first and last 5 black pixels in the every row of the array.
- If the calculated average black level is greater than the target black level then set the *OffSign* bit of the OCR register to a logic 1, else set it to a logic 0.
- The offset can be adjusted by running the following binary search algorithm on the *OffMag* parameter in the OCR register:
- For n=6 to 1 step -1
- {
  Set *OffMag* bit n in the OCR register to a logic one by writing over the I^2C compatible interface.
  Read a full frame and calculate the average black level ($BL_{average}$) of the first and last 5 black pixels in the every row of the array
  If ($BL_{average}$ < 100) then
  Reset *OffMag* bit n in the OCR register to 0
  else
  Keep *OffMag* bit n set to one.
  }
- Enable the black level compensation block (if desired) by writing a logic 0 to bit 4 of the **Main Configuration Register 0** (MCFG0: address 02Hex)

Functional Description (continued)

10.0 SERIAL BUS

The serial bus interface consists of the *sda* (serial data), *sclk* (serial clock) and *sadr* (device address select) pins. The KAC-9628 can operate only as a slave.

The *sclk* pin is an input, it only and controls the serial interface, all other clock functions within KAC-9628 use the master clock pin, *mclk*.

10.1 Start/Stop Conditions

The serial bus will recognize a logic 1 to logic 0 transition on the *sda* pin while the *sclk* pin is at logic 1 as the ***start*** condition. A logic 0 to logic 1 transition on the *sda* pin while the *sclk* pin is at logic 1 is interrupted as the ***stop*** condition as shown in Figure 31.

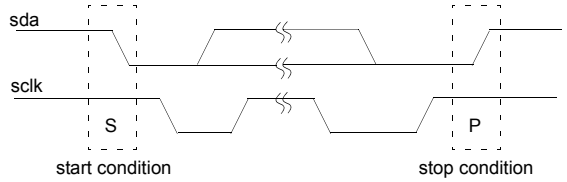


Figure 31. Start/Stop Conditions

10.2 Device Address

The serial bus *Device Address* of the KAC-9628 is set to 1010101 when *sadr* is tied low and 0110011 when *sadr* is tied high. The value for s*adr is* set at power up.

10.3 Acknowledgment

The KAC-9628 will hold the value of the *sda* pin to a logic 0 during the logic 1 state of the *Acknowledge* clock pulse on *sclk* as shown in Figure 32.

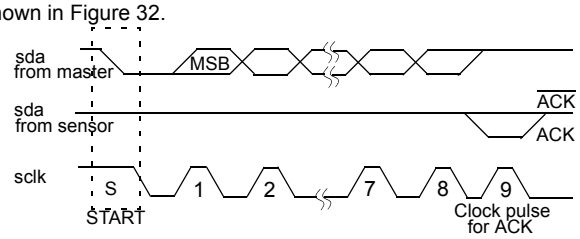


Figure 32. Acknowledge

10.4 Data Valid

The master must ensure that data is stable during the logic 1 state of the *sclk* pin. All transitions on the *sda* pin can only occur when the logic level on the sclk pin is “0” as shown in Figure 33.

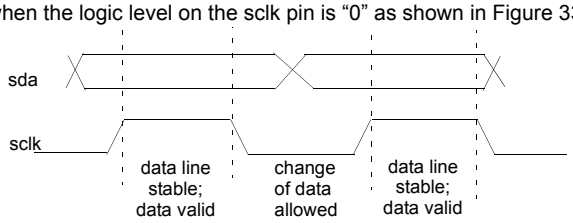


Figure 33. Data Validity

10.5 Byte Format

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an *Acknowledge*. The most significant bit of the byte is should always be transmitted first. See Figure 34.

10.6 Write Operation

A write operation is initiated by the master with a *Start Condition* followed by the sensor’s *Device Address* and $\overline{Write}$ bit. When the master receives an *Acknowledge* from the sensor it can transmit 8 bit internal register address. The sensor will respond with a second *Acknowledge* signaling the master to transmit 8 write data bits. A third *Acknowledge* is issued by the sensor when the data has been successfully received.
The write operation is completed when the master asserts a *Stop Condition* or a second *Start Condition*. See Figure 35.

10.7 Read Operation

A read operation is initiated by the master with a *Start Condition* followed by the sensor’s *Device Address* and *Write* bit. When the master receives an *Acknowledge* from the sensor it can transmit the internal *Register Address* byte. The sensor will respond with a second *Acknowledge*. The master must then issue a new *Start Condition* followed by the sensor’s *Device Address* and *read* bit. The sensor will respond with an Acknowledged followed by the *Read Data* byte.
The read operation is completed when the master asserts a *Not Acknowledge* followed by *Stop Condition* or a second *Start Condition*. See Figure 36.

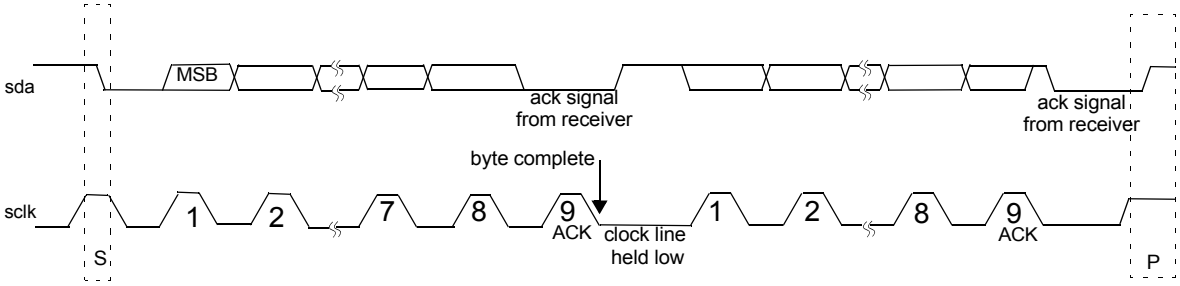
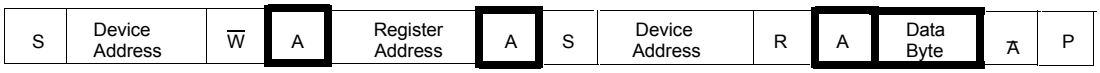


Figure 34. Serial Bus Byte Format

bold **sensor action**

Figure 35. Serial Bus Write Operation



bold **sensor action**

Figure 36. Serial Bus Read Operation

Functional Description (continued)

11.0 DIGITAL VIDEO PORT

The captured image is placed onto a flexible 12-bit digital port as shown in Figure 9. The digital video port consists of a programmable 12-bit digital Data Out Bus (*d[11:0]*) and three programmable synchronisation signals (*hsync, vsync, pclk*).

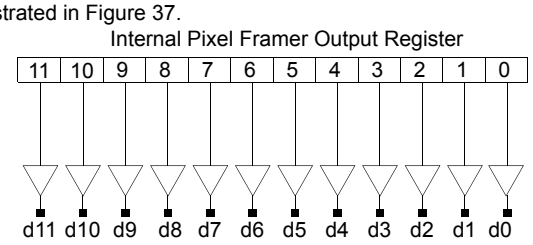
By default the synchronisation signals are configured to operate in "*master*" mode. They can be programed to operate in "*slave*" mode.

The following sections are a detailed description of the timing and programming modes of digital video port.

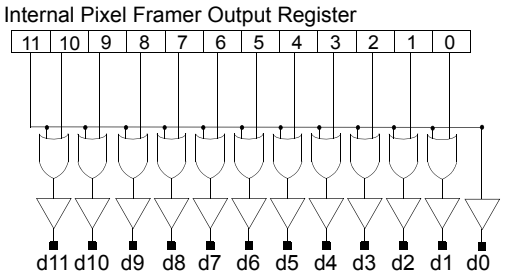
Pixel data is output on a 12-bit digital video bus. This bus can be tri-stated by asserting the *TriState* bit in the VIDEOMODE1 register.

11.1 Digital Video Data Out Bus (d[11:0])

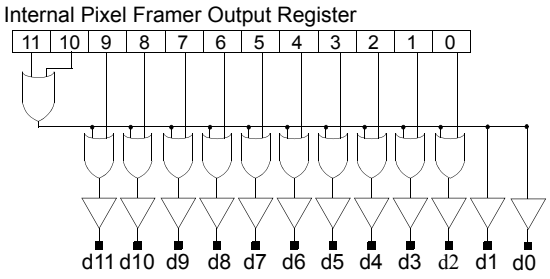
A programmable matrix switch is provided to map the output of the internal pixel framer to the pins of the digital video bus as illustrated in Figure 37.



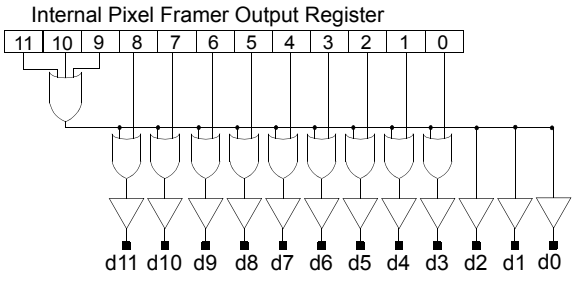
a) MSB Bit 11, Switch Mode (default)



b) MSB Bit 10, Switch Mode



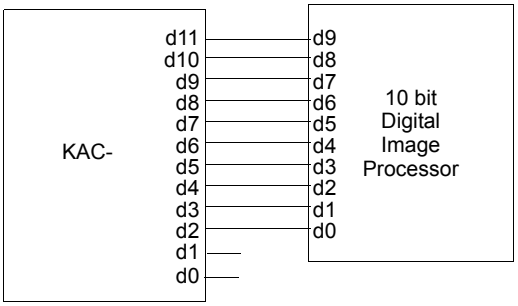
c) MSB bit 9, Switch Mode



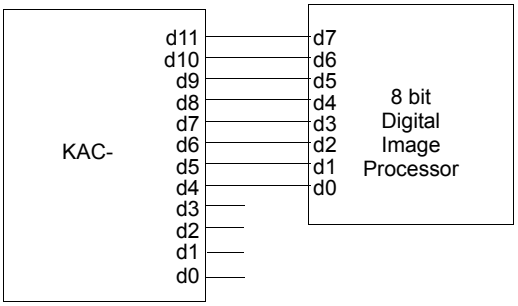
d) MSB bit 8, Switch Mode

Figure 37. Digital Video Bus Switching Modes

This feature allows a programmable digital gain to be implemented when connecting the sensor to 8 or 10 bit digital video processing systems as illustrated in Figure 38. The unused bits on the digital video bus can be optionally tri-stated.



a) KAC-9628 Connected to a 10 bit Digital Image Processors



b) KAC-9628 Connected to a 8 bit Digital Image Processors

Figure 38. Example of connection to 10/8 bit systems

Synchronisation Signals in Master Mode

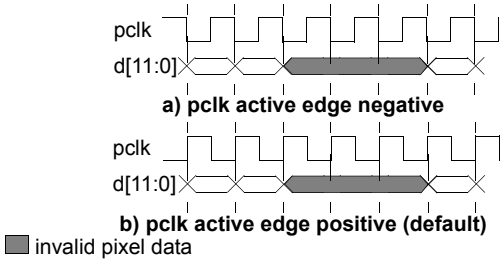
By default the sensor's digital video port's synchronisation signals are configured to operate in master mode. In master mode the integrated timing and control block controls the flow of data onto the 12-bit digital port, three synchronisation outputs are provided:

pclk	is the pixel clock output pin.
hsync	is the horizontal synchronisation output signal.
vsync	is the vertical synchronisation output signal.

11.2 Pixel Clock Output Pin (pclk) (Master Mode)

The pixel clock output pin, *pclk,* is provided to act as a synchronisation reference for the pixel data appearing at the digital video out bus pins d[11:0]. This pin can be programmed to operate in two modes:

- In free running mode the pixel clock output pin, *pclk,* is always running with a fixed period. Pixel data appearing on the digital video bus *d[11:0]* are synchronized to a specified active edge of the clock as shown in Figure 39.



a) pclk active edge negative

b) pclk active edge positive (default)

Figure 39. *pclk* in Free Running Mode

- In data ready mode, the pixel clock output pin (*pclk*) will produce a pulse with a specified level every time valid pixel data appears on the digital video bus *d[11:0]* as shown in Figure 40.

Functional Description (continued)

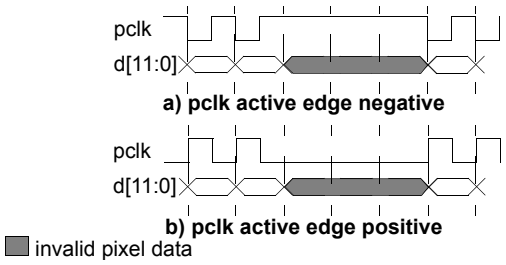


Figure 40. *pclk* in Data Ready Mode

By default the pixel clock is a free running active low (pixel data changes on the positive edge of the clock) with a period equal to the internal *hclk*. The active edge of the clock can be programmed such that pixel data changes on the positive or negative edge of the clock.

11.3 Horizontal Synchronisation Output Pin (hsync)

The horizontal synchronisation output pin, *hsync*, is used as an indicator for row data. The hsync output pin can be programmed to operate in two modes as follows:

- Level mode should be used when the pixel clock, *pclk,* is programmed to operate in *free running mode.* In level mode the *hsync* output pin will go to the specified level (high or low) at the start of each row and remain at that level until the last pixel of that row is read out on d[11:0] as shown in Figure 41. The *hsync* level is always synchronized to the active edge of *pclk*.

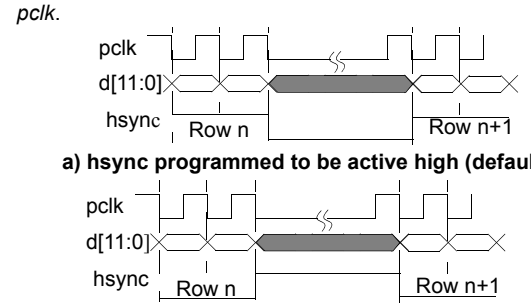


Figure 41. *hsync* in Level Mode

- Pulse mode should be used when the pixel clock, *pclk,* is programmed to operate in *data ready mode.* In pulse mode the *hsync* output pin will produce a pulse at the end of each row. The width of the pulse will be a minimum of four *pclk* cycles and its polarity can be programmed as shown in Figure 42. The *hsync* level is always synchronized to the active edge of *pclk*

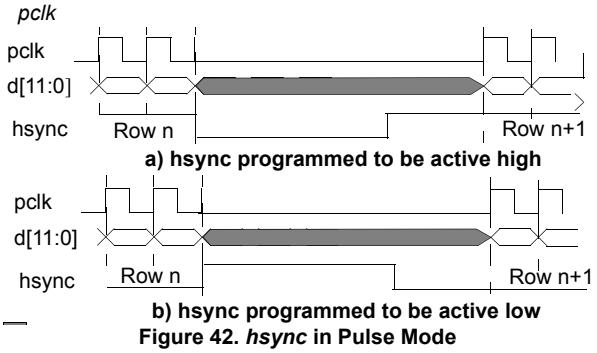


Figure 42. *hsync* in Pulse Mode

By default the first pixel data at the beginning of each row is placed on the digital video bus as soon as *hsync* is activated. It is possible to program up to 15 dummy pixels to be readout at the beginning of each row before the real pixel data is readout. This feature is supported for both *level* and *pulse* mode.

11.4 Vertical/Horizontal Synchronisation Pin (vsync)

The vertical synchronisation output pin, *vsync,* is used as an indicator for pixel data within a frame. The *vsync* output pin can be programmed to operate in two modes as follows:

- Level mode should be used when the pixel clock, *pclk,* is programmed to operate in *free running mode.* In level mode the *vsync* output pin will go to the specified level (high or low) at the start of each frame and remain at that level until the last pixel of that row in the frame is placed on d[11:0] as shown in Figure 43. The *hsync* level is always synchronized to the active edge of *pclk*.

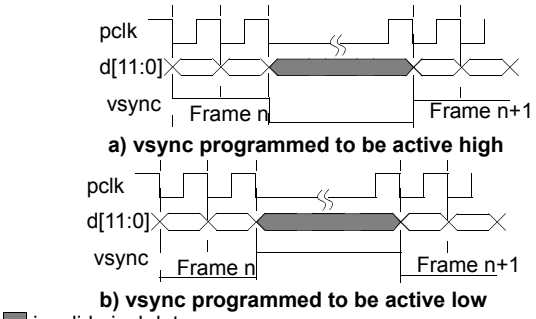


Figure 43. vsync in Level Mode

- Pulse mode should be used when the pixel clock, *pclk,* is programmed to operate in *data ready mode.* In pulse mode the *vsync* output pin will produce a pulse at the end of each frame. The width of the pulse will be a minimum of four *hclk* cycles and its polarity can be programmed as shown in Figure 44. The *vsync* level is always synchronized to the active edge of *pclk*.

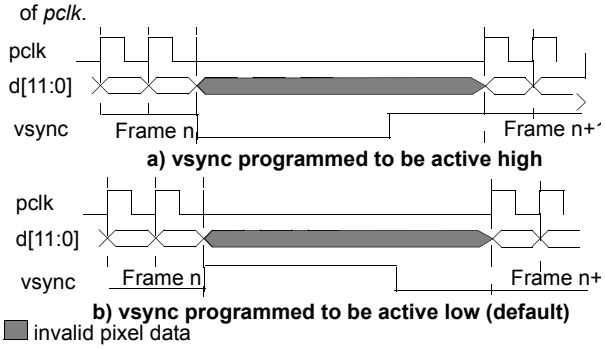


Figure 44. vsync in pulse mode

11.5 Odd/Even Mode

In odd/even mode the *vsync* signal is used to indicate when pixel data from an odd and even field is being placed on the digital video bus *d[11:0]*. The polarity of *vsync* can still be programmed in this mode as shown in Figure 45

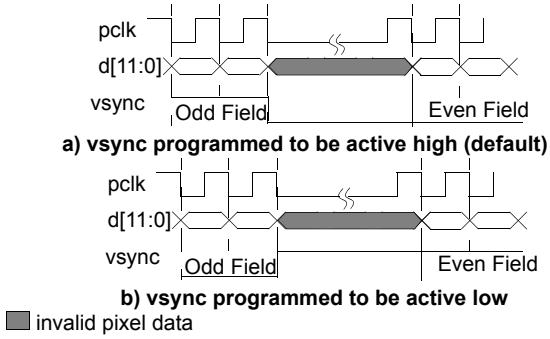


Figure 45. *vsync* in odd/even Mode

Functional Description (continued)

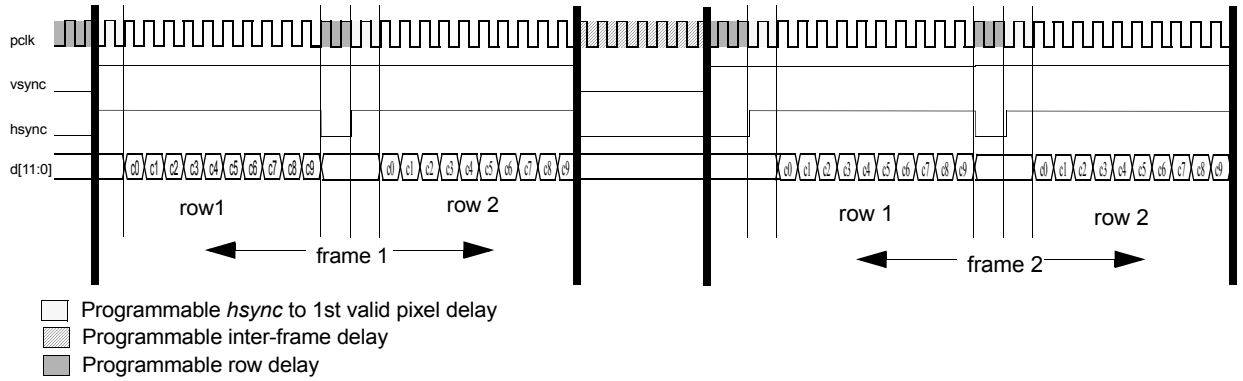


Figure 46. Example of Digital Video Port Timing in Progressive Scan Mode

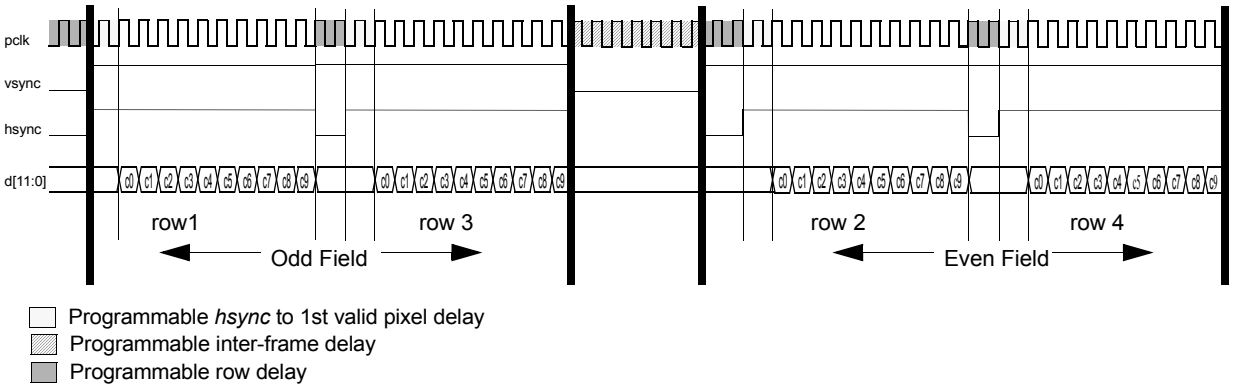


Figure 47. Example of Digital Video Port Timing in Interlaced Mode

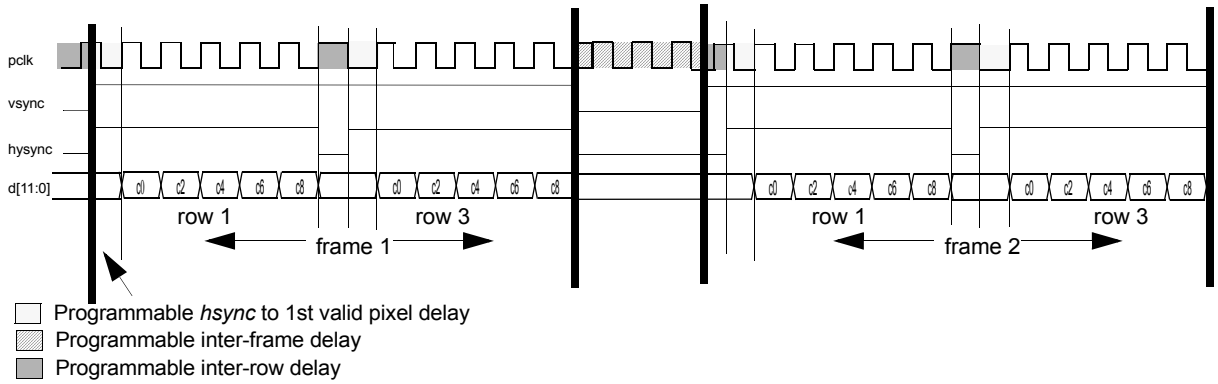


Figure 48. Example of Digital Video Port Timing in 2:1 Sub-sampling Mode

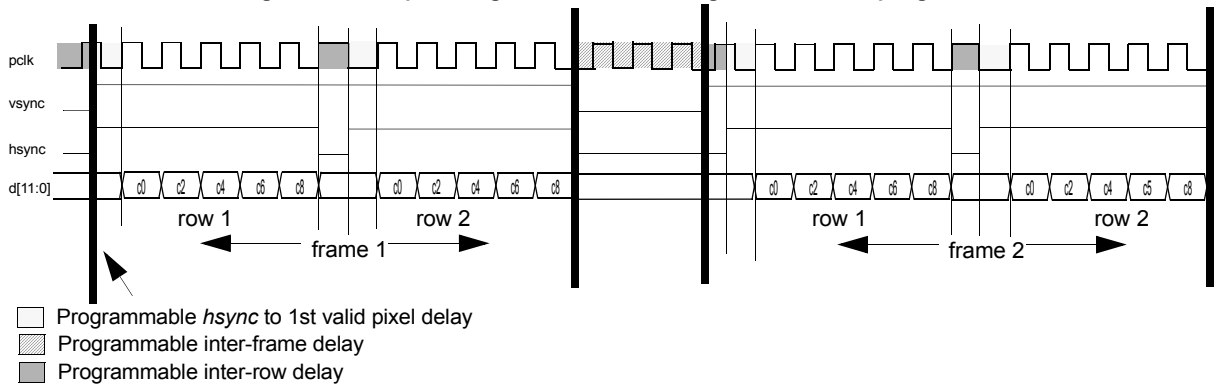


Figure 49. Example of Digital Video Port Timing in 4:2 Sub-sampling Mode

Functional Description (continued)

11.6 Synchronisation Signals in Slave Mode

The sensor's digital video port's synchronisation signals can be programmed to operate in slave mode. In slave mode the integrated timing and control block will only start frame and row processing upon the receipt of triggers from an external source.

Only two synchronization signals are used in slave mode as follows:

hsync is the row trigger input signal.
vsync is the frame trigger input signal.

Figure 50 shows the KAC-9628's digital video port in slave mode connected to a digital video processor master DVP.

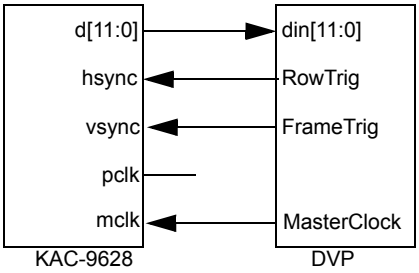


Figure 50. KAC-9628 in slave mode

11.7 Row Trigger Input Pin (hsync)

The row trigger input pin, *hsync*, is used to trigger the processing of a given row. It must be activated for at least two "*mclk*" cycle. The first pixel data will appear at *d[11:0]* "X_{mclk}"periods after the assertion of the row trigger, were X_{mclk} is given by:

$$X_{mclk} = 124 + DW_{StAd}$$

Where:

DW_{StAd} is the value of the display window column start address.

The polarity of the active level of the row trigger is programmable. By default it is active high.

11.8 Frame Trigger Input Pin (vsync)

The frame trigger input pin, *vsync*, is used to reset the row address counter and prepare the array for row processing. It must be activated for at least one "*mclk*" cycle and no more than 96 mclk cycles after the activation of *hsync* as illustrated in Figure 52.

The polarity of the active level of the row trigger is programmable. By default it is active high.

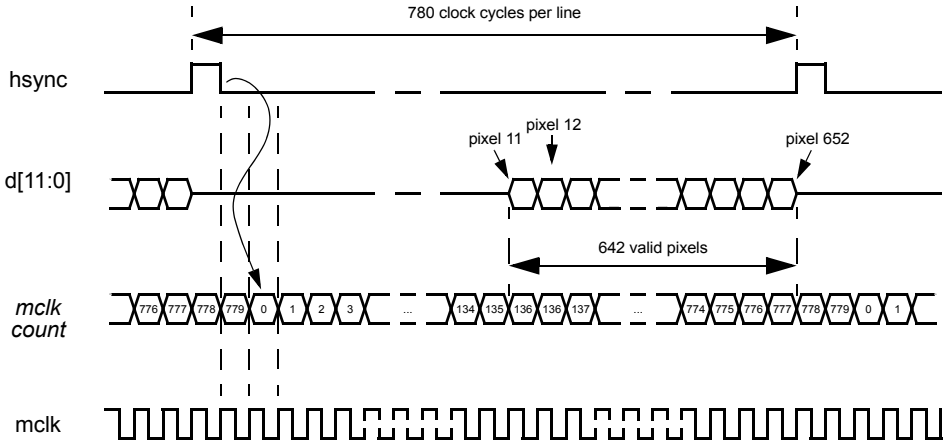


Figure 51. hsync slave mode timing diagram for centred display window of 642 pixels

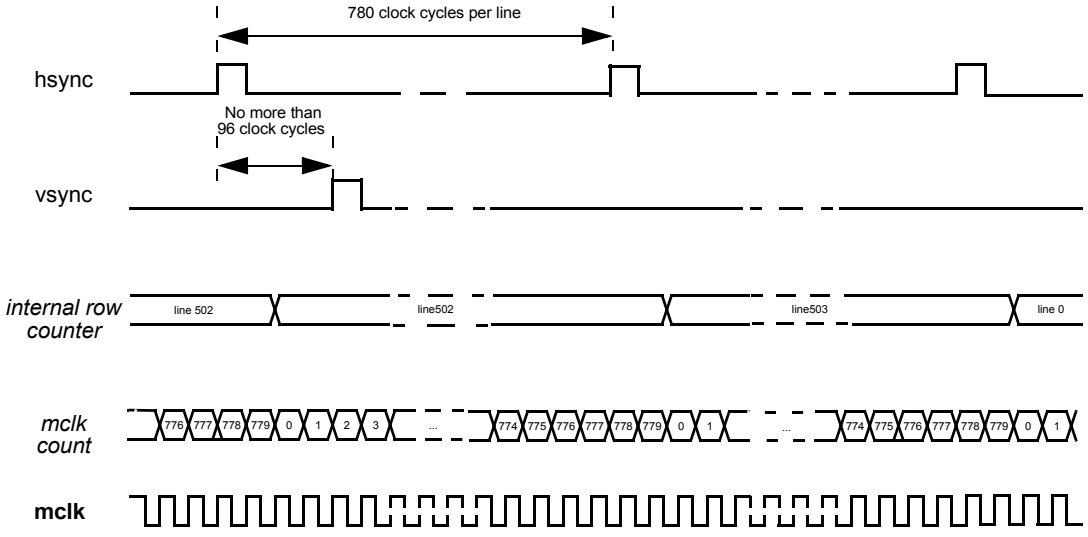


Figure 52. vsync slave mode timing diagram for scan window of 504 rows.

MEMORY MAP

ADDR	Register	Reset Value	Notes	Description
00h	UPDATE	00h		Update Settings Register.
01h	REV	Latest Silicon		Revision Register
02h	MCFG0	00h		Main Configuration Register 0
03h	MCFG1	00h		Main Configuration Register 1
04h	PCR	00h		Power Control Register.
05h	VCLKGEN	04h		Video Clock Generator
06h	VMODE0	00h		Video Mode 0 Register
07h	VMODE1	00h		Video Mode 1 Register
08h	VMODE2	00h		Video Mode 2 Register
09h	SNAPMODE	00h		Snapshot Mode 0 Register
0Ah		00h		Reserved
0Bh	SROWS	00h	note a	Scan Window Row Start Register
0Ch	SROWE	FBh	note a	Scan Window Row End Register
0Dh	SWLSB	00h	note a	Scan Window Mode B LSB Register
0Eh	DROWS	00h		Display Window Row Start Register
0Fh	DROWE	FBh		Display Window Row End Register
10h	DCOLS	00h		Display Window Column Start Register
11h	DCOLE	A5h		Display Window Column End Register
12h	DWLSB	32h		Display Window LSB Register.
13h	ITIMEH	00h	note a	Integration Time High Register
14h	ITIMEL	00h	note a	Integration Time Low Register
15h	RDELAYH	00h	note a	Row Delay High Register
16h	RDELAYL	00h	note a	Row Delay Low Register
17h	FDELAYH	00h	note a	Frame Delay High Register
18h	FDELAYL	00h	note a	Frame Delay Low Register
19h	VGAIN	00h		Video Gain Register
1Ah	BGAIN	00h		Blue Pixels Gain Register
1Bh	GGAIN	00h		Green Pixels Gain Register
1Ch	RGAIN	00h		Red Pixels Gain Register
1Dh	BP1SLOPEH	00h	note a	Break Point 1 Slope High Register
1Eh	BP1SLOPEL	00h	note a	Break Point 1 Slope Low Register
1Fh	BP1LEVA	00h		Break Point 1 Level Register A
20h	BP2SLOPEH	00h	note a	Break Point 2 Slope High Register
21h	BP2SLOPEL	00h	note a	Break Point 2 Slope Low Register
22h	BP1LEVB	00h		Break Point 1 Level Register B

MEMORY MAP (continued)

ADDR	Register	Reset Value	Notes	Description
23h 24h		00h		Reserved for factory use, must be set to 00 Hex.
25h	BP2LEV	00h		Break Point 2 Level Register
26h	BLCOEFF	00h		Black Level Compensation Coefficient Register
27h	BPTH0H	00h		Bad pixel Threshold 0 High Register
28h	BPTH0L	00h		Bad pixel Threshold 0 Low Register
29h	BPTH1H	00h		Bad pixel Threshold 1 High Register
2Ah	BPTH1L	00h		Bad pixel Threshold 1 Low Register
2Bh	OCR	00h		Offset Compensation Register.
3Bh 7Fh				Reserved for future use.

Note a: Programmed setting will only take effect after the *UpdateSettings* bit in the UPDATE register is set

Register Set (continued)

The following section describes all available registers in the KAC-9628 register bank and their function.

Register Name **Settings Update Register**
Mnemonic **UPDATE**
Address **00 Hex**
Type **Read/Write**
Reset Value **00 Hex.**

Bit	Bit Symbol	Description
7:1		Reserved
0	UpdateSettings	Set to inform the integrated timing and control circuit to update the sensor with the new settings. This bit is self resetting. If this bit is set anytime between the start of vertical blanking until 4 rows before the end of the frame the values will take effect in the next frame. If the update bit is set from 3 rows before end of frame until the start of vertical blanking the registers will either take effect in the next frame or the frame after.

Register Name **Device Rev Register**
Mnemonic **REV**
Address **01 Hex**
Type **Read Only.**

Bit	Bit Symbol	Description
7:0	SiRev	The silicon revision register.

Register Name **Main Configuration 0**
Address **02 Hex**
Mnemonic **MCFG0**
Type: **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7	PwrUpBusy	**(Read Only Bit)** Indicates that power on initialization is in progress. The sensor is ready for use when this bit is at logic 0.
6	PwrDown	Set to power down the sensor. Writing a logic 1 to this register bit has the same effect as taking the *pdwn* pin high. Clear (the default) this bit to power up the sensor.
5	BPCorrection	Set to enable the bad pixel detection and correction circuit. Clear (the default) to switch it off.
4	$\overline{\text{BlkLComp}}$	Set to disable the black level compensation circuit. Clear (the default) to switch it on.
3		Reserved
2	BPmode	Set to configure the bad pixel correction circuit to operating in monochrome mode (this should be used with monochorme sensors) Clear the (the default) to set the bad pixel correction circuit to operate in color mode (this should be used with color sensors).
1		Reserved
0	GainMode	Set to route all pixels to the green gain amplifier. Clear (the default) to route the green, green and blue pixels to the green,green and blue amplifiers.

Register Set (continued)

Register Name **Main Configuration 1**
Address **03 Hex**
Mnemonic **MCFG1**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7	ColorMode	Set when using a monochrome sensor. When this bit is at a logic 1, Sub-Sampling is set to 2:1 and every other row is read out during interlace readout-mode. Clear (the default) when using a color sensor. When this bit is at logic 0, sub-sampling is set to 4:2 and every other row pair is read out during interlace mode.
6	ScanMode	Set to configure the sensor to operate in interlace readout mode. Clear (the default) to set the sensor to operate in progressive scan read out mode.
5	HSubSamEn	Set to enable horizontal sub-sampling. Clear (the default) to disable horizontal sub-sampling. NOTE: When horizontal sub-sampling is enabled Pclk is divided by 2. The Hsync active time is the same in both sub-sampled and non sub-sampled mode. Therefore frame rate does not increase with horizontal sub-sampling.
4	VSubSamEn	Assert to enable vertical sub-sampling. Clear (the default) to disable vertical sub-sampling.
3		Reserved
2	SlaveMode	Use to configure the digital video port's synchronisation signal to operate in slave mode. By default the digital video's port's synchronization signals are configured to operate in master mode.
1:0		Reserved

Register Name **Power Control Register 1**
Address **04 Hex**
Mnemonic **PCR**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7:4		Reserved
3	PwdnPGA	Assert to power down the programmable video gain amplifier. Clear (the default) to power up the video gain amplifiers.
2:1	PwdnGA [1:0]	Assert (11) to power down the programmable color gain amplifiers. Clear (00, the default) to power up the analog gain amplifiers.
0	PwDnADC	Assert to power down the 12 bit analog to digital convertor. Clear (the default) to power up the 12 bit analog to digital convertor.

Register Name **Hclk Generator Register**
Address **05 Hex**
Mnemonic **VCLKGEN**
Type **Read/Write**
Reset Value **04 Hex.**

Bit	Bit Symbol	Description
7:6	PumpClkGen	Use to divide the frequency of the sensors master clock input, *mclk* to generate the internal charge pump clock, *PumpClk* as shown in the table below. 00 *PumpClk = mclk* 01 *PumpClk = mclk/2* 10 *PumpClk = mclk/4* 11 *PumpClk = mclk/8*
5		Reserved
4:0	HclkGen	Use to divide the frequency of the sensors master clock input, *mclk* to generate the internal sensor clock, *Hclk*. Program 00 Hex (the default) for *Hclk* to equal *mclk* or divide *mclk* by any number between 1 and 31.

Register Set (continued)

Register Name Digital Video Mode 0
Address 06 Hex
Mnemonic VMODE0
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6	PixDataSel	Use to program the number of active bits on the digital video bus *d[11:0]*, starting from the MSB (*d[11]*). Inactive bits are tri-stated.: 00 — 12 bit mode, bits *d[11:0]* of the digital video bus are active. This is the default. 01 — 10 bit mode, bits *d[11:2]* of the digital video bus are active. 10 — 8 bit mode, bits *d[11:4]* of the digital video bus are active. 11 — Reserved.
5:4	PixDataMsb	Use to program the routing of the MSB output of the internal video A/D to a bit on the digital video bus. 00 — A/D [11:0] -> d[11:0]. 01 — A/D [10:0] -> d[11:1] 10 — A/D [9:0] -> d[11:2] 11 — A/D [8:0] -> d[11:3]
3:0		Reserved

Register Name Digital Video Mode 1
Address 07 Hex
Mnemonic VMODE1
Type Read/Write
Reset Value 00 Hext

Bit	Bit Symbol	Description
7	PixClkMode	Assert to set the *pclk* to “data ready mode”. Clear, the default, to set *pclk* to “*free running mode*”.
6	VsyncMode	Assert to set the *vsync* pin to “pulse mode”. Clear (the default) to set the *vsync* signal to “level mode”.
5	HsyncMode	Assert to force the *hsync* signal to pulse for a minimum of four pixel clocks at the end of each row. Clear (the default) to force the *hsync* signal to a level indicating valid data within a row.
4	PixClkPol	Assert to set the active edge of the pixel clock to negative. Clear (the default) to set the active edge of the clock to positive.
3	VsynPol	Assert to force the *vsync* signal to generate a logic 0 during a frame readout *(Level Mode),* or a negative pulse at the end of a frame readout *(Pulse Mode)*. Clear (the default) to force the *vsync* signal to generate a logic 1 during a frame readout *(Level Mode),* or a negative pulse at the end of a frame readout *(Pulse Mode)*.
2	HsynPol	Assert to force the *hsync* signal to generate a logic 0 during a row readout *(Level Mode),* or a negative pulse at the end of a row readout *(Pulse Mode)*. Clear (the default) to force the *hsync* signal to generate a logic 1 during a row readout *(Level Mode),* or a negative pulse at the end of a readout *(Pulse Mode)*.
1	OddEvenEn	Assert to force the *vsync* pin to act as an odd/even field indicator. Clear (the default) to force the *vsync* pin to act as a vertical synchronization signal.
0	TriState	Assert to tri-state all output signals (data and control) on the digital video port. Clear (default) to enable all signals (data and control) on the digital video port.

Register Set (continued)

Register Name Digital Video Mode 2
Address 08 Hex
Mnemonic VMODE2
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4	HsyncAdjust	Use to program the leading edge of *hsync* to the first valid pixel at the beginning of each row. This can be 0-hex to F-hex corresponding to 0 - 15 pixel clocks. Default 0.
3:0		Reserved

Register Name Snapshot Mode Configuration Register
Address 09 Hex
Mnemonic SNAPMODE
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6	SsFrames	Program to set the number of frames required before readout during a snapshot with no external shutter, (see Figure 26). By default these two bits are set to 00. Set to any value but 00 for snapshot to function properly..: 00 Reserved 01 one frame 10 two frames 11 three frames
5	ShutterMode	Assert to indicate that an external shutter will be used during snapshot mode. Clear (the default) to indicate that snapshot mode will be carried out without the aid of an external shutter.
4	ExtSynPol	Assert to set the active level of the *extsync* signal to 0. Clear (the default) to set the active level of the *extsync* signal to 1.
3		Reserved
2	SnapshotMod	Assert to set the *snapshot* pin to level mode. In level mode the sensor will continually run snapshot sequences as long as the *snapshot* pin is held to the active level. Clear (the default) to set the *snapshot* signal to pulse mode. In pulse mode the sensor will only carry out one snapshot sequence per pulse applied to the *snapshot* pin.
1	SnapShotPol	Assert to set the snapshot pin to be active on the positive edge. Clear (the default) to set the snapshot pin to be active on the negative edge.
0	SnapEnable	Set to enable the external *snapshot* pin. Clear (the default) to disable the external *snapshot* pin.

Register Name Scan Window Row Start Register
Address 0B Hex
Mnemonic SROWS
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	SwStartRow [8:1]	Use to program the scan window's start row address MSBs. If bit 6 of register DWLSB is set to 1 the start row address is incremented by 1 else the raw value is used.

Register Name Scan Window Row End Register
Address 0C Hex
Mnemonic SROWE
Type Read/Write
Reset Value FB Hex

Bit	Bit Symbol	Description
7:0	SwEndRow [8:1]	Use to program the scan window's end row address MSBs. If bit 6 of register DWLSB is set to 1 the end row address is incremented by 1. else the raw value is used.

Register Name Scan Window Mode B LSB Register
Address 0DHex
Mnemonic SWLSB
Type Read/Write
Reset Value 00 Hexx

Bit	Bit Symbol	Description
7	SwMode	Use to program the scan window's addressing mode. Set to a logic one for mode b and a logic 0 for mode a.
6:2		Reserved
1	SwEndRow [0]	Use to program bit 0 of the scan window's end row address.
0	SwStartRow [0]	Use to program bit 0 of the scan window's start row address.

Register Name Display Window Row Start Register
Address 0E Hex
Mnemonic DROWS
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	DwStartRow	Use to program the display window's start row address MSBs. The LSB can be programmed using the DWLSB register.

Register Name Display Row End Register
Address 0F Hex
Mnemonic DROWE
Type Read/Write
Reset Value FB Hex

Bit	Bit Symbol	Description
7:0	DwEndRow	Use to program the display window's end row address. The LSB can be programmed using the DWLSB register.

Register Set (continued)

Register Name Display Window Column Start Register
Address 10 Hex
Mnemonic DCOLS
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	DwStartCol	Use to program the display window's start column address MSBs. The two LSBs can be programmed using the DWLSB register.

Register Name Display Window Column End Register
Address 11 Hex
Mnemonic DCOLE
Type Read/Write
Reset Value A5 Hex

Bit	Bit Symbol	Description
7:0	DwEndCol	Use to program the display window's end column address MSBs. The two LSBs can be programmed using the DWLSB register.

Register Name Display Window LSB register
Address 12 Hex
Mnemonic DWLSB
Type Read/Write
Reset Value 32 Hex

Bit	Bit Symbol	Description
7		Reserved
6	SwLsb	Assert to increment the value of the scan window start and end row addresses by 1. Clear (the default) to use the raw values.
5	DwCel[1]	Use to program bit 1 of the display window's end column address. Default is 1.
4	DwCel[0]	Use to program bit 0 of the display window's end column address. Default is 1.
3	DwCSL[1]	Use to program bit 1 of the display window's start column address. Default is 0.
2	DwCSL [0]	Use to program bit 0 of the display window's start column address. Default is 0.
1	DwERLsb	Use to program bit 0 of the display window's end row address. Default is 1.
0	DwSRLsb	Use to program bit 0 of the display window's start row address. Default is 0.

Register Name Integration Time High Register
Address 13 Hex
Mnemonic ITIMEH
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:4		Reserved
3:0	Itime[11:8]	Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset.

Register Name Integration Time Low Register
Address 14 Hex
Mnemonic ITIMEL
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	Itime[7:0]	Program to set the integration time of the array. The value programmed in the register is the number of rows ahead of the selected row to be reset.

Register Name Row Delay High Register
Address 15 Hex
Mnemonic RDELAYH
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:3		Reserved
2:0	Rdelay[10:8]	Use to program the MSBs of the row delay.

Register Name Row Delay Low Register
Address 16 Hex
Mnemonic RDELAYL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Rdelay[7:0]	Use to program the LSBs of the row delay.

Register Name Frame Delay High Register
Address 17
Mnemonic FDELAYH
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4		Reserved
3:0	FDelay[11:8]	Use to program the MSBs of the frame delay.

Register Set (continued)

Register Name Frame Delay Low Register
Address 18 Hex
Mnemonic FDELAYL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	FDelay [7:0]	Use to program the LSBs of the frame delay.

Register Name Video Gain Register
Address 19 Hex
Mnemonic VGAIN
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	VidGain	Use to program the overall video gain. 00hex corresponds to a gain of 0dB while 3Fhex corresponds to a gain of 15dB. Steps are in log-arithmic increments.

Register Name Blue Pixels Gain Register
Address 1A Hex
Mnemonic BGAIN
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	BlueGain	Use to program the gain of green pixels. 00hex corresponds to a gain of 0dB while 7Fhex corre-sponds to a gain of 14dB. Steps are in linear increments.

Register Name Green Pixels Gain Register
Address 1B Hex
Mnemonic GGAIN
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	GreenGain	Use to program the gain of green pixels. 00hex corresponds to a gain of 0dB while 7Fhex corre-sponds to a gain of 14dB. Steps are in linear increments.

Register Name Red Pixels Gain Register
Address 1C Hex
Mnemonic RGAIN
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	RedGain	Use to program the gain of red pixels. 00hex corresponds to a gain of 0dB while 7Fhex corre-sponds to a gain of 14dB. Steps are in linear increments.

Register Name Break Point 1 Slope High Register
Address 1D Hex
Mnemonic BP1SLOPEH
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:6		Reserved
5:0	Bp1Slope[13:8]	This register allows the slope of the curve up to the first breakpoint (slope 0 in figure 24) to be programed. When the high and low registers are cleared no breakpoint will result.

Register Name Break Point 1 Slope Low Register
Address 1E Hex
Mnemonic BP1SLOPEL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Bp1Slope[7:0]	This register allows the slope of the curve up to the first breakpoint (slope 0 in figure 24) to be programed. When the high and low registers are cleared no breakpoint will result.

Register Name Break Point 3 Level Register
Address 1F Hex
Mnemonic BP1LEVA
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Bp1LevelA	This register defines the level at which the first breakpoint is applied (break point 1 in figure 24). Note *Bp1LevelB* (register BP1LEVB) must be pro-grammed to be equal to *Bp1LevelA*

Register Name Break Point 2 Slope High Register
Address 20 Hex
Mnemonic BP2SLOPEH
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:0	Bp2Slope[13:8]	This register allows the slope of the curve to the second breakpoint (slope 1 in figure 24) to be programed. When the high and low registers are cleared no breakpoint will result.

Register Set (continued)

Register Name Break Point 2 Slope Low Register
Address 21 Hex
Mnemonic BP2SLOPEL
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Bp2Slope[7:0]	This register allows the slope of the curve to the second break point (slope 1 in figure 24) to be programed. When the high and low registers are cleared no breakpoint will result.

Register Name Break Point 1 Level Register
Address 22 Hex
Mnemonic BP1LEVB
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Bp1LevelB	This register defines the level at which the first breakpoint is applied (break point 1 in figure 24). Note *Bp1LevelA* (register BP1LEVA) must be pro-grammed to be equal to *Bp1LevelB*

Register Name Break Point 2 Level Register
Address 25 Hex
Mnemonic BP2LEV
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	Bp2Level	This register defines the level at which the first breakpoint is applied (break point 2 in figure 24).

Register Name Black Level Compensation Coefficient Register
Address 26 Hex
Mnemonic BLCOEFF
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:6		Reserved
5:3	Clip[2:0]	Use to define the number of MSBs of the incoming black pixels. If set to zero no clipping will occur 000 No Clipping 001 drop d[11], use d[10:0] 010 drop d[11:10], use d[9:0] 011 drop d[11:9], use d[8:0] 100 drop d[11:8], use d[7:0] 101 drop d[11:7], use d[6:0] 110 drop d[11:6], use d[5:0] 111 drop d[11:5], use d[4:0]
2:0	Alpha[2:0]	Exponential averaging coefficient for black pixels. Increasing the value of alpha decreases the rate of convergence of the black level compensation block.

Register Name Bad Pixel Threshold 0 High Register
Address 27 Hex
Mnemonic BPTH0H
Type Read/Write
Reset Value 00 Hex.

Bit	Bit Symbol	Description
7:0	BpT0 [11:4]	Use to program the MSBs of the bad pixel correction threshold 0.

Register Name Bad Pixel Threshold 0 Low Register
Address 28 Hex
Mnemonic BPTH0L
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:4	BpT0 [3.0]	Use to program the LSBs of the bad pixel correction threshold 0.
3:0		Reserved

Register Name Bad Pixel Threshold 1 High Register
Address 29 Hex
Mnemonic BPTH1H
Type Read/Write
Reset Value 00 Hex

Bit	Bit Symbol	Description
7:0	THR1[11.4]	Use to program the MSBs of the bad pixel correction threshold 1.

Register Set (continued)

Register Name **Bad Pixel Threshold 1 Low Register**
Address **2A Hex**
Mnemonic **BPTH1L**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7:4	THR1 [3.0]	Use to program the MSBs of the bad pixel correction threshold 1.
3:0		Reserved

Register Name **Offset Compensation Register**
Address **2BH Hex**
Mnemonic **OCR**
Type **Read/Write**
Reset Value **00 Hex**

Bit	Bit Symbol	Description
7	OffSign	Sign of the Offset value. A logic 0 indicates a positive offset will be added while a logic 1 indicates a negative offset will be added.
6:1	OffMag	Magnitude of the offset to be added or subtracted.
0		Reserved. This bit must be set to a logic 0.

Timing Information

1.0 DIGITAL VIDEO PORT MASTER MODE TIMING

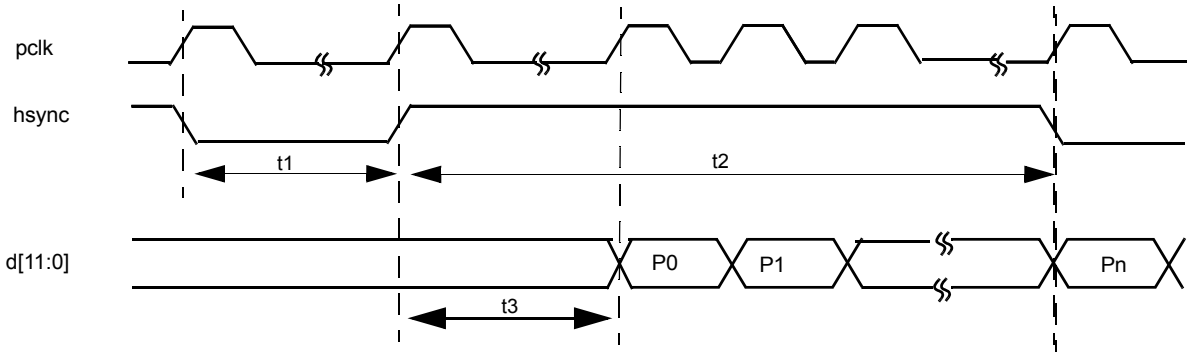


Figure 53. Row Timing Diagram

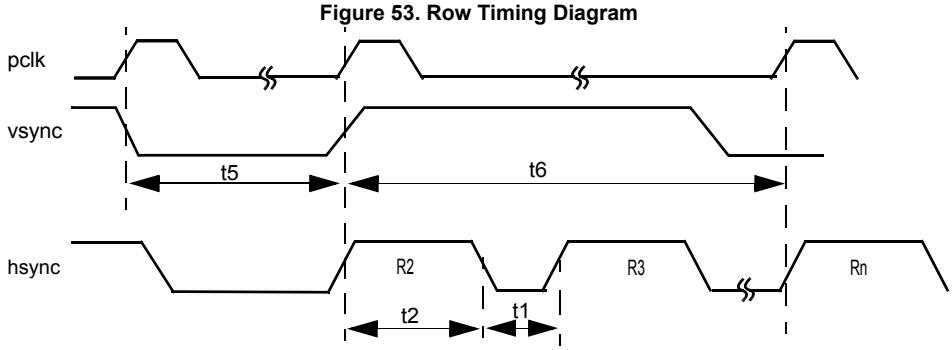


Figure 54. Frame Timing

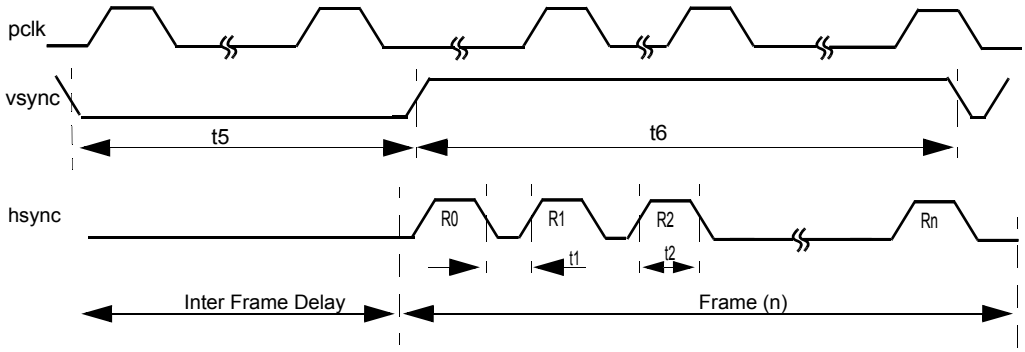


Figure 55. Frame Delay Timing (With Inter Frame Delay).

Label	Descriptions	Min	Typ	Max
t0	pclk period	74.4ns	83.3ns	1.0µs

t1	hsync low level mode pulse mode	(116-*HsyncAdjust* + R_{delay}) *pclk 16 * *pclk*	(see note a)
t2	hsync high level mode pulse mode	(664 -*HsyncAdjust*) **pclk* 764 * *pclk*	(see note a)
t3	first valid pixel data after *hsync* active	*HsyncAdjust* * *pclk*	(see note a)
t5	vsync low level mode pulse mode	(F_{delay} + 116) **pclk* 16 * *pclk*	(see note a)
t6	vsync high level mode pulse mode	(*FN_{Hclk}* - 116 - F_{delay}) * *pclk* 16 * *pclk*	(see note a)

Note a: See *Frame Rate Programming* section for more details

Timing Information (continued)

2.0 DIGITAL VIDEO PORT SLAVE MODE TIMING

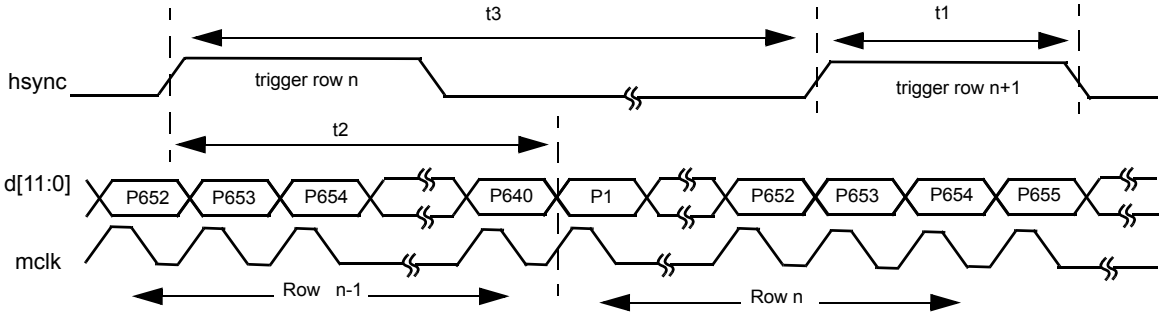


Figure 56. Slave Mode Row Trigger and Readout Timing

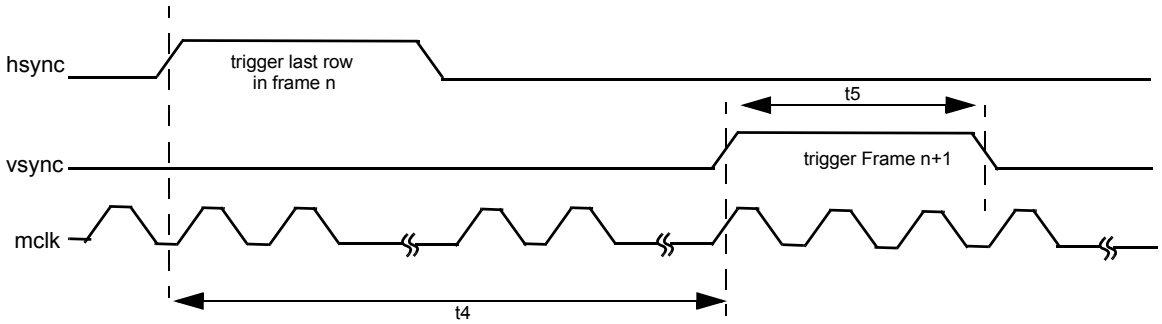


Figure 57. Slave Mode *d[11:0]*, *hsync* & *vsync* to *pclk* Timing

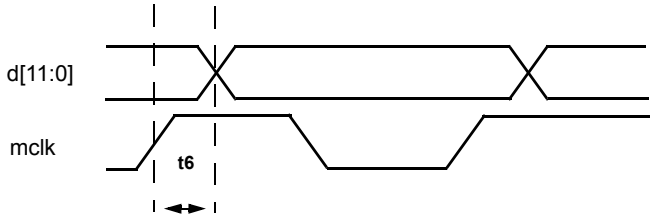


Figure 58. Rising Edge of *mclk* to Valid Pixel Data

The following specifications apply for all supply pins = +3.0V & C_L = 10pF unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

Label	Descriptions	Min	Typ	Max
t1	Pulse width of row trigger	2 * mclk		
t2	First pixel out after rising edge of row trigger	124 * mclk		124 * mclk
t3	Minimum time between row triggers.	780 * mclk		
t4	Max time to assert next frame trigger after last row trigger.			96 * mclk
t5	Pulse width of Frame trigger	2 * mclk		
t6	Time to valid pixel data after rising edge of mclk		44ns	

Timing Information (continued)

3.0 DIGITAL VIDEO PORT SINGLE FRAME CAPTURE (SNAPSHOT MODE) TIMING

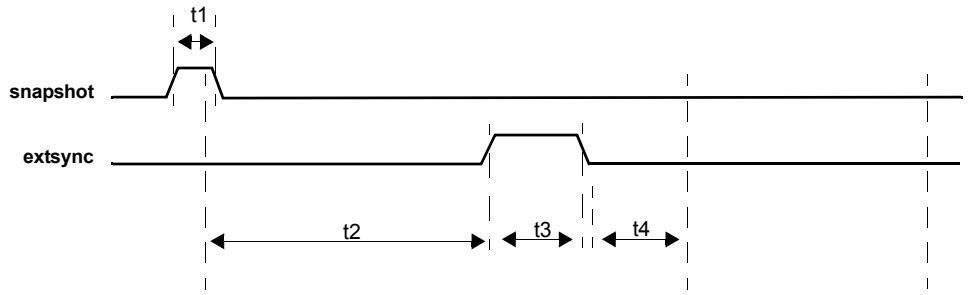


Figure 59. Snapshot Mode Timing With External Shutter

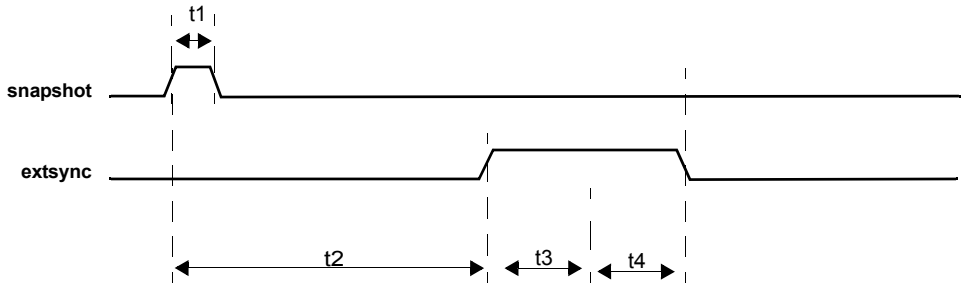


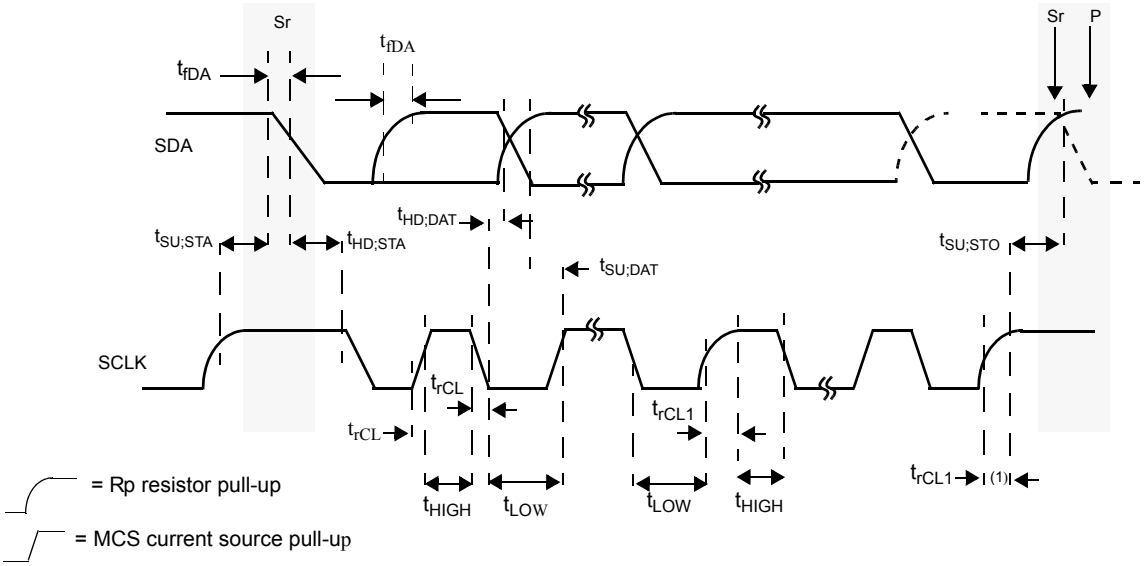
Figure 60. Snapshot Timing Without External Shutter

Label	Descriptions	Equation
t1	Minimum Snapshot Trigger Pulse Width	2 * *mclk* (see notes a & b)
t2	Minimum time from Snapshot Pulse to *extsync*	FN_{Hclk} (see notes a & b)
t3	Array Integration Time	FN_{Hclk} (see notes a & b)
t4	Pixel Read Out	FN_{Hclk} (see notes a & b)

Note a: See 5.0*Frame Rate Programming* section for more details
Note b: See *Snapshot Mode* for more details

Timing Information (continued)

4.0 SERIAL BUS TIMING



(1) Rising edge of the first SCLK pulse after an acknowledge bit.

Figure 61. I²C Compatible Serial Bus Timing.

The following specifications apply for all supply pins = +3.3V, C_L = 10pF, and *sclk* = 400KHz unless otherwise noted. **Boldface limits apply for TA = T_{MIN} to T_{MAX}:** all other limits T_A = 25°C (Note 7)

PARAMETER	SYMBOL	MIN	MAX	UNIT
sclk clock frequency	f_{SCLH}	0	400	KHz
Set-up time (repeated) START condition	$t_{SU;STA}$	0.6	-	µS
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	-	µS
LOW period of the *sclk* clock	t_{LOW}	1.3	-	µS
HIGH period of the *sclk* clock	t_{HIGH}	0.6	-	µS
Data set-up time	$t_{SU;DAT}$	180	-	nS
Data hold time	$t_{HD;DAT}$	0	0.9	µS
Set-up time for STOP condition	$t_{SU;STO}$	0.6		µS
Capacitive load for *sda* and *sclk* lines	C_b		400	pF

Package Information