Green-Mode PWM Controller with HV Start-Up Circuit and OTP Protection

Rev.00

General Description

The LD7578 integrates several functions of protections in a SOP-8 package. It minimizes the component counts and the circuit space.

The device provides functions of low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. Also, the LD7578 features more protections like OLP (Over Load Protection), OVP (Over Voltage Protection), and external OTP (Over Temperature Protection) to prevent the circuit from being damaged under abnormal conditions.

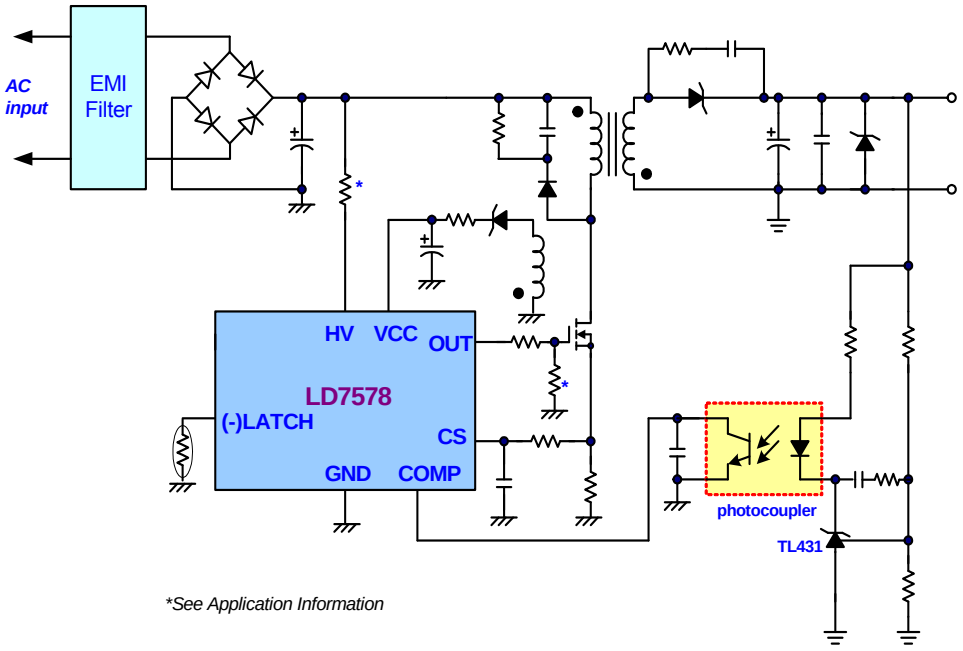
Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Non-Audible-Noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc
- OLP (Over Load Protection)
- OTP through a NTC/Latch-Off Mode
- 500mA Driving Capability

Applications

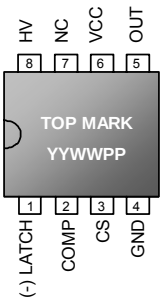
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

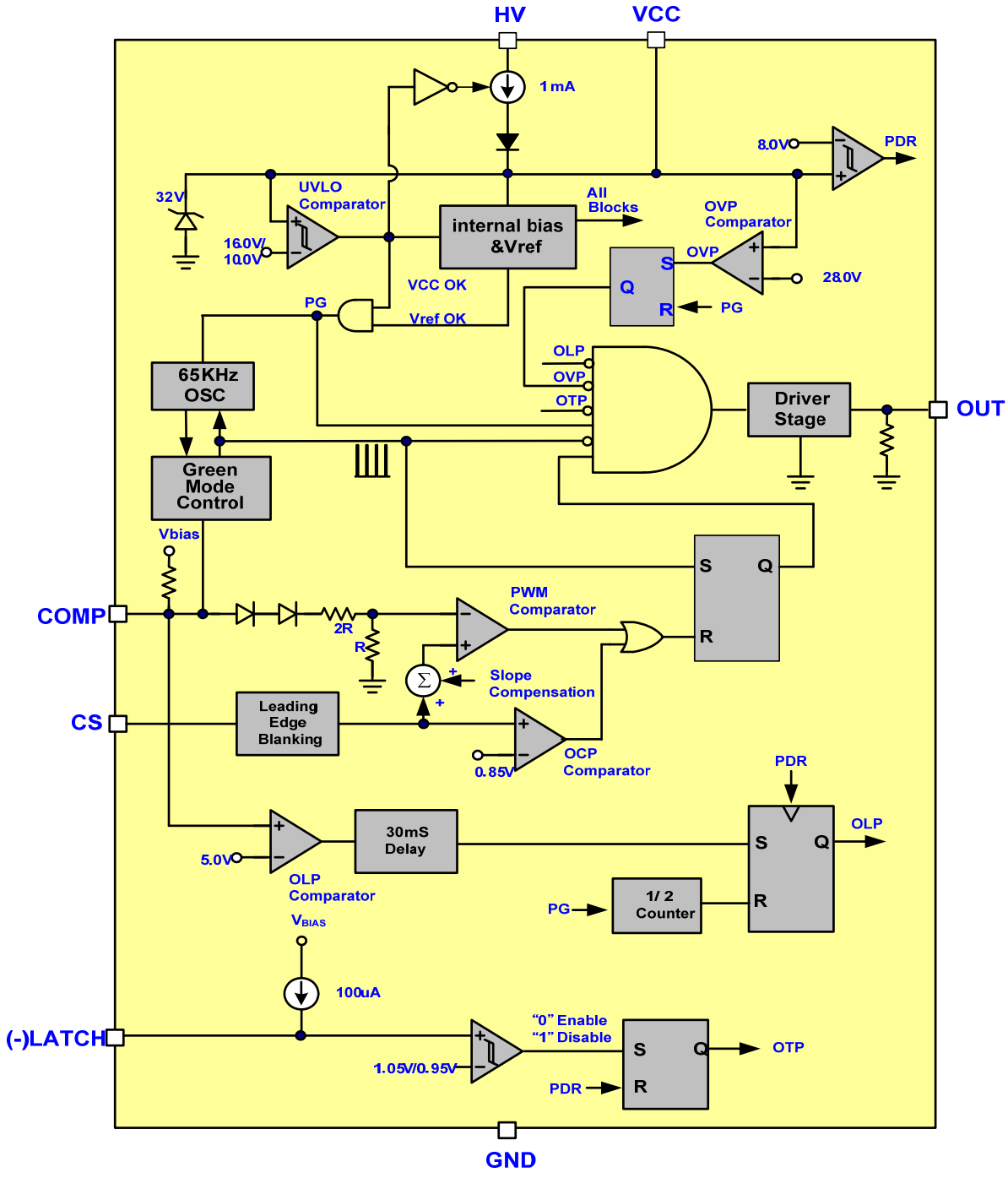
Part number	Package		Top Mark	Shipping
LD7578 GS	SOP-8	Green package	LD7578GS	2500 /tape & reel
LD7578 GN	DIP-8	Green package	LD7578GN	3600 /tube /Carton

The LD7578 is ROHS compliant/ Green Package.

Pin Descriptions

PIN	NAME	FUNCTION
1	(-) LATCH	Pulling this pin below 0.95V will shutdown the controller and enter latch mode unless AC power-on recycles. By connecting a NTC from this pin to ground, it will achieve the OTP protection function. Keep this pin float to disable the latch protection function.
2	COMP	Voltage feedback pin. By connecting a photo-coupler to close the control loop, it can achieve the regulation.
3	CS	Current sense pin, for sensing the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to positive terminal of bulk capacitor to provide the startup current for the controller. When VCC voltage trips UVLO(on), this HV loop will be turned off to save the power loss of the startup circuit.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
High-Voltage Pin, HV	-0.3V~500V
COMP, (-)LATCH, CS	-0.3 ~7V
Junction Temperature	150°C
Operating Ambient Temperature	-20°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model	250V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	Vcc< UVLO(on), HV=500V	0.5	1.0	1.5	mA
Off-State Leakage Current	Vcc> UVLO(off), HV=500V		8.9	35	μA
Supply Voltage (Vcc Pin)					
Startup Current			320		μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		3.3	3.8	mA
	V_{COMP}=3V		3.3	3.8	mA
	OLP tripped		0.78		mA
	OVP tripped		0.88		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		26.5	28.0	29.5	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		1.5	2.2	mA
Open Loop Voltage	COMP pin open		6.0		V
Green Mode Threshold VCOMP			2.35		V
Burst Mode Threshold VCOMP			1.4		V
Current Sensing (CS Pin)					
Maximum Input Voltage		0.80	0.85	0.90	V
Leading Edge Blanking Time	COMP>1.9V		250		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency		60	65	70	KHz
Green Mode Frequency			22		KHz
Temp. Stability	(-40°C ~105°C)			5	%
Voltage Stability	(VCC=11V-25V)			1	%

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Latch Protection ((-)LATCH Pin)					
(-)LATCH Pin Source Current		92	100	108	μA
Turn-On Trip Level		1.00	1.05	1.10	V
Turn-Off Trip Level		0.90	0.95	1.00	V
De-latch Vcc Level	(PDR, Power Down Reset)	7.2	8.0	8.8	V
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	9			V
Rising Time	Load Capacitance=1000pF		100		nS
Falling Time	Load Capacitance=1000pF		30		nS
OLP (Over Load Protection)					
OLP Trip Level			5.0		V
OLP Delay Time	FS=65KHz		30		mS

Typical Performance Characteristics

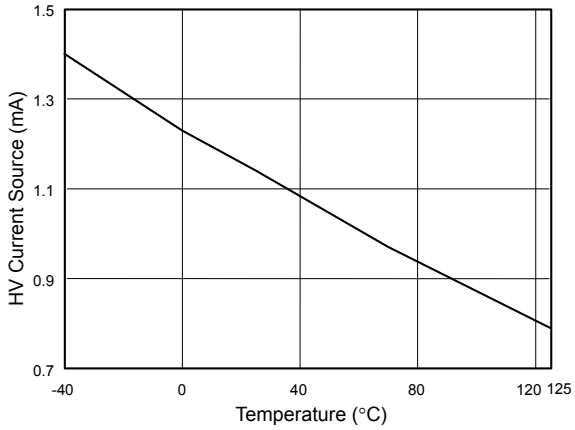


Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

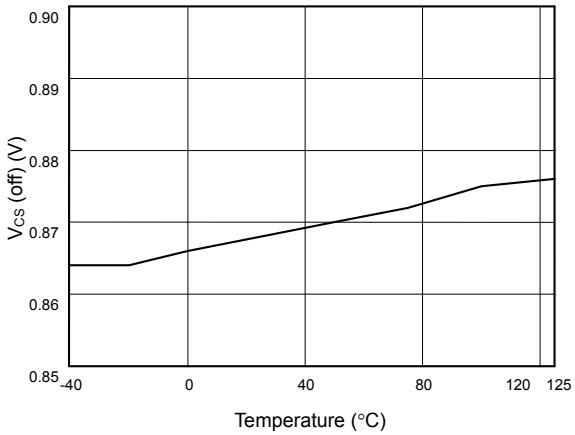


Fig. 2 V_{CS} (off) vs. Temperature

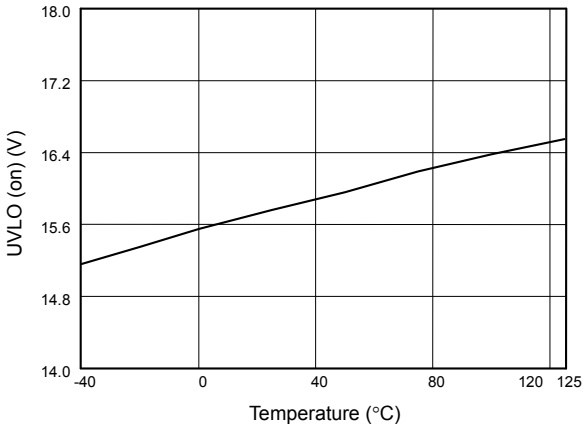


Fig. 3 UVLO (on) vs. Temperature

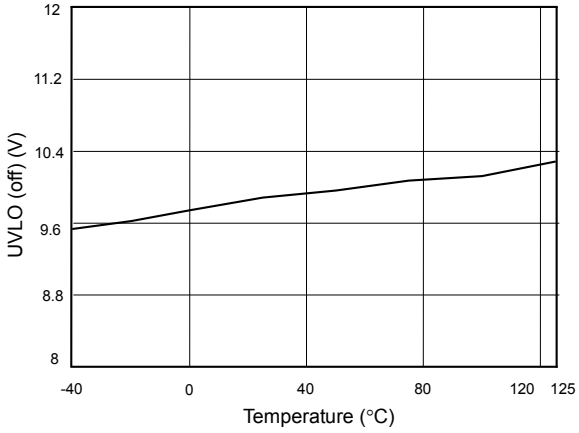


Fig. 4 UVLO (off) vs. Temperature

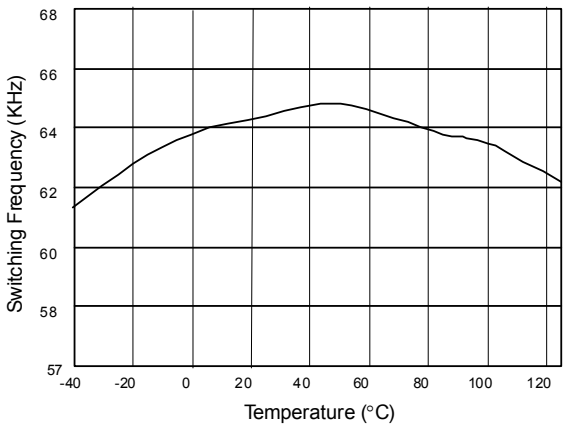


Fig. 5 TC of Switching Frequency

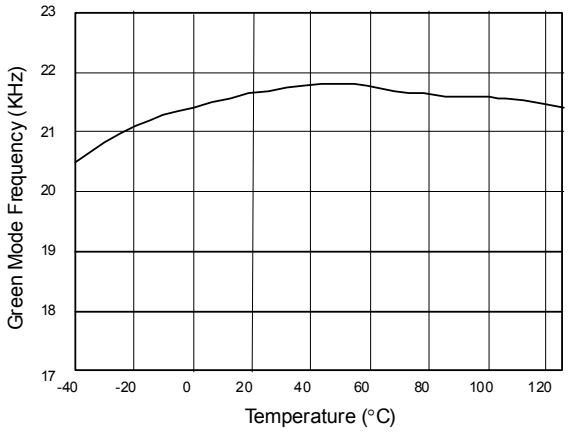


Fig. 6 TC of Green Mode frequency

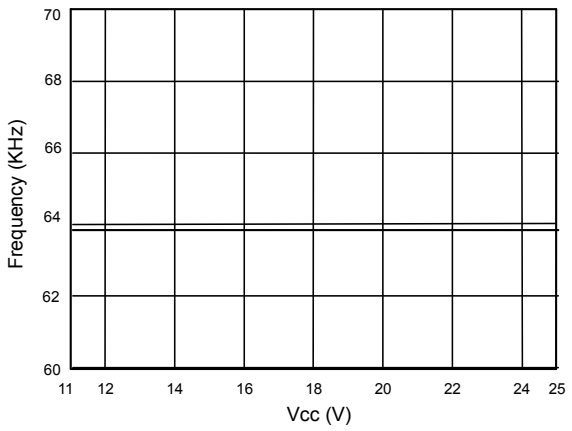


Fig. 7 Frequency vs. Vcc

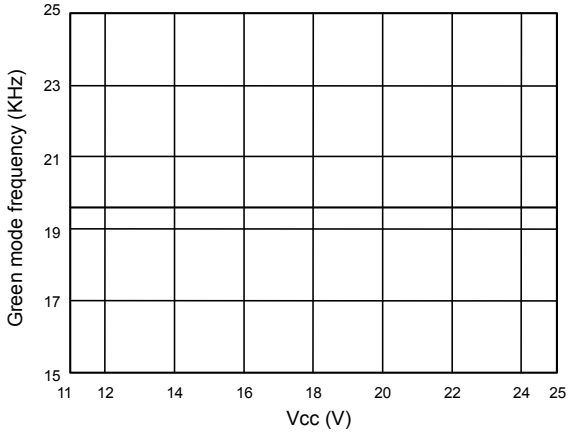


Fig. 8 Green mode frequency vs. Vcc

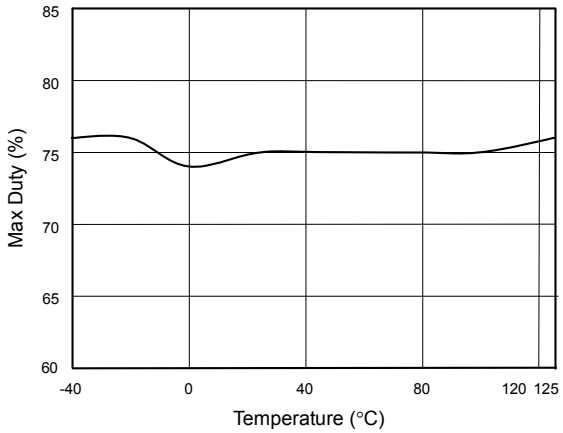


Fig. 9 Max Duty vs. Temperature

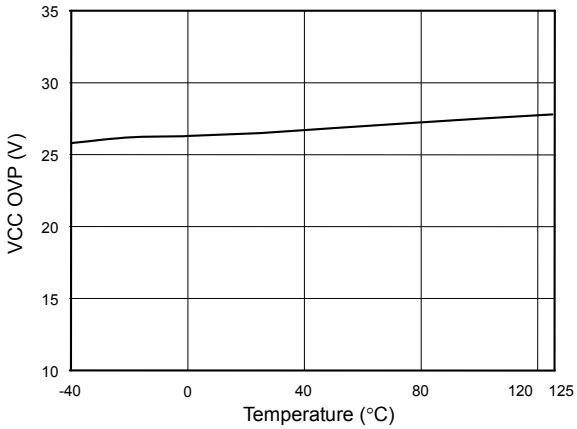


Fig. 10 VCC OVP vs. Temperature

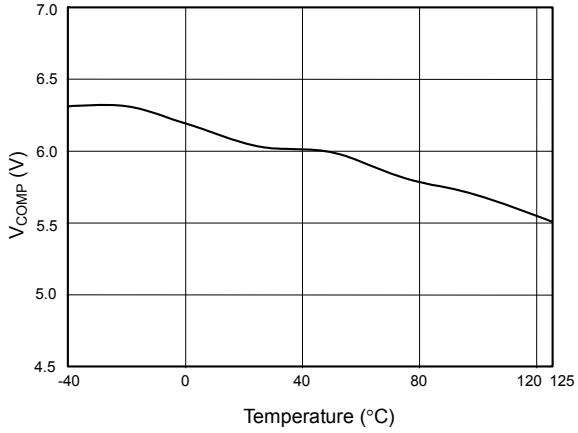


Fig. 11 V_{COMP} open loop voltage vs. Temperature

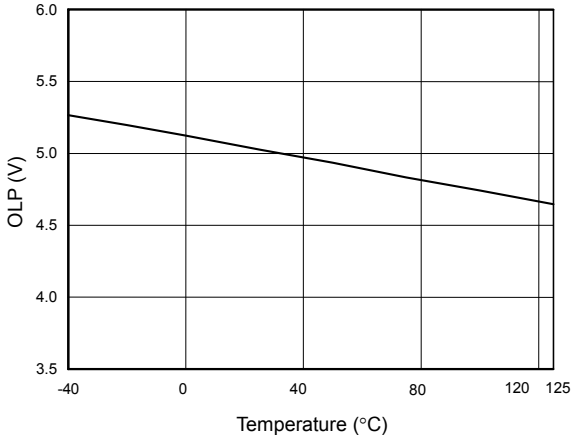


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is becoming more and more important for switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation forces the PWM controllers to powerfully integrate more functions, thereby reducing the external part count. The LD7578 is ideal for these applications to provide an easy and cost effective solution; and its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

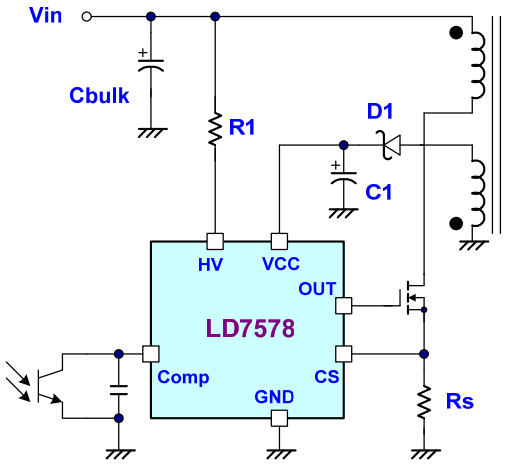


Fig. 13

Traditional circuits power on the PWM controller through a startup resistor to constantly provide current from a rectified voltage to the capacitor connected to Vcc pin. Nevertheless, this startup resistor was usually of larger resistance, and it therefore required more power and longer time to start up.

To achieve the optimized topology, as shown in figure 13, The LD7578 is built in with high voltage startup circuit to optimize the power saving. During the startup sequence, a high-voltage current source sinks current from C_{BULK} capacitor to provide the startup current as well as to charge the Vcc capacitor C1. During the initialization of the startup, Vcc voltage is lower than the UVLO(off) threshold thus the current source is on to supply a current of 1mA. Meanwhile, the Vcc current consumed by the LD7578 is as low as 320μA thus most of the HV current is utilized to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost the same no matter whether operation condition is under low-line or high-line.

When Vcc voltage reaches UVLO(on) threshold, the LD7578 is powered on to start issuing the gate drive signal, the high-voltage current source is then disabled, and the Vcc supply current will be only provided from the auxiliary winding of the transformer. Therefore, the power losses on the startup circuit beyond the startup period can be eliminated and the power saving can be easily achieved. In general application, a 39KΩ resistor is still recommended to be placed in high voltage path to limit the current if there is a negative voltage applying in any case.

An UVLO comparator is included to detect the voltage on the V_{CC} pin to ensure the supply voltage is high enough to power on the LD7578 PWM controller and to drive the power MOSFET. As shown in Fig. 14, a Hysteresis is provided to prevent shutdown caused by the voltage dip during startup. The turn-on and turn-off threshold levels are set at 16V and 10.0V, respectively.

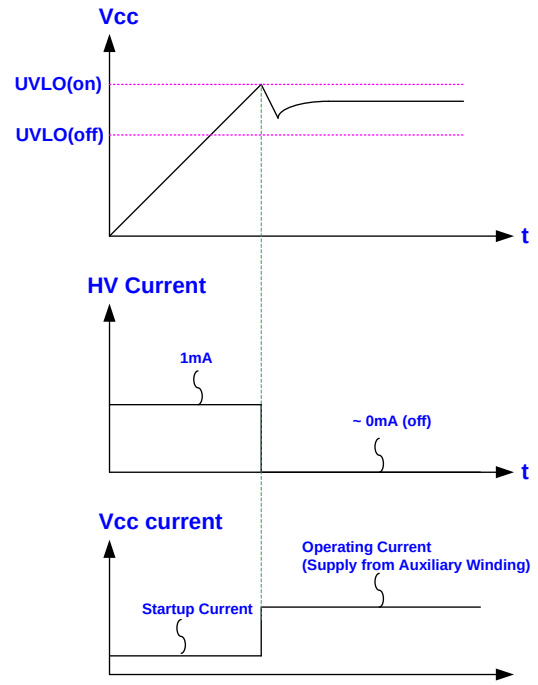


Fig. 14

Current Sensing, Leading-edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feeds back both current signal and voltage signal to close the control loop and to achieve voltage regulation. LD7578 detects the primary MOSFET current from the CS pin, which is applied not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 250nS leading-edge blanking (LEB) time is incorporated in the input of CS pin to prevent the false-trigger caused by any current spike. For low power applications, if the total pulse width of each turn-on spike is less than 250nS and the negative spike on the CS pin is not as low as -0.3V, the R-C filter (as shown in Fig.15) can be eliminated. Nevertheless, it is strongly recommended to remain a small R-C filter (as shown in Fig. 16) for higher power applications to avoid the CS pin being damaged by negative turn-on spikes.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. The maximum duty-cycle of the LD7578 is limited to 75% in order to avoid the transformer flux saturation.

Voltage Feedback Loop

The voltage feedback signal is issued from the TL431 in the secondary side through the photo-coupler to COMP pin of the LD7578. The input stage of the LD7578, like the UC384X, is incorporated with 2 diodes voltage offset circuit and a voltage divider with 1/3 ratio. Therefore,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally, eliminating external corresponding components on a board.

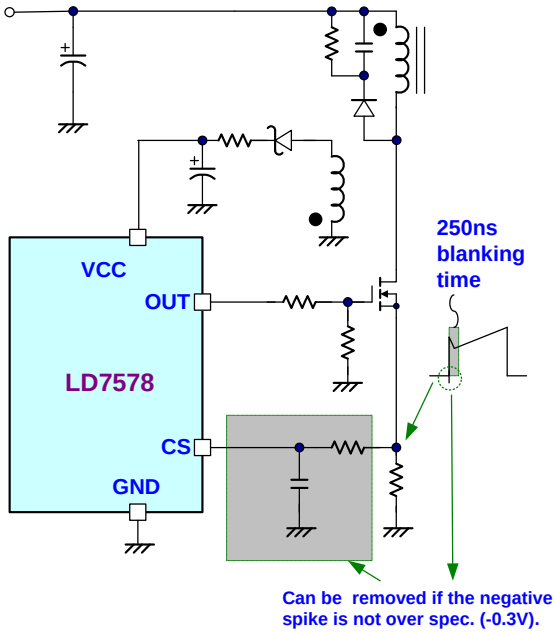


Fig. 15

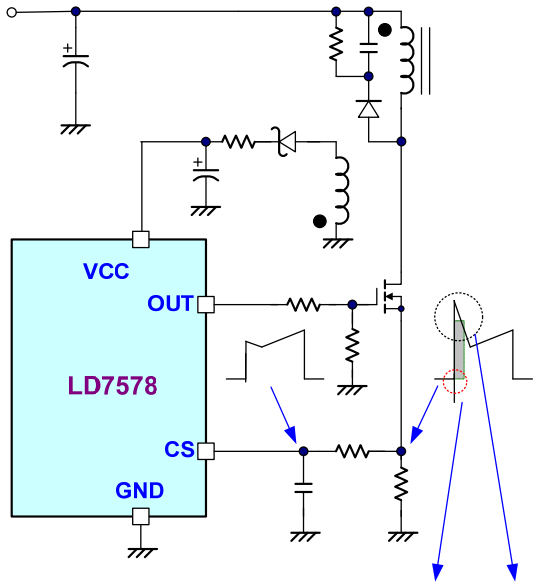


Fig. 16

Oscillator and Switching Frequency

The switching frequency of the LD7578 is fixed as 65KHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

Stability is crucial for current mode control when it operates at more than 50% of duty-cycle. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In the LD7578, the internal slope compensation circuit has been implemented to simplify the external circuit design.

On/Off Control

Pulling COMP pin below 1.2V will turn off the LD7578 and disable the gate output pin of the LD7578. The off-mode will be released when the pull-low signal at COMP pin is removed.

Dual-Oscillator Green-Mode Operation

Lots of topologies have been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or by reducing the switching frequency.

What the LD7578 uses to implement the power-saving operation is Leadtrend Technology’s own IP. By using this dual-oscillator control, the burst -mode frequency can be well controlled and further to avoid the generation of audible noise.

Over Load Protection (OLP)

To protect the circuit from being damaged under over load condition or short condition, a smart OLP function is built in with the LD7578, as shown in Figure 17 shows the waveforms of the OLP operation. If output voltage drops, the feedback system tends to force the voltage loop toward the saturation (6V) and then pulls the voltage of COMP pin to high. Whenever the V_{COMP} trips to the OLP threshold 5.0V and continues over 30mS, OLP is activated and then turns off the gate output to stop the switching of power circuit. The 30mS delay time is to prevent the false trigger from the power-on and turn-off transient.

A divide-2 counter is implemented to reduce the input average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-2 counter starts to count the number of UVLO(off). The latch is released if the 2nd UVLO(off) point is counted then the power circuit is recovered to switch again.

By using such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within the safe operating area.

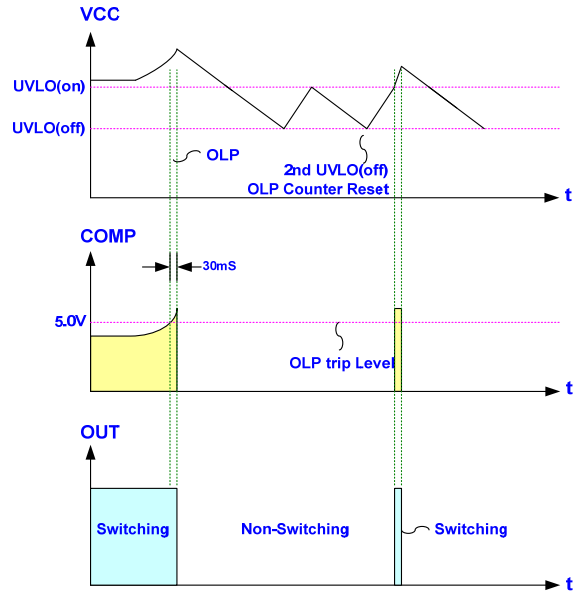


Fig. 17

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 30V maximum. To prevent the V_{GS} from fault condition, the LD7578 is implemented with over-voltage protection on Vcc. After the Vcc voltage is higher than OVP threshold voltage, the output gate drive circuit will be shut down, thus stopping the switching of the power MOSFET. As there is no power to maintain Vcc voltage, it drops over time, and will turn on high voltage startup circuit when it trips down to UVLO($_{OFF}$). The switch of the power MOSFET will resume after Vcc voltage rises back to UVLO($_{ON}$).

The Vcc OVP function in the LD7578 is an auto-recovery type protection. If the OVP condition, usually caused by the feedback loop opened, is not released, the Vcc will trip to the OVP level again, re-shutting down the output. The Vcc waveform in Fig. 18 shows this auto-recovery type protection, presenting a hiccup mode.

On the other hand, the removal of the OVP condition should render the Vcc level back to normal level, causing the output automatically returning to the normal operation.

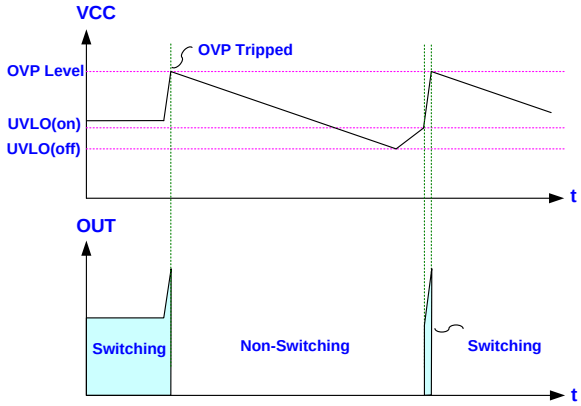


Fig. 18

(-)Latch Pin and Over Temperature Protection (OTP) --- Latched Mode Protection

The heat generated under some fault conditions may cause damage on components and the consequences may be hazardous to the employed system or users. Thus, over temperature protection (OTP) is required. The OTP circuit can be implemented by using a NTC to sense a hot-spot in power circuit like power MOSFET or output rectifier. It can be easily achieved by connecting a NTC to the (-)LATCH pin of LD7578. As the device temperature or ambient temperature rises high, the resistance of the NTC decreases. So, the voltage on the (-)LATCH pin could be read as below.

$$V_{(-)Latch} = 100\mu A \cdot R_{NTC}$$

When the $V_{(-)LATCH}$ falls below the threshold voltage (0.95V typical), LD7578 will shutdown the gate output and then latch the power supply off unless either Vcc drops below 8V (power down reset) or $V_{(-)LATCH}$, as the temperature is cooled down, rises over a threshold voltage about 1.05V. Accordingly, there are two methods to restart the circuit: one is to cool down the circuit for recovery and the other to re-plug the AC power. The detailed operation is depicted as figure 19.

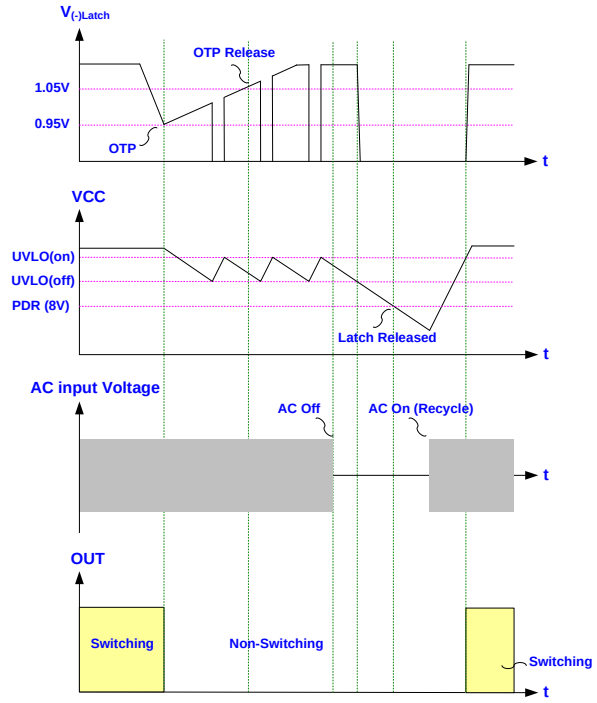


Fig. 19

Pull-Low Resistor on the Gate Pin of MOSFET

An anti-floating resistor is implemented in the OUT pin to prevent any uncertain output, which may cause MOSFET working abnormally or false triggering-on. However, such design won't cover the conditions of disconnection of gate resistor R_G. It is still strongly recommended to have a resistor connected at the MOSFET gate terminal (as shown in figure 21) to provide extra protection for fault conditions.

This external pull-low resistor is to prevent the MOSFET from being damaged during power-on when the gate resistor is disconnected. In such a single-fault condition, as shown in figure 22, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the coupling through the gate-to-drain capacitor C_{GD}. Therefore, the gate of MOSFET should be pulled low to maintain MOSFET in an off-state no matter the gate resistor is disconnected or opened in any case.

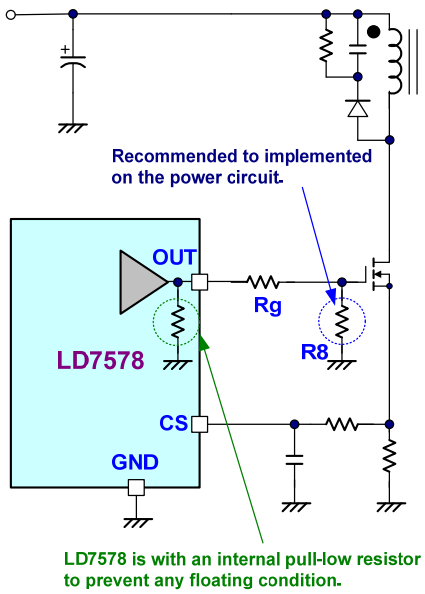


Fig. 20

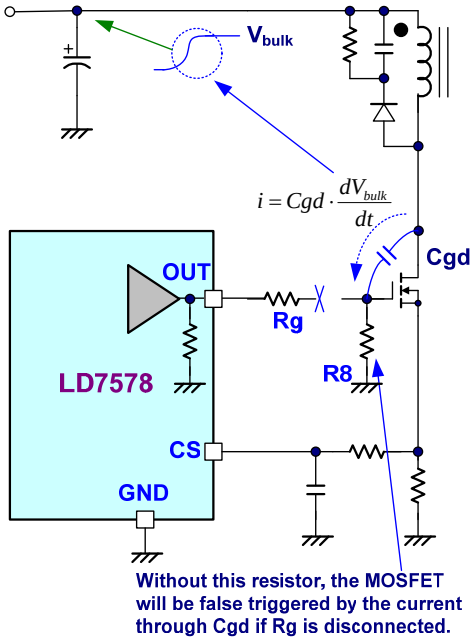


Fig. 21

Protection Resistor on the Hi-V Path

In some other Hi-V processes and designs, there is probably some parasitic SCR caused around HV pin, V_{CC} and GND. As shown in figure 23, a small negative spike in the HV pin may trigger this parasitic SCR and cause the latchup between V_{CC} and GND. Such latchup will damage the chip easily because of the equivalent short-circuit induced.

The LD7578 has eliminated the parasitic SCR efficiently. Figure 24 shows the equivalent circuit of the LD7578's Hi-V structure, illustrating that the LD7578 is capable to sustain negative voltage and superior than similar products. Even though, a 40KΩ resistor is still recommended to be placed on the Hi-V path.

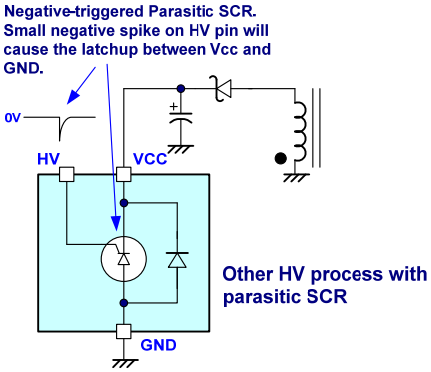


Fig. 22

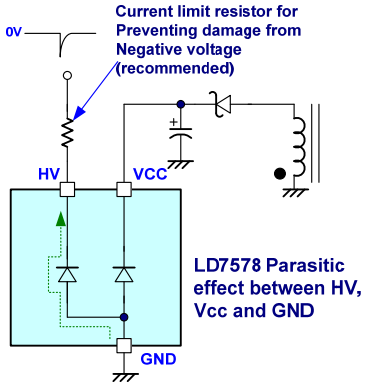
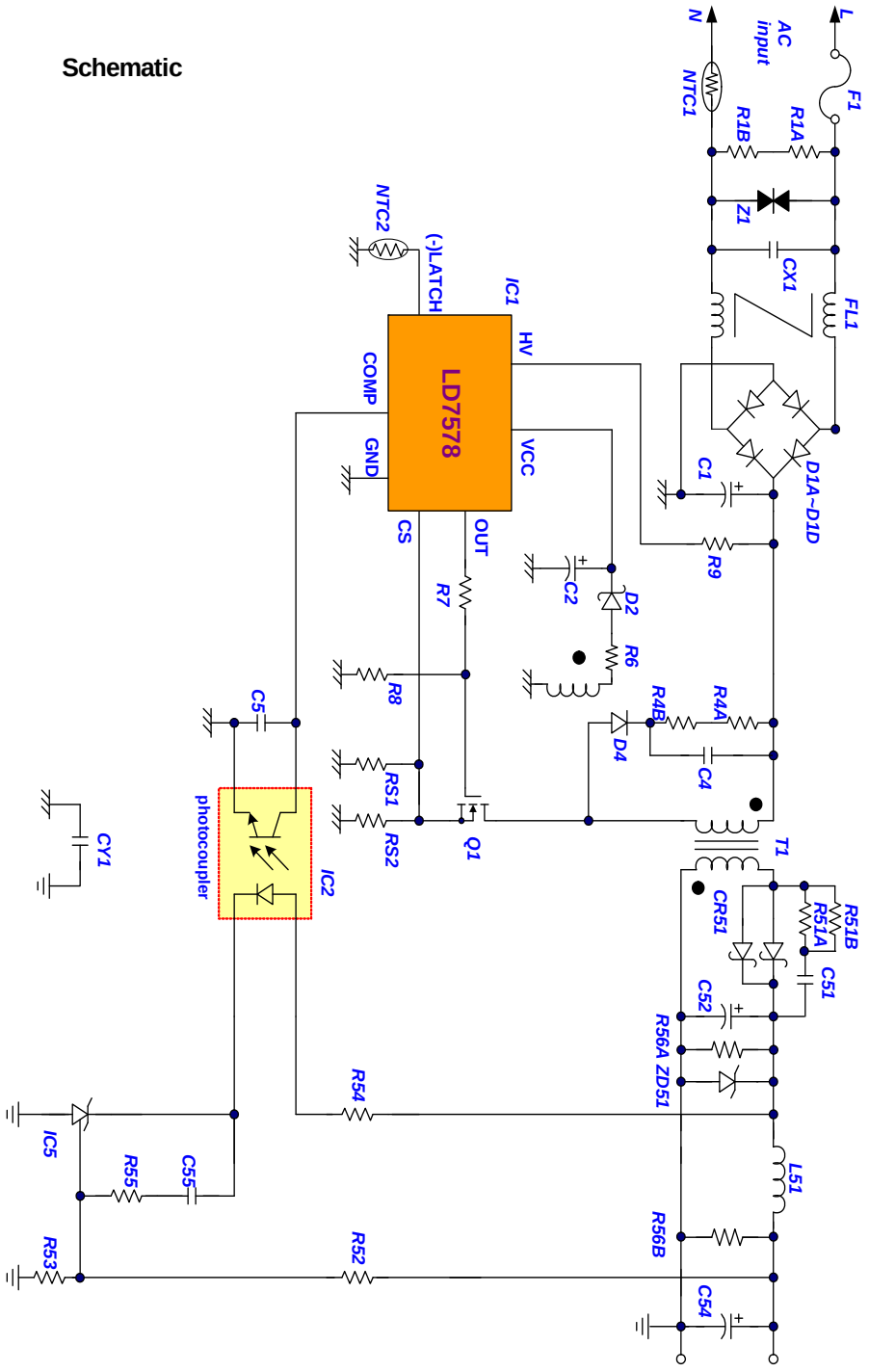


Fig. 23

Reference Application Circuit --- 10W (5V/2A) Adapter

Pin < 0.15W when Pout = 0W & Vin = 264Vac

Schematic



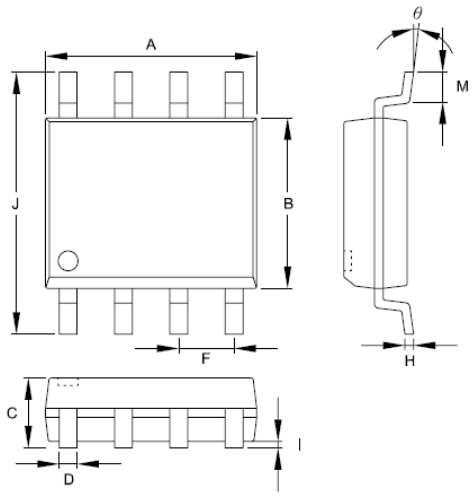
BOM

P/N	Component Value	Original
R1A	N/A	
R1B	N/A	
R4A	39KΩ, 1206	
R4B	39KΩ, 1206	
R6	2.2Ω, 1206	
R7	10Ω, 1206	
R8	10KΩ, 1206	
R9	39KΩ, 1206	
RS1	2.7Ω, 1206, 1%	
RS2	2.7Ω, 1206, 1%	
RT	100KΩ, 0805, 1%	
R51A	100Ω, 1206	
R51B	100Ω, 1206	
R52	2.49KΩ, 0805, 1%	
R53	2.49KΩ, 0805, 1%	
R54	100Ω, 0805	
R55	1KΩ, 0805	
R56A	2.7KΩ, 1206	
R56B	N/A	
NTC1	5Ω, 3A	08SP005
FL1	20mH	UU9.8
T1	EI-22	
L51	2.7μH	

P/N	Component Value	Note
C1	22μF, 400V	L-tec
C2	22μF, 50V	L-tec
C4	1000pF, 1000V, 1206	Holystone
C5	0.01μF, 16V, 0805	
C51	1000pF, 50V, 0805	
C52	1000μF, 10V	L-tec
C54	470μF, 10V	L-tec
C55	0.022μF, 16V, 0805	
CX1	0.1μF	X-cap
CY1	2200pF	Y-cap
D1A	1N4007	
D1B	1N4007	
D1C	1N4007	
D1D	1N4007	
D2	PS102R	
D4	1N4007	
Q1	2N60B	600V, 2A
CR51	SB540	
ZD51	6V2C	
IC1	LD7578GS	SOP-8
IC2	EL817B	
IC51	TL431	1%
F1	250V, 1A	
Z1	N/A	

Package Information

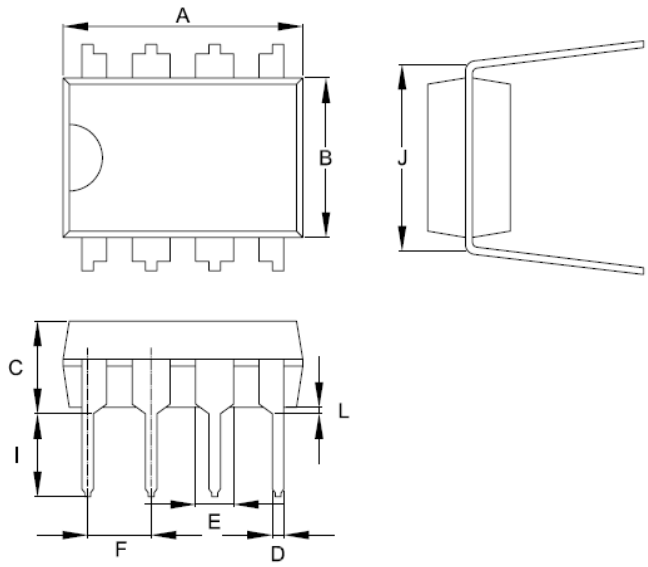
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	10/8/2008	Original Specification