# High Voltage Green-Mode PWM Controller with Brown-Out Protection

***Rev. 00b***

## General Description

The LD7577JA integrated several functions of protections, and EMI-improved solution in a SOP-7, SOP-8/or DIP-8 package. It minimizes the component counts and the circuit space, and it's perfect for the low cost of applications.

It provides functions of low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. Also, the LD7577JA features more protections like OLP (Over Load Protection), OVP (Over Voltage Protection), and brownout protection to prevent the circuit being damaged from the abnormal conditions.

Furthermore, the LD7577JA features frequency trembling to suppress the noise and is an excellent solution for EMI filter design.

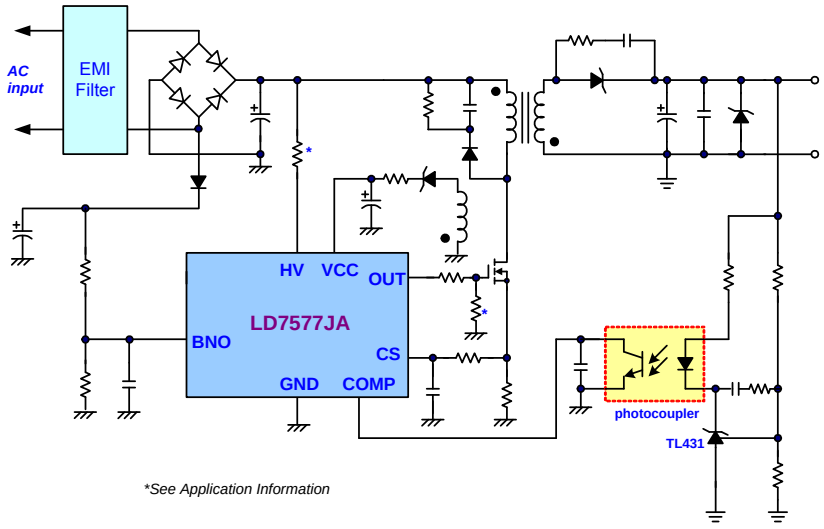
## Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Non-Audible-Noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Trembling
- Internal Slope Compensation
- Internal Over Current compensation
- OVP (Over Voltage Protection) on Vcc
- AC Input OVP (Over Voltage Protection)
- OLP (Over Load Protection)
- Brownout Protection
- 500mA Driving Capability

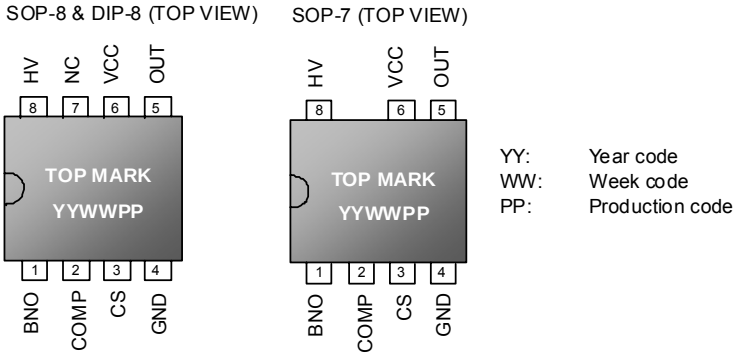
## Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

## Typical Application



## Pin Configuration




## Ordering Information

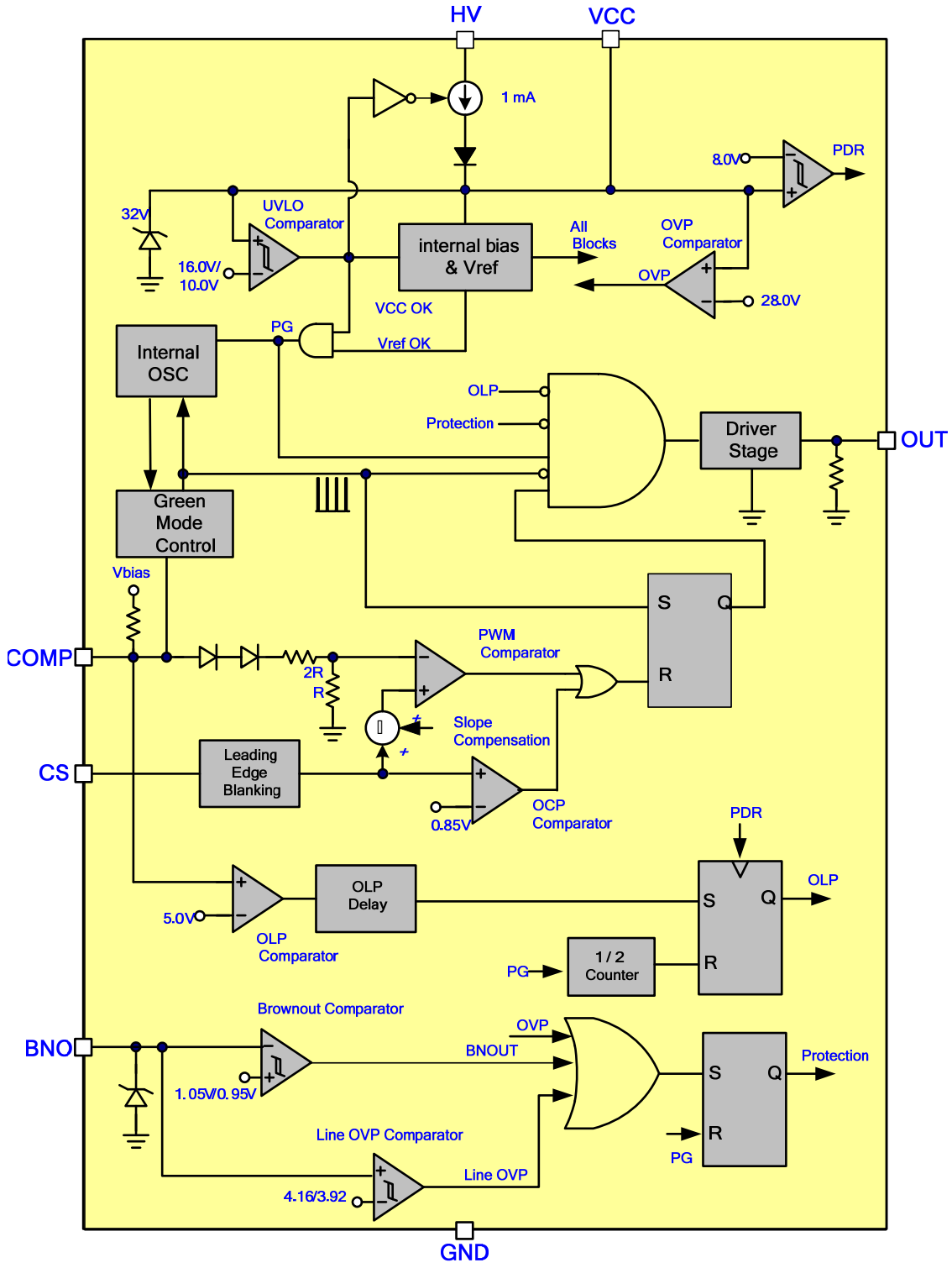
| Part number | Switching Freq. | Package | Top Mark | Shipping |
|---|---|---|---|---|
| LD7577JA GR | 65KHz | SOP-7 | LD7577JAGS | 2500 /tape & reel |
| LD7577JA GS | 65KHz | SOP-8 | LD7577JAGS | 2500 /tape & reel |
| LD7577JA GN | 65KHz | DIP-8 | LD7577JAGN | 3600 /tube /Carton |

Note: The LD7577JA is Green packaged.

## Pin Descriptions

| SOP-8<br>DIP-8 | SOP-7 | NAME | FUNCTION |
|---|---|---|---|
| 1 | 1 | BNO | Brownout Protection Pin. Connect a resistor divider between this pin and bulk capacitor voltage to set the brownout level. If the voltage is below threshold voltage, the PWM output will be disabled. The BNO pin also provides AC over voltage protection. As soon as the voltage is over 4.16V, the OVP will be tripped and the gate drive will be turned off. |
| 2 | 2 | COMP | Voltage feedback pin. Through the connection of a photo-coupler, it can close the control loop and achieve the regulation. |
| 3 | 3 | CS | Current sense pin. Connect it to sense the MOSFET current. |
| 4 | 4 | GND | Ground. |
| 5 | 5 | OUT | Gate drive output to drive the external MOSFET. |
| 6 | 6 | VCC | Supply voltage pin. |
| 7 | --- | NC | Unconnected Pin. |
| 8 | 8 | HV | Connect this pin to positive terminal of bulk capacitor to provide the startup current for the controller. When VCC voltage trips UVLO(on), this HV loop will be turned off to save the power loss of the startup circuit. |

## Block Diagram



## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage VCC | -0.3V~30V |
| High-Voltage Pin, HV | -0.3V~500V |
| COMP, BNO, CS | -0.3V ~7V |
| OUT | -0.3V ~Vcc+0.3V |
| Maximum Junction Temperature | 150°C |
| Operating Ambient Temperature Range | -40°C to 85°C |
| Operating Junction Temperature Range | -40°C to 125°C |
| Storage Temperature Range | -65°C to 150°C |
| Package Thermal Resistance (SOP-7, SOP-8) | 160°C/W |
| Package Thermal Resistance (DIP-8) | 100°C/W |
| Power Dissipation (SOP-7, SOP-8, at Ambient Temperature = 85°C) | 400mW |
| Power Dissipation (DIP-8, at Ambient Temperature = 85°C) | 650mW |
| Lead temperature (Soldering, 10sec) | 260°C |
| ESD Voltage Protection, Human Body Model (except HV Pin) | 2.5KV |
| ESD Voltage Protection, Machine Model | 250V |
| Gate Output Current | 500mA |

**Caution:**

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## Electrical Characteristics

($T_A$ = +25°C unless otherwise stated, $V_{CC}$=15.0V)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **High-Voltage Supply (HV Pin)** | | | | | |
| High-Voltage Current Source | $V_{CC}$< UVLO(on), HV=500V | 0.5 | 1.0 | 1.5 | mA |
| Off-State Leakage Current | $V_{CC}$> UVLO(off), HV=500V | | | 35 | μA |
| **Supply Voltage (Vcc Pin)** | | | | | |
| Startup Current | | | 320 | | μA |
| Operating Current (with 1nF load on OUT pin) | $V_{COMP}$=0V,Fsw=65KHz | | 3.3 | | mA |
| | $V_{COMP}$=3V,Fsw=65KHz | | 3.6 | | mA |
| | OLP Tripped | | 0.78 | | mA |
| | OVP Tripped | | 0.88 | | mA |
| UVLO (off) | | 9.0 | 10.0 | 11.0 | V |
| UVLO (on) | | 15.0 | 16.0 | 17.0 | V |
| OVP Level | | 26.5 | 28.0 | 29.5 | V |
| **Voltage Feedback (Comp Pin)** | | | | | |
| Short Circuit Current | $V_{COMP}$=0V | | 1.5 | 2.2 | mA |
| Open Loop Voltage | COMP pin open | | 5.8 | | V |
| Green Mode Threshold VCOMP | | | 2.35 | | V |
| Burst Mode Threshold VCOMP | | | 1.4 | | V |
| **Current Sensing (CS Pin)** | | | | | |
| Maximum Input Voltage(Vcs_off) | | 0.80 | 0.85 | 0.90 | V |
| Leading Edge Blanking Time | COMP >1.9V | | 320 | | nS |
| | COMP <1.9V | | 750 | | nS |
| Input impedance | | 1 | | | MΩ |
| Delay to Output | | | 100 | | nS |
| **Oscillator for Switching Frequency** | | | | | |
| Frequency | $F_{SW}$=65KHz | 60 | 65 | 70 | KHz |
| Trembling Frequency | | | ±4 | | KHz |
| Green Mode Frequency | $F_{SW}$=65KHz | | 22 | | KHz |
| Modulation Frequency | $F_{SW}$=65KHz | | 86 | | Hz |
| Temp. Stability | | | | 5 | % |
| Voltage Stability | VCC=11V-25V | | | 1 | % |

| | | | | | |
|---|---|---|---|---|---|
| **Brownout Protection & Line Compensation (BNO Pin)** | | | | | |
| Brownout Turn-On Trip Level | | 1.00 | 1.05 | 1.10 | V |
| Brownout Turn-off Trip Level | | 0.90 | 0.95 | 1.00 | V |
| Line Voltage OVP-Off Level | | 4.06 | 4.16 | 4.26 | V |
| Line Voltage OVP-On Level | | 3.82 | 3.92 | 4.02 | V |
| Saturation Voltage on BNO Pin | IBNO=1.5μA | | 6.0 | | V |
| **Gate Drive Output (OUT Pin)** | | | | | |
| Output Low Level | VCC=15V, Io=20mA | | | 1 | V |
| Output High Level | VCC=15V, Io=20mA | 9 | | | V |
| Rising Time | Load Capacitance=1000pF | | 100 | 160 | nS |
| Falling Time | Load Capacitance=1000pF | | 30 | 60 | nS |
| **OLP (Over Load Protection)** | | | | | |
| OLP Trip Level | | | 5.0 | | V |
| OLP Delay Time | Fsw=65KHz | | 30 | | mS |
| De_Latch VCC Level | PDR (Power Down Reset) | | 8.0 | | V |

## Typical Performance Characteristics

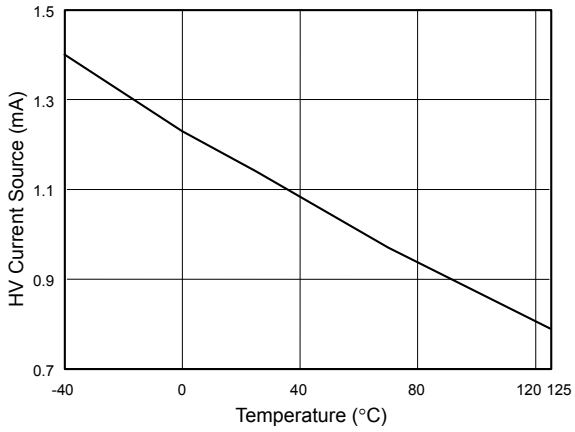



Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

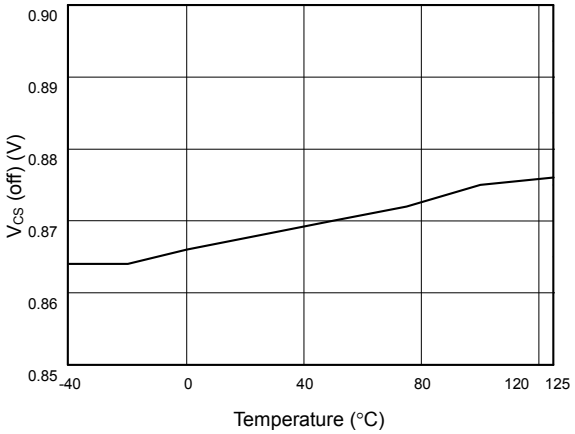



Fig. 2 $V_{CS}$ (off) vs. Temperature

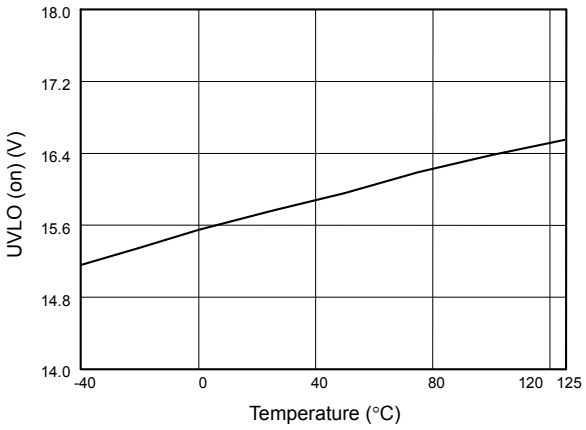



Fig. 3 UVLO (on) vs. Temperature

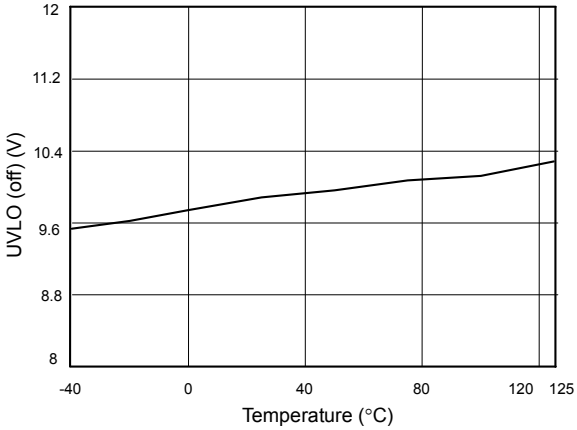



Fig. 4 UVLO (off ) vs. Temperature

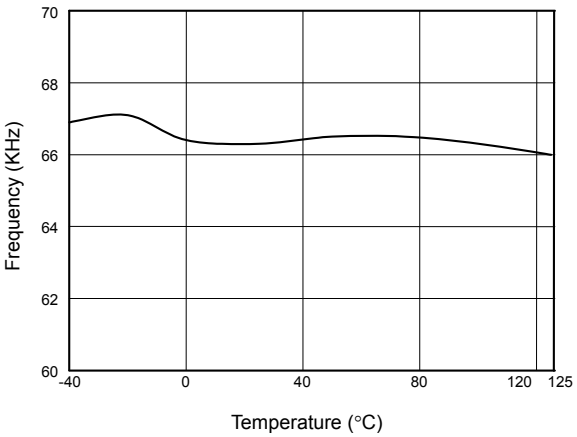



Fig. 5 Frequency vs. Temperature

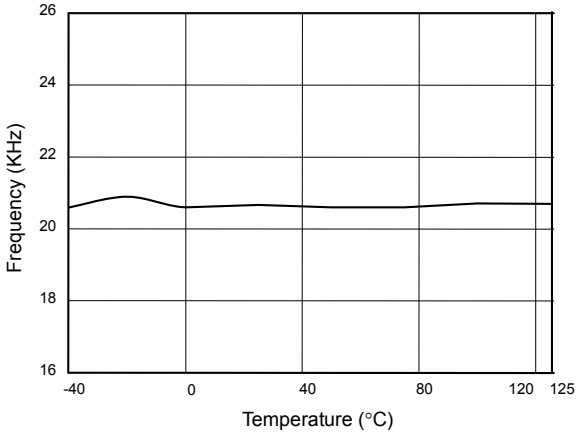



Fig. 6 Green Mode Frequency vs. Temperature

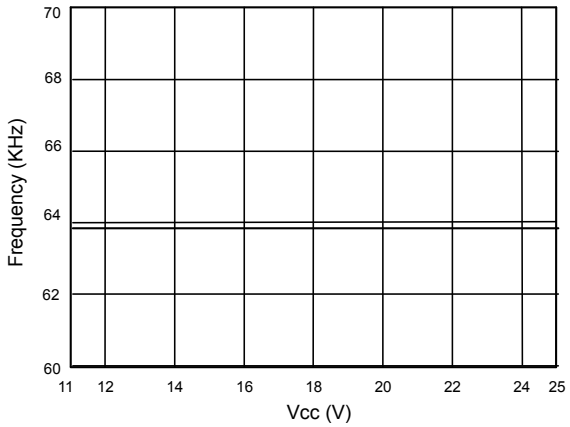



Fig. 7 Frequency vs. Vcc

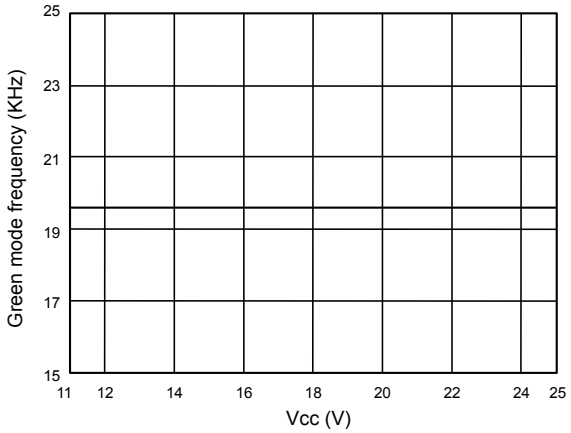



Fig. 8 Green mode frequency vs. Vcc

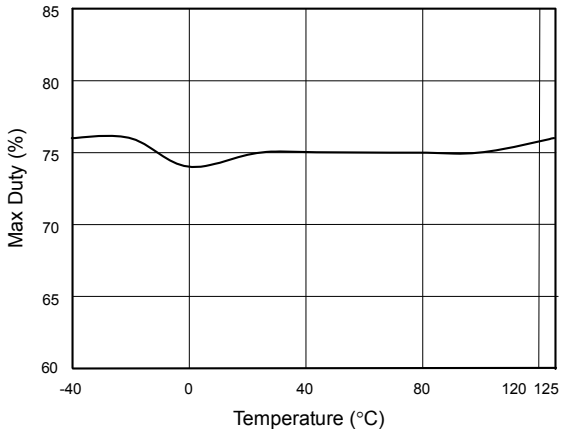



Fig. 9 Max Duty vs. Temperature

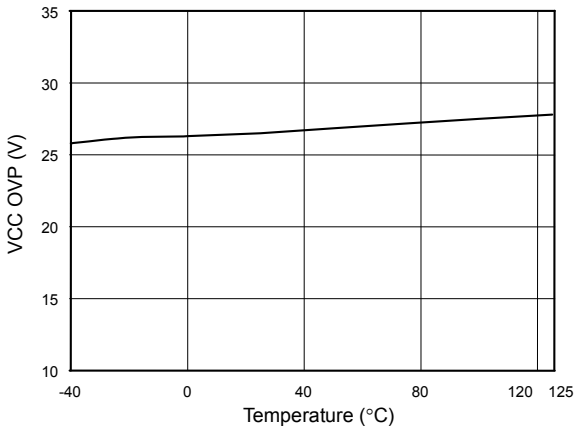



Fig. 10 VCC OVP vs. Temperature

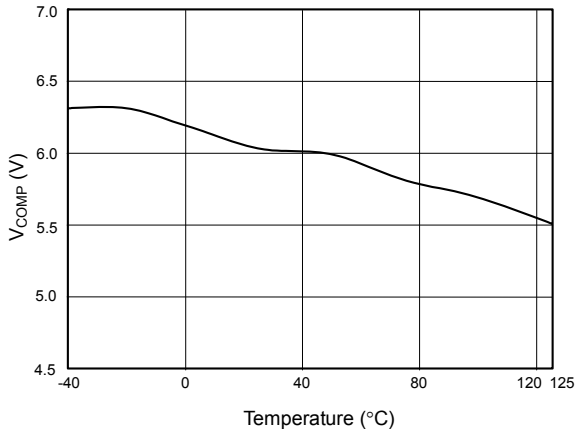



Fig. 11 $V_{COMP}$ open loop voltage vs. Temperature

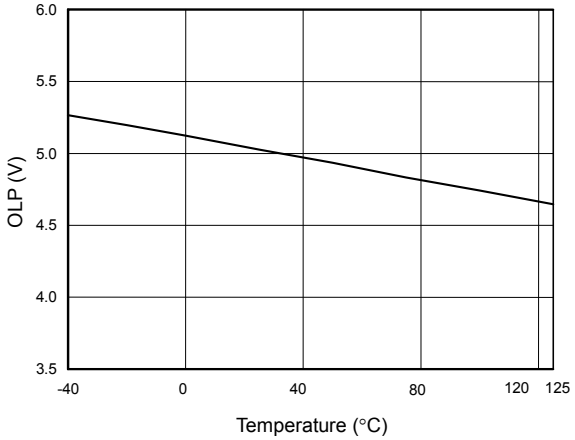



Fig. 12 OLP-Trip Level vs. Temperature

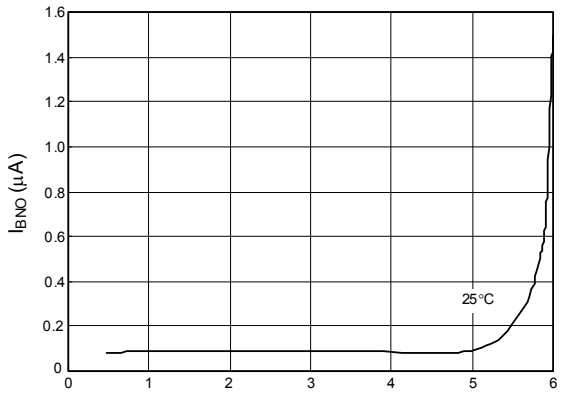



Fig. 13 $V_{BNO}$ vs. $I_{BNO}$

# Application Information

## Operation Overview

As long as the green power requirement becomes a trend and the power saving is becoming more and more important for switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation forces the PWM controllers to powerfully integrate more functions, thereby reducing the external part count. The LD7577JA is ideal for these applications to provide an easy and cost effective solution; and its detailed features are described as below.

## Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

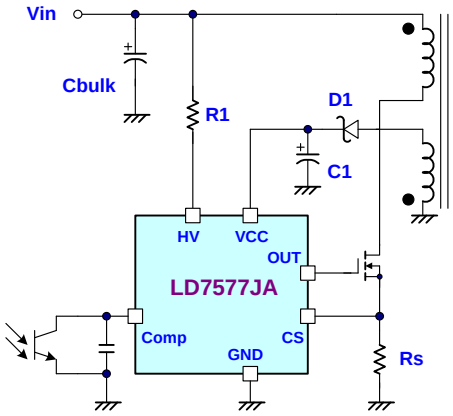



Fig. 14

Traditional circuits' power on the PWM controller through a startup resistor to constantly provide current from a rectified voltage to the capacitor connected to Vcc pin. Nevertheless, this startup resistor was usually of larger resistance, and it therefore required more power and more time to start up.

To achieve the optimized topology, as shown in figure 14, The LD7577JA is built in with high voltage startup circuit to optimize the power saving. During the startup sequence, a high-voltage current source sinks current from $C_{BULK}$ capacitor to provide the startup current as well as to charge the Vcc capacitor C1. During the initialization of the startup, Vcc voltage is lower than the UVLO(off) threshold thus the current source is on to supply a current of 1mA. Meanwhile, the Vcc current consumed by the LD7577JA is as low as 320μA thus most of the HV current is utilized to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost the same no matter whether operation condition is under low-line or high-line.

When Vcc voltage reaches UVLO(on) threshold, the LD7577JA is powered on to start issuing the gate drive signal, the high-voltage current source is then disabled, and the Vcc supply current will be only provided from the

auxiliary winding of the transformer. Therefore, the power losses on the startup circuit beyond the startup period can be eliminated and the power saving can be easily achieved. In general application, a 39KΩ resistor is still recommended to be placed in high voltage path to limit the current if there is a negative voltage applying in any case.

An UVLO comparator is included to detect the voltage on the $V_{CC}$ pin to ensure the supply voltage is high enough to power on the LD7577JA PWM controller and in addition to drive the power MOSFET. As shown in Fig. 15, a Hysteresis is provided to prevent the shutdown caused by the voltage dip during startup. The turn-on and turn-off threshold levels are set at 16V and 10.0V, respectively.

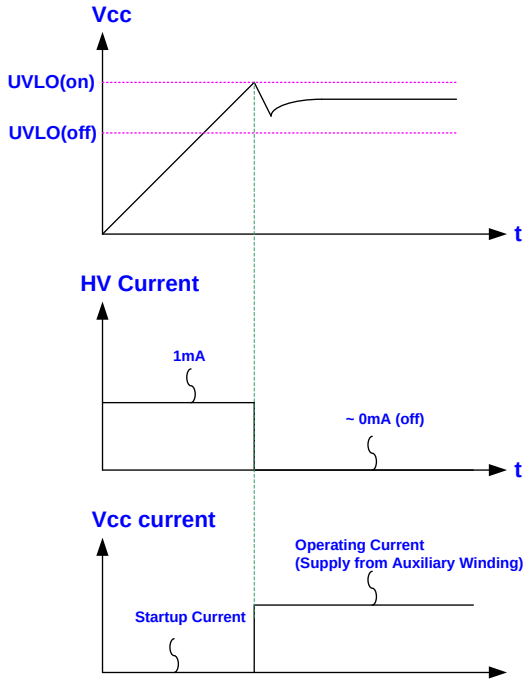



**Fig. 15**

## Current Sensing, Leading-edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feeds back both current signal and voltage signal to close the control loop and to achieve voltage regulation. LD7577JA detects the primary MOSFET current from the CS pin, which is applied not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 250nS leading-edge blanking (LEB) time is incorporated in the input of CS pin to prevent the false-trigger caused by any current spike. For low power applications, if the total pulse width of each turn-on spike is less than 250nS and the negative spike on the CS pin is not as low as -0.3V, the R-C filter (as shown in Fig.16) can be eliminated. Nevertheless, it is strongly recommended to remain a small R-C filter (as shown in Fig. 17) for higher power applications to avoid the CS pin being damaged by negative turn-on spikes.

## Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of the LD7577JA is limited to 75% in order to avoid the transformer flux saturation.

## Voltage Feedback Loop

The voltage feedback signal is issued from the TL431 in the secondary side through the photo-coupler to COMP pin of the LD7577JA. The input stage of the LD7577JA, like the UC384X, is incorporated with 2 diodes voltage offset circuit and a voltage divider with 1/3 ratio. Therefore,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally, eliminating external corresponding components on a board.

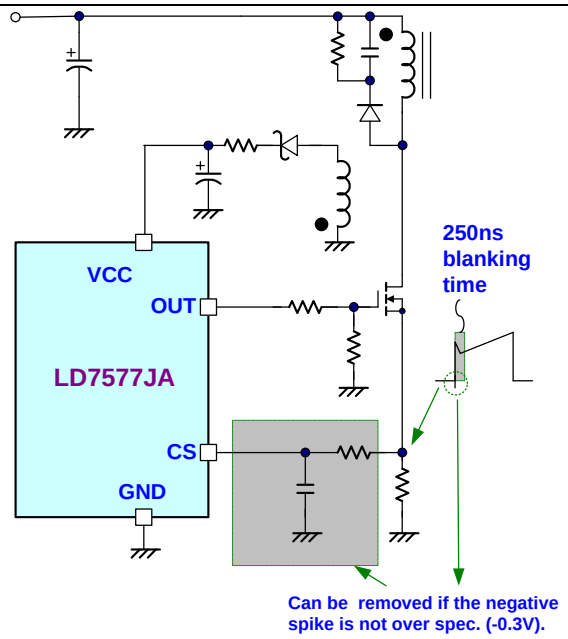



Fig. 16

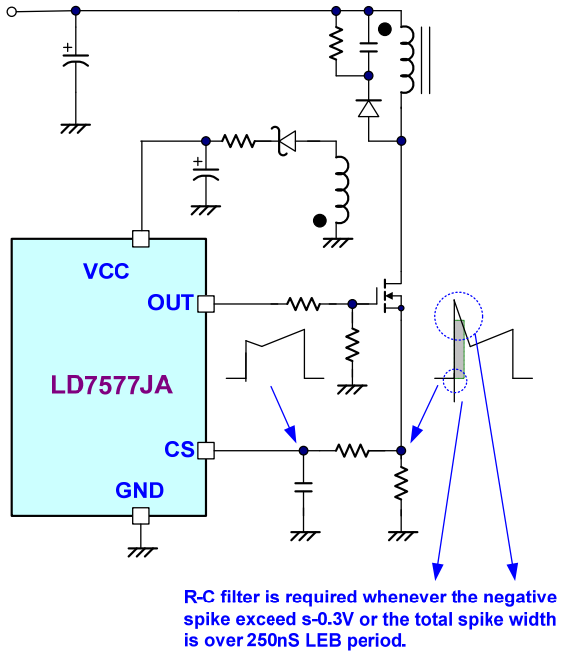



Fig. 17

## Oscillator and Switching Frequency

The switching frequency of the LD7577JA is fixed as 65KHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

## Frequency Trembling

The LD7577JA is implemented an adjustable frequency Trembling function which provides the power supply designers to choose the optimized EMI performance and lowest system cost. The Trembling frequency is fixed internally ±4KHz which is incorporated with the 65KHz switching frequency.

## Internal Slope Compensation

Stability is crucial for current mode control when it operates at more than 50% of duty-cycle. To stabilize the control loop, the slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In the LD7577JA, the internal slope compensation circuit has been implemented to simplify the external circuit design.

## On/Off Control

Pulling COMP pin below 1.2V will turn off the LD7577JA and disable the gate output pin of the LD7577JA. The off-mode will be released when the pull-low signal at COMP pin is removed.

## Dual-Oscillator Green-Mode Operation

Lots of topologies have been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or by reducing the switching frequency.

What the LD7577JA uses to implement the power-saving operation is Leadtrend Technology's own IP. By using this dual-oscillator control, the burst -mode frequency can be well controlled and further to avoid the generation of audible noise.

## Over Load Protection (OLP)

To protect the circuit from being damaged under over load condition or short condition, a smart OLP function is built in with the LD7577JA, as shown in Figure 18 shows the waveforms of the OLP operation. If output voltage drops, the feedback system tends to force the voltage loop toward the saturation (5.8V) and then pulls the voltage of COMP pin to high. Whenever the $V_{COMP}$ trips to the OLP threshold 5.0V and continues over 30mS, OLP is activated and then turns off the gate output to stop the switching of power circuit. The 30mS delay time is to prevent the false trigger from the power-on and turn-off transient.

A divide-2 counter is implemented to reduce the input average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-2 counter starts to count the number of UVLO(off). The latch is released if the 2nd UVLO(off) point is counted then the power circuit is recovered to switch again.

By using such protection mechanism, the average input power can be reduced to a very low level so that the component temperature and stress can be controlled within the safe operating area.

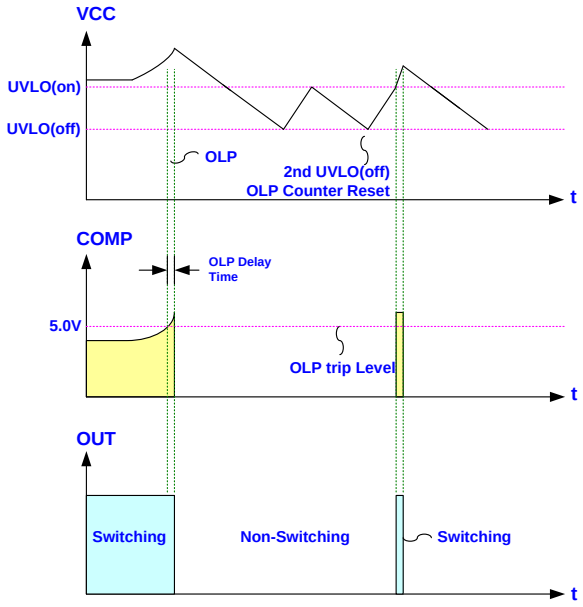



**Fig. 18**

## OVP (Over Voltage Protection) on Vcc

The $V_{GS}$ ratings of the nowadays power MOSFETs are mostly with 30V maximum. To prevent the $V_{GS}$ from fault condition, the LD7577JA is implemented with over-voltage protection on Vcc. As long as the Vcc voltage is higher than OVP threshold voltage, the output gate drive circuit will be shut down, thus to stop the switching of the power MOSFET until the next UVLO($_{ON}$).

The Vcc OVP function in the LD7577JA is an auto-recovery type protection. If the OVP condition, usually caused by the feedback loop opened, is not released, the Vcc will trip to the OVP level again, re-shutting down the output. The Vcc waveform in Fig. 19 shows this auto-recovery type protection, presenting a hiccup mode.

On the other hand, the removal of the OVP condition should render the Vcc level back to normal level, causing the output automatically returning to the normal operation.

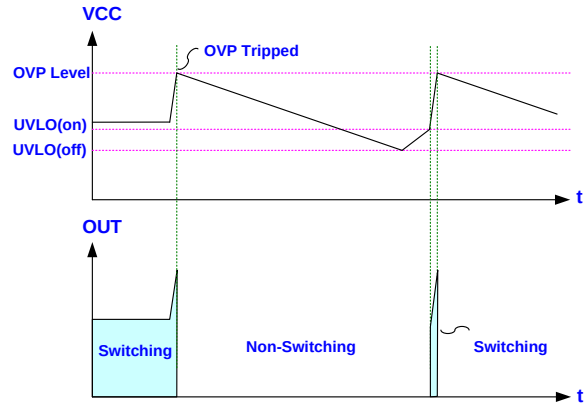



**Fig. 19**

## Brownout Protection & Line voltage OVP (Over voltage protection)

The LD7577JA is programmable to set the brownout protection point and the line voltage OVP point though BNO pin.

The voltage across the BNO pin is proportional to the bulk capacitor voltage, referred as the line voltage. A brownout comparator is implemented to detect the abnormal line condition. As soon as the condition is detected, it will shut down the controller to prevent the damage. Figure 20 shows the operation. When $V_{BNO}$ falls below 0.95V, the gate output will be kept off even Vcc has already achieved UVLO($_{ON}$). It therefore makes Vcc hiccup between UVLO($_{ON}$) and UVLO($_{OFF}$). Unless the line voltage is large enough to pull $V_{BNO}$ larger than 1.05V, the gate output will not start switching even when the next UVLO($_{ON}$) is tripped. A hysteresis is implemented to prevent the false trigger during turn-on and turn-off.

The comparator built in BNO will disable switching from Gate-out as soon as it detects excessive high line voltage and BNO voltage over 4.16V. VCC will then operate in hiccup mode between UVLO-on and UVLO-off. The Gate-out will not resume switching until VBNO falls below 3.92V. Therefore, it can prevent excessive high line voltage from damaging the external components. Fig. 21 shows the operation.

In order to protect BNO pin from being damaged during the dividing resistors floating, an internal zener diode is implemented in BNO pin. Fig. 13 shows the sinking capability of the zener diode. To protect BNO pin, the current flowing in BNO pin must be below 1.5μA, as shown in Fig. 13.

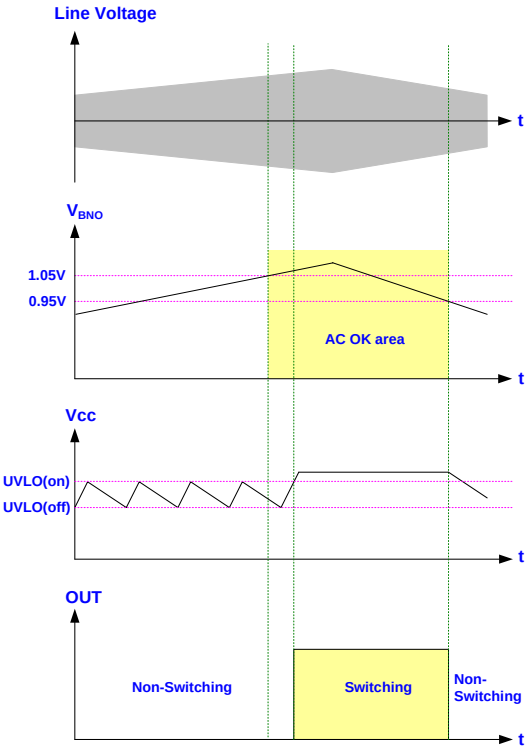



**Fig. 20**

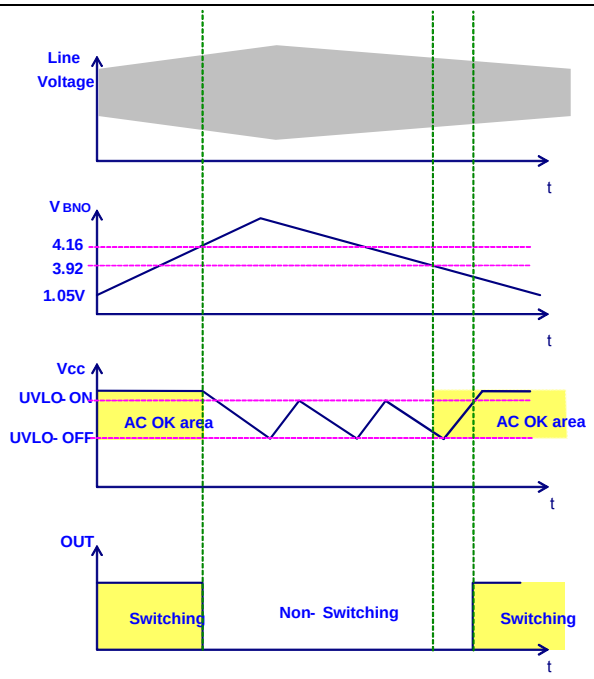



Fig.21

## Pull-Low Resistor on the Gate Pin of MOSFET

An anti-floating resistor is implemented in the OUT pin to prevent any uncertain output, which may cause MOSFET to work abnormally or false trigger on. However, such design may not apply in all the disconnection of gate resistor $R_G$. It is still strongly recommended to have a resistor connected at the MOSFET gate terminal (as shown in figure 22) to provide extra protection in fault conditions.

This external pull-low resistor is to prevent the MOSFET from being damaged during power-on when the gate resistor is disconnected. In such single-fault condition, as shown in figure 23, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the coupling through the gate-to-drain capacitor $C_{GD}$. Therefore, the MOSFET gate should be pulled low to maintain in a off-state no matter the gate resistor is disconnected or opened in any case.

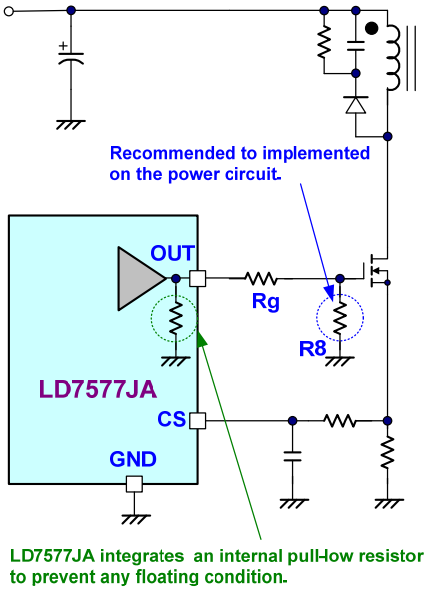



Fig. 22

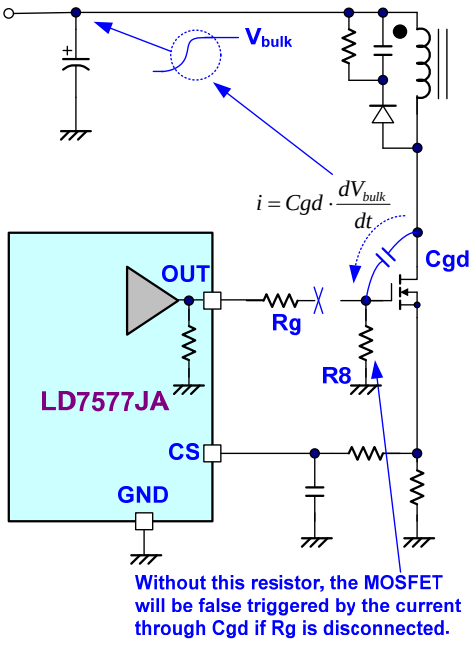



Fig. 23

## Protection Resistor on the Hi-V Path

In some other Hi-V processes and designs, there is probably some parasitic SCR caused around HV pin, $V_{CC}$ and GND. As shown in figure 24, a small negative spike in the HV pin may trigger this parasitic SCR and cause the latchup between $V_{CC}$ and GND. Such latchup will damage the chip easily because of the equivalent short-circuit induced.

The LD7577JA has eliminated the parasitic SCR efficiently. Figure 25 shows the equivalent circuit of the LD7577JA's Hi-V structure. It illustrates the LD7577JA is capable to sustain negative voltage and superior than similar products. Even though, a 40KΩ resistor is still recommended to be placed on the Hi-V path.

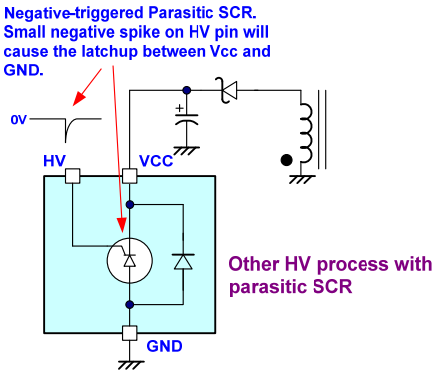



**Fig. 24**

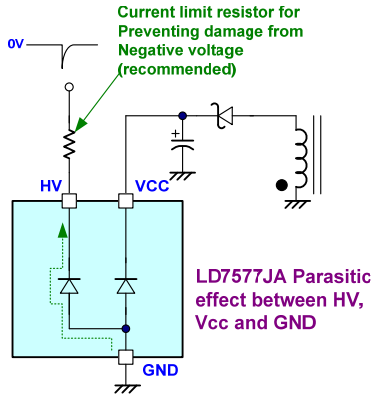
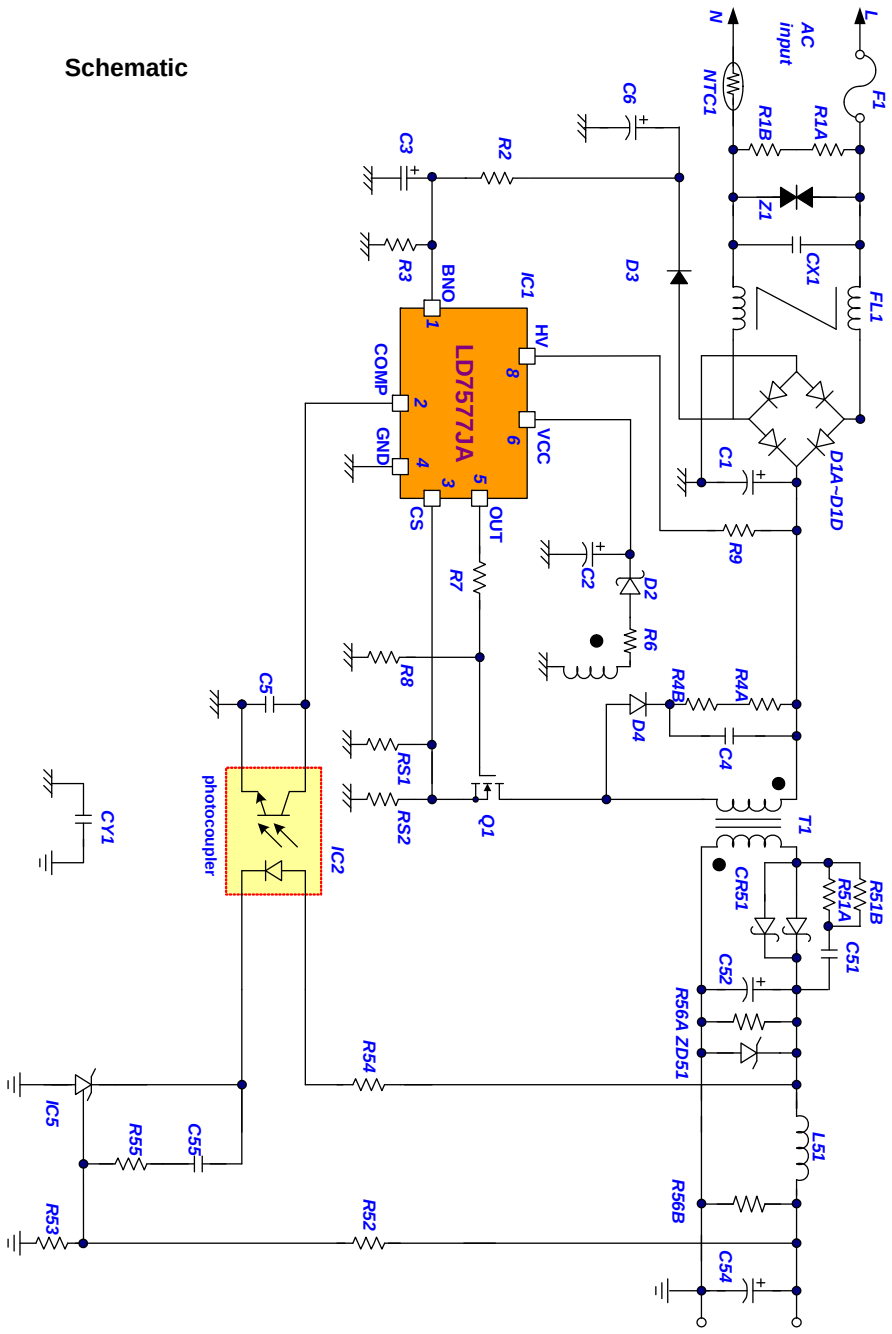



**Fig. 25**

## Reference Application Circuit --- 10W (5V/2A) Adapter

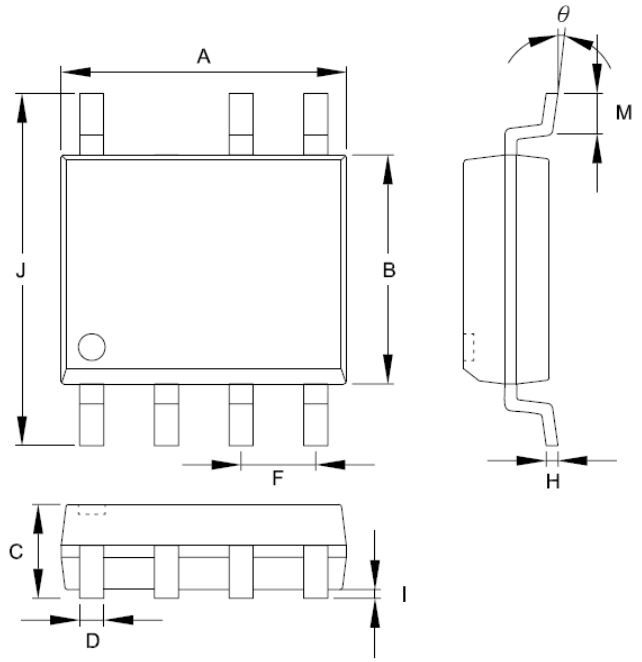
***Pin < 0.15W when Pout = 0W & Vin = 264Vac***

**Schematic**



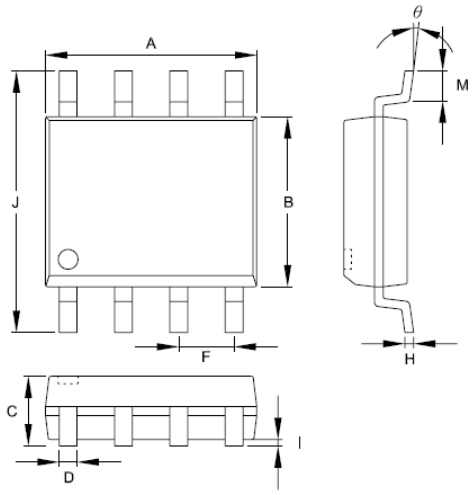
## Package Information

**SOP-7**




| Symbols | Dimensions in Millimeters | | Dimensions in Inch | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.178 | 0.229 | 0.007 | 0.009 |
| I | 0.102 | 0.254 | 0.004 | 0.010 |
| J | 5.791 | 6.198 | 0.228 | 0.244 |
| M | 0.406 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

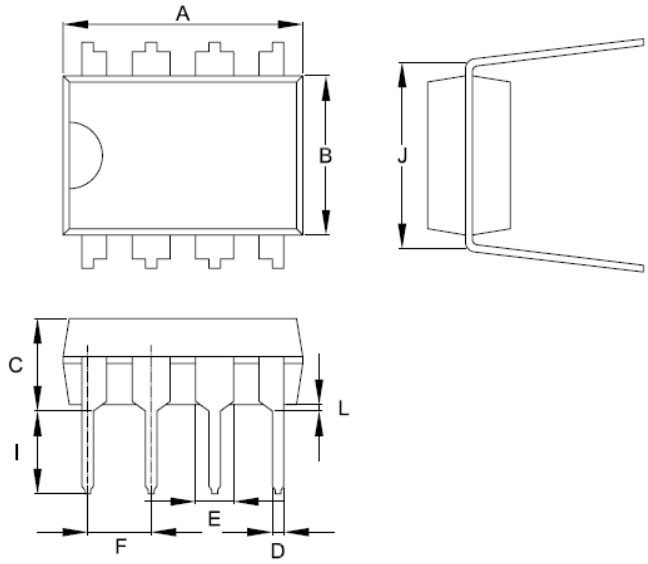
**SOP-8**




| Symbols | Dimensions in Millimeters | | Dimensions in Inch | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.178 | 0.229 | 0.007 | 0.009 |
| I | 0.102 | 0.254 | 0.004 | 0.010 |
| J | 5.791 | 6.198 | 0.228 | 0.244 |
| M | 0.406 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

## Package Information

**DIP-8**




| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 9.017 | 10.160 | 0.355 | 0.400 |
| B | 6.096 | 7.112 | 0.240 | 0.280 |
| C | ----- | 5.334 | ------ | 0.210 |
| D | 0.356 | 0.584 | 0.014 | 0.023 |
| E | 1.143 | 1.778 | 0.045 | 0.070 |
| F | 2.337 | 2.743 | 0.092 | 0.108 |
| I | 2.921 | 3.556 | 0.115 | 0.140 |
| J | 7.366 | 8.255 | 0.29 | 0.325 |
| L | 0.381 | ------ | 0.015 | -------- |

### Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

## Revision History

| Rev. | Date | Change Notice |
|---|---|---|
| 00 | 5/4/2009 | Original Specification |
| 00a | 7/27/2009 | ESD Voltage Protection, Human Body Model (except HV Pin)..... 2.5KV<br>Leading Edge Blanking Time update |
| 00b | 11/26/2009 | 1. Package option: SOP-7<br>2. Top mark information |