



GLT4160L04

4M X 4 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

SEPT 2004 (Rev.4.3)

Features :

- * 4,194,304 words by 4 bits organization.
- * Fast access time and cycle time
- * Low power dissipation.
- * Read-Modify-Write, RAS -Only Refresh, CAS -Before-RAS Refresh, Hidden Refresh.
- * 2,048 refresh cycles per 32ms.
- * Available in 300 mil 26(24) SOJ and TSOPII.
- * 3.3V±0.3V Vcc Power Supply voltage.
- * All inputs and Outputs are LVTTTL compatible.
- * Extended Data-Out (EDO) Page access cycle.
- * Self-refresh Capability. (S-Version).

Description :

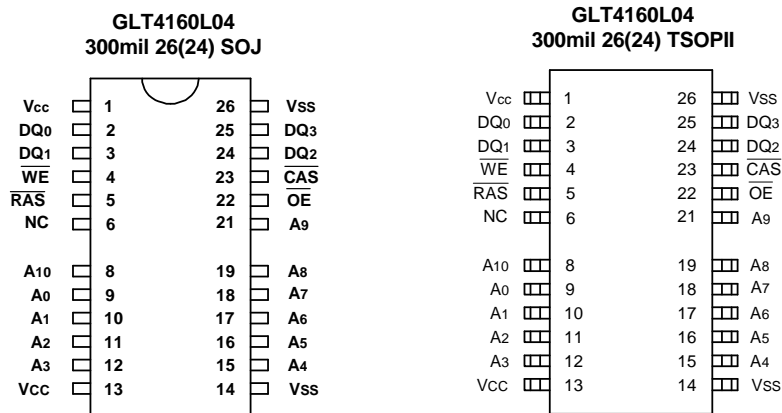
The GLT4160L04 is a high-performance CMOS dynamic random access memory containing 16,777,216 bits organized in a x4 configuration. The GLT4160L04 offers page cycle access with Extended Data Output. The GLT4160L04 has 11 row- and 11 column-addresses, and accepts 2048-cycle refresh in 32 ms.

The GLT4160L04 provides EDO PAGE MODE operation which allows for fast data access within a row-address defined boundary, up to 2048 x 4 bits with cycle times as short as 18ns.

HIGH PERFORMANCE	40	50	60	70
Max. $\overline{\text{RAS}}$ Access Time, (t_{RAC})	40 ns	50 ns	60 ns	70 ns
Max. Column Address Access Time, (t_{AA})	20 ns	25 ns	30 ns	35 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	18 ns	20 ns	25 ns	30 ns
Min. Read/Write Cycle Time, (t_{RC})	70 ns	84 ns	104 ns	124 ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	12 ns	13 ns	15 ns	20 ns

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Pin Configuration :

Pin Descriptions:

Name	Function
A ₀ - A ₁₀	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
DQ ₀ - DQ ₃	Data Inputs / Outputs
V _{CC}	+3.3V Power Supply
V _{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
0°C to +70°C
 For Extended Temperature.....-20°C to 85°C
 Storage Temperature(plastic).....-55°C to +150°C
 Voltage Relative to V_{SS}.....-0.5V to + 4.6V
 Short Circuit Output Current.....20mA
 Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

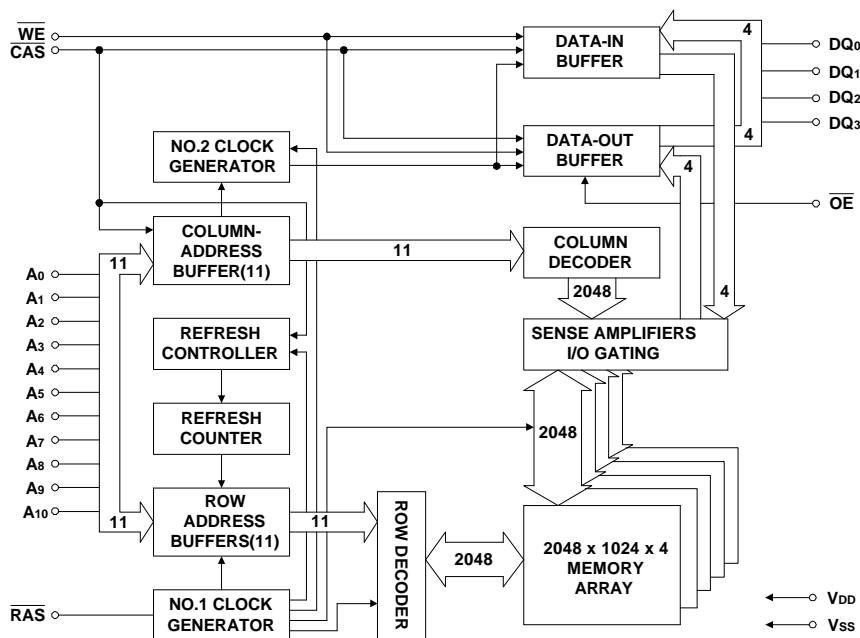
T_A=25°C, V_{CC}=3.3V±0.3V, V_{SS}=0V

Symbol	Parameter	Max.	Unit
C _{IN1}	Address Input	5	pF
C _{IN2}	RAS, CAS, WE, OE	7	pF
C _{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200µs and then, execute eight CAS-before-RAS or RAS-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :




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Truth Table:

Function		RAS	CAS	WE	OE	ADDRESS		DATA-IN/OUT
						t _R	t _C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out,Data-In
EDO-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out,Data-In
	2nd cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out,Data-In
RAS -ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

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DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, -20°C to 85°C V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I _{LI}	Input Leakage Current (any input pin)	0V ≤ V _{IN} ≤ V _{CC} +0.3V (All other pins not under test=0V)		-5		+5	μA	
I _{LO}	Output Leakage Current (for High-Z State)	0V ≤ V _{out} ≤ V _{CC} Output is disabled (Hiz)		-5		+5	μA	
I _{CC1}	Operating Current, Random READ/WRITE	t _{RC} = t _{RC} (min.)	t _{RAC} = 40ns t _{RAC} = 50ns t _{RAC} = 60ns t _{RAC} = 70ns			130 120 80 70	mA	1,2
I _{CC2}	Standby Current (TTL)	RAS, CAS at V _{IH} other inputs ≥ V _{SS}				1	mA	
I _{CC3}	Refresh Current, RAS -Only	RAS cycling, CAS at V _{IH} t _{RC} = t _{RC} (min.)	t _{RAC} = 40ns t _{RAC} = 50ns t _{RAC} = 60ns t _{RAC} = 70ns			130 120 80 70	mA	2
I _{CC4}	Operating Current, EDO Page Mode	RAS at V _{IL} , CAS address cycling: t _{PC} =t _{PC} (min.)	t _{RAC} = 40ns t _{RAC} = 50ns t _{RAC} = 60ns t _{RAC} = 70ns			130 120 80 70	mA	1,2
I _{CC5}	Refresh Current, CAS Before RAS	RAS, CAS address cycling: t _{RC} =t _{RC} (min.)	t _{RAC} = 40ns t _{RAC} = 50ns t _{RAC} = 60ns t _{RAC} = 70ns			130 120 80 70	mA	2
I _{CC6}	Standby Current, (CMOS)	RAS ≥ V _{CC} -0.2V, CAS ≥ V _{CC} -0.2V, All other inputs V _{SS}				300	μA	1,5
I _{CC7}	Self refresh Current	RAS = CAS = 0.2V, WE = OE = A ₀ -A ₁₀ =V _{CC} -0.2V or 0.2V DQ ₀ -DQ ₃ =V _{CC} -0.2V, 0.2V or Open				300	μA	
V _{IL}	Input Low Voltage			-0.3		+0.8	V	3
V _{IH}	Input High Voltage			2.0		V _{CC} +0.3	V	4
V _{OL}	Output Low Voltage	I _{OL} = 2mA				0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -2mA		2.4			V	

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC}(max.) is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified ICC(max.) is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
- Specified V_{IL}(min.) is steady state operation. During transitions V_{IL}(min.) may undershoot to -1V for a period not to exceed 15ns. All AC parameters are measured with V_{IL}(min.) ≥ V_{SS} and V_{IH}(max.) ≤ V_{CC}.
- Specified V_{IH}(max.) is steady state operation. During transitions V_{IH}(max.) may overshoot to V_{CC}+1V for a period not to exceed 15ns. All AC parameters are measured with V_{IL}(min.) ≥ V_{SS} and V_{IH}(max.) ≤ V_{CC}.
- S-Version.

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AC Characteristics
 $T_A = 0^\circ\text{C to } 70^\circ\text{C}, -20^\circ\text{C to } 85^\circ\text{C}$ $V_{CC} = 3.3\text{ V} \pm 0.3\text{V}$, $V_{IH}/V_{IL} = 3/0\text{ V}$, $V_{OH}/V_{OL} = 2/0.8\text{V}$

 An initial pause of 200 μs and 8 CAS-before-RAS or RAS-only refresh cycles are required after power-up.

Parameter	Symbol	40		50		60		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	t_{RC}	70		84		104		124		ns	
Read Modify Write Cycle Time	t_{RWC}	91		116		140		170		ns	
RAS Precharge Time	t_{RP}	25		30		40		50		ns	
RAS Pulse Width	t_{RAS}	40	10K	50	10k	60	10k	70	10k	ns	
Access Time from RAS	t_{RAC}		40		50		60		70	ns	1,2,3
Access Time from CAS	t_{CAC}		12		13		15		20	ns	1,5,7
Access Time from Column Address	t_{AA}		20		25		30		35	ns	1,5,6
CAS to Output Low-Z	t_{CLZ}	3		3		3		3		ns	
CAS to Output High-Z	t_{CEZ}	3	8	3	13	3	15	3	20	ns	
RAS Hold Time	t_{RSH}	12		13		15		20		ns	
CAS Hold Time	t_{CSH}	34		38		45		50		ns	
CAS Pulse Width	t_{CAS}	7	10k	8	10k	10	10k	15	10k	ns	
RAS to CAS Delay Time	t_{RCD}	18	28	20	37	20	45	20	50	ns	
RAS to Column Address Delay Time	t_{RAD}	13	20	15	25	15	30	15	35	ns	7
CAS to RAS Precharge Time	t_{CRP}	5		5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	8		10		10		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	6		8		10		15		ns	
Column Address to RAS Lead Time	t_{RAL}	20		25		30		35		ns	
Column Address Hold Time Referenced to RAS	t_{AR}	34		40		45		50		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to CAS	t_{RCH}	0		0		0		0		ns	4
Read Command Hold Time Referenced to RAS	t_{RRH}	0		0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	6		10		10		15		ns	
Write Command Pulse Width	t_{Wp}	6		10		10		15		ns	
Write Command to RAS Lead Time	t_{RWL}	12		13		15		30		ns	
Write Command to CAS Lead Time	t_{CWL}	8		8		10		15		ns	



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AC Characteristics

Parameter	Symbol	40		50		60		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	t_{DS}	0		0		0		0		ns	10
Data Hold Time	t_{DH}	7		8		10		15		ns	10
Data Hold Time Referenced to RAS	t_{DHR}	36		40		45		50		ns	
RAS to WE Delay Time	t_{RWD}	54		67		79		94		ns	
CAS to WE Delay Time	t_{CWD}	24		30		34		44		ns	
Column Address to WE Delay Time	t_{AWD}	32		42		49		59		ns	
CAS Precharge to WE Delay	t_{CPWD}	47		47		54		64		ns	
RAS to CAS Precharge Time	t_{RPC}	5		5		5		5		ns	
CAS precharge time (CAS Before RAS counter test cycle)	t_{CPT}	20		20		20		25		ns	
Access Time from CAS Precharge	t_{CPA}		22		28		35		40	ns	
EDO Page Mode Cycle Time	t_{PC}	18		20		25		30		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	50		47		56		71		ns	
CAS Precharge Time (EDO Page Mode)	t_{CP}	6		8		10		10		ns	
RAS Pulse Width (EDO Page Mode Only)	t_{RASP}	40	100k	50	100k	60	100k	70	100k	ns	
RAS Hold Time from CAS precharge	t_{RHCP}	30		30		35		40		ns	
Access Time from OE	t_{OEA}		12		13		15		20	ns	
OE to Data Delay Time	t_{OED}	8		13		15		20		ns	
OE to Output Low-Z	t_{OLZ}	3		3		3		3		ns	
OE to Output High-Z	t_{OEZ}	3	8	3	13	3	15	3	20	ns	
WE to Data Delay	t_{WED}	15		15		15		20		ns	
OE Command Hold Time	t_{OEH}	7		13		15		20		ns	
Data Output Hold after CAS low	t_{DOH}	3		5		5		5		ns	
RAS to Output High-Z	t_{REZ}	3	8	3	13	3	15	3	20	ns	
WE to Output High-Z	t_{WEZ}	3	10	3	13	3	15	3	20	ns	
OE to CAS Hold Time	t_{OCH}	5		5		5		5		ns	
CAS Hold Time to OE	t_{CHO}	5		5		5		5		ns	
OE Precharge Time	t_{OEP}	5		5		5		5		ns	
WE Puts width (EDO mixed read write cycle)	t_{WPE}	5		5		5		5		ns	
CAS Set-Up Time for CAS-before-RAS Cycle	t_{CSR}	5		5		5		5		ns	

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Parameter	Symbol	40		50		60		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
CAS Hold Time for CAS-before-RAS Cycle	t_{CHR}	8		10		10		15		ns	
WE to RAS precharge time (CAS Before RAS refresh)	t_{WRP}	10		10		10		10		ns	
WE to RAS hold time (CAS Before RAS refresh)	t_{WRH}	10		10		10		10		ns	
Transition Time	t_T	2	50	2	50	2	50	2	50	ns	11
Refresh Period (2,048 cycles)	t_{REF}		32		32		32		32	ms	
Refresh Period (S-Version)	t_{REF}		128		128		128		128	ms	
RAS Pulse Width (CAS Before RAS Self refresh)	t_{RASS}	100		100		100		100		μ s	
RAS precharge Time (CAS Before RAS Self refresh)	t_{RPS}	70		90		110		130		ns	
CAS Hold Time (CAS Before RAS Self refresh)	t_{CHS}	-50		-50		-50		-50		ns	

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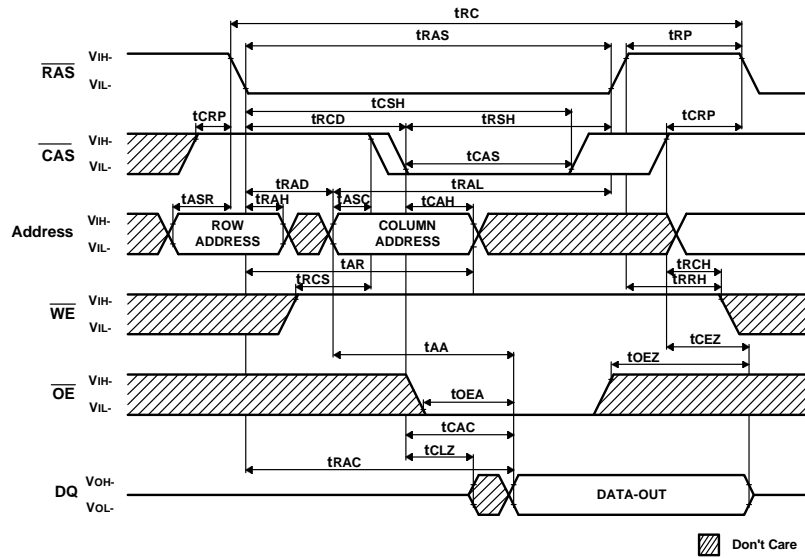
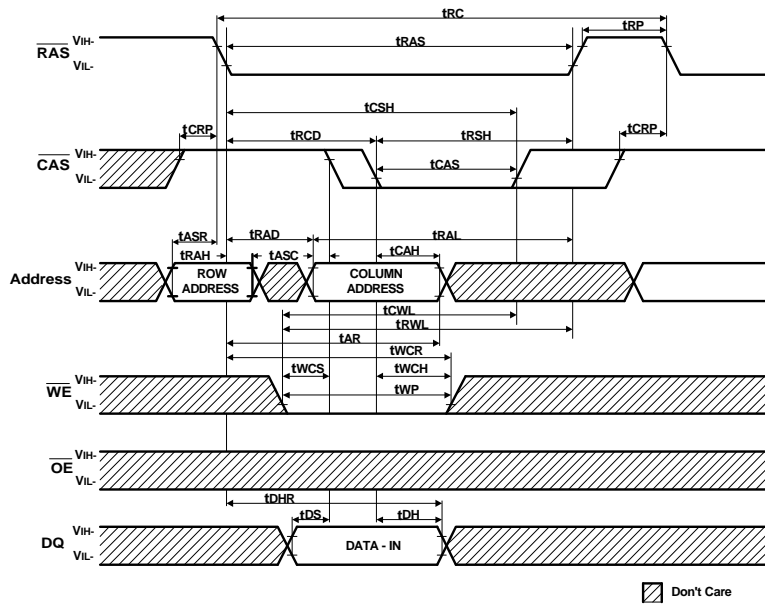
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TEST MODE CYCLE

Parameter	Symbol	40		50		60		70		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Random read or write cycle time	t_{RC}	89		89		109		129		ns	
Read-modify-write cycle time	t_{RWC}	121		121		145		175		ns	
Access time from \overline{RAS}	t_{RAC}		55		55		65		75	ns	1,2,3,7
Access time from \overline{CAS}	t_{CAC}		18		18		20		25	ns	1,3,7
Access time from column address	t_{AA}		30		30		35		40	ns	1,2,7
\overline{RAS} pulse width	t_{RAS}	55	10k	55	10k	65	10k	75	10k	ns	
\overline{CAS} pulse width	t_{CAS}	13	10k	13	10k	15	10k	20	10k	ns	
\overline{RAS} hold time	t_{RSH}	18		18		20		25		ns	
\overline{CAS} hold time	t_{CSH}	43		43		50		55		ns	
Column address to \overline{RAS} lead time	t_{RAL}	30		30		35		40		ns	
\overline{CAS} to \overline{WE} delay time	t_{CWD}	35		35		39		49		ns	8
\overline{RAS} to \overline{WE} delay time	t_{RWD}	72		72		84		99		ns	8
Column address to \overline{WE} delay time	t_{AWD}	47		47		54		64		ns	8
\overline{CAS} Precharge to \overline{WE} delay time	t_{CPWD}	52		52		59		69		ns	8
EDO Page Mode cycle time	t_{PC}	25		25		30		35		ns	
EDO page mode read-modify-write cycle time	t_{PRWC}	53		53		61		76		ns	
\overline{RAS} Pulse width (EDO page cycle)	t_{RASP}	55	100k	55	100k	65	100k	75	100k	ns	
Access time form \overline{CAS} precharge	t_{CPA}		33		33		40		45	ns	1
\overline{OE} access time	t_{OEA}		18		18		20		25	ns	
\overline{OE} to data delay	t_{OED}	18		18		20		25		ns	
\overline{OE} command hold time	t_{OEH}	18		18		20		25		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		10		ns	

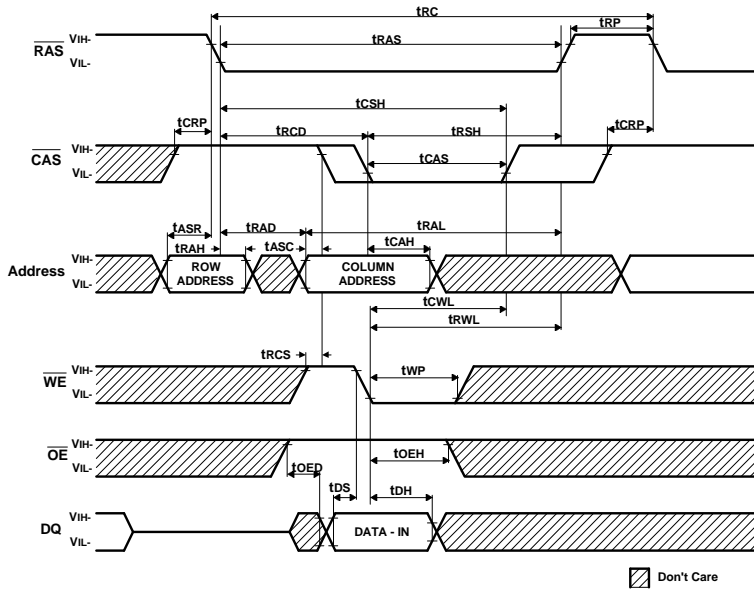
Notes:

1. Measure with a load equivalent to one TTL input and 100 pF.
2. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max.})$. If t_{RCD} is greater than $t_{\text{RCD}}(\text{max.})$, access time will be t_{CAC} dominant.
3. Assumes that $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max.})$. If t_{RAD} is greater than $t_{\text{RAD}}(\text{max.})$, access time will be controlled by t_{AA} .
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{AA} , t_{CAC} and t_{CPA} .
6. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max.})$.
7. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max.})$.
8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. $t_{\text{WCS}}(\text{min.})$ must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.
11. t_{T} is measured between $V_{\text{IH}}(\text{min.})$ and $V_{\text{IL}}(\text{max.})$. AC-measurements assume $t_{\text{T}} = 2 \text{ ns}$.

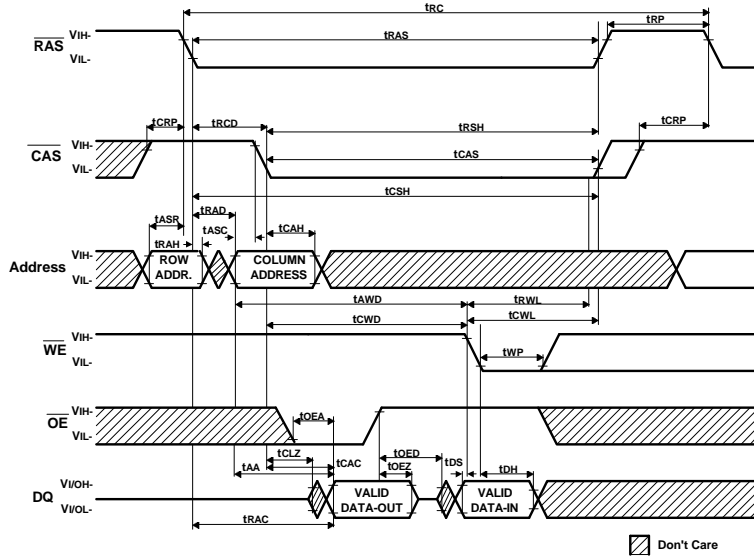
Read CYCLE

Early Write Cycle NOTE : D_{OUT} = OPEN

OE Controlled Write Cycle NOTE : D_{OUT} = OPEN
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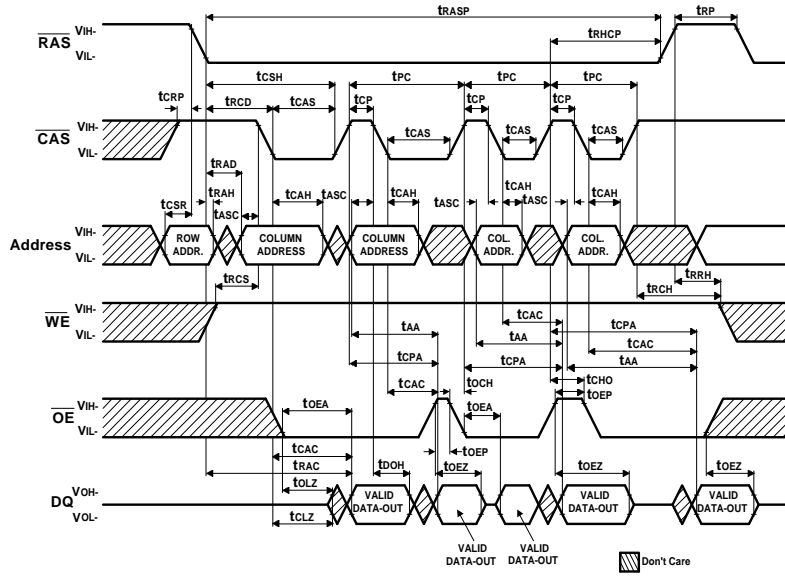
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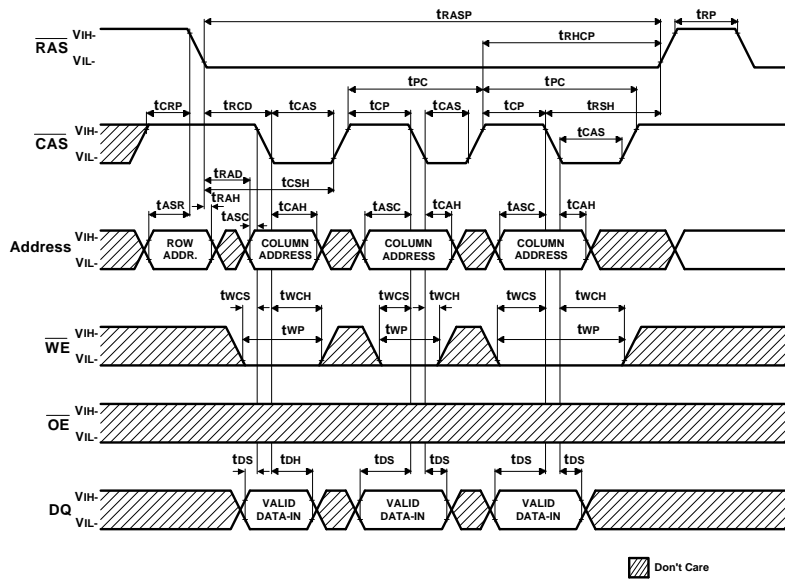
Read - Modify - Write Cycle



EDO Page Mode Read Cycle NOTE : D_{OUT} = OPEN



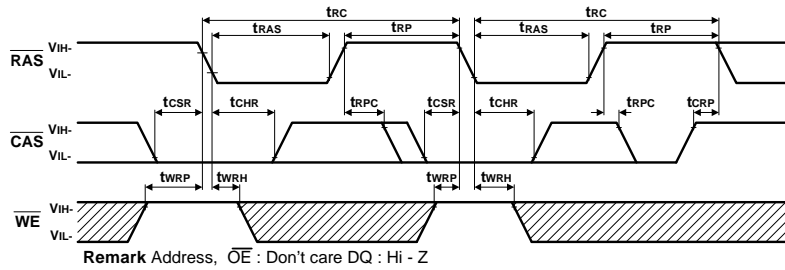
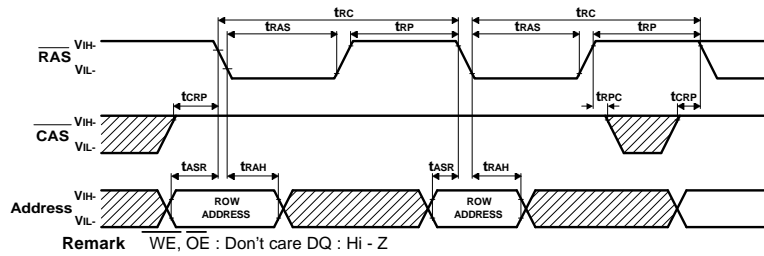
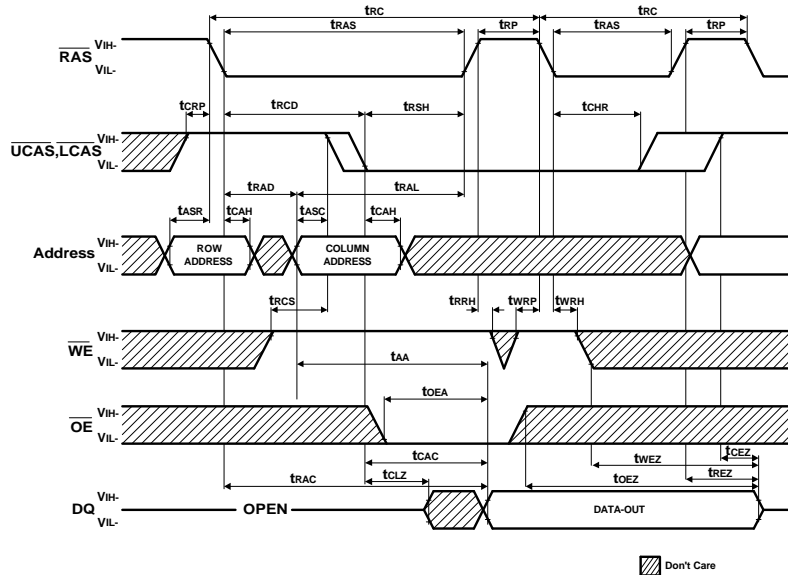
EDO Page Mode Early Write Cycle NOTE : D_{OUT} = OPEN



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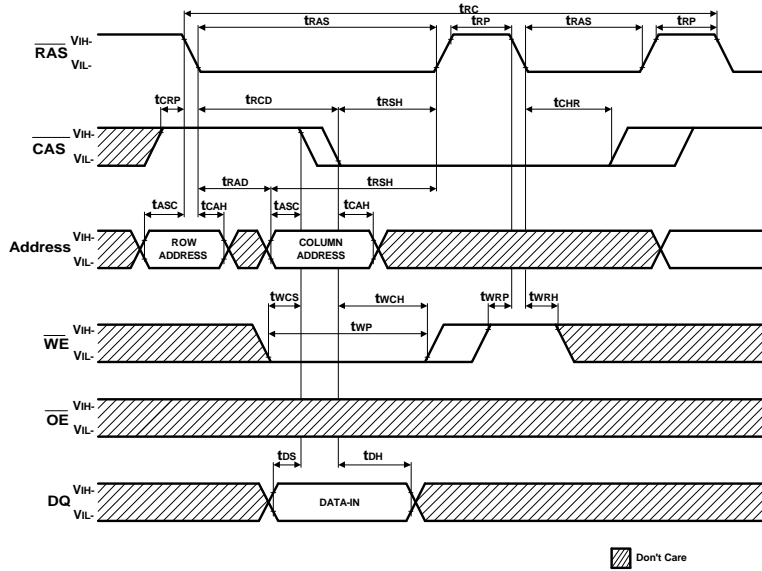
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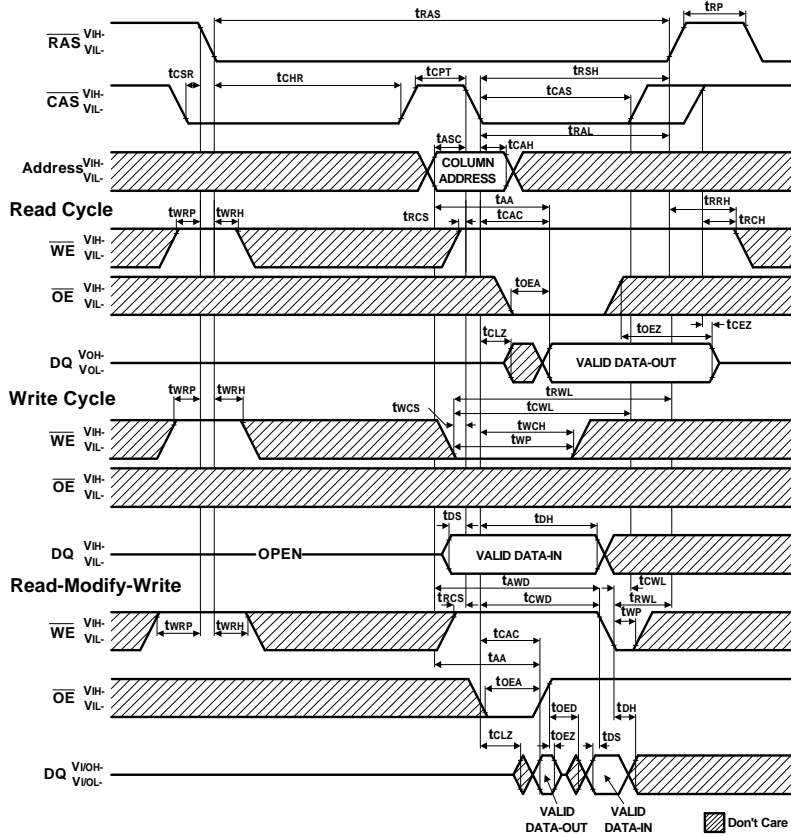
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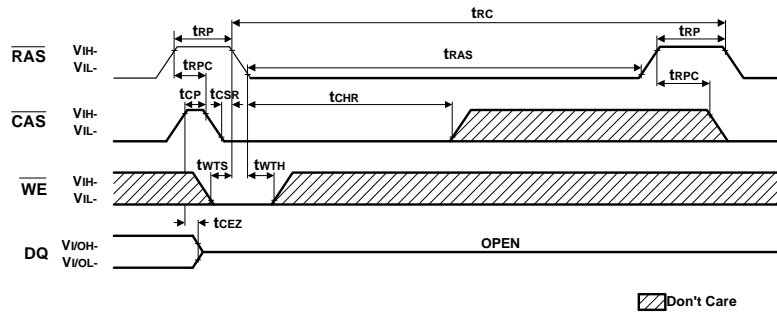
CAS - Before - RAS Refresh Cycle

RAS-Only Refresh Cycle

Hidden Refresh Cycle (Read)

Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN
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CAS-Before RAS Refresh Counter Test Cycle


TEST MODE IN CYCLE

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the x 16-bit organization during test mode. Don't care about the input levels of the CAS input A0, A1 .

(1) Setting the mode

Executing the test mode cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle) sets the test mode.

(2) Write / read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell be checked.

Output = "1" Normal write (all memory cells)

Output = "0" Abnormal write

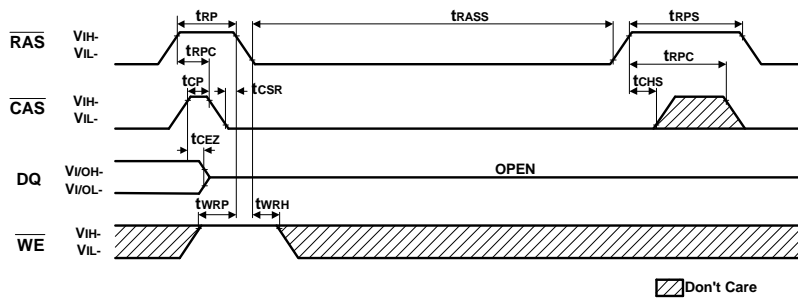
(3) Refresh

Refresh in the test mode must be performed with the $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle or with the $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. The $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle use the same counter as the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{\text{RAS}}$ only refresh cycle or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : \overline{OE} , Address = Don't Care



GLT4160L04

4M X 4 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

SEPT 2004 (Rev.4.3)

Ordering Information

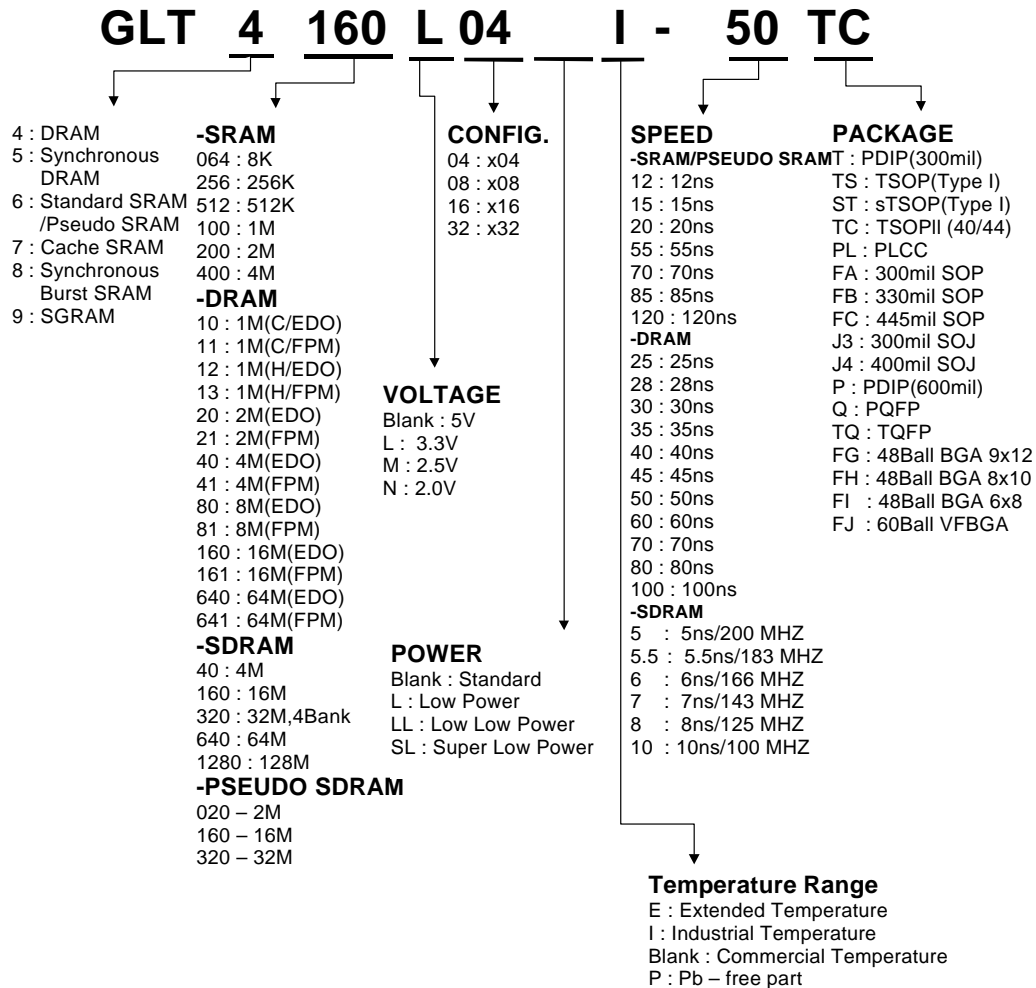
Part Number	SPEED	POWER	FEATURE	TEMPERATURE	PACKAGE
GLT4160L04-40J3	40ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04-50J3	50ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04-60J3	60ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04-70J3	70ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04E-40J3	40ns	Normal	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04E-50J3	50ns	Normal	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04E-60J3	60ns	Normal	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04E-70J3	70ns	Normal	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04S-40J3	40ns	Self Refresh	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04S-50J3	50ns	Self Refresh	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04S-60J3	60ns	Self Refresh	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04S-70J3	70ns	Self Refresh	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04SE-40J3	40ns	Self Refresh	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04SE-50J3	50ns	Self Refresh	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04SE-60J3	60ns	Self Refresh	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04SE-70J3	70ns	Self Refresh	EDO	Extended	SOJ 300mil 26(24)L
GLT4160L04P-40J3	40ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04P-50J3	50ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04P-60J3	60ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04P-70J3	70ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160L04I-40J3	40ns	Normal	EDO	Industrial	SOJ 300mil 26(24)L
GLT4160L04I-50J3	50ns	Normal	EDO	Industrial	SOJ 300mil 26(24)L
GLT4160L04I-60J3	60ns	Normal	EDO	Industrial	SOJ 300mil 26(24)L
GLT4160L04I-70J3	70ns	Normal	EDO	Industrial	SOJ 300mil 26(24)L
GLT4160L04-40TC	40ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04-50TC	50ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04-60TC	60ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04-70TC	70ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04E-40TC	40ns	Normal	EDO	Extended	TSOPII 300mil
GLT4160L04E-50TC	50ns	Normal	EDO	Extended	TSOPII 300mil
GLT4160L04E-60TC	60ns	Normal	EDO	Extended	TSOPII 300mil
GLT4160L04E-70TC	70ns	Normal	EDO	Extended	TSOPII 300mil
GLT4160L04S-40TC	40ns	Self Refresh	EDO	Commercial	TSOPII 300mil
GLT4160L04S-50TC	50ns	Self Refresh	EDO	Commercial	TSOPII 300mil
GLT4160L04S-60TC	60ns	Self Refresh	EDO	Commercial	TSOPII 300mil
GLT4160L04S-70TC	70ns	Self Refresh	EDO	Commercial	TSOPII 300mil
GLT4160L04SE-40TC	40ns	Self Refresh	EDO	Extended	TSOPII 300mil
GLT4160L04SE-50TC	50ns	Self Refresh	EDO	Extended	TSOPII 300mil
GLT4160L04SE-60TC	60ns	Self Refresh	EDO	Extended	TSOPII 300mil
GLT4160L04SE-70TC	70ns	Self Refresh	EDO	Extended	TSOPII 300mil
GLT4160L04P-40TC	40ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04P-50TC	50ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04P-60TC	60ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04P-70TC	70ns	Normal	EDO	Commercial	TSOPII 300mil
GLT4160L04I-40TC	40ns	Normal	EDO	Industrial	TSOPII 300mil
GLT4160L04I-50TC	50ns	Normal	EDO	Industrial	TSOPII 300mil
GLT4160L04I-60TC	60ns	Normal	EDO	Industrial	TSOPII 300mil
GLT4160L04I-70TC	70ns	Normal	EDO	Industrial	TSOPII 300mil

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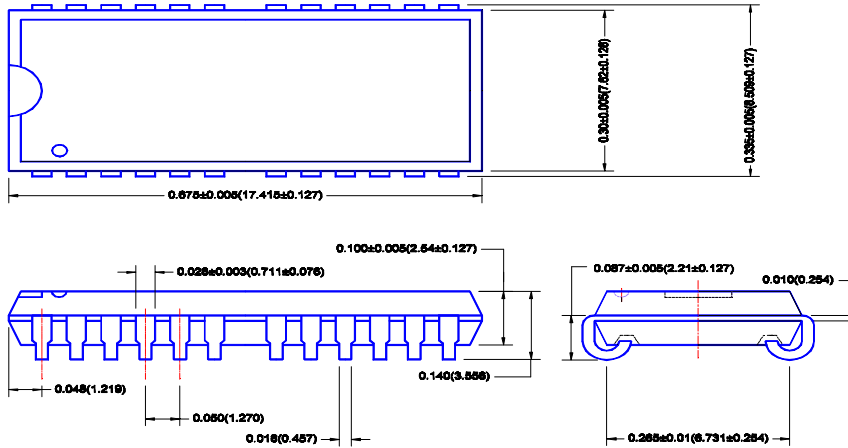
- 20 -

Parts Numbers (Top Mark) Definition :


Package Information

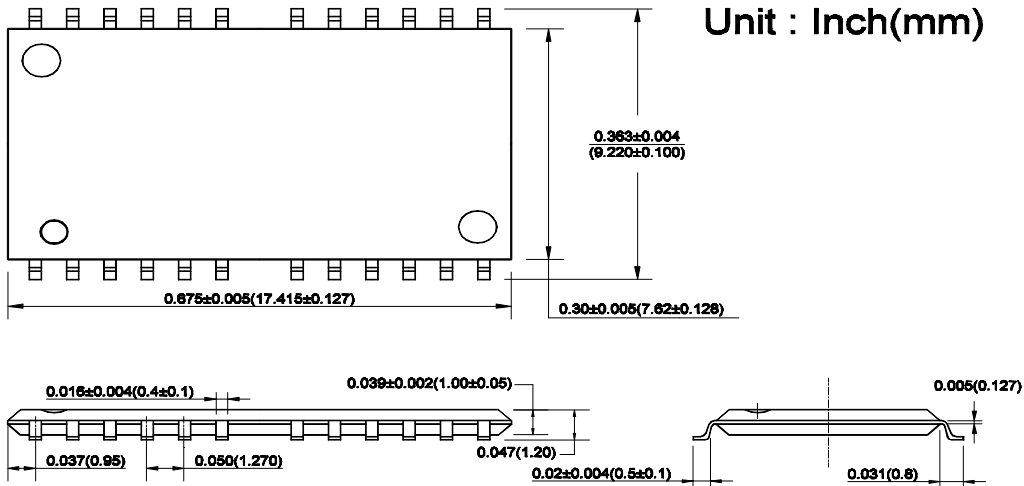
300mil 24/26 Lead Thin Small Outline Package SOJ

Unit : Inch(mm)



300mil 24/26 Lead Thin Small Outline Package (TSOP) TYPE II

Unit : Inch(mm)



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