MP7614

15 V CMOS
Multiplying 14-Bit
Digital-to-Analog Converter

FEATURES

- **Full Four-Quadrant Multiplication**
- **Excellent Stability Over Temperature and Time**
- **Guaranteed Monotonic**
- **TTL/5 V CMOS Compatible**
- **Low Sensitivity to Output Amplifier V_{OS}**
- **Low Glitch Energy**
- **16-Bit Version: MP7616**

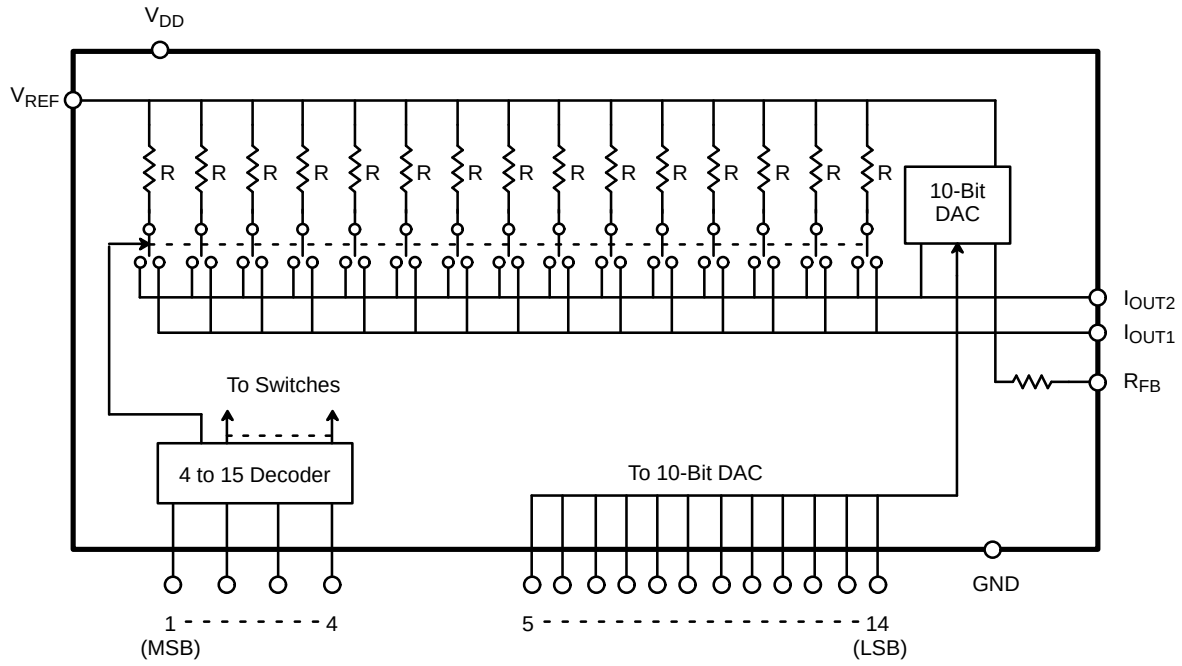
GENERAL DESCRIPTION

The MP7614 is a high density 14-bit CMOS multiplying Digital-to-Analog Converter. Silicon nitride passivation and untrimmed silicon chromium resistors have been combined to provide long term stability and reliability. Using the most significant bit (MSB) segmentation technique, the MP7614 features 13-bit (0.012%) differential and 12-bit (0.01%) integral linearity.

To achieve 13-bit linearity without laser trim, the MP7614 digitally decodes the four MSB's into 15 equal current sources, rather than the standard binary-weighted sources. Each resistor contributes only 1/16 full scale output thus reducing the matching accuracy requirement of the resistor and CMOS switches from 0.0015% to 0.006%.

The decoding technique achieves an eightfold improvement in differential linearity stability over temperature, an eightfold improvement in relative accuracy due to aging effects (long term stability), a fourfold improvement in glitch amplitude, and a tenfold reduction in sensitivity to output amplifier offset voltage.

SIMPLIFIED BLOCK DIAGRAM



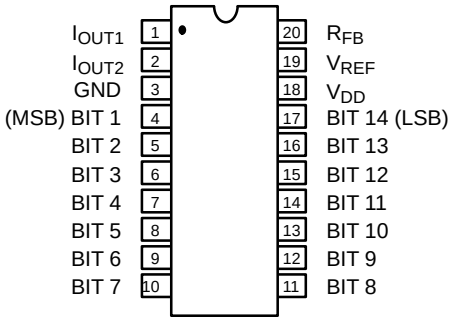
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7614JN	±4	±4	±0.8
Plastic Dip	–40 to +85°C	MP7614KN	±2	±2	±0.8
SOIC	–40 to +85°C	MP7614KS	±2	±2	±0.8
Ceramic Dip	–40 to +85°C	MP7614KD	±2	±2	±0.8
Ceramic Dip	–55 to +125°C	MP7614TD*	±2	±2	±0.8

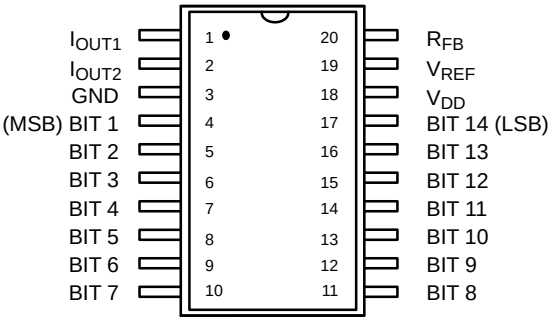
*Contact factory for non-compliant military processing

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin CDIP, PDIP (0.300")
D20, N20



20 Pin SOIC (Jedec, 0.300")
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6
10	BIT 7	Data Input Bit 7

PIN NO.	NAME	DESCRIPTION
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10
14	BIT 11	Data Input Bit 11
15	BIT 12	Data Input Bit 12
16	BIT 13	Data Input Bit 13
17	BIT 14	Data Input Bit 14 (LSB)
18	V_{DD}	Positive Power Supply
19	V_{REF}	Reference Input Voltage
20	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	14			14		Bits	
Integral Non-Linearity[5] (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, S				±4		±4		
K, T				±2		±2		
Differential Non-Linearity[5]	DNL						LSB	
J, S				±4		±4		
K, T				±2		±2		
Gain Error	GE		0.8			±0.8	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		±1.0			±2.0	ppm/°C	ΔGain/ΔTemperature
Non-Linearity Tempco[2]			±0.2			±0.5	ppm/°C	
Differential Linearity Tempco[2]			±0.2			±0.5	ppm/°C	
Power Supply Rejection Ratio	PSRR		±5	±50		±50	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
Output Leakage Current[6]	I_{OUT}		±1	±10		±200	nA	
DYNAMIC PERFORMANCE[2]								
Current Settling Time	t_S		2				µs	To 0.01% of FSR; all digital inputs low to high and high to low
Feedthrough at I_{OUT1}	F_T		1	2			mV p-p	V_{REF} = 20 V p-p @ 10 kHz
REFERENCE INPUT								
Input Resistance	R_{IN}	1	3	10	1	10	kΩ	
DIGITAL INPUTS[3]								
Logical “1” Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical “0” Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1.0		±1.0	µA	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		100				pF	DAC Inputs all 1’s
	C_{OUT1}		50				pF	DAC Inputs all 0’s
	C_{OUT2}		50				pF	DAC Inputs all 1’s
	C_{OUT2}		100				pF	DAC Inputs all 0’s
POWER SUPPLY[4]								
Functional Voltage Range[2]	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}		0.4	4		4	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1. Full Scale Range (FSR) is 10V for unipolar mode.
2. Guaranteed but not production tested.
3. Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4. Specified values guarantee functionality. Refer to other parameters for accuracy.
5. Linearity error is degraded by 65µV for every mV of voltage offset at output amplifier.
6. Output leakage current refers to I_{OUT1}. 1 LSB of current constantly flows into I_{OUT2} (30nA at 5 kΩ input impedance, V_{REF} = +10 V) due to ladder termination into I_{OUT2}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... 0 to +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 900mW
Derates above 75°C ..... 12mW/°C

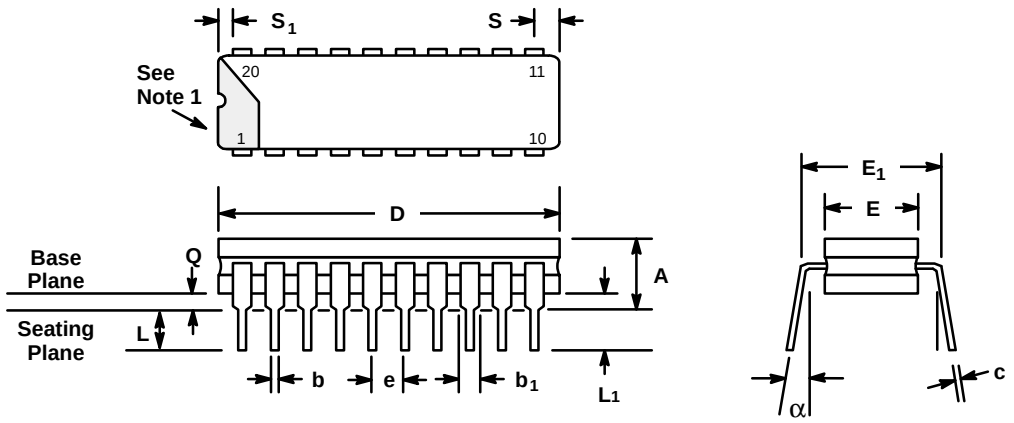
NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

Refer to Section 8 for Applications Information

20 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)
D20

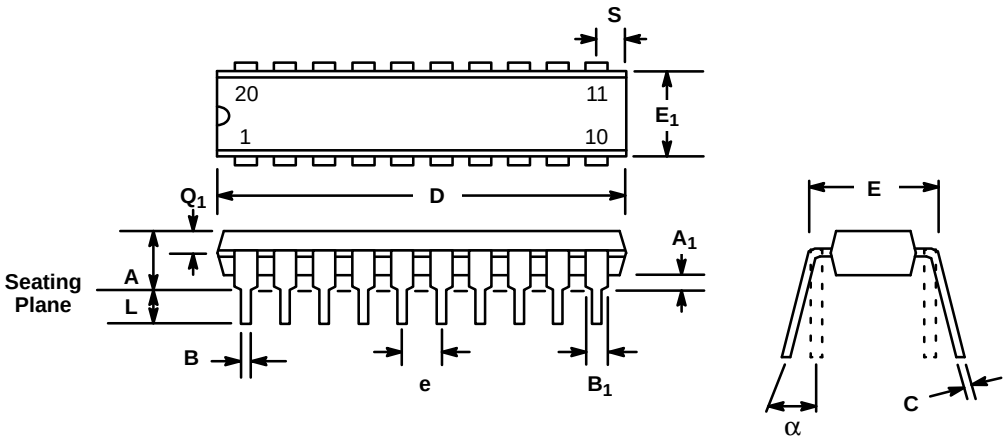


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.356	0.584	—
b_1	0.038	0.065	0.965	1.65	2
c	0.008	0.015	0.203	0.381	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.070	0.381	1.78	3
S	—	0.080	—	2.03	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

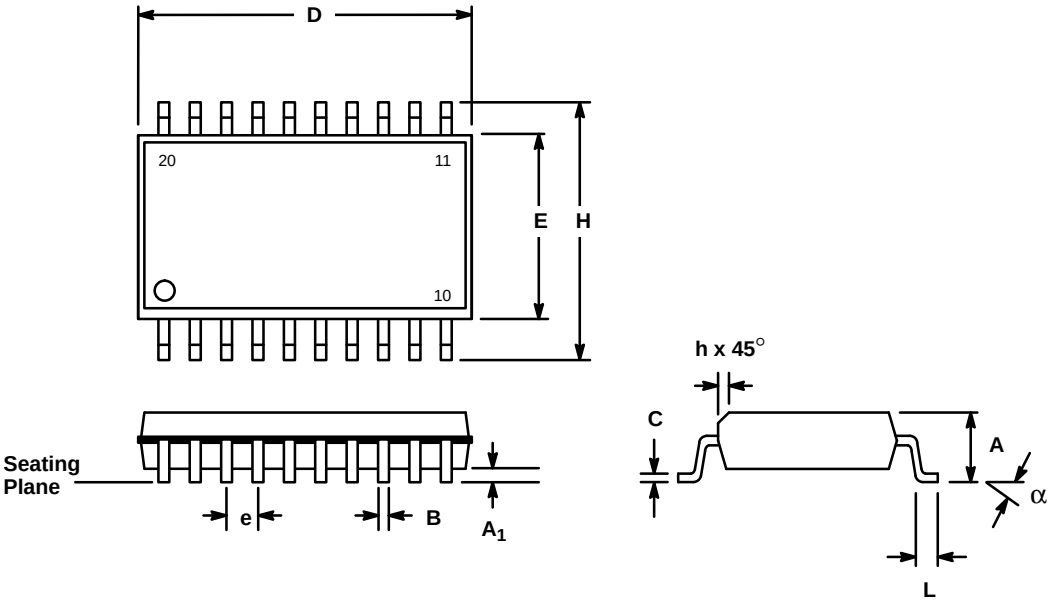
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

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