PL-3507 (For Chip Rev D)
Hi-Speed USB & IEEE 1394 Combo to IDE Bridge Controller

Product Datasheet

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Prolific Technology Inc.

7F, No. 48, Sec. 3, Nan Kang Rd.
Nan Kang, Taipei 115, Taiwan, R.O.C.
Telephone: +886-2-2654-6363
Fax: +886-2-2654-6161
E-mail: sales@prolific.com.tw
Website: http://www.prolific.com.tw

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Revision History

Revision	Description	Date
1.1	➢ Update datasheet to add Chip Rev 2D information	August 28, 2007
1.0C	➢ Section 3: Modify Functional Block Diagram	August 2, 2005
1.0B	➢ Note: Chip Rev 1D does not support internal ROM code and requires external Flash to load firmware.	July 29, 2005
1.0A	➢ PL-3507 (Chip Rev D) Datasheet – Formal Release	April 29, 2005
0.9A	➢ PL-3507 (Chip Rev D) Datasheet – Preliminary Release	April 22, 2005

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1.0 Features

- Provides hot-swap function to select active device USB or 1394
- Provides auto-detect function to select active device between USB and 1394
- IEEE 1394-1995 and IEEE P1394a Compliant
- Universal Serial Bus Specification 1.1 and 2.0 Compliant
- USB Mass Storage Class Bulk-Only Transport Specification Compliant. No driver installation needed in Windows ME or above, Mac OS 9.x or above, and Linux (kernel 2.4.18 or above). Windows 98 requires additional driver installation provided by Prolific.
- AT Attachment with Packet Interface Extension (ATA/ATAPI-7) Compliant
- ATA interface support PIO mode 0~4, Multiword DMA mode 0~2, and Ultra-DMA mode 0~4
- Built-in hardware automated SBP2 protocol engine for 1394 connection which includes:
  - Management ORB fetch engine
  - Command ORB fetch engine
  - Page table fetch engine
  - Response packet generate engine
- On-Chip 3.3V to 2.5V regulator
- Built-in USB 1.1 & 2.0 PHY
- 4k bytes of shared data FIFO for USB/1394
- Embedded 8-bit micro controller
- Vendor/Product related information could be customized by external EEPROM
- Content of EEPROM can be updated through USB interface using vendor software
- Firmware can be upgraded through USB interface using ICP function with Parallel Flash
- Multi-function General Purpose I/O (GPIO) pins for LED function, button function, etc.
- FireWIRE and i.LINK 1394 Compliant Logo (TA ID #200404004)
- USB-IF Hi-Speed Logo Certified (TID No. 40002614)
- Backward Pin-to-Pin Compatible with PL-3507 Chip Rev C (contact Prolific FAE)
- Inexpensive LQFP package type: LQFP128pin (14x14mm)
- Note: Chip Rev 1D does not have an internal ROM code and requires an external Flash to load the firmware. Chip 2D have internal ROM code (see Chip Revision History section.)

2.0 Product Overview

The PL-3507 is a high performance combo bridge solution for connecting USB 2.0 and 1394 to ATA or ATAPI data storage devices, e.g. hard disk drives, CD-ROM, CD-R, CD-RW and DVD. The USB interface of PL-3507 supports USB 1.1 or USB 2.0 specifications to allow connections to host computer via USB port at maximum data transfer rate 480 Mbps.

The 1394 interface of the PL-3507 is in compliant with IEEE Std 1394-1995 and IEEE P1394a specification supporting data transfer rate 100, 200 and 400 Mbps, and built-in SBP2 (Serial Bus Protocol 2) hardware engine to enhance sustained data transfer rate up to 40 MBytes/sec.

The ATA/ATAPI interface provides signaling and timing for PIO mode 0-4, DMA mode 0-2, and Ultra DMA mode 0-4.

3.0 Functional Block Diagram

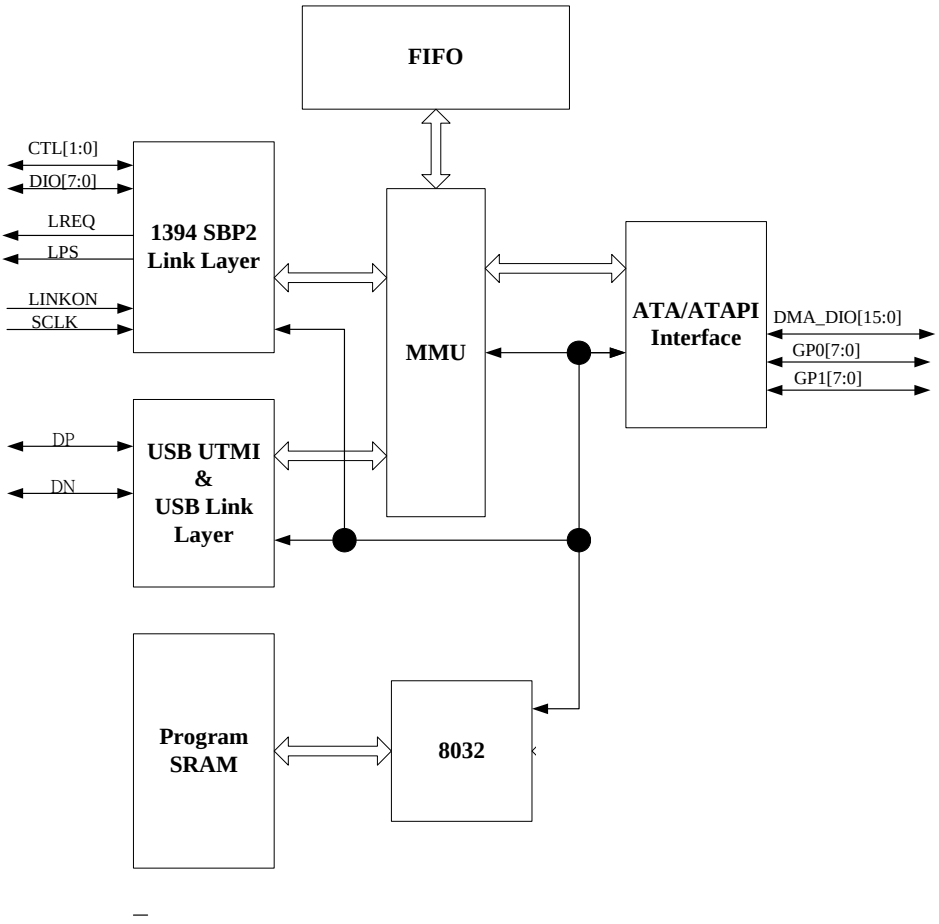


Figure 3-1 Block Diagram of PL-3507D (Chip Rev D)

4.0 System Application Diagram

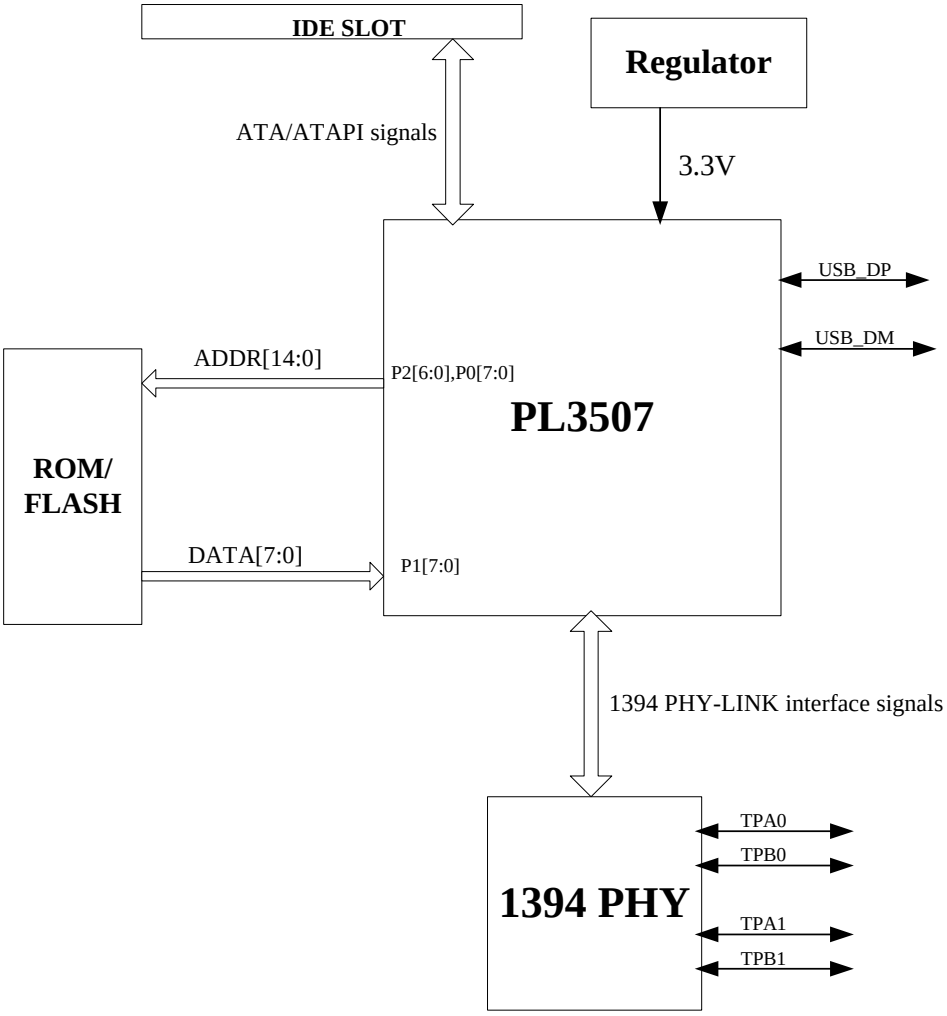


Figure 4-1 System Application Diagram of PL-3507D (Chip Rev D)

5.0 Pin Assignment Outline

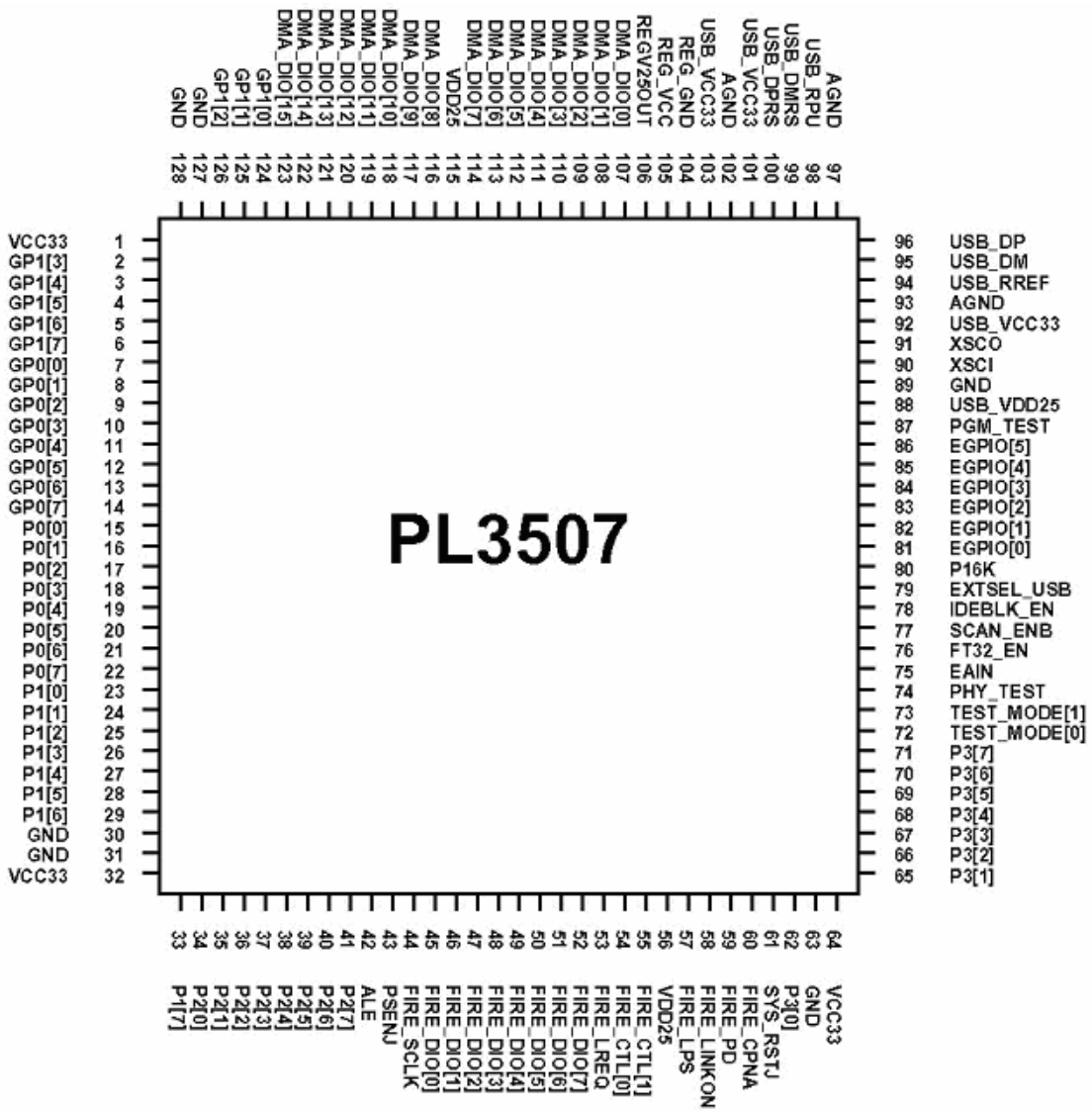


Figure 5-1 Pin Assignment Outline of PL-3507 (Chip Rev D)

6.0 Pin Assignment & Description

6.1 GPIO (ATA / ATAPI Interface)

Table 6-1 Pin Assignment & Description [GPIO (ATA/ATAPI Interface)]

Name	Pin No.	I/O	Description
GP1[0] : IDERSTJ	124	I/O (O)	Reset signal of ATA/ATAPI devices
GP1[1] : DIOWJ	125	I/O (O)	(DIOWJ): For modes other than ultra DMA burst in/out, this is a write strobe signal.
: STOP			(STOP): For ultra DMA burst in/out, host can use this signal to stop ultra DMA burst transfer.
GP1[2] : DIORJ	126	I/O (O)	(DIORJ): For modes other than ultra DMA burst in/out, this is a read strobe signal.
: HDMARDYN			(HDMARDYN): For ultra DMA data in burst, it is asserted by host to indicate to the device that the host is ready to accept ultra DMA burst in data.
: HSSTROBE			(HSSTROBE): For ultra DMA data out burst, this signal is a data strobe signal from host.
GP1[3] : DMACKJ	2	I/O (O)	DMA acknowledge to ATA/ATAPI devices
GP1[4] : IORDY	3	I/O (I)	(IORDY): For PIO mode 3 and above, this signal is negated to extend the transfer cycle of any host ATA register access.
: DDMADRDYN			(DDMADRDYN): For ultra DMA data out burst, it is asserted by ATA device to indicate to the host that the device is ready to accept ultra DMA burst out data.
: DSTROBE			(DSTROBE): For ultra DMA data in burst, this signal is a data strobe signal from device.
GP1[5] : INTRQ	4	I/O (I)	ATA/ATAPI interrupt request
GP1[6] : DMARQ	5	I/O (I)	DMA request from ATA/ATAPI devices
GP1[7] : PROM_ADDR[15]	6	I/O	External ROM/Flash address bit [15]
GP0[0] : DA0	7	I/O (O)	Device address bus, used by host to access a register or data port in the storage device.
GP0[1] : DA1	8	I/O (O)	Device address bus, used by host to access a register or data port in the storage device.
GP0[2] : DA2	9	I/O (O)	Device address bus, used by host to access a register or data port in the storage device.
GP0[3] : CSJ0	10	I/O (O)	Chip select signal from host, used to select the command block registers.
GP0[4] : CSJ1	11	I/O (O)	Chip select signal from host, used to select the control block registers.
GP0[5] : PROM_WR	12	I/O	External flash write signal
GP0[6] : PROM_CE	13	I/O	External flash chip enable signal
GP0[7] : USBVCC	14	I/O	USBVCC input through a 10k resistor
DMA_DIO[0:7]	107~114	I/O	Bidirectional data bus between the host and storage device.
DMA_DIO[8:15]	116~123	I/O	Bidirectional data bus between the host and storage device.

6.2 1394 PHY-Link Interface

Table 6-2 Pin Assignment & Description [1394 PHY-Link Interface]

Name	Pin No.	I/O	Description
FIRE_CTL[0:1]	54~55	I/O	1394 PHY-LINK control bus
FIRE_DIO[0:7]	45~52	I/O	1394 PHY-LINK data bus
FIRE_LREQ	53	O	1394 Link layer request indicator
FIRE_SCLK	44	I	1394 System clock supplied by PHY. 49.152MHz
FIRE_LPS	57	O	1394 Link power status
FIRE_LINKON	58	I	1394 Link power on request signal from PHY
FIRE_PD	59	O	Power down 1394 PHY
FIRE_CPNA	60	I	Cable power status input from 1394 PHY.

6.3 Microcontroller Interface

Table 6-3 Pin Assignment & Description [Microcontroller Interface

Name	Pin No.	I/O	Description
P0[0:7] : PROM_ADDR[0:7]	15~22	I/O (O)	Port 0 or External ROM/FLASH address bus [0:7]
P2[0:6] : PROM_ADDR[8:14]	34~40	I/O (O)	Port 2[0:6] or External ROM/FLASH address bus [8:14].
P2[7] : PROM_OE	41	I/O (O)	Port 2[7] or External ROM/FLASH output enable signal.
P1[0:7]	23~29, 33	I/O (I)	Port 1 or External ROM/FLASH data input bus
P3[0:7]	62, 65~71	I/O	Port 3
ALE	42	I/O	Micro-controller Address latch enable signal
PSENJ	43	I/O	Micro-controller Program storage enable signal
EAIN	75	I	Micro-controller external access signal

6.4 USB Interface

Table 6-4 Pin Assignment & Description [USB Interface]

Name	Pin No.	I/O	Description
USB_DP	96	I/O	USB 2.0 data pin Data+
USB_DM	95	I/O	USB 2.0 data pin Data-
USB_RREF	94	I	Connects to external resistor
USB_RPU	98	I	Connects to external resistor
USB_DPRS	100	I/O	USB 1.1 data pin Data+, connects to external resistor.
USB_DMRS	99	I/O	USB 1.1 data pin Data-, connects to external resistor.
XSCI	90	I	Crystal oscillator input (12 MHz)
XSCO	91	O	Crystal oscillator output (12 MHz)

6.5 Miscellaneous

Table 6-5 Pin Assignment & Description [Miscellaneous]

Name	Pin No.	I/O	Description
SYS_RSTJ	61	I	Reset signal, active low
PGM_TEST	87	I	Program memory test mode
TEST_MODE[0:1]	72~73	I	00: Normal operation mode
PHY_TEST	74	I	USB PHY test mode
FT32_EN	76	I	1: internal 8032 enable 0: internal 8032 disable, use external micro-controller.
SCAN_ENB	77	I	Scan enable signal for scan test modes
SCAN_IN[0]	78	I	Scan test input
EXTSEL_USB	79	I	1: Select USB as active device 0: Select 1394 as active device
P16K	80	I	1: Select 16k bytes of shadow program SRAM size. 0: Select 24k bytes of shadow program SRAM size.

6.6 Regulator

Table 6-6 Pin Assignment & Description [Regulator]

Name	Pin No.	I/O	Description
REG_25VOUT	106	O	Regulator 2.5 Volt output
REG_VCC	105	I	Regulator 3.3 Volt input
REG_GND	104	I	Regulator ground

6.7 Power/Ground Pins

Table 6-7 Pin Assignment & Description [Power/Ground Pins]

Name	Pin No.	I/O	Description
VDD25	56,115	I	2.5 Volt input for core logic
USB_VDD25	88	I	2.5 Volt input for USB PHY logic
VCC33	1,32,64	I	3.3 Volt input for pad cells
USB_VCC33	92, 101, 103	I	3.3 Volt input for USB PHY
GND	30, 31, 63, 89, 127, 128	I	Digital ground pins
AGND	93, 97, 102		Analog ground pins for USB PHY

6.8 Extra GPIO Pins

Table 6-8 Pin Assignment & Description [Extra GPIO Pins]

Name	Pin No.	I/O	Description
EGPIO[0:5]	81~86	I/O	General Purpose I/O pins

7.0 Functional Description

7.1 General Function

The PL-3507 is a combined USB 2.0 and 1394 to ATA/ATAPI bridge controller for connecting host computers to IDE storage devices like Hard Disk and Optical Disk Drive. The PL-3507 has auto-detect capability to provide connections either from USB to ATA/ATAPI or 1394 to ATA/ATAPI devices.

The CPU program code comes from the internal ROM code (Chip Rev 2D only) or external flash device. During power-on of device, the PL-3507 hardware will automatically detect the availability of an external flash device to load the firmware program code instead of the chip internal ROM code.

The external program storage device used are shadowed into internal program SRAM during power on or active device switching, where the instruction codes of “USB “ and “1394” reside in address location “0000h~5ffffh” and “8000h~effffh” separately in the external program devices. At the power on moment, active device is determined by the state of input pin “EXTSEL_USB”, if it’s logic one, the 24k byte instruction codes of external program memory starting from location 0000h will be loaded into internal program memory, otherwise the instruction codes starting from location 8000h will be loaded. When active device is switching due to USB or 1394 cable connection status changes, the corresponding instruction code will be loaded into internal program memory before reset ends.

Only one interface (USB or 1394) can be active at a time to be used for transferring data between host computer and ATA/ATAPI devices. When both two interfaces are connected to the host computer, a “first-come-first-serve” algorithm is used to select the active device. The connection detection of both two interfaces are through cable power from USB cable and 1394 cable, when the connection status changes, interrupts will happen via INT1 to inform the firmware. If both two interfaces (USB and 1394) are connected before power-on, the status of pin “EXTSEL_USB” will determine which interface (USB or 1394) will be active after power-on, if the logic value of “EXTSEL_USB” is one, USB will be the active device, otherwise 1394 will be the active device.

When connecting to host computers through 1394 cable, host will read configuration ROM from the PL-3507 in order to be recognized as a SBP2 storage device, and then host will send login request packets via management ORBs to complete login process. After login is finished, the host computer can start to transfer data to/from ATA/ATAPI devices through the PL-3507 by command ORB packets. The PL-3507 has built in a SBP2 hardware engine that can enhance data transfer rate up to 36 Mbytes/sec.

When connecting to host computers through USB cable, host computer will get device descriptor from the PL-3507 in order to be recognized as a mass storage class device, and then the host can start to transfer data to/from ATA/ATAPI devices through the PL-3507.

7.2 Clock and Reset Module

The Clock and reset module not only control the system clocks for USB, 1394 and 8032, but is also responsible for generating interrupts when USB/1394 connection status changes. At power on instance, the active device is determined by the status of the hardware pin “EXTSEL_USB”, if any connection status changes, an interrupt will be generated to report it. The firmware can read the status from clock configuration register to know the current connection status and make a decision if active device switch is necessary. After the bit “SEL_ACTIVE_DEV” is changed by the firmware, the instruction codes of the new active device will be loaded into the internal program memory and then a system reset will be generated during the loading of instruction codes.

Interrupt 1 is used to report USB/1394 cable connection status with host computer and extra GPIO’s interrupts. If USB/1394 cable connection status changes, an interrupt (CABLE_DINT) will be generated. There are three conditions that will generate such an interrupt:

- The bit status of “DETECT_USB” changes, caused by USB cable plug/unplug.
- The bit status of “DETECT_1394” changes, caused by 1394 cable plug/unplug.
- The bit status of “EXT_SEL_USB” changes, caused by manual switch (optional).

Extra general-purpose input/output (GPIO) pins also have interrupt capability; they can be configured as level/edge trigger type interrupts with positive/negative polarity.

EGPIO[5] is connected to internal USB remote wake-up port that can wake-up the PL-3507 from sleep mode. All the sources of interrupt 1 can wake-up the PL-3507 from sleep mode no matter how PL-3507 went to sleep either from USB or 1394.

When active device is USB, the 1394 related blocks in the PL-3507 are turned-off for saving power, vice versa. In order to consume less power, the firmware can turn off clock source of non-active device. If the active device is USB, firmware can write a logic one value to bit 1 of clock configuration register to turn off 1394 clock source from physical layer chip. If the active device is 1394, the USB clock source from internal USB PHY can be kept running or stopped by USB suspend procedures before switching the active device to 1394.

7.3 Program and External Data Memory

The PL-3507 uses internal ROM code (Chip 2D only) or external flash for CPU program execution. During power on moment, the content of the internal ROM code or external program flash will be shadowed into internal program SRAM for CPU program execution.

The PL-3507 also provides external data memory for firmware to store data or information. Using

shadow SRAM, only 1K bytes external data memory can be used for firmware to store data or information and program size is limited to 23K bytes.

7.4 External Flash Memory Programming Control

In-circuit programming (ICP) via USB cable can be achieved by directly controlling the flash address, control registers and P1 of FT8032 (P1 are used for flash data port). When host sends special commands for programming flash contents, the firmware can use flash address registers for intended address, port1 of FT8032 for intended data and flash control register for read/write control. The starting address of USB firmware code should be located at “0000h” in the external flash, and 1394 firmware code should be at “8000h”.

8.0 DC Characteristics

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	2.5V Power Supply	-0.3 to 3.0	V
	3.3V Power Supply	-0.3 to 3.9	
V_{IN3}	Input Voltage of 3.3V I/O	-0.3 to V_{CC3} +0.3	V
	Input Voltage of 3.3V I/O with 5V Tolerance	-0.3 to 5.5	
T_{STG}	Storage Temperature	-40 to 150	^{o}C

8.2 Recommended Operating Conditions

Table 8-2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DD25}, USB_V_{DD25}	Core Power Supply	2.25	2.5	2.75	V
V_{CC33}	Power Supply of 3.3V I/O	3.0	3.3	3.6	V
USB_V_{CC33}	Power Supply of USB PHY	3.0	3.3	3.6	V
REG_V_{CC}	Power Supply of Regulator	3.0	3.3	3.6	V
REG_25V_{OUT}	Power Supply of Regulator	2.25	2.5	2.75	V
VIN_3	Input Voltage of 3.3V I/O	0	3.3	3.6	V
	Input Voltage of 3.3V I/O with 5V Tolerance	0	3.3	5.25	
T_J	Commercial Junction Operating Temperature	0	25	115	^{o}C

8.3 Leakage Current and Capacitance

Table 8-3 Leakage Current and Capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Leakage Current	No pull-up or pull-down	-10		10	uA
I_{OZ}	Tri-state Leakage Current		-10		10	uA
C_{IN}	Input Capacitance			3.1		pF
C_{OUT}	Output Capacitance			3.1		pF
C_{BID}	Bi-directional Buffer Capacitance			3.1		pF

Note: The capacitances listed above do not include PAD capacitance. One can estimate pin capacitance by adding pad's capacitance that is about 0.1 pf and the package capacitance.

8.4 Recommended Supply Voltage & Operating Junction Temperature Ranges

Table 8-4 Recommended Supply Voltage & Operating Junction Temperature Ranges

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS/LVTTL			0.8	V
V_{IH}	Input High Voltage	CMOS/LVTTL	2.0			V
V_T	Switching Threshold	CMOS/LVTTL		1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage	CMOS/LVTTL	0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage	CMOS/LVTTL		1.6	2.0	V
V_{OL}	Output Low Voltage	IOL=2,4…16 mA			0.4	V
V_{OH}	Output High Voltage	IOL=2,4…16 mA	2.4			V
R_{PU}/ R_{PD}	Input Pull-up/down resistance		40	75	190	

9.0 Ordering Information

Table 9-1 Ordering Information

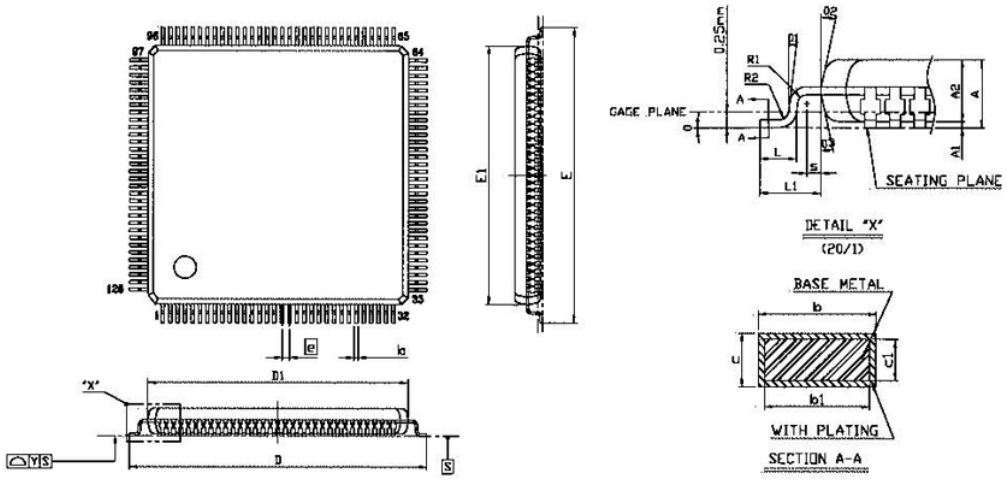
Part Number	Package Type
PL-3507D	128-pin LQFP
PL-3507D-LF	128-pin LQFP Lead-Free

Note: The chip version can be found on the chip-marking showing: "*YYWW2D*" (datecode + chip version).

Where: *YY* – last two digits of the year
WW – week of the year
2D – chip version

Example: "*06102D*" – means year 2006 + week no. 10 + 2D chip version.

10.0 Outline Diagram



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6.3	7.5
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	16.00 BSC			630 BSC		
D1	14.00 BSC			551 BSC		
E	16.00 BSC			630 BSC		
E1	14.00 BSC			551 BSC		
e	0.40 BSC			16 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		

NOTES:
1.REFER TO JEDEC MS-026/BEE REV. B
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

Figure 10-1 Outline Diagram of PL-3507 LQFP128