Advanced Information
Preliminary Datasheet

OV9625 Color CMOS SXGA (1.3 MPixel) CAMERACHIP™
OV9121 B&W CMOS SXGA (1.3 MPixel) CAMERACHIP™

General Description

The OV9625 (color) and OV9121 (black and white) are high-performance 1.3 mega-pixel CAMERACHIPS™ for digital still image and video camera products.

Both devices incorporate a 1280 x 1024 (SXGA) image array and an on-chip 10-bit A/D converter capable of operating at up to 15 frames per second (fps) at full resolution and an improved micro lens design to decrease shading. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. The control registers allow for flexible control of timing, polarity, and CameraChip operation, which, in turn, allows the engineer a great deal of freedom in product design.

Features

- Optical Black Level Calibration (BLC)
- Improved micro lens design to decrease shading
- Video or snapshot operations
- Programmable/Auto Exposure and Gain Control
- Programmable/Auto White Balance Control
- Horizontal and vertical sub-sampling (4:2 and 4:2)
- Programmable image windowing
- Variable frame rate control
- On-chip R/G/B channel and luminance average counter
- Internal/External frame synchronization
- SCCB slave interface
- Power-on reset and power-down mode

Ordering Information

Product	Package
OV09625-C00A (Color, SXGA, VGA)	CLCC-48
OV09121-C00A (B&W with microlens, SXGA, VGA)	CLCC-48

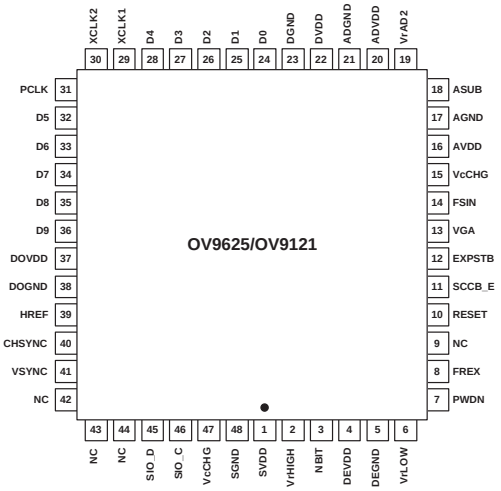
Applications

- Digital still cameras
- PC camera/dual mode
- Video conference applications
- Machine vision
- Security cameras
- Biometrics

Key Specifications

Array Size	**SXGA**	1280 x 1024
	VGA	640 x 480
Power Supply	**Core**	2.5VDC ± 10%
	Analog	3.3VDC ± 10%
	I/O	3.3VDC ± 10%
Power Requirements	**Active**	< 50 mA
	Standby	< 10 µA
Output Formats (10-bit)		Raw RGB Data
Lens Size		1/2"
Max. Image Transfer Rate	**SXGA**	15 fps
	VGA	30 fps
Sensitivity		1.0 V/Lux-sec
S/N Ratio		54 dB
Dynamic Range		60 dB (due to ADC limitations)
Scan Mode		Progressive
Gamma Correction		N/A
Electronics Exposure	**SXGA**	Up to 1050:1
	VGA	Up to 500:1
Pixel Size		5.2 µm x 5.2 µm
Dark Current		28 mV/s
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		6.66 mm x 5.32 mm
Package Dimensions		.560 in. x .560 in.

Figure 1 OV9625/OV9121 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV9625/OV9121 image sensor. The OV9625/OV9121 includes:

- Image Sensor Array (1280 x 1024 resolution)
- Gain Control
- Channel Balance
- 10-Bit Analog-to-Digital Converter
- Black Level Compensation
- SCCB Interface
- Digital Video Port
- Timing Generator

Figure 2 Functional Block Diagram

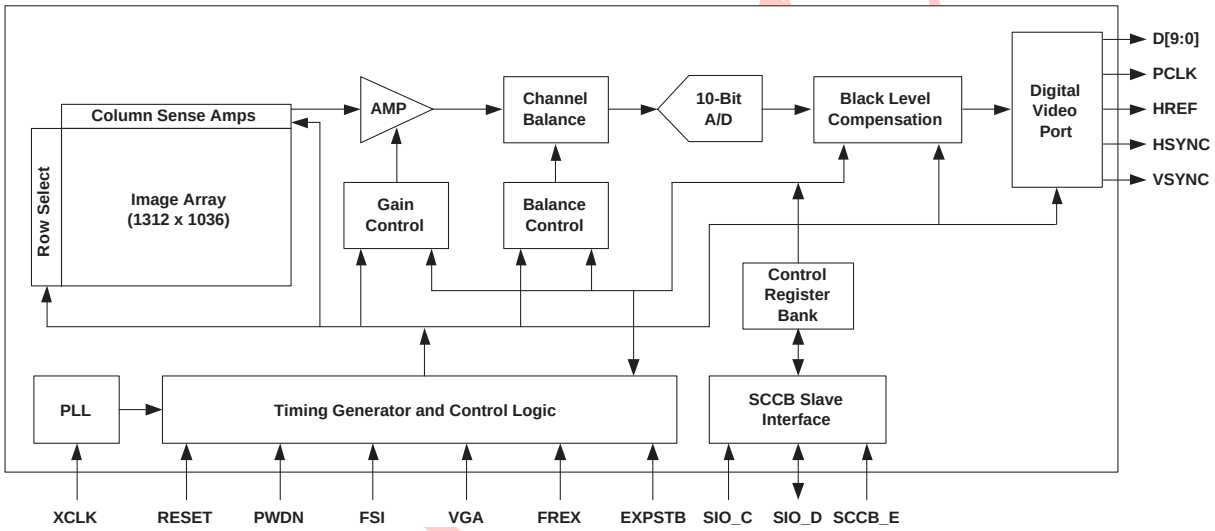
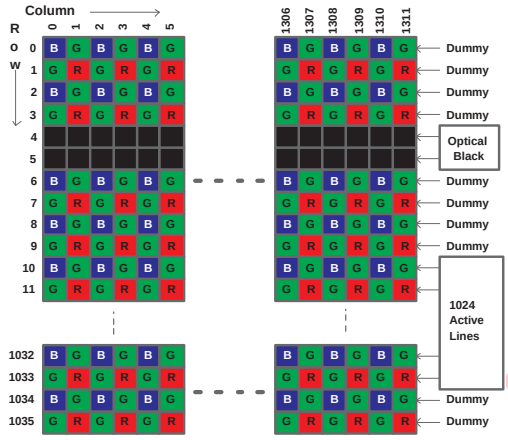


Image Sensor Array

The OV9625/OV9121 sensor is a 1/2-inch format CMOS imaging device. The sensor contains 1,359,232 pixels. Figure 3 shows the active regions of sensor array.

Figure 3 Sensor Array Region



The color filters are Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 1,359,232 pixels, 1,310,720 are active. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

Gain Control

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier. The amplifier gain can either be programmed by the user or controlled by the internal automatic gain control circuit (AGC). The gain adjustment range is 0-24 dB.

Channel Balance

The amplified signals are then balanced with a channel balance block. In this block, Red/Blue channel gain is increased or decreased to match Green channel luminance level and gamma correction is performed. The adjustment range is 54 dB. This function can be done manually by the user or with the internal automatic white balance controller (AWB).

10-Bit Analog-to-Digital Converter

The balanced signal then will be digitized by the on-chip 10-bit ADC. It can operate at up to 12 MHz, and is fully synchronous to the pixel clock. The actual conversion rate is determined by the frame rate.

Black Level Compensation

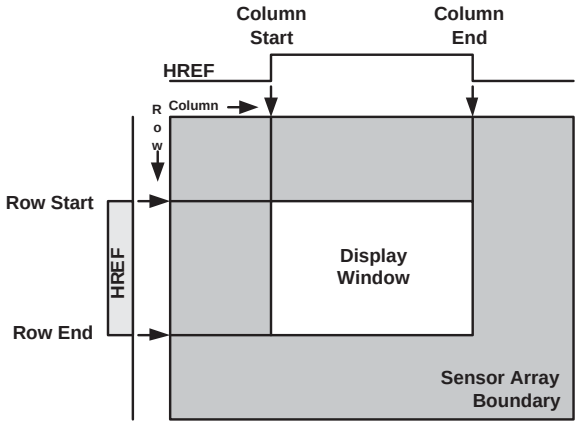
After the pixel data has been digitized, black level calibration can be performed before the data is output. The black level calibration block subtracts the average signal level of optical black pixels to compensate for the dark current in the pixel output. Black level calibration can be disabled by the user.

Windowing

OV9625/OV9121 allows the user to define window size or region of interest (ROI), as required by the application. Window size setting (in pixels) ranges from 2 x 4 to 1280 x 1024 (SXGA) or 2 x 2 to 640 x 480 (VGA), and can be anywhere inside the 1312 x 1036 boundary. Note that modifying window size or window position does not alter the frame or pixel rate. The windowing control merely alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical ROI. The default window size is 1280 x 1024. See Figure 4 and registers HREFST, HREFEND, VSTRT, VEND, and COMM for details. The maximum output window size is 1292 columns by 1024 rows.

Note that after writing to register COMH (0x12) to change the sensor mode, registers related to the sensor's cropping window will be reset back to its default value.

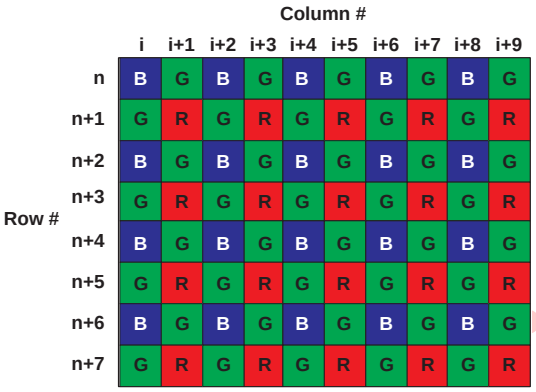
Figure 4 Windowing



Sub-sampling Mode

Default resolution for the OV9625/OV9121 is 1280 x 1024 pixels, with all active pixels being output (see Figure 5). The OV9625/OV9121 can be programmed to output in 640 x 480 (VGA) sized images for applications where higher resolution image capture is not required.

Figure 5 Pixel Array

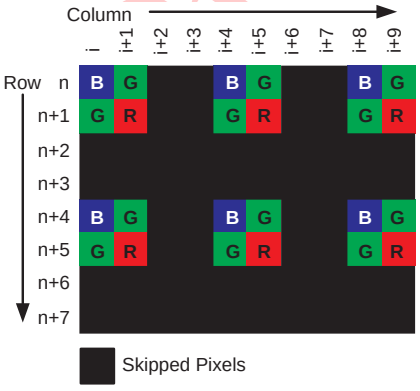


For VGA resolution, the following sub-sampling method is available:

Progressive Sub-sampling

The entire array is sub-sampled for maximal image quality. Both horizontal and vertical pixels are sub-sampled to an aspect ration of 4:2 as illustrated in Figure 6.

Figure 6 Sub-Sampling Mode



Slave Operation Mode

The OV9625/OV9121 can be programmed to operate in slave mode (default is master mode).

When used as a slave device, the OV9625/OV9121 changes the HSYNC and VSYNC outputs to input pins for use as horizontal and vertical synchronization input triggers supplied by the master device. The master device must provide the following signals:

1. System clock MCLK to XCLK1 pin
2. Horizontal sync MHSYNC to CHSYNC pin
3. Vertical frame sync MVSYNC to VSYNC pin

See Figure 7 for slave mode connections and Figure 8 for detailed timing considerations. In this mode, the clock for all devices should be the same. Otherwise, the devices will suffer from flickering at line frequency.

Figure 7 Slave Mode Connection

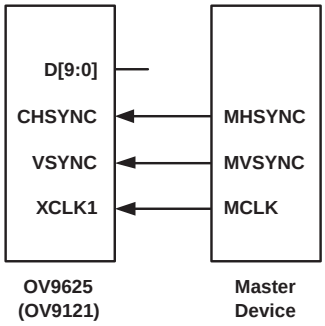
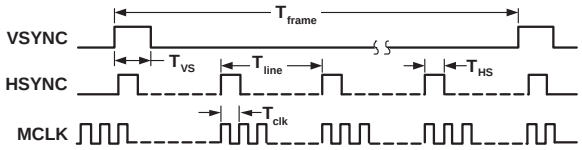


Figure 8 Slave Mode Timing



NOTE:

1) $T_{HS} > 6\ T_{clk}$, Tvs > T_{line}
2) T_{line} = 1520 x T_{clk} (SXGA); T_{line} = 800 x T_{clk} (VGA)
3) T_{frame} = 1050 x T_{line} (SXGA); T_{frame} = 500 x T_{line} (VGA)

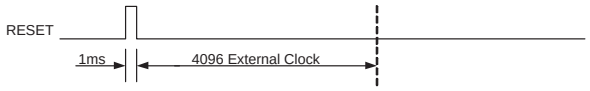
Channel Average Calculator

OV9625/OV9121 provides average output level data for the R/G/B channels along with frame-averaged luminance level. Access to the data is via the serial control port. Average values are calculated from 128 pixels per line (64 in VGA).

Reset

The RESET pin (pin 10) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the RESET pin is low.

Figure 9 RESET Timing Diagram



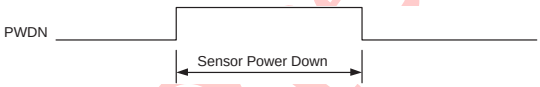
There are two ways for a sensor reset:

1. Hardware reset - Pulling the RESET pin high and keeping it high for at least 1 ms. As shown in Figure 9, after a reset has been initiated, the sensor will be most stable after the period shown as 4096 External Clock.
2. Software reset - Writing 0x80 to register 0x12 (see "COMH" on page 20) for a software reset. If a software reset is used, a reset operation done twice is recommended to make sure the sensor is stable and ready to access registers. When performing a software reset twice, the second reset should be initiated after the 4096 External Clock period as shown in Figure 9.

Power-Down Mode

The PWDN pin (pin 7) is active high. There is an internal pull-down (weak) resistor in the sensor so the default status of the PWDN pin is low.

Figure 10 PWDN Timing Diagram



Two methods of power-down or standby operation are available with the OV9625/OV9121.

- Hardware power-down may be selected by pulling the PWDN pin (pin 7) high (+3.3VDC). When this occurs, the OV9625/OV9121 internal device clock is halted and all internal counters are reset. The current draw is less than 10 µA in this standby mode.
- Software power-down can be effected by setting the COMC[4] register bit high. Standby current will be less then 1 mA when in software power-down. All register content is maintained in standby mode.

SCCB Interface

OV9625/OV9121 provides an on-chip SCCB serial control port that allows access to all internal registers, for complete control and monitoring of OV9625/OV9121 operation.

Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the SCCB interface.

Video Output

RGB Raw Data Output

The OV9625 CAMERACHIP offers 10-bit RGB raw data output.

B&W Output

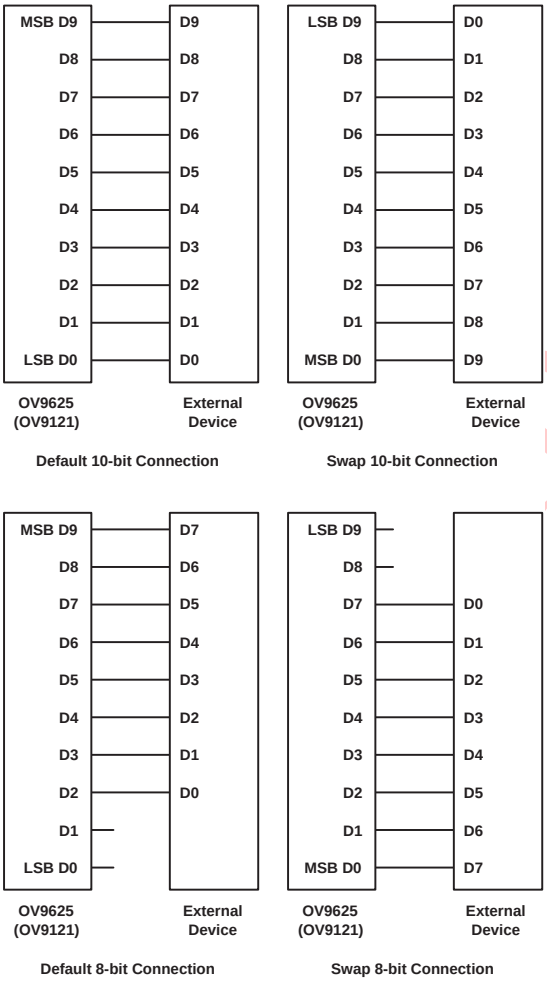
The OV9121 offers 10-bit luminance signal data output.

Digital Video Port

MSB/LSB Swap

OV9625/OV9121 has a 10-bit digital video port. The MSB and LSB can be swapped with the control registers. Figure 11 shows some examples of connections with external devices.

Figure 11 Connection Examples



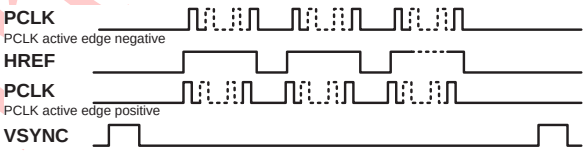
Line/Pixel Timing

The OV9625/OV9121 digital video port can be programmed to work in either master or slave mode.

In both master and slave modes, pixel data output is synchronous with PCLK (or MCLK if port is a slave), HREF and VSYNC. The default PCLK edge for valid data is the negative edge but may be programmed with register COMK[4] (see "COMK" on page 22) for the positive edge. Basic line/pixel output timing is illustrated in Figure 14 and Figure 15.

To minimize image capture circuitry and conserve memory space, PCLK output can be programmed with register COMK[5] (see "COMK" on page 22) to be qualified by the active video period as defined by the HREF signal. See Figure 12 for details.

Figure 12 PCLK Output Only at Valid Pixels



Pixel Output Pattern

Table 1 shows the output data order from the OV9625/OV9121. The data output sequence following the first HREF and after VSYNC is: $B_{0,0}$ $G_{0,1}$ $B_{0,2}$ $G_{0,3}$… $B_{0,1278}$ $G_{0,1279}$. After the second HREF, the output is $G_{1,0}$ $R_{1,1}$ $G_{1,2}$ $R_{1,3}$… $G_{1,1278}$ $R_{1,1279}$…, etc. If the OV9625/OV9121 is programmed to output VGA resolution data, horizontal and vertical sub-sampling will occur. The default output sequence for the first line of output will be: $B_{0,0}$ $G_{0,1}$ $B_{0,4}$ $G_{0,5}$… $B_{0,1276}$ $G_{0,1277}$. The second line of output will be: $G_{1,0}$ $R_{1,1}$ $G_{1,4}$ $R_{1,5}$… $G_{1,1276}$ $R_{1,1277}$.

Table 1 Data Pattern

R/C	0	1	2	3	. . .	1278	1279
0	$B_{0,0}$	$G_{0,1}$	$B_{0,2}$	$G_{0,3}$	. . .	$B_{0,1278}$	$G_{0,1279}$
1	$G_{1,0}$	$R_{1,1}$	$G_{1,2}$	$R_{1,3}$	. . .	$G_{1,1278}$	$R_{1,1279}$
2	$B_{2,0}$	G_2	$B_{2,2}$	$G_{2,3}$	. . .	$B_{2,1278}$	$G_{2,1279}$
3	$G_{3,0}$	$R_{3,1}$	$G_{3,2}$	$R_{3,3}$	. . .	$G_{3,1278}$	$R_{3,1279}$
. .					. .		
1022	$B_{1022,0}$	$G_{1022,1}$	$B_{1022,2}$	$G_{1022,3}$		$B_{1022,1278}$	$G_{1022,1279}$
1023	$G_{1023,0}$	$R_{1023,1}$	$G_{1023,2}$	$R_{1023,3}$		$G_{1023,1278}$	$R_{1023,1279}$

Timing Generator

In general, the timing generator controls the following functions:

- Frame Exposure Mode Timing
- Frame Rate Timing
- Frame Rate Adjust

Frame Exposure Mode Timing

OV9625/OV9121 supports frame exposure mode. Typically the frame exposure mode must work with the aid of an external shutter.

The frame exposure pin, FREX (pin 8) is the frame exposure mode enable pin and EXPSTB (pin 12) serves as the exposure start trigger for the sensor. There are two ways to set Frame Exposure mode:

- Control both FREX and EXPSTB pins - Frame Exposure mode can be set by pulling both FREX and EXPSTB pins high at the same time (see Figure 19).
- Control FREX only and keep EXPSTB low - In this case, the pre-charge time is tline and sensor exposure time is the period after pre-charge until the shutter closes (see Figure 18).

When the external master device asserts the FREX pin high, the sensor array is quickly pre-charged and stays in reset mode until the EXPSTB pin is pulled low by the external master (sensor exposure time can be defined as the period between EXPSTB low to shutter close). After the FREX pin is pulled low, the video data stream is then clocked to the output port in a line-by-line manner. After completing one frame of data output, OV9625/OV9121 will output continuous live video data unless in single frame transfer mode. Figure 18 and Figure 19 show the detailed timing for this mode.

For frame exposure, register AEC (0x10) must be set to 0xFF and register GAIN (0x00) should be no larger than 0x10 (maximum 2x gain).

Frame Rate Timing

Default frame timing is illustrated in Figure 16 and Figure 17. Refer to Table 2 for the actual pixel rate at different frame rates.

Table 2 Frame and Pixel Rates

Frame Rage (fps)	15	10	7.5	6	5
PCLK (MHz)	24	16	12	9.6	8
NOTE: Based on 24 MHz external clock and internal PLL on, frame rate is adjusted by the main clock divide method.					

Frame Rate Adjust

OV9625/OV9121 offers three methods of frame rate adjustment.

1. Clock prescaler (see "CLKRC" on page 20)
   By changing the system clock divide ratio, the frame rate and pixel rate will change together. This method can be used for dividing the frame/pixel rate by: 1/2, 1/3, 1/4 … 1/64 of the input clock rate.
2. Line adjustment (see "COML" on page 24 and see "FRARL" on page 25)
   By adding dummy pixel timing in each line, the frame rate can be changed while leaving the pixel rate as is.
3. Vertical sync adjustment
   By adding dummy line periods to the vertical sync period (see "ADDVSL" on page 25 and see "ADDVSH" on page 25), the frame rate can be altered while the pixel rate remains the same.

After changing registers COML (0x2A) and FRARL (0x2B) to adjust the dummy pixels, it is necessary to write to register COMH (0x12) or CLKRC (0x11) to reset the counter. Generally, OmniVision suggests users write to register COMH (0x12) (to change the sensor mode) as the last one. However, if you want to adjust the cropping window, it is necessary to write to those registers after changing register COMH (0x12). To use COMH to reset the counter, it is necessary to generate a pulse on resolution control register bit COMH[6].

Pin Description

Table 3 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	SVDD	Power	3.3 V power supply for the pixel array
02	VrHIGH	Analog	Sensor high reference - bypass to ground using a 0.1 µF capacitor
03	NBIT	Analog	Sensor bit line reference - bypass to ground using a 0.1 µF capacitor
04	DEVDD	Power	3.3 V power supply for the sensor array decoder
05	DEGND	Power	Ground for the sensor array decoder
06	VrLOW	Analog	Sensor low reference - bypass to ground using a 0.1 µF capacitor
07	PWDN	Input (0)[a]	Power down mode enable, active high
08	FREX	Input (0)	Snapshot trigger, used to activate a snapshot sequence
09	NC	—	No connection
10	RESET	Input (0)	Chip reset, active high
11	SCCB_E	Input (0)	SCCB interface enable, active low
12	EXPSTB	Input (0)	Snapshot exposure start trigger 0: Sensor starts exposure - only effective in snapshot mode 1: Sensor stays in reset mode
13	VGA	Input (0)	Sensor Resolution Selection 0: SXGA resolution (1280 x 1024) 1: VGA resolution (640 x 480)
14	FSIN	Input (0)	Frame synchronization input
15	VcCHG	Analog	Sensor reference - bypass to ground using a 1 µF capacitor
16	AVDD	Power	3.3 V power supply for analog circuits
17	AGND	Power	Ground for analog circuits
18	ASUB	Power	Ground for analog circuit substrate
19	VrAD2	Analog	A/D converter reference - bypass to ground using a 0.1 µF capacitor
20	ADVDD	Power	3.3 V power supply for A/D converter
21	ADGND	Power	Ground for A/D converter
22	DVDD	Power	2.5 V power supply for digital circuits
23	DGND	Power	Ground for digital circuits
24	D0	Output	Digital video output bit[0]
25	D1	Output	Digital video output bit[1]
26	D2	Output	Digital video output bit[2]
27	D3	Output	Digital video output bit[3]
28	D4	Output	Digital video output bit[4]

Table 3 Pin Description (Continued)

Pin Number	Name	Pin Type	Function/Description
29	XCLK1	Input	Crystal clock input
30	XCLK2	Output	Crystal clock output
31	PCLK	Output	Pixel clock output
32	D5	Output	Digital video output bit[5]
33	D6	Output	Digital video output bit[6]
34	D7	Output	Digital video output bit[7]
35	D8	Output	Digital video output bit[8]
36	D9	Output	Digital video output bit[9]
37	DOVDD	Power	3.3 V power supply for digital video port
38	DOGND	Power	Ground for digital video port
39	HREF	Output	Horizontal reference output
40	CHSYNC	Output	Horizontal synchronization output when chip is in master mode.
41	VSYNC	Output	Vertical synchronization output when chip is in master mode.
42	NC	—	No connection
43	NC	—	No connection
44	NC	—	No connection
45	SIO_D	I/O	SCCB serial interface data I/O
46	SIO_C	Input	SCCB serial interface clock input
47	VcCHG	Analog	Sensor reference - bypass to ground using a 1 µF capacitor
48	SGND	Power	Ground for pixel array.

a. Input (0) represents an internal pull-down low resistor.

Electrical Characteristics

Table 4 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +125ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	3.3V
	V_{DD-C}	2.5V
	V_{DD-IO}	3.3V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+1V
Lead Temperature, Surface-mount process		+230ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 5 DC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD-A}	Supply voltage (DEVDD, ADVDD, AVDD, SVDD)	3.0	3.3	3.6	V
V_{DD-IO}	Supply voltage (DOVDD)	3.0	3.3	3.6	V
V_{DD-C}	Supply voltage (DVDD)	2.25	2.5	2.75	V
I_{DD1}	Active (Operating) Current		40	60	mA
I_{DD2}	Standby Current		1		mA
I_{DD3}	Standby Current		10		µA
Digital Inputs					
V_{IL}	Input voltage LOW			0.8	V
V_{IH}	Input voltage HIGH	2			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3 V)					
V_{OH}	Output voltage HIGH	2.4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB Inputs					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	2.5	3.3	V_{DD} + 0.5	V

Table 6 AC Characteristics (T_A = 25°C, V_{DD} = 3V)

Symbol	Parameter	Min	Typ	Max	Unit
ADC Parameters					
B	Analog bandwidth		12		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	Settling time for hardware reset			<1	ms
	Settling time for software reset			<1	ms
	Settling time for VGA/XSGA mode change			<1	ms
	Settling time for register setting			<300	ms

Table 7 Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Oscillator and Clock Input					
f_{OSC}	Frequency (XCLK1, XCLK2)	8	24	48	MHz
t_r, t_f	Clock input rise/fall time			2	ns
	Clock input duty cycle	45	50	55	%

Timing Specifications

Figure 13 SCCB Timing Diagram

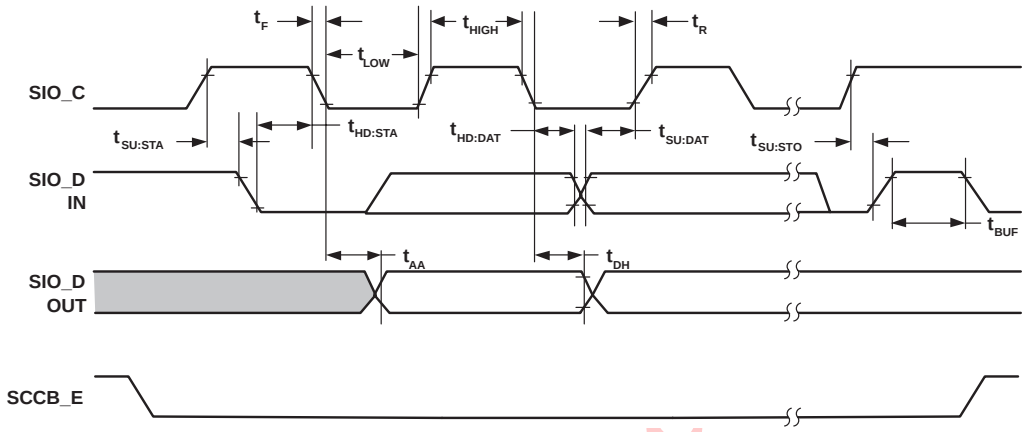


Table 8 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 14 SXGA Line/Pixel Output Timing

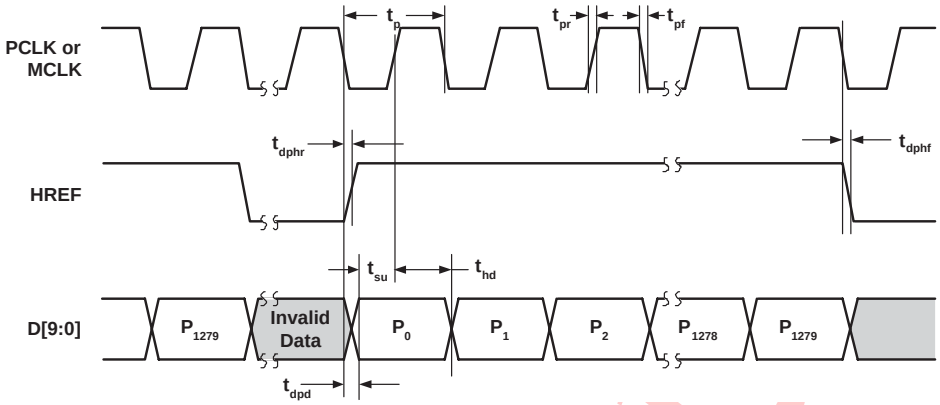


Figure 15 VGA Line/Pixel Output Timing

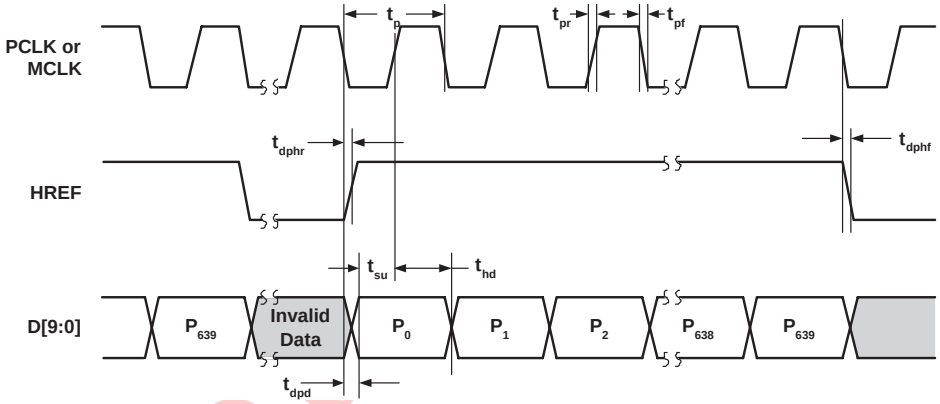


Figure 16 SXGA Frame Timing

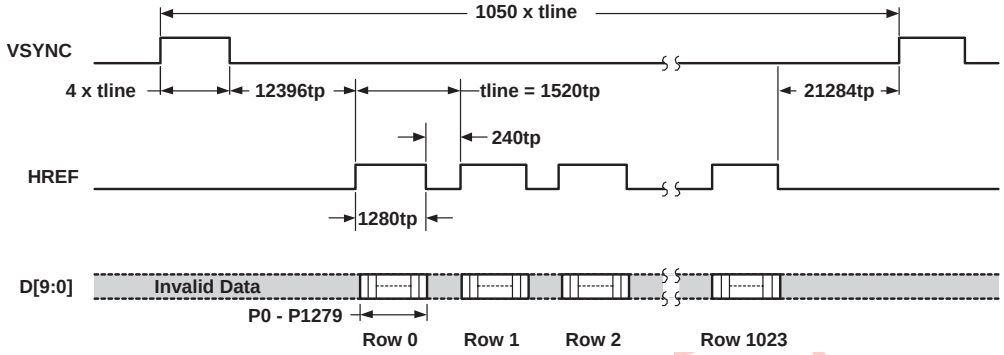
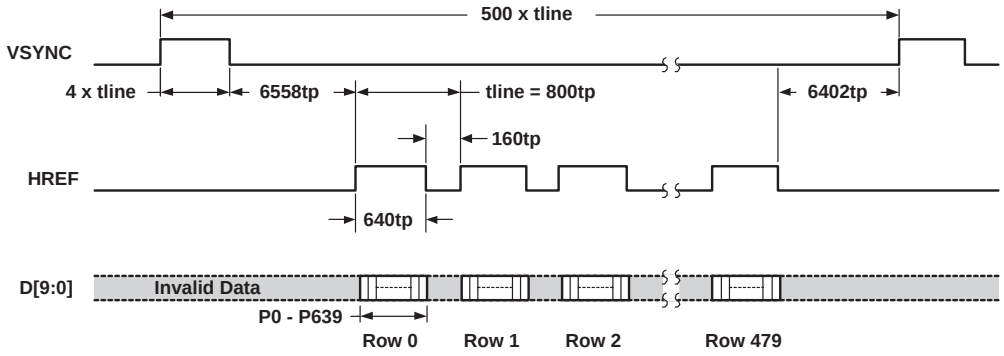


Figure 17 VGA Frame Timing



The specifications shown in Table 9 apply for DVDD = +2.5V, DOVDD = +3.3V, T_A = 25°C, sensor working at 15 fps, external loading = 30 pF.

Table 9 Pixel Timing Specification

Symbol	Parameter	Min	Typ	Max	Unit
t_p	PCLK period			20.83	ns
t_{pr}	PCLK rising time		10		ns
t_{pf}	PCLK falling time		5		ns
t_{dphr}	PCLK negative edge to HREF rising edge	0		5	ns
t_{dphf}	PCLK negative edge to HREF negative edge	0		5	ns
t_{dpd}	PCLK negative edge to data output delay	0		5	ns
t_{su}	Data bus setup time	15			ns
t_{hd}	Data bus hold time	8			ns

Figure 18 Frame Exposure Timing with EXPSTB Staying Low

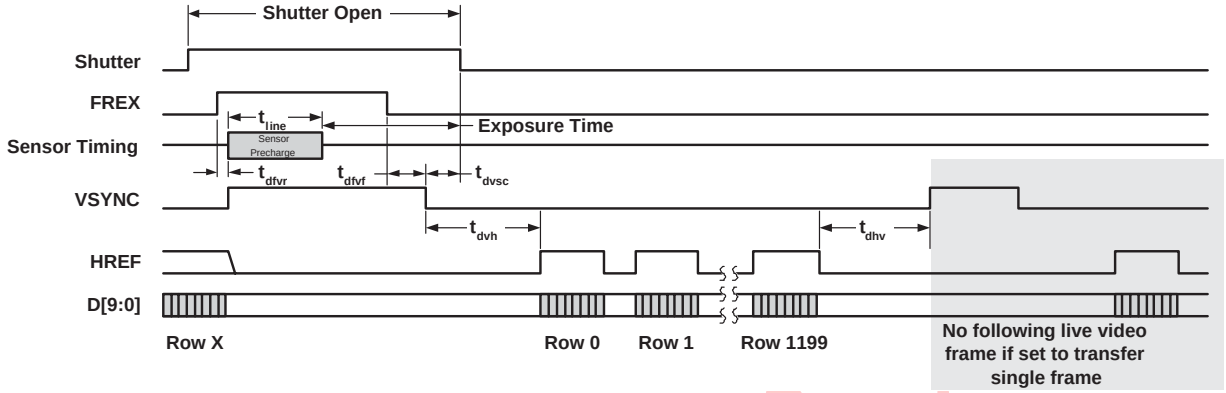


Figure 19 Frame Exposure Timing with EXPSTB Asserted

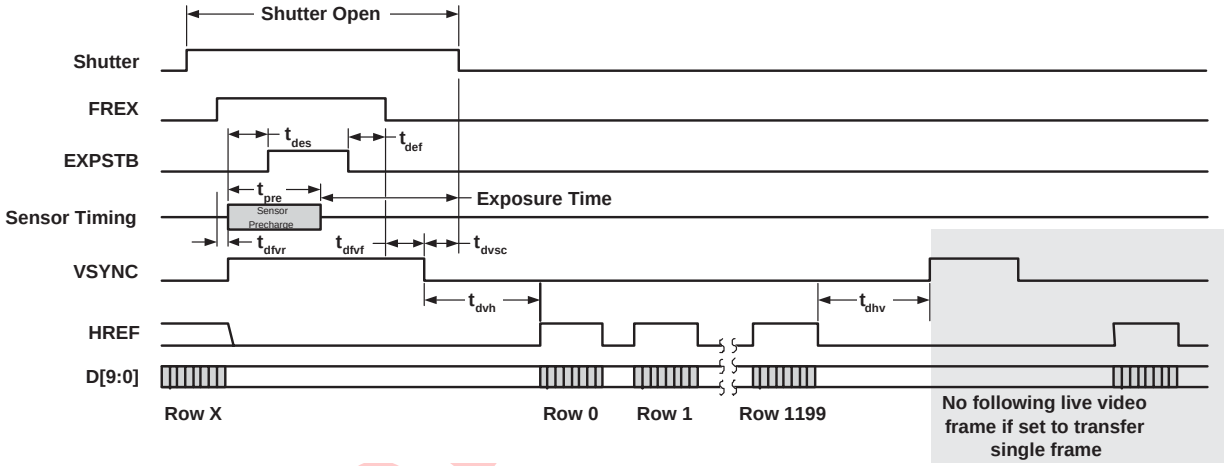


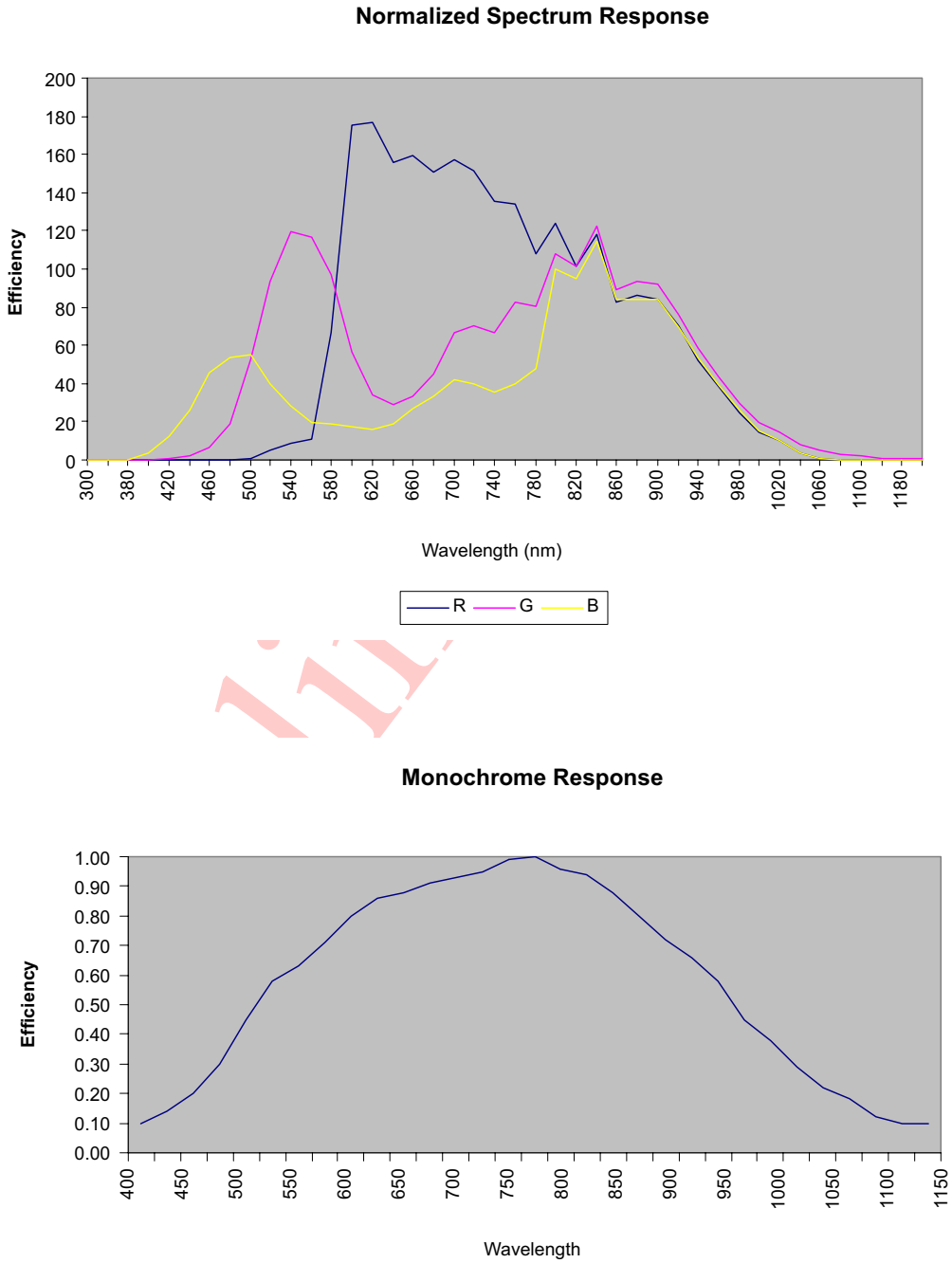
Table 10 Frame Exposure Timing Specifications

Symbol	Min	Typ	Max	Unit
tline		1520 (SXGA)		tp
		800 (VGA)		tp
tvs		4		tline
tdfvr	8		9	tp
tdfvf			4	tline
tdvsc			2	tline
tdhv		21044 (SXGA)		tp
		6402 (VGA)		tp
tdvh		12396 (SXGA)		tp
		6558 (VGA)		tp
tdes			1500 (SXGA)	tp
			780 (VGA)	tp

NOTE 1) FREX must stay high long enough to ensure the entire sensor has been reset.
2) Shutter must be closed no later then 3040tp (1600tp for VGA) after VSYNC falling edge.

OV9625/OV9121 Light Response

Figure 20 OV9625/OV9121 Light Response



Register Set

Table 11 provides a list and description of the Device Control registers contained in the OV9625/OV9121. The device slave addresses are 60 for write and 61 for read.

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain Control Bit[7:6]: Reserved Bit[5:0]: Gain control gain setting • Range: 1x to 8x Set COMI[0] = 0 (see "COMI" on page 21) to disable AGC
01	BLUE	80	RW	Blue gain control MSB, 8 bits (LSB 2 bits in COMA[3:2], see "COMA" on page 17) ***Note:*** *This function is not available on the B&W OV9121.*
02	RED	80	RW	Red gain control MSB, 8 bits (LSB 2 bits in COMA[1:0], see "COMA" on page 17) ***Note:*** *This function is not available on the B&W OV9121.*
03	COMA	40	RW	Common Control A Bit[7:4]: AWB update threshold Bit[3:2]: BLUE channel lower 2 bits gain control Bit[1:0]: RED channel lower 2 bits gain control ***Note:*** *This function is not available on the B&W OV9121.*
04	COMB	00	RW	Common Control B Bit[7,4]: AWB – Update speed select 00: Slow 01: Slowest 10: Fast 11: Fast Bit[6:5]: AWB – Step select 00: 1023 steps 01: 255 steps 10: 511 steps 11: 255 steps Bit[3]: Reserved Bit[2:0]: AEC lower 3 bits, AEC[2:0] (see "AEC" on page 19 for most significant 8 bits, AEC[10:3])
05	BAVG	00	RW	B Channel Average
06	GbAVG	00	RW	G Channel Average - picked G pixels in the same line with B pixels.
07	GrAVG	00	RW	G Channel Average - picked G pixels in the same line with R pixels.
08	RAVG	00	RW	R Channel Average

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	COMC	0C	RW	Common Control C Bit[7:5]: Reserved Bit[4]: Sleep or power-down mode enable 0: Normal 1: Sleep mode Bit[3:2]: Crystal oscillator output current 00: Weakest 11: Strongest Bit[1:0]: Output Drive Select 00: Weakest 01: Double capability 10: Double capability 11: Triple drive current
0A	PIDH	96	R	Product ID Number MSB (Read only)
0B	PIDL	B1	R	Product ID Number LSB (Read only)
0C	COMD	28	RW	Common Control D Bit[7]: Reserved Bit[6]: Swap MSB and LSB at the output port Bit[5:2]: Reserved Bit[1]: Sensor precharge voltage selection 0: Selects internal reference as precharge voltage 1: Selects SVDD as precharge voltage Bit[0]: Snapshot option 0: Enable live video output after snapshot sequence 1: Output single frame only
0D	COME	00	RW	Common Control E Bit[7]: Reserved Bit[6]: Anti-blooming control 0: Anti-blooming ON 1: Anti-blooming OFF Bit[5:3]: Reserved Bit[2]: Clock output power-down pin status 0: Maintain internal default states at power-down 1: Tri-state the VSYNC and CHSYNC pins upon power-down Bit[1]: Reserved Bit[0]: Digital port output 0: Enable data port output 1: Disable data port output

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0E	COMF	01	RW	Common Control F Bit[7]: System clock selection 0: Use 24 MHz system clock 1: Use 48 MHz system clock Bit[6:3]: Reserved Bit[2]: Port output range selection 0: Output data range is [001] to [3FE] 1: Output data range is [000] to [3FF] Bit[1]: Reserved Bit[0]: AEC option 0: Disable this function 1: Enable larger AEC step increase with correct exposure time
0F	COMG	47	RW	Common Control G Bit[7]: Optical black output selection 0: Disable 1: Enable Bit[6]: Black level calibrate selection 0: Use electrical black reference 1: Use optical black pixels to calibrate Bit[5:4]: Reserved Bit[3]: Channel offset adjustment 0: Disable offset adjustment 1: Enable offset adjustment, B/Gb/Gr/R channel offset levels stored in registers RBIAS (see "BBIAS" on page 24), GbBIAS (see "GbBIAS" on page 24), GrBIAS (see "GrBIAS" on page 24) and RBIAS (see "RBIAS" on page 25). Bit[2]: Data range selection 0: Data range limited to [010] to [3F0] 1: Full range Bit[1]: ADC black level calibration bias selection 0: 040 1: 010 Bit[0]: ADC black level calibration enable 0: Disable 1: Enable
10	AEC	43	RW	Automatic Exposure Control Most Significant 8 bits for AEC[10:3] (least significant 3 bits, AEC[2:0], in register COMB[2:0] - see "COMB" on page 17). AEC[10:0]: Exposure time $T_{EX} = t_{LINE}$ x AEC[10:0] Set COMI[2] = 0 (see "COMI" on page 21) to disable the AEC.

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
11	CLKRC	00	RW	Clock Rate Control Bit[7]: Internal PLL ON/OFF selection 0: PLL disabled 1: PLL enabled Bit[6]: Digital video port master/slave selection 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XCLK1 pin Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLKRC[5:0] + 1)
12	COMH	20	RW	Common Control H Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6]: Resolution selection 0: SXGA 1: VGA Bit[5]: Average luminance value pixel counter ON/OFF 0: OFF 1: ON Bit[4]: Reserved Bit[3]: Master/slave selection 0: Master mode 1: Slave mode Bit[2]: Window output selection 0: Output only pixels defined by window registers 1: Output all pixels Bit[1]: Color bar test pattern 0: OFF 1: ON Bit[0]: Reserved

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COMI	07	RW	Common Control I Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: AEC speed/step selection 0: Small steps (slow) 1: Big steps (fast) Bit[5]: Banding filter ON/OFF 0: OFF 1: ON, set minimum exposure to 1/120s Bit[4]: Banding filter option 0: Set to 0, if system clock is 48 MHz and the PLL is ON. 1: Set to 1, if system clock is 24 MHz and the PLL is ON or if the system clock is 48 MHz and the PLL is OFF. Bit[3]: Reserved Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14	COMJ	76	RW	Common Control J Bit[7:6]: AGC gain ceiling 00: 2x 01: 4x 10: 8x 11: 8x Bit[5:4]: Reserved Bit[3]: Auto banding filter 0: Banding filter is always ON/OFF depending on COMI[5] setting (see “COMI” on page 21) 1: Automatically disable banding filter if light is low Bit[2]: VSYNC drop option 0: VSYNC is always output 1: VSYNC is dropped if frame data is dropped Bit[1]: Frame data drop option 0: Disable data drop 1: Drop data frame if exposure is not within tolerance. In AEC mode, data is normally dropped when data is out of range Bit[0]: Freeze current Exposure and Gain values 0: Normal 1: Freeze

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COMK	00	RW	Common Control K Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK edge selection 0: Data valid on PCLK falling edge 1: Data valid on PCLK rising edge Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative
16	RSVD	XX	–	Reserved
17	HREFST	1D (13 in VGA)	RW	Horizontal Window Start Most Significant 8 bits, LSB in register COMM[1:0] (see "COMM" on page 26). HREFST[9:0]: Selects the beginning of the horizontal window, each LSB represents two pixels. Adjustment steps must be 2 pixels. ***Note:*** *1. HFREFST[9:0] should be less than HREFEND[9:0].* *2. For maximum output window size of 1292x1024, minimum value of this register is 0x1C.*
18	HREFEND	BD (63 in VGA)	RW	Horizontal Window end most significant 8 bits, LSB in register COMM[3:2] (see "COMM" on page 26). HREFEND[9:0]: Selects the end of the horizontal window, each LSB represents two pixels. Adjustment steps must be 2 pixels. ***Note:*** *1. HREFEND[9:0] should be larger than HREFST[9:0].* *2. For maximum output window size of 1292x1024, maximum value of this register is 0xBD.*

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
19	VSTRT	01 (02 in VGA)	RW	Vertical Window line start most significant 8 bits, LSB in register COMM[4] (see "COMM" on page 26). Bit[8:0]: Selects the start of the vertical window, each LSB represents four scan lines in SXGA or two scan lines in VGA. ***Note:*** *1. VSTRT[8:0] should be less than VEND[8:0].* *2. For maximum output window size of 1292x1024, minimum value of this register is 0x01.*
1A	VEND	81 (7A in VGA)	RW	Vertical Window line end most significant 8 bits, LSB in register COMM[5] (see "COMM" on page 26). Bit[8:0]: Selects the end of the vertical window, each LSB represents four scan lines in SXGA and two scan lines in VGA. ***Note:*** *1. VEND[8:0] should be larger than VSTRT[8:0].* *2. For maximum output window size of 1292x1024, maximum value of this register is 0x81.*
1B	PSHFT	00	RW	Pixel Shift Bit[7:0]: Pixel delay count. Provides a method to fine tune the output timing of the pixel data relative to the HREF pulse. It physically shifts the video data output time in units of pixel clock counts. The largest delay count is [FF] and is equal to 255 x PCLK.
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-1F	RSVD	XX	–	Reserved
20	BOFF	10	RW	B Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 (see "COMG" on page 19) Bit[7]: Offset direction 0: Add BOFF[6:0] 1: Subtract BOFF[6:0] Bit[6:0]: B channel offset adjustment value
21	GbOFF	0F	RW	Gb Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 (see "COMG" on page 19) Bit[7]: Offset direction 0: Add GbOFF[6:0] 1: Subtract GbOFF[6:0] Bit[6:0]: Gb channel offset adjustment value
22	GrOFF	EF	RW	Gr Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 (see "COMG" on page 19) Bit[7]: Offset direction 0: Add GrOFF[6:0] 1: Subtract GrOFF[6:0] Bit[6:0]: Gr channel offset adjustment value

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
23	ROFF	EF	RW	R Channel Offset Adjustment - auto controlled by internal circuit if COMG[0] = 1 (see "COMG" on page 19) Bit[7]: Offset direction 0: Add ROFF[6:0] 1: Subtract ROFF[6:0] Bit[6:0]: R channel offset adjustment value
24	AEW	A0	RW	Luminance Signal High Range for AEC/AGC Operation AEC/AGC values will decrease in auto mode when average luminance is greater than AEW[7:0]
25	AEB	88	RW	Luminance Signal Low Range for AEC/AGC Operation AEC/AGC values will increase in auto mode when average luminance is less than AEB[7:0].
26	VV	F4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode (COMI[7] = 1, see "COMI" on page 21) Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0].
27	BBIAS	80	RW	B Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 (see "COMG" on page 19). Bit[7]: Offset direction 0: Add BBIAS[6:0] 1: Subtract BBIAS[6:0] Bit[6:0]: B channel offset adjustment value
28	GbBIAS	80	RW	Gb Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 (see "COMG" on page 19). Bit[7]: Offset direction 0: Add GbBIAS[6:0] 1: Subtract GbBIAS[6:0] Bit[6:0]: Gb channel offset adjustment value
29	GrBIAS	80	RW	Gr Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 (see "COMG" on page 19). Bit[7]: Offset direction 0: Add GrBIAS[6:0] 1: Subtract GrBIAS[6:0] Bit[6:0]: Gr channel offset adjustment value
2A	COML	00	RW	Common Control L Bit[7]: Line interval adjustment. Interval adjustment value is in COML[6:5] and FRARL[7:0] (see "FRARL" on page 25). 0: Disabled 1: Enabled Bit[6:5]: Line interval adjust value MSB 2 bits Bit[4]: Reserved Bit[3:2]: HSYNC timing end point adjustment MSB 2 bits Bit[1:0]: HSYNC timing start point adjustment MSB 2 bits

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2B	FRARL	00	RW	Line Interval Adjustment Value LSB 8 bits The frame rate will be adjusted by changing the line interval. Each LSB will add 2/1520 T_{frame} in SXGA and 2/800 T_{frame} in VGA mode to the frame period.
2C	RBIAS	80	RW	R Channel Offset Manual Adjustment Value - effective only when COMG[3] = 1 (see "COMG" on page 19). Bit[7]: Offset direction 0: Add RBIAS[6:0] 1: Subtract RBIAS[6:0] Bit[6:0]: R channel offset adjustment value
2D	ADDVSL	00	RW	VSYNC Pulse Width LSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each LSB count will add 1 x t_{line} to the VSYNC active period.
2E	ADDVSH	00	RW	VSYNC Pulse width MSB 8 bits Bit[7:0]: Line periods added to VSYNC width. Default VSYNC output width is 4 x t_{line}. Each MSB count will add 256 x t_{line} to the VSYNC active period.
2F	YAVG	00	RW	Luminance Average This register will auto update when COMH[5] = 1 (see "COMH" on page 20). Average Luminance is calculated from the B/Gb/Gr/R channel average as follows: (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] +RAVG[7:0])/4
30	HSDY	08	RW	HSYNC Position and Width Start Point Lower 8 bits This register and COML[1:0] (see "COML" on page 24) define the HSYNC start position, each LSB will shift HSYNC start point by 1 pixel period.
31	HEDY	30	RW	HSYNC Position and Width End Point Lower 8 bits This register and COML[3:2] (see "COML" on page 24) define the HSYNC start position, each LSB will shift HSYNC start point by 1 pixel period.

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
32	COMM	0A (0Ffor VGA)	RW	Common Control M Bit[7:6]: Reserved Bit[5]: Vertical window end position LSB (MSBs in register VEND[7:0] - see "VEND" on page 23) Bit[4]: Vertical window start position LSB (MSBs in register VSTRT[7:0] - see "VSTRT" on page 23) Bit[3:2]: Horizontal window end position LSBs (MSBs in register HREFST[7:0] - see "HREFEND" on page 22) Bit[1:0]: Horizontal window start position LSBs (MSBs in register HREFST[7:0] - see "HREFST" on page 22) ***Note:*** *For maximum output window size of 1292x1024, value of this register should be 0x0D.*
33	CHLF	28	RW	Current Control Bit[7:6]: Sensor current control 00: Minimum 11: Maximum Bit[5]: Sensor current range control 0: CHLF[7:6] current control at normal range 1: CHLF[7:6] current at half range Bit[4]: Sensor current double ON/OFF 0: Normal 1: Double current Bit[3]: Sensor buffer current control 0: Normal 1: Half current Bit[2]: Column buffer current control 0: Normal 1: Half current Bit[1]: Analog DSP current control 0: Normal 1: Half current Bit[0]: ADC current control 0: Normal 1: Half current
34	RSVD	XX	–	Reserved
35	VBLM	90	RW	Reference Voltage Control
36	VCHG	17	RW	Sensor Precharge Voltage Control Bit[7]: Reserved Bit[6:4]: Sensor precharge voltage control 000: Lowest voltage 111: Highest voltage Bit[3:0]: Sensor array common reference control 000: Lowest voltage 111: Highest voltage

Table 11 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
37	ADC	04	RW	ADC Reference Control Bit[7:4]: Reserved Bit[3]: ADC input signal range 0: Input signal x 1 1: Input signal x 0.7 Bit[2:0]: ADC range control 000: Minimum 111: Maximum
38	ACOM	12	RW	Analog Common Control Bit[7]: Analog gain control 0: Normal 1: Gain increase 1.5x Bit[6]: Analog black level calibration control 0: Analog BLC ON 1: Analog BLC OFF Bit[5:0]: Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV9625/OV9121 uses a 48-pin ceramic package. Refer to Figure 21 for package information and Figure 22 for the array center on the chip.

Figure 21 OV9625/OV9121 Package Specifications

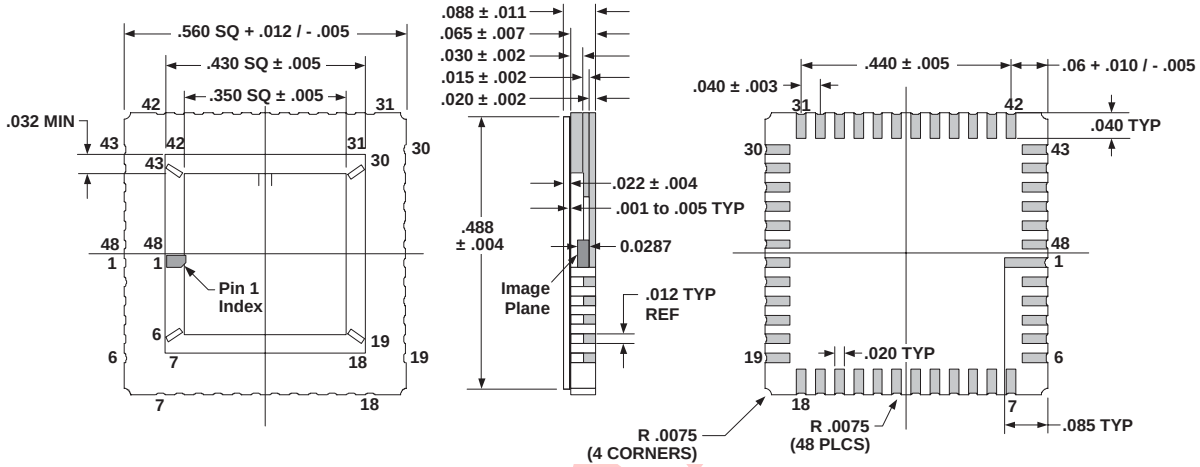
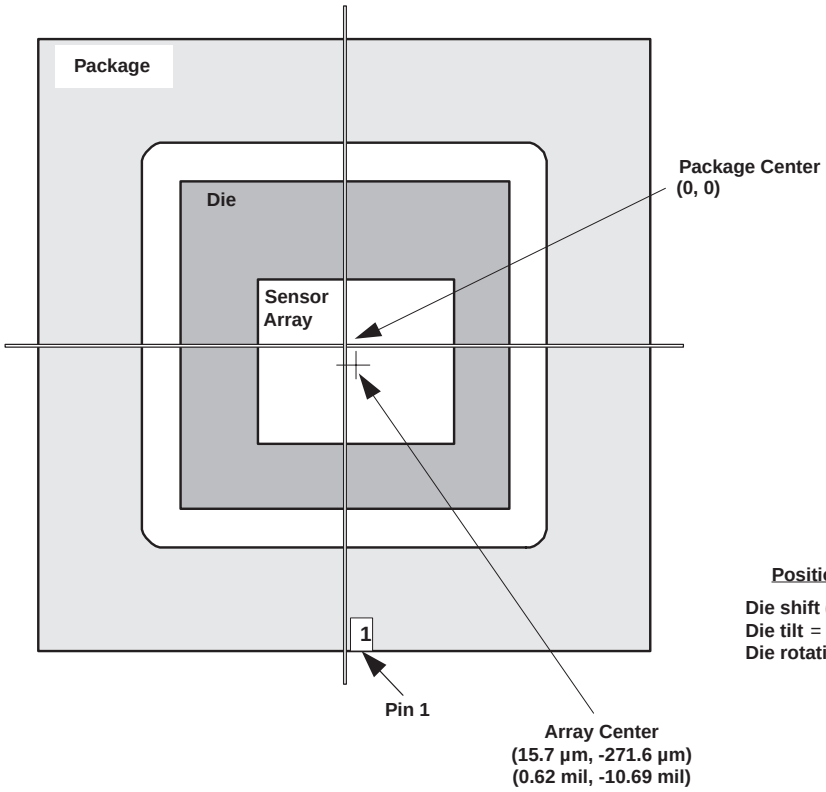


Table 12 OV9625/OV9121 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 + 0.30 / -0.13 SQ	.560 + .012 / - .005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	8.89 ± 0.13 SQ	.350 ± .005 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.08	.040 ± .003
Package Edge to First Lead Center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	12.40 ± 0.10 SQ / 13.00 ± 0.10 SQ	.488 ± .004 SQ / .512 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Sensor Array Center

Figure 22 OV9625/OV9121 Sensor Array Center



Positional Tolerances

Die shift (x,y) = 0.15 mm (6 mils) max.
Die tilt = 1 degrees max.
Die rotation = 3 degrees max.

Important: Most optical systems invert and mirror the image so the chip is usually mounted on the board with pin 1 (SVDD) down as shown.

NOTE: Picture is for reference only, not to scale.

Note:

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