YAMAHA

YMF781

APL-1
Automobile sound PLayer-1

■Overview

YMF781 (APL-1: hereinafter described as APL-1) is an LSI, integrating synthesizer, ADPCM decoder and a CPU for control in one chip.
Various sounds used in common automobiles, motor cycles, and electric appliances, such as alarm sound, operation sound, and melody sound, and pseudo engine sound for an electric car can be generated with a little CPU load.
A control CPU incorporated enables APL-1 control by a simple command (API) from the external host CPU.

Note: For API, refer to the APL-1 API specifications.

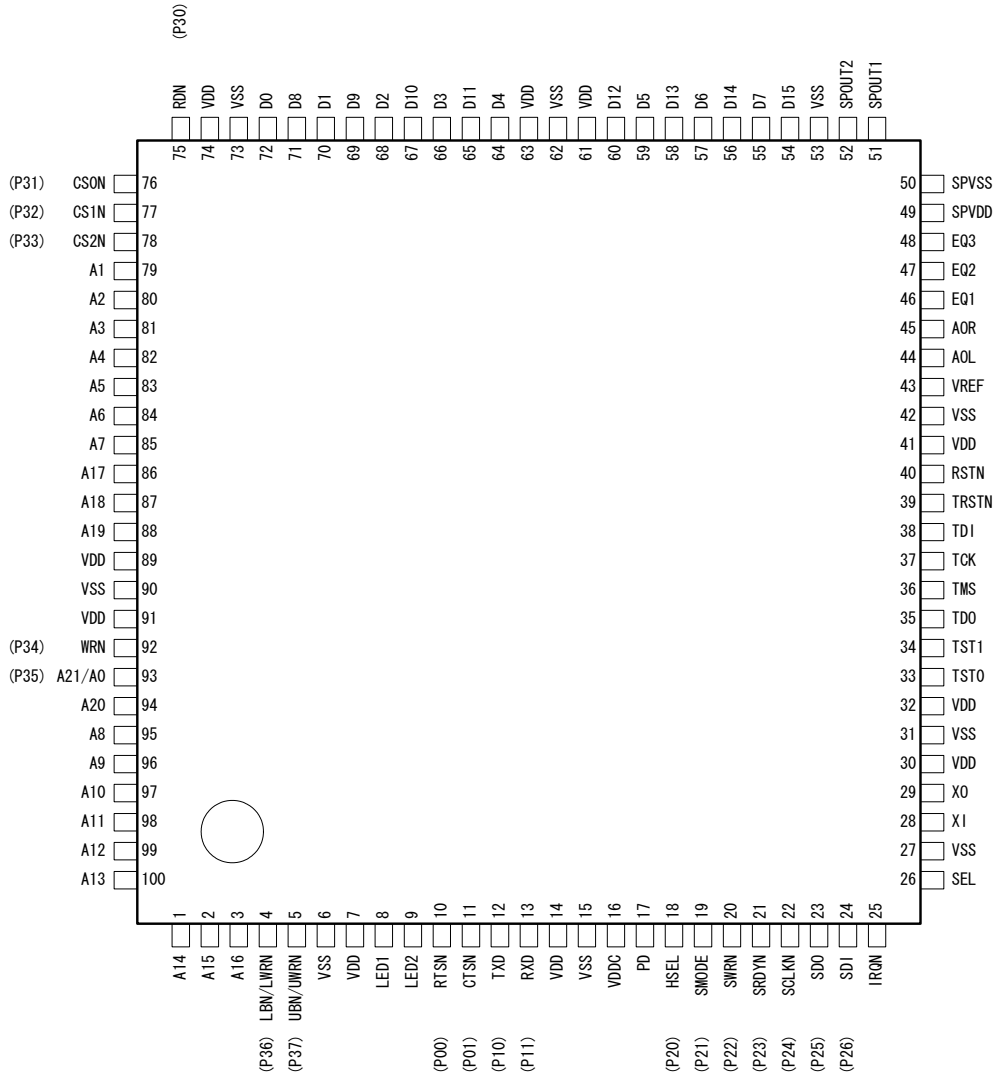
■Features

- ●CPU is incorporated and enabling controls for synthesizer and other functions by the simple commands.
- ●Stereo hybrid synthesizer that can generate up to 64 voices simultaneously.
- ●Time change low pass filter function by AL (Analog Lite) synthesizer is built in.
- ●ADPCM and PCM stream playback is possible.
- ●The default tone for FM and Wave Table synthesizer is built in ROM, and registration of a tone to SRAM is possible.
- ●Speaker amplifier and equalizer circuit is built in.
- ●Stereo / monaural analog output terminal is equipped.
- ●Two control circuits for LED lighting are built in.
  The synchronization with contents and compulsive control are also possible.
- ●The inspection function is built in as an external memory interface function.
- ●APL-1 control interface
  Three interfaces are provided: Clock Sync Serial, Asynchronous Serial (UART) and Command Port (Mode, which identify commands by the changes of bus.)
- ●Power down function is built in.
- ●Input and output port
  Some terminals can be used as an Input/Output port, which can be controlled from the host CPU.
- ●Malfunction prevention function owing to the electrostatic noise and electromagnetic noise is built in.
- ●Core power supply 3.3V (3.0V to 3.6V)
- ●I/O power supply 3.3V and 5.0V are changed. 3.3V (3.0V to 3.6V) 5.0V(4.75V to 5.25V)
- ●Speaker amplifier power supply 3.3V (3.0V to 3.6V)
- ●100pin plastic SQFP, pin lead plating with Pd-free (YMF781-SZ)

YAMAHA CORPORATION

YMF781 CATALOG
CATALOG No.: LSI-4MF781A3
2004.10

■Terminal Assignment



< 100 pin SQFP Top View >

■Terminal Functions

No.	Terminal Name (Port)	I/O (Output Type)	Functions
1	A14	O (4mA)	External memory Address bus 14
2	A15	O (4mA)	External memory Address bus 15
3	A16	O (4mA)	External memory Address bus 16
4	LBN/LWRN (P36)	O (4mA)	External memory Low byte enable
5	UBN/UWRN (P37)	O (4mA)	External memory Upper byte enable
6	VSS	-	Ground
7	VDD	-	Power Supply (3.3V)
8	LED1	O (4mA)	LED output 1
9	LED2	O (4mA)	LED output 2
10	RTSN (P00)	O (4mA)	Asynchronous Serial (UART) transmission request output VDDC is used
11	CTSN (P01)	Ish	Asynchronous Serial (UART) transmission request input VDDC is used
12	TXD (P10)	O (4mA)	Asynchronous Serial (UART) transmission output VDDC is used
13	RXD (P11)	Ish	Asynchronous Serial (UART) reception input VDDC is used
14	VDD	-	Power supply (3.3V)
15	VSS	-	Ground
16	VDDC	-	Power supply (3.3V/5.0V)
17	PD	Ish	Power-down VDDC is used
18	HSEL (P20)	Ish	Serial interface selection (Asynchronous / clock sync) VDDC is used
19	SMODE (P21)	Ish	Clock sync serial mode selection (MSB/LSB first) VDDC is used
20	SWRN (P22)	Ish	Clock sync serial write enable VDDC is used
21	SRDYN (P23)	Ish/O (4mA)	Clock sync serial ready VDDC is used
22	SCLKN (P24)	Ish	Clock sync serial clock VDDC is used
23	SDO (P25)	Ish/O (4mA)	Clock sync serial data output VDDC is used
24	SDI (P26)	Ish	Clock sync serial data input VDDC is used
25	IRQN	O (4mA)	Interrupt output VDDC is used
26	SEL	Ish	Port selection (clock sync serial / port2) VDDC is used
27	VSS	-	Ground
28	XI	I	X'tal connection
29	XO	O	X'tal connection
30	VDD	-	Power supply (3.3V)
31	VSS	-	Ground
32	VDD	-	Power supply (3.3V)
33	TST0	Ish	Test input terminal Normally, connect to the ground and use.
34	TST1	Ish	Test input terminal Normally, connect to the ground and use.
35	TDO	O	Test output terminal Normally, use without connection.
36	TMS	Ish	Test input terminal Normally, connect to the power supply (VDD) and use.
37	TCK	Ish	Test input terminal Normally, connect to the power supply (VDD) and use.
38	TDI	Ish	Test input terminal Normally, connect to the power supply (VDD) and use.
39	TRSTN	Ish	Test input terminal normally, connect to the Ground and use.
40	RSTN	Ish	Hardware reset
41	VDD	-	Power supply (3.3V)
42	VSS	-	Ground
43	VREF	A-	Analog Reference Signal
44	AOL	AO	Analog Lch output or Lch+Rch output (monaural)
45	AOR	AO	Analog Rch output
46	EQ1	A-	Equalizer terminal 1
47	EQ2	A-	Equalizer terminal 2
48	EQ3	A-	Equalizer terminal 3
49	SPVDD	-	Power supply for exclusive use of speaker (3.3V)
50	SPVSS	-	Ground for exclusive use of speaker

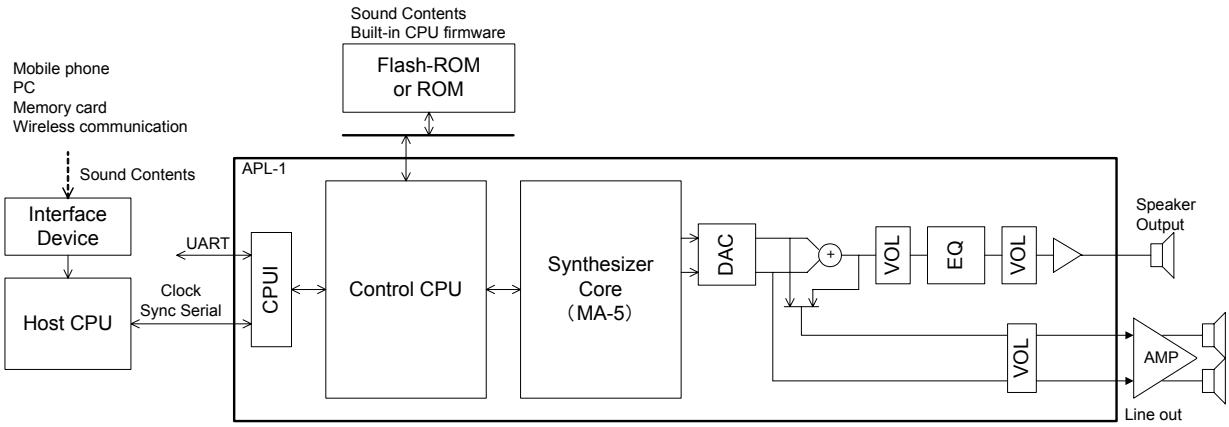
Note1: O: CMOS output terminal, I: CMOS input terminal, Ish: Schmitt CMOS input terminal, A: Analog terminal
Note2: The current value of the ( ) in the I/O (output type) indicates the output drive capability of its terminal.
Note3: The power supply, VDDC can be switched to 3.3V or 5.0V.
Note4: For the terminals without the description of "VDDC is used" in the table, VDD (only 3.3V) is used to drive it.

No.	Terminal Name (Port)	I/O (Output Type)	Function
51	SPOUT1	AO	Speaker connection terminal 1
52	SPOUT2	AO	Speaker connection terminal 2
53	VSS	-	Ground
54	D15	Ish/O (2mA)	External memory Data Bus 15
55	D7	Ish/O (2mA)	External memory Data Bus 7
56	D14	Ish/O (2mA)	External memory Data Bus 14
57	D6	Ish/O (2mA)	External memory Data Bus 6
58	D13	Ish/O (2mA)	External memory Data Bus 13
59	D5	Ish/O (2mA)	External memory Data Bus 5
60	D12	Ish/O (2mA)	External memory Data Bus 12
61	VDD	-	Power Supply (3.3V)
62	VSS	-	Ground
63	VDD	-	Power Supply (3.3V)
64	D4	Ish/O (2mA)	External memory Data Bus 4
65	D11	Ish/O (2mA)	External memory Data Bus 11
66	D3	Ish/O (2mA)	External memory Data Bus 3
67	D10	Ish/O (2mA)	External memory Data Bus 10
68	D2	Ish/O (2mA)	External memory Data Bus 2
69	D9	Ish/O (2mA)	External memory Data Bus 9
70	D1	Ish/O (2mA)	External memory Data Bus 1
71	D8	Ish/O (2mA)	External memory Data Bus 8
72	D0	Ish/O (2mA)	External memory Data Bus 0
73	VSS	-	Ground
74	VDD	-	Power Supply (3.3V)
75	RDN (P30)	O (4mA)	External memory Read Enable
76	CS0N (P31)	O (4mA)	External memory Chip Select 0
77	CS1N (P32)	O (4mA)	External memory Chip Select 1
78	CS2N (P33)	O (4mA)	External memory Chip Select 2
79	A1	O (4mA)	External memory Address Bus 1
80	A2	O (4mA)	External memory Address Bus 2
81	A3	O (4mA)	External memory Address Bus 3
82	A4	O (4mA)	External memory Address Bus 4
83	A5	O (4mA)	External memory Address Bus 5
84	A6	O (4mA)	External memory Address Bus 6
85	A7	O (4mA)	External memory Address Bus 7
86	A17	O (4mA)	External memory Address Bus 17
87	A18	O (4mA)	External memory Address Bus 18
88	A19	O (4mA)	External memory Address Bus 19
89	VDD	-	Power Supply (3.3V)
90	VSS	-	Ground
91	VDD	-	Power Supply (3.3V)
92	WRN (P34)	O (4mA)	External memory Write Enable
93	A21/A0 (P35)	O (4mA)	External memory Address Bus 21/0
94	A20	O (4mA)	External memory Address Bus 20
95	A8	O (4mA)	External memory Address Bus 8
96	A9	O (4mA)	External memory Address Bus 9
97	A10	O (4mA)	External memory Address Bus 10
98	A11	O (4mA)	External memory Address Bus 11
99	A12	O (4mA)	External memory Address Bus 12
100	A13	O (4mA)	External memory Address Bus 13

Note1: O: CMOS output terminal, I: CMOS input terminal, Ish: Schmitt CMOS input terminal, A: Analog terminal
Note2: The current value of the ( ) in the I/O (output type) indicates the output drive capability of its terminal.
Note3: The power supply, VDDC can be switched to 3.3V or 5.0V.
Note4: For the terminals without the description of "VDDC is used" in the table, VDD (only 3.3V) is used to drive it.

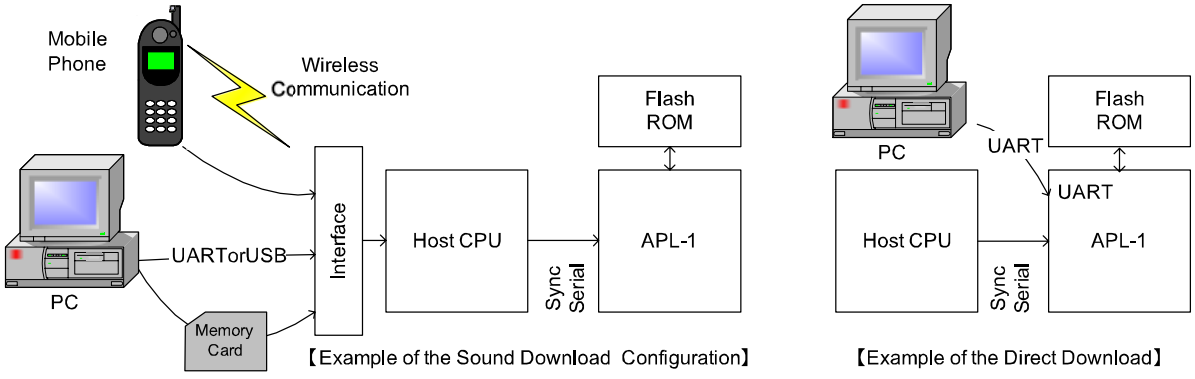
■Overview of the Operation

APL-1 includes the Synthesizer Core, the CPU for control and its peripheral circuit.
The CPU controls most of the controls such as Synthesizer Core and Input/Output Port.
Since the Synthesizer Core controls are all controlled by the built-in CPU, sound contents can be played by a simple command from the external.
The sound contents are stored in the external ROM.
Since the sound contents support formats in SMAF, SMAF/Phrase and SMAF/Audio, ROM data can be created by the development tool dedicated for APL-1.
The firmware in the built-in CPU is stored in the external ROM and can be updated by the exchange of ROM, or by the download via the APL-1 Control Interface.
Likewise, for the sound contents, it can be updated by the exchange of ROM, or by the download via the APL-1 Control Interface.
APL-1 Control Interface: Clock Sync Serial, Asynchronous Serial (UART), is incorporated and can be selected by the terminal. (Mode 1)

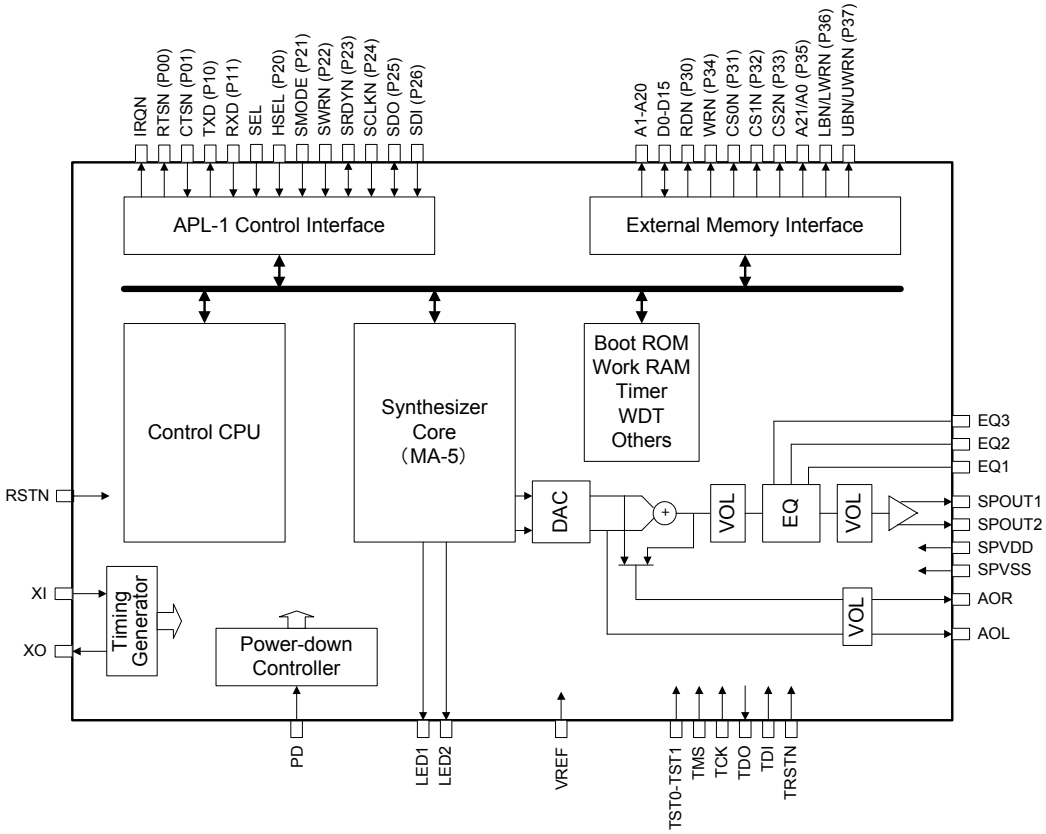


Note: A configuration diagram, which mode 1 is selected as an APL-1 Control Interface, is shown.

The download of the sound contents and the update of the APL-1 firmware are normally performed via the host CPU. When it is difficult to mount a download function in host CPU, the download of sound contents and the update of the firmware can be performed directly by using the asynchronous serial (UART). However, the connection destination is restricted to PC Asynchronous Serial (UART).



■Block Diagram



■Overview of the block

The overview function of each block and the flow of a signal are explained.

Control CPU
The Control CPU controls APL-1 in all as well as the Synthesizer Core controls such as a sequencer function.

Synthesizer Core
Hybrid Synthesizer Core equivalent to MA-5, which is a synthesizer LSI for mobile phone.
The synthesizer performs play of the sound contents, LED controls, etc.

External Memory Interface
The interface connects APL-1 to the external memory.
Accessible memory space is up to 8MByte. (CS0N:4MByte＋CS1N:2MByte＋CS2N:2MByte.)
SRAM with the specification of byte access is necessary.
From P30-P37 can be used as the output port when only one external ROM is used.

APL-1 Control Interface
APL-1 is controlled through the APL-1 Control Interface.
Mode 1 and Mode 2 can be selected according to the settings of SEL terminal.
In Mode 1, Clock Sync Serial and Asynchronous Serial (UART) can be switched and used by the HSEL terminal.
In Mode 2, Asynchronous Serial (UART) and command port (A mode, which identify command by the change of data that inputted into P20-P26) can be used at the same time.
P01 and P11 can be used as input port, and P00 and P10 can be used as output port, depending on the settings.

Timing Generator
Clocks used in the APL-1 are generated.

Power-down Controller
The controller controls APL-1 in the power-saving mode.

Boot ROM, Work RAM, Timer, WDT, etc.
The peripheral devices of the Control CPU in the APL-1.

■Electrical Characteristics

●Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
SPVDD terminal - Power supply Voltage (Speaker Amplifier section)	SPVDD	-0.3	6.0	V
VDD terminal - Power supply Voltage	VDD	-0.3	4.2	V
VDDC terminal - Power supply Voltage	VDDC	-0.3	7.0	V
SPOUT1, SPOUT2 terminal - Supplied voltage	V_{INSP}	-0.3	SPVDD+0.3	V
Analog Input Voltage	V_{INA}	-0.3	VDD+0.3	V
Digital Input Voltage (1) (*1)	V_{IND1}	-0.3	VDDC+0.3	V
Digital Input Voltage (2) (*2)	V_{IND2}	-0.3	VDD+0.3	V
Storage Temperature	T_{STG}	-50	125	℃

Conditions: VSS = SPVSS = 0V

(*1) Relevant terminals: RXD, CTSN, PD, HSEL, SMODE, SWRN, SCLKN, SDI, and SEL
(When Port is used: P01, P11, and P20-P26)

(*2) Relevant terminals: Other input terminals

●Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
SPVDD Operating Voltage (Speaker Amplifier section)	SPVDD	3.0	3.3	3.6	V
VDD Operating Voltage	VDD	3.0	3.3	3.6	V
VDDC Operating Voltage (compatible with 3.3V/5.0V)	VDDC	3.0	3.3	3.6	V
		4.75	5.0	5.25	V
Operating Ambient Temperature	T_{OP}	-40	25	85	℃

Conditions: VSS = SPVSS = 0V

●Consumption Current

Item	Condition	Min.	Typ.	Max.	Unit
Normal operating Condition	VDD + VDDC		50	80	mA
	SPVDD when in no output		4		mA
	when in 8ohm, 330mW Output		187		mA
Stand-by 1 Mode	VDD + VDDC		25	40	mA
Stand-by 2 Mode	VDD + VDDC		5	10	mA
Shutdown Mode (T_{OP} = 25℃)	VDD + VDDC + SPVDD (*1)		6	10	μA
(T_{OP} = 85℃)				50	μA

Conditions: T_{OP}= -40 to 85℃, VDD= 3.0 to 3.6V, VDDC= 3.0 to 3.6V or 4.75 to 5.25V, Capacitor load=50pF

(*1): VDD=VDDC=SPVDD=3.30V, and for Input terminals, V_{IL}=VSS, V_{IH}= VDD or VDDC

●DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage "H" level (1) *1)	V_{IH1}		0.70×VDDC			V
Input voltage "L" level (1) (*1)	V_{IL1}				0.30×VDDC	V
Schmitt Width (1) (*1)	V_{SW1}			0.15×VDDC		V
Input voltage "H" level (2) (*2)	V_{IH2}		0.70×VDD			V
Input voltage "L" level (2) (*2)	V_{IL2}				0.30×VDD	V
Schmitt Width (2) (*2)	V_{SW2}			0.15×VDD		V
Output voltage "H" level(1) (*1)	V_{OH1}	I_{OH} = -2mA	0.8×VDDC			V
Output voltage "L" level (1) (*1)	V_{OL1}	I_{OL} = +4mA			0.2×VDDC	V
Output voltage "H" level (2) (*2)	V_{OH2}	I_{OH} = -2mA(*3)	0.8×VDD			V
Output voltage "L" level (2) (*2)	V_{OL2}	I_{OL} = +4mA(*3)			0.2×VDD	V
Input Leak Current	IL		-10		10	μA
Input Capacitance	CI				15	pF

Conditions: T_{OP}= -40 to 85℃, VDD= 3.0 to 3.6V, VDDC= 3.0 to 3.6V or 4.75 to 5.25V, Capacitor load=50pF

(*1) Relevant terminals: RXD, CTSN, PD, HSEL, SMODE, SWRN, SCLKN, SDI, and SEL
(when Port is used: P01, P11, and P20-P26)

(*2) Relevant terminals: Other Input Terminals

(*3) Except for D0 to D15 terminal: I_{OH} = -1mA, I_{OL} = +2mA

●AC Characteristics

Input/Output level measurement conditions: V_{IH} = 0.75 × VDD or 0.75 × VDDC
(unless otherwise specified) V_{IL} = 0.25 × VDD or 0.25 × VDDC
V_{OH} = 0.75 × VDD or 0.75 × VDDC
V_{OL} = 0.25 × VDD or 0.25 × VDDC

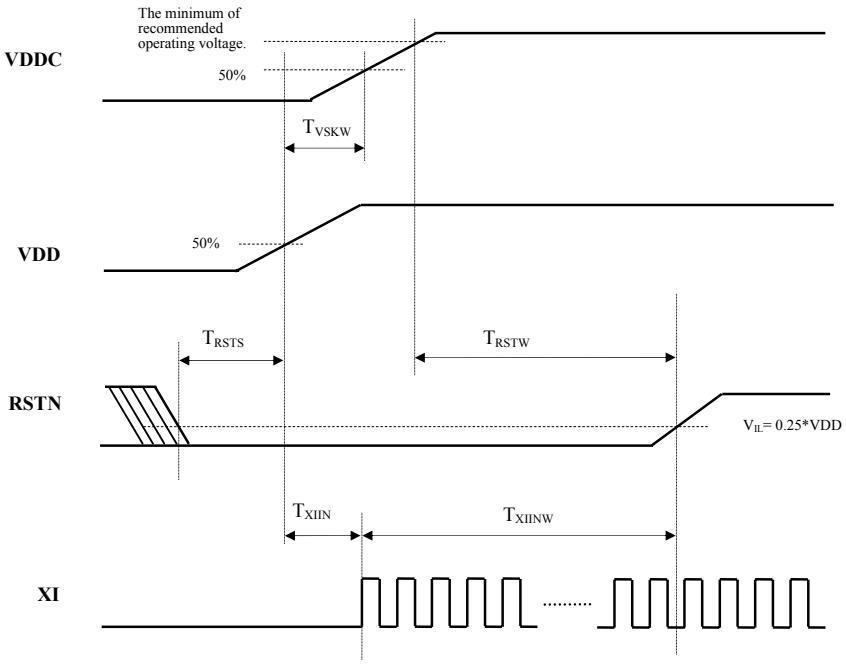
▪Reset and Clock Timing

RSTN, XI, and other input signals

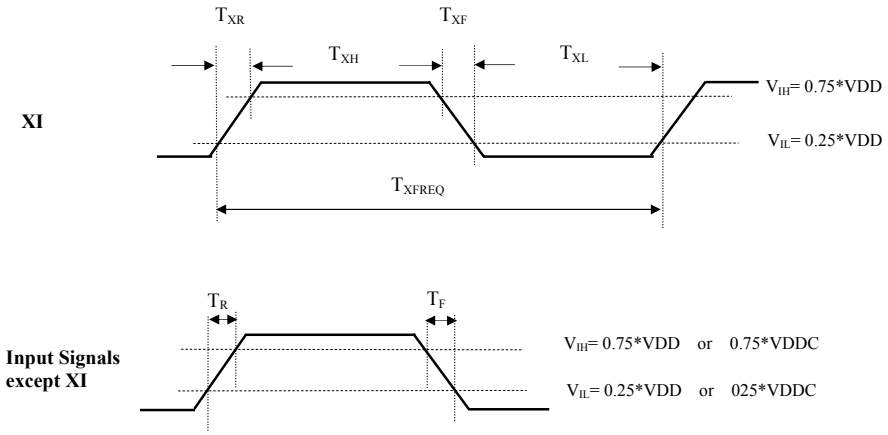
Item	Symbol	Min.	Typ.	Max.	Unit
RSTN "L" pulse width (When in power-up and in shut-down-cancel)	T_{RSTW}	20			ms
(When power supply and clock is in stable)		100			μs
RSTN (undefined→L) set-up time	T_{RSTS}	0			μs
VDD→VDDC power up time difference	T_{VSKW}	0		3	ms
XI Frequency	$1 / T_{XFREQ}$		6.144		MHz
XI Rising time and Falling time	T_{XR} , T_{XF}			20	ns
XI High time	T_{XH}	60			ns
XI Low time	T_{XL}	60			ns
XI Input delay time	T_{XIIN}			1	ms
XI Input time	T_{XIINW}	1			ms
Internal clock frequency	$1/T_{CW}$		18.432		MHz
Input signals except XI Rising time and Falling time	T_R, T_F			15	ns

Conditions: T_{OP}= -40 to 85℃, VDD= 3.0 to 3.6V, VDDC= 3.0 to 3.6V or 4.75 to 5.25V, Capacitor load=50pF

- Clock input to the XI terminal is necessary during the reset.
- Be sure to power VDD first when independent power supply is used for the supply of VDD and VDDC.



The reset width is defined from a point that VDDC reaches to the minimum of recommended operating voltage.
RSTN input must be "L" level at the point where VDD reaches to 50%.



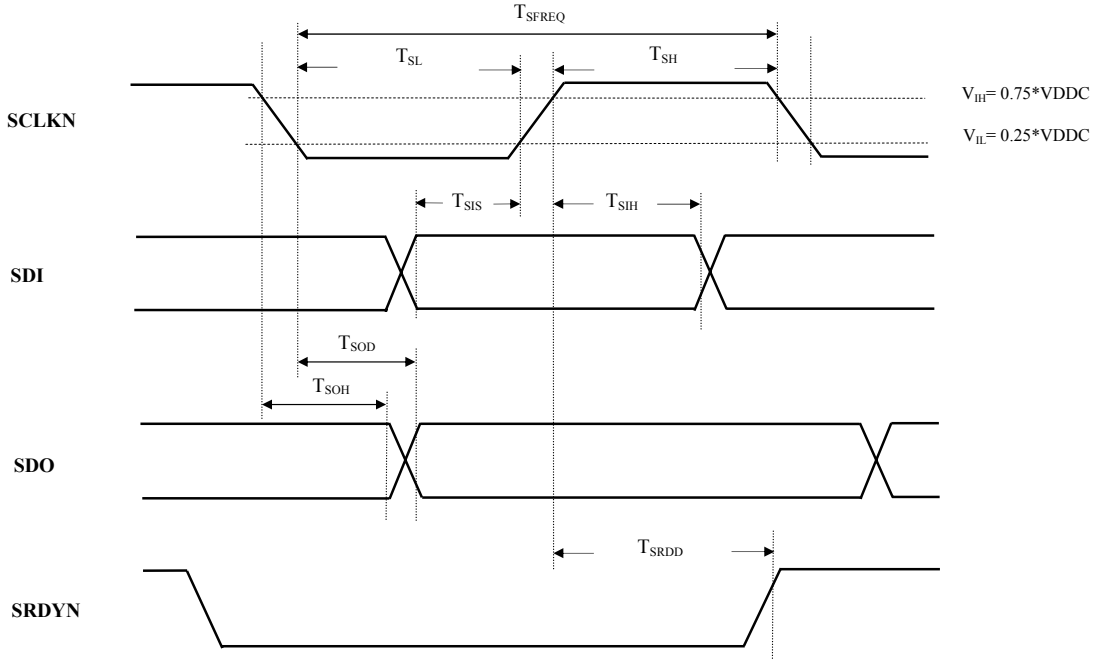
▪Clock Sync Serial Interface

Item	Symbol	Min.	Typ.	Max.	Unit
SCLKN frequency (Serial transfer speed)	1 / T_{SFREQ}		1	2	MHz
SCLKN High time	T_{SH}	220			ns
SCLKN Low time	T_{SL}	220			ns
SDI set-up time	T_{SIS}	0			ns
SDI hold time	T_{SIH}	75			ns
SDO output delay time	T_{SOD}			200	ns
SDO output hold time (*1)	T_{SOH}	110			ns
SRDYN output delay time (L→H) (*2)	T_{SRDD}			300	ns

Conditions: T_{OP}= -40 to 85℃, VDD= 3.0 to 3.6V, VDDC= 3.0 to 3.6V or 4.75 to 5.25V, Capacitor load=50pF

(*1) The last SDO output data is held until the next SCLKN falling edge is detected.

(*2) Time to the High level in synchronization with SCLKN, when the first 1 bit is transmitted or received. The falling timing depends on the transmit/receive process of the internal Control CPU.



・Asynchronous Serial Interface（UART）

Item	Symbol	Min.	Typ.	Max.	Unit
Transfer Frequency (Baud rate: fixed to x16)	$1 / T_{RXD}$	9		144	kHz
RXD allowable frequency error (*1)		-2		+2	%

Conditions: T_{OP}= -40 to 85℃, VDD= 3.0 to 3.6V, VDDC= 3.0 to 3.6V or 4.75 to 5.25V, Capacitor load=50pF

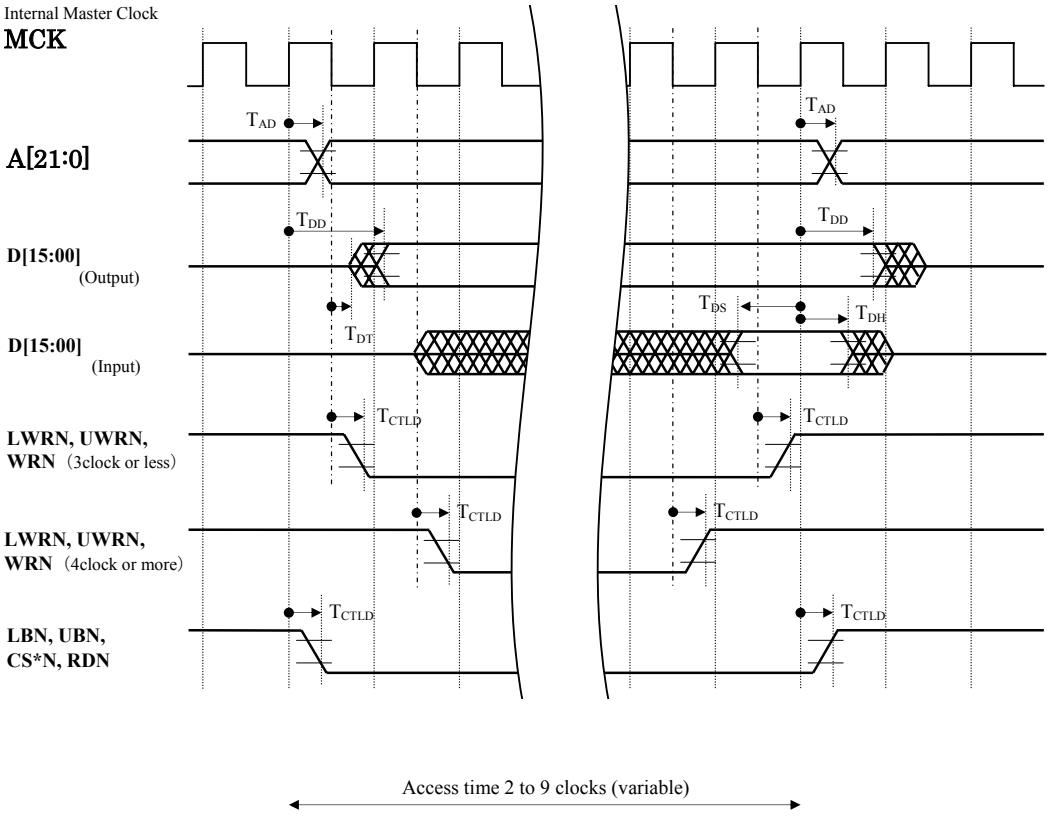
(*1) In the case of 10 bits including the start bit and the stop bit.

・External Memory Interface

Item	Symbol	Min.	Typ.	Max.	Unit
Data (D) Set-up time	T_{DS}	10			ns
Data (D) Hold time	T_{DH}	10			ns
Address (A) Output Delay time	T_{AD}			40	ns
Control Signal Output Delay time (*1)	T_{CTLD}			40	ns
Data (D) Output Delay time	T_{DD}			80	ns
Data (D) Output turn-on time	T_{DT}			20	ns

Conditions: T_{OP}= -40 to 85℃, VDD= 3.0 to 3.6V, VDDC= 3.0 to 3.6V or 4.75 to 5.25V, Capacitor load=50pF

(*1) LBN/LWRN, UBN/UWRN, WRN, RDN, and CS*N



※Note that the output timing of LWRN, UWRN, and WRN differs in the access time of 3 clocks or less and that of 4 clocks or more.

●Analog Characteristics

Conditions: T_{OP}=25℃, VDD=3.30V, SPVDD=3.30V

•SP Amplifier

Item	Min.	Typ.	Max.	Unit
Gain Settings (Fixed)		±2		times
Minimum load resistance (RL)		8		Ω
Maximum Output Voltage Width (RL=8Ω)		5.5		Vp-p
Maximum Output Power (RL=8Ω, THD+N≦1.0%)		480		mW
THD + N (RL=8Ω, f=1kHz, 330mW output)		0.03		%
Quiescent noise (A-filter: weighing filter)		-90		dBV
PSRR (f=1kHz)		90		dB
Amplitude Center voltage		0.5×VDD		V
Differential Output Voltage		10	50	mV
Connectable maximum load capacitance to SPOUT1, SPOUT2 terminal (*)			1000	pF

(*): MAX 1000pF can be connected to the SPOUT1 terminal and the SPOUT2 terminal.

•EQ Amplifier

Item	Min.	Typ.	Max.	Unit
Possible Gain Setting Range			30	dB
Maximum Output Voltage Amplitude		3.0		Vp-p
THD + N (f=1kHz)			0.05	%
Quiescent noise (A-filter)		-90		dBV
Input Impedance	10			MΩ
Feedback resistor between EQ2-EQ3	20			kΩ

•SP Volume

Item	Min.	Typ.	Max.	Unit
Volume Setting Range	-30		0	dB
Volume Step Width		1		dB
THD + N (f=1kHz)			0.05	%

•EQ Volume

Item	Min.	Typ.	Max.	Unit
Volume Setting Range	-30		0	dB
Volume Step Width		1		dB
Quiescent noise (A-filter)		-90		dBV
Maximum Output Current	132			μA
Maximum Output Voltage Amplitude		1.65		Vp-p
Output Impedance		300	600	Ω

•HP Volume

Item	Min.	Typ.	Max.	Unit
Volume Setting Range	-30		0	dB
Volume Step Width		1		dB
Quiescent noise (A-filter)		-90		dBV
Maximum Output Current	132			μA
Maximum Output Voltage Amplitude		1.65		Vp-p
Output Impedance		300	600	Ω

•VREF

Item	Min.	Typ.	Max.	Unit
VREF Voltage		0.5×VDD		V

•DAC

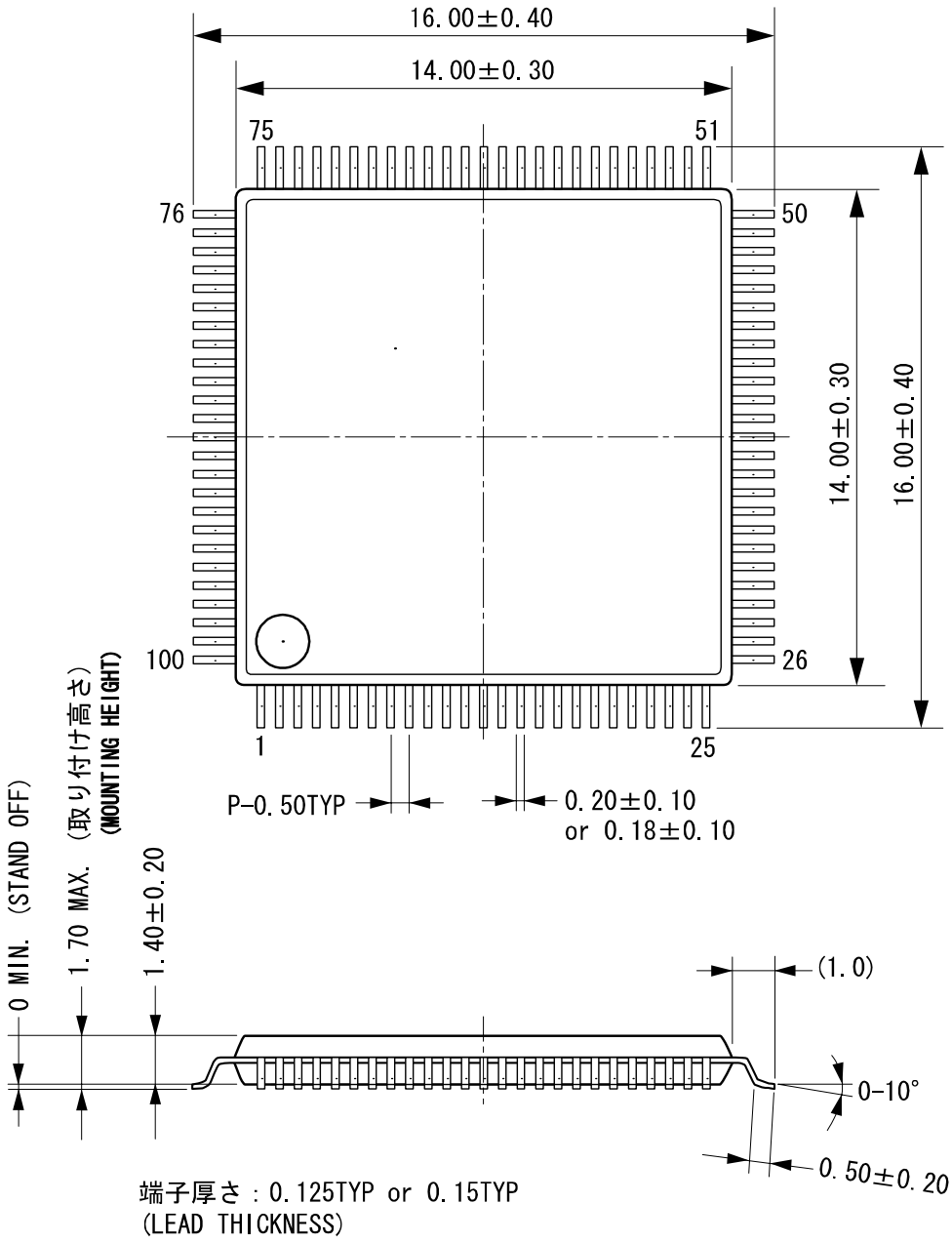
Item	Min.	Typ.	Max.	Unit
Resolution		16		Bit
Full scale Output Voltage		1.65		Vp-p
THD+N (f= 1kHz)			0.5	%
Quiescent noise (A-filter)		-85	80	dBV
Frequency Characteristics (f=50Hz to 20kHz)	-3.0 (*)		+0.5	dB

(*) A drop of the high range response owing to the aperture effect.

MEMO

■Package Outline

C-PK100SP-1



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位：mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

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