YAMAHA

YMF795

APL-2

Automobile sound Player-2

Outline

YMF795 is a sound source LSI to reproduce high quality melody and effect sound for in-car product. Yamaha's original FM synthesizer embedded as a sound source can create various timbres, and also a sequencer embedded can simultaneously generate up to four sounds with four different timbres without giving load to the controller.

Serial port is prepared as a controller interface, and no restriction of data capacity is present because melody data is reproduced in real-time through FIFO.

A built-in amplifier to drive the dynamic speaker with 500mW power allows connecting a speaker directly.

This LSI is equipped with an analog-output pin also for the earphone jack.

In addition, supporting the standby mode can reduce the consumption current to 1 μA during the standby.

Features

- YAMAHA's original FM sound source function
- Built-in sequencer
- Capable of producing up to 4 different sounds simultaneously (4 independent timbres available).
- 500mW output speaker amplifier
- Sound quality correcting equalizer circuit
- Serial interface
- Arbitrary frequency of input clock from 2.685 MHz to 27.853 MHz in 55.93 kHz steps, as well as 2.688, 8.4, 12.6, 14.4, 19.2, 19.68, 19.8, and 27.82 MHz clock inputs
- Analog output for earphone
- Power-down mode (Typ. 1μA or less)
- Supply voltage (Digital and Analog): 3.3V±10 %
- 24-pin SSOP. The plating of pins is lead-free. (YMF795-EZ)

YAMAHA CORPORATION

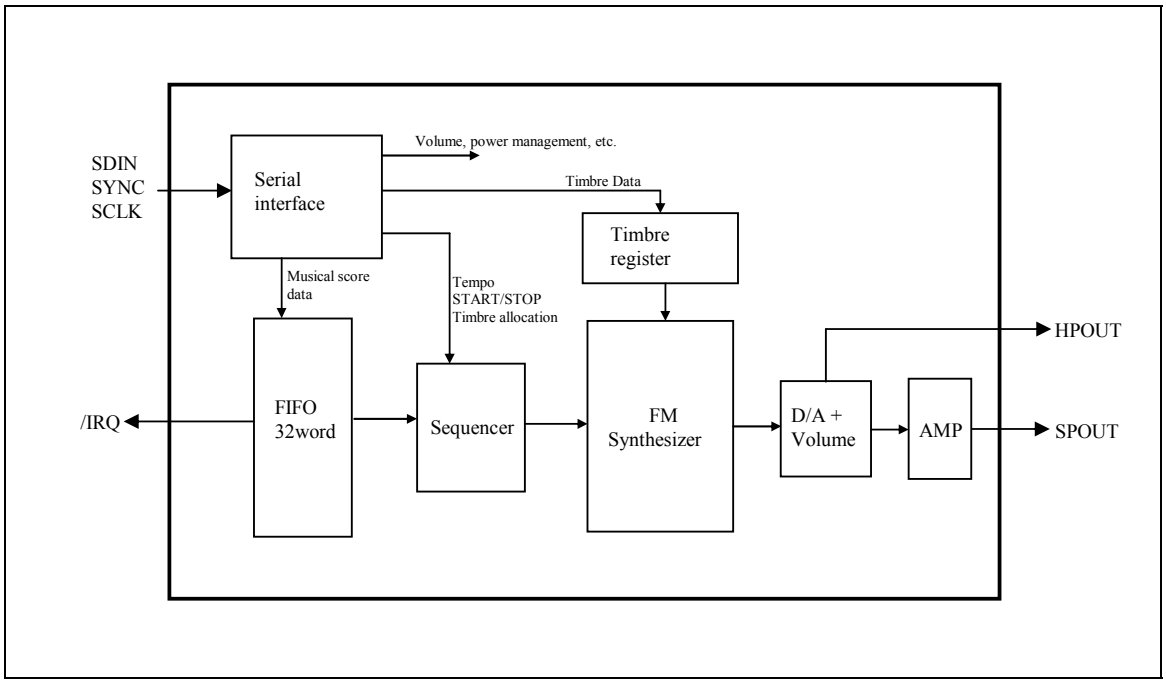
YMF795 CATALOG
CATALOG No.:LSI-4MF795A20
2005. 11

Contents

■General Description of YMF795

YMF795 is controlled through the serial interface.

Internal configuration the LSI has is shown below.



Data inputted to the serial interface is converted into the parallel data and transferred to each function block according to its index address.

The musical score data is stored in the 32-word FIFO first and then transferred to the sequencer which interprets data to control sound generation of the FM synthesizer.

The timbre register is where up to 8 timbre data can be stored.

And, as the sequencer controlling register, registers for start/stop and tempo are provided.

In order to have sound generate, the following controls must be performed to this LSI.

1) Initial status setting (cancellation of power-down, clock selection, etc).
2) Timbre data setting.
3) Writing of the musical score data into FIFO before starting the sequence.
4) To write the next musical score data write before the FIFO becomes empty, and to receive the interrupt signal from FIFO during reproduction.
   (For the details, refer to “Settings and procedure required for a piece generation” (P.24).

■Block Description

1) Serial interface block

The block receives serial data and then identifies its Index data to send control data to each function block.

2) FIFO block

FIFO temporarily stores musical score data. Musical score data up to 32 can be stored. The musical score data are processed in the sequencer when they are generated as sounds and those processed are deleted one after another. When the amount of remaining data amount in FIFO reaches the value or less of register setting (IRQ point), it outputs an interrupt signal to the outside to request the subsequent musical score data.

3) Sequencer block

When the sequencer receives the START command, it sequentially starts reading the musical score data which have been stored in FIFO. The processed musical score data are deleted.

4) Timbre register block

The block stores timbre data in this register which can set up to 8 timbres. Settings of this register must be completed before sound generation. The register is initialized by hardware reset; however, in the following operations, contents of a register are not cleared, and the value written last is held.

- Software reset (CLR bit of Index32h)
- During power-down mode, and after its cancellation.

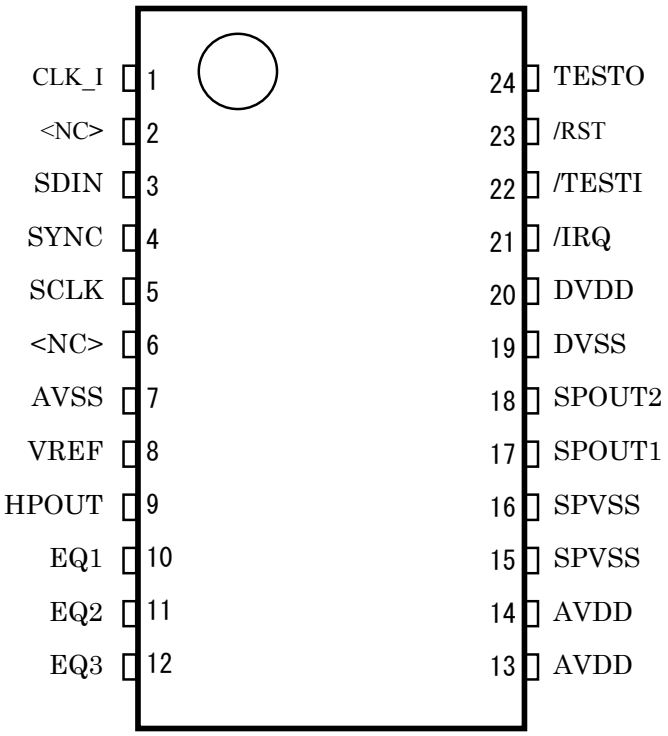
5) FM synthesizer block

The block synthesizes and generates timbres according to settings. Four sounds can be generated at the same time.

6) D/A, volume, and amplifier blocks

The output from the synthesizer is D/A-converted, and volume processing is performed. After that, the data is output from the speaker or the earphone output pin.

■**Pin Configuration**



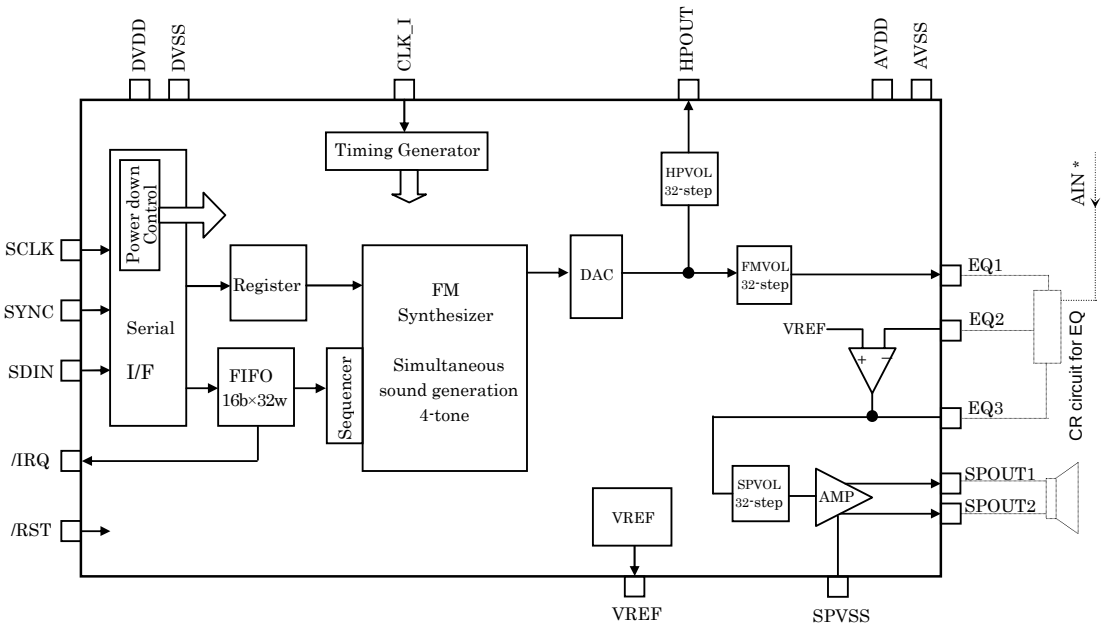
< 24-pin SSOP TOP VIEW >

■Pin Description

No.	Pin	I/O	Function
1	CLK_I	Ish	Clock input pin
2	<NC>	-	Be sure to use in no-connection. The pin is nowhere connected in the chip.
3	SDIN	I	Serial I/F data input
4	SYNC	I	Serial I/F synchronous signal input
5	SCLK	Ish	Serial I/F bit clock input
6	<NC>	-	Be sure to use in no-connection. The pin is nowhere connected in the chip.
7	AVSS	-	Analog ground
8	VREF	A	Analog reference voltage pin Connect a 0.1 µF capacitor between this pin and analog ground pin.
9	HPOUT	AO	Analog output pin for earphone
10	EQ1	AO	Equalizer pin 1
11	EQ2	AI	Equalizer pin 2
12	EQ3	AO	Equalizer pin 3
13	AVDD	-	Analog power supply (+3.3V) Connect 0.1 µF and 4.7 µF capacitors between this pin and analog ground pin
14			
15	SPVSS	-	Analog ground exclusively used for speaker
16			
17	SPOUT1	AO	Speaker output pin 1
18	SPOUT2	AO	Speaker output pin 2
19	DVSS	-	Digital ground
20	DVDD	-	Digital power supply (+3.3 V) Connect 0.1 µF and 4.7 µF capacitors between this pin and digital ground pin.
21	/IRQ	O	Interrupt signal output
22	/TESTI	I	LSI test input pin (Be sure to connect to DVDD.)
23	/RST	I	Hardware reset pin
24	TESTO	O	LSI TEST output pin (Be sure to use in no-connection)

Note : Ish = Schmitt input pin AI = Analog input pin A0 = Analog output pin

■Block Diagram



Concerning AIN signal inputted into equalizer circuit

It is possible to make the analog mixing between synthesizer output and other analog source in the equalizer circuit and output the resulting sound through the speaker.

■Register Map

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	Description
$00h	BL1	BL0	NT3	NT2	NT1	NT0	CH1	CH0	VIB	TI3	TI2	TI1	TI0	TK2	TK1	TK0	Note data
	0	0	1	1	0	0	CH1	CH0	VCHE	TI3	TI2	TI1	TI0	VCH2	VCH1	VCH0	Rest data
$10 - 2Fh	ML2	ML1	ML0	VIB	EGT	SUS	RR3	RR2	RR1	RR0	DR3	DR2	DR1	DR0	AR3	AR2	Timbre data
	AR1	AR0	SL3	SL2	SL1	SL0	TL5	TL4	TL3	TL2	TL1	TL0	WAV	FL2	FL1	FL0	(for 1 Operator)
$30h	0	V32	V31	V30	0	V22	V21	V20	0	V12	V11	V10	0	V02	V01	V00	Timbre allocation data
$31h	0	0	0	0	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0	Tempo data
$32h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLR	ST	FM Control
$33h	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKSEL			CLK_I select
$34h	0	0	0	0	0	0	0	0	0	0	IRQE	IRQ Point					IRQ Control
$35h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0	Speaker Volume
$36h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0	FM Volume
$37h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0	HPOUT Volume
$38h	0	0	0	0	0	0	0	0	0	0	0	AP4	AP3	AP2	AP1	DP	Power Management
$39h	0	0	0	0	0	0	0	CLKSET									CLK_I Select
$40 - EFh	Reserved (access prohibited)																Reserved
$F0 - FFh	For LSI TEST(access prohibited)																LSI TEST

Note : Access to the spaces of “Reserved” and “For LSI TEST” in the above table is prohibited.

Be sure to write “0” to the empty bit, although writing “1” there will not affect the LSI operation.

■Explanation of Registers

The YMF795 has three types of control registers: musical score data, timbre data, and other control data.

□Musical score data register

$00h Musical score data

The musical score data are written into the 32-word FIFO. There are two types of musical score data: note data and rest data.

Note data Default: 0000h

Index	B15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$00h	BL1	BL0	NT3	NT2	NT1	NT0	CH1	CH0	VIB	TI3	TI2	TI1	TI0	TK2	TK1	TK0

BL1 – BL0 : Octave block setting

Three octave blocks are available for sound range setting. The setting range is 1 to 3. Do not set "0."

In addition, the sound generation range is affected by the coefficient called "Multiple (multiplying factor for sound generation frequency)."

By combining the octave block and Multiple settings, sounds can be generated in the range as listed in the table blow.

Since the setting range of "Multiple" coefficient is 0 to 7, actually, sounds wider than those given in the table below can be generated.

	Multiple = 1 (x1)	Multiple = 2 (x2)	Multiple = 4 (x4)
BL[1:0] = 01b	C#3 (139Hz) D3 (147Hz) D#3 (156Hz) E3 (165Hz) F3 (175Hz) F#3 (185Hz) G3 (196Hz) G#3 (208Hz) A3 (220Hz) A#3 (233Hz) B3 (247Hz) C4 (262Hz)	C#4 (277Hz) D4 (294Hz) D#4 (311Hz) E4 (330Hz) F4 (349Hz) F#4 (370Hz) G4 (392Hz) G#4 (415Hz) A4 (440Hz) A#4 (466Hz) B4 (494Hz) C5 (523Hz)	C#5 (554Hz) D5 (587Hz) D#5 (622Hz) E5 (659Hz) F5 (698Hz) F#5 (740Hz) G5 (784Hz) G#5 (831Hz) A5 (880Hz) A#5 (932Hz) B5 (988Hz) C6 (1046Hz)
BL[1:0] = 10b	C#4 (277Hz) D4 (294Hz) D#4 (311Hz) E4 (330Hz) F4 (349Hz) F#4 (370Hz) G4 (392Hz) G#4 (415Hz) A4 (440Hz) A#4 (466Hz) B4 (494Hz) C5 (523Hz)	C#5 (554Hz) D5 (587Hz) D#5 (622Hz) E5 (659Hz) F5 (698Hz) F#5 (740Hz) G5 (784Hz) G#5 (831Hz) A5 (880Hz) A#5 (932Hz) B5 (988Hz) C6 (1046Hz)	C#6 (1109Hz) D6 (1175Hz) D#6 (1245Hz) E6 (1319Hz) F6 (1397Hz) F#6 (1480Hz) G6 (1568Hz) G#6 (1661Hz) A6 (1760Hz) A#6 (1865Hz) B6 (1976Hz) C7 (2093Hz)
BL[1:0] = 11b	C#5 (554Hz) D5 (587Hz) D#5 (622Hz) E5 (659Hz) F5 (698Hz) F#5 (740Hz) G5 (784Hz) G#5 (831Hz) A5 (880Hz) A#5 (932Hz) B5 (988Hz) C6 (1046Hz)	C#6 (1109Hz) D6 (1175Hz) D#6 (1245Hz) E6 (1319Hz) F6 (1397Hz) F#6 (1480Hz) G6 (1568Hz) G#6 (1661Hz) A6 (1760Hz) A#6 (1865Hz) B6 (1976Hz) C7 (2093Hz)	C#7 (2217Hz) D7 (2349Hz) D#7 (2489Hz) E7 (2637Hz) F7 (2794Hz) F#7 (2960Hz) G7 (3136Hz) G#7 (3322Hz) A7 (3520Hz) A#7 (3729Hz) B7 (3951Hz) C8 (4186Hz)

NT3 - NT0 : Pitch setting

Four bits from NT3 to 0 are used to specify the pitch. The bit assignment is as follows.

NT[3:0]	Pitch
0h	Setting Prohibited
1h	C#
2h	D
3h	D#
4h	Setting Prohibited
5h	E
6h	F
7h	F#
8h	Setting Prohibited
9h	G
Ah	G#
Bh	A
Ch	Setting Prohibited
Dh	A#
Eh	B
Fh	C

About “Setting Prohibited.”

Although LSI never hangs, unusual sound may be generated. Never set it.

CH1 - CH0 : Part setting

As the sound source section can simultaneously generate sounds in 4 parts, set the part of a note by using CH1 and 0 bits.

CH[1:0]	Part setting
00b	0
01b	1
10b	2
11b	3

VIB : Vibrato setting

This bit is used to set ON/OFF of Vibrato function for each note: “0” for OFF and “1” for ON. The vibrato frequency is 6.4 Hz and the modulation depth is ±13.47 cent.

Note that Vibrato function becomes OFF when VIB bit of timbre data ($10-2Fh) is “0.”

TI3 - TI0 : Interval setting

These bits are used to set the interval time before the processing of the next note and rest. The interval "48" represents the time for the whole note.

TI [3:0]	Interval
0h	0
1h	2
2h	3
3h	4
4h	6
5h	8
6h	9
7h	12
8h	18
9h	24
Ah	48
Bh	0
Ch	16
Dh	24
Eh	36
Fh	48

TK2 – TK0 : Note (sound length) designation

These 3 bits are used to designate the note (sound length). Depending on the value of interval setting (TI3 - 0), the length varies as shown in the following table. The interval "48" represents the time for the whole note.

	TI [3:0] = 0 to Ah								TI [3:0] = B to Fh							
TK[2:0]	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Sound length	1	2	3	5	7	8	11	17	15	23	29	32	35	41	47	Tie, Slur

■ Caution ■

When KEY is turned on again while release rate is not completely finished yet in the same channel, timbre may change.

This happens in both sustained sound and decaying sound.

The reason why it happens is that both envelope and phase in the career side and modulator side of the FM sound source deviate.

The hardware creating the phase and envelope of FM sound source starts its operation according to the following two conditions.

- End of the release rate.
- Occurrence of Key ON.

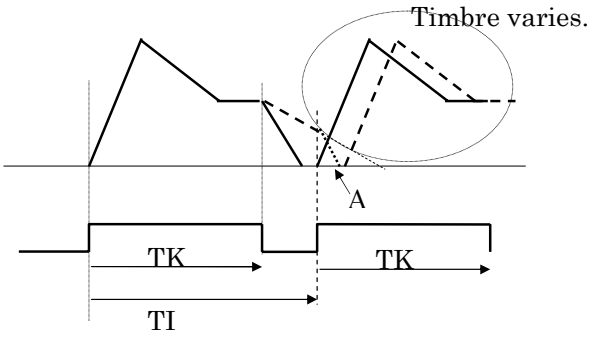
Timbre data is created on the assumption that modulator, phase between careers, and envelope operate at the same timing; therefore, timbre may vary when this condition is not met.

Description mentioned above is explained with the envelope waveform.

For example, assume that a timbre of which only release time differs between carrier and modulator is present. If operation is in the state completely stopped, it shifts to the Attack rate in conjunction with KEY ON. If the previous sound generation is being released and is not in a state completely stopped, the release settings is forcibly hastened (8.94 ms) and a stopped state is shifted to the attack rate state. (Dotted line of A)

Although envelope indicated in a solid line changes to the attack rate state soon at the second KEY ON, shifting to the attack rate state is not immediately performed because sound indicated in a dotted line is not completely stopped. The release time is hastened to stop the state, and then the state stopped is shifted to the attack rate state.

The starting time deviation of both envelopes and phase caused by this deviation causes a change of timbre.



How to avoid this symptom:

Be sure to observe “Try to pronounce under the condition that the release is completely stopped.”

Rest data Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$00h	0	0	1	1	0	0	CH1	CH0	VCHE	TI3	TI2	TI1	TI0	VCH2	VCH1	VCH0

CH1 - CH0 : Part setting

Using CH1 or 0 bit, set the part of each rest.

CH[1:0]	Part designation
00b	0
01b	1
10b	2
11b	3

TI3 - TI0 : Interval setting

These bits are used to set the interval time before the processing of the next note and rest.

The interval “48” represents the time for the whole note.

The following table is exactly the same as that for the note data.

TI [3:0]	Interval
0h	3
1h	2
2h	3
3h	4
4h	6
5h	8
6h	9
7h	12
8h	18
9h	24
Ah	48
Bh	1
Ch	16
Dh	24
Eh	36
Fh	48

VCHE, VCH2 – VCH0 : Timbre change function

Although the maximum number of timbres that can be simultaneously used is four, the timbre can be changed during sound reproduction by setting these bits. Set VCHE to “1” and set a timbre number by using VCH2 to VCH0. Switching of timbre in rest data is made according to the designated time of the sequence data. After the next note to generate, the timbre in a part specified by CH0 and CH1 will be changed.

Make the change of a timbre after sound generation of a part to change is completely stopped.

The state at which sound generation is completely stopped is not a state where TK (sound length) is ended but a state where release time of envelope is completed.

Note that unusual sound may be instantaneously generated if switching the timbre while sound generation is not completely stopped.

If the timbre allocation is changed by using this function, the $30h register itself will be rewritten.

□**Timbre data register**

$10 – 2Fh Timbre data

Eight timbre data can be registered into the register and four data out of them can be simultaneously reproduced.

Timbre is made by setting both [parameters for the modulator] and [parameters for the carrier].

(For details of the modulator and the carrier, please refer to "General description of FM sound generator" (page 41)).

Index 10h, 11h …… 1st timbre_ timbre data for the modulator
Index 12h, 13h …… 1st timbre_ timbre data for the carrier
Index 14h, 15h …… 2nd timbre_ timbre data for the modulator
Index 16h, 17h …… 2nd timbre_ timbre data for the carrier
……Omitted…….
Index 2Ch, 2Dh …… 8th timbre_ timbre data for the modulator
Index 2Eh, 2Fh …… 8th timbre_ timbre data for the carrier

The following bit assignment is used for both modulator and carrier.
The setting must be completed before any sound is generated. Change of the timbre parameter during sound generation is prohibited.

Timbre data Default: 0000h

Index	B15	b14	b13	b12	B11	b10	B9	b8	b7	b6	b5	b4	b3	b2	b1	b0
EVEN	ML2	ML1	ML0	VIB	EGT	SUS	RR3	RR2	RR1	RR0	DR3	DR2	DR1	DR0	AR3	AR2
ODD	AR1	AR0	SL3	SL2	SL1	SL0	TL5	TL4	TL3	TL2	TL1	TL0	WAV	FL2	FL1	FL0

ML2 - ML0 : Multiple setting

"Multiple" is the multiplying factor for sound generating frequency. The output frequency is determined by the octave, pitch, and multiple settings on the carrier side. Adjusting the Multiple on the Modulator side allows various timbre creation.

ML [2:0]	Multiplying factor for frequency
0h	X 1/2
1h	X 1
2h	X 2
3h	X 3
4h	X 4
5h	X 5
6h	X 6
7h	X 7

VIB : Vibrato

This bit is used to set ON/OFF of vibrato function. “0” for OFF, “1” for ON.

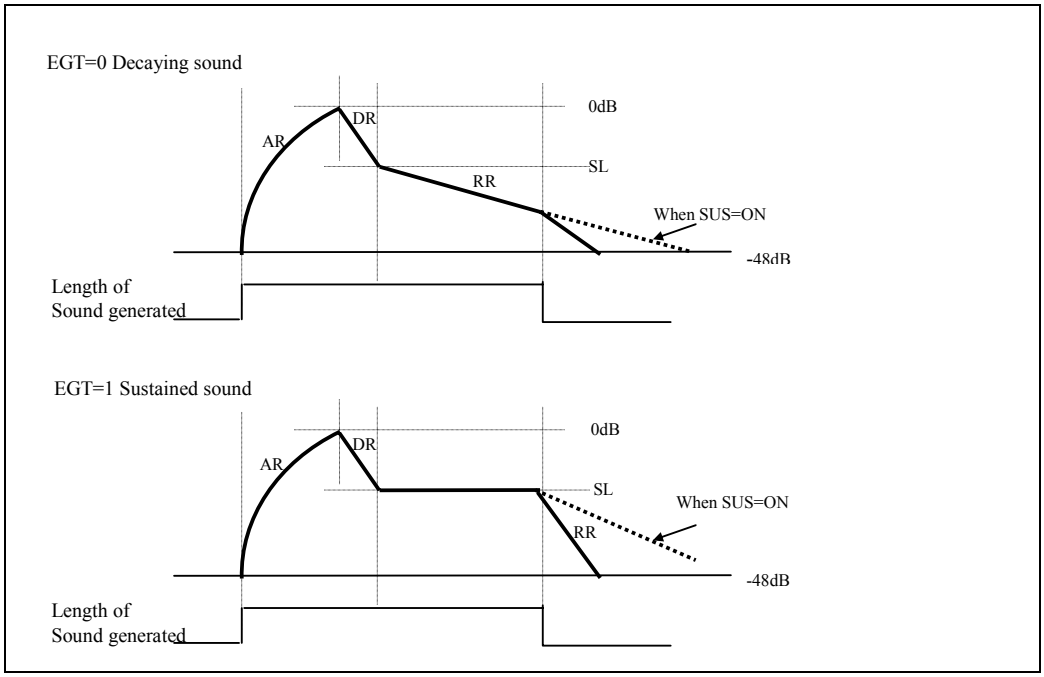
The vibrato frequency is 6.4 Hz and the modulation depth is ±13.47cent.

EGT : Envelope waveform type

This bit is used to select the type of the envelope waveform.

“0” for the decaying sound and “1” for the sustained sound.

Envelope waveforms shown below are for the decaying sound and sustained sound.



AR3 - AR0 : Attack Rate setting

“Attack Rate” is a time interval from the time sound starts generating (-48dB) to the time sound reaches at the maximum volume (0dB). The table on the next page is shown as the time taken from -48dB to 0dB.

DR3 - DR0 : Decay Rate setting

“Decay Rate” is a time interval taken for decay from 0 dB to the time it reaches at the Sustain Level (SL). The table on the next page is shown as the time taken from 0 dB to -48 dB.

RR3 - RR0 : Release Rate setting

Definition of the Release Rate differs between decaying sound and sustained sound.

- Decaying sound: Decaying time from the Sustain Level to the end of the sound generation. The sound decays taking 286 ms (time taken from 0 dB to -48 dB) after the end of the sound generation.
- Sustained sound: Decaying time from the end of the sound generation.

SL3 - SL0 : Sustain level setting

The Sustain Level, in the case of decaying sound, is the transition level from the Decay Rate to the Release Rate, and in the case of sustained sound, is a level held.

SL	SL3	SL2	SL1	SL0
Weighted bit (dB)	-24	-12	-6	-3

AR[3:0] DR[3:0] RR[3:0]	Attack rate -48 to 0dB (ms)	Decay Rate, Release Rate 0 to -48dB (ms)
Fh	0	2.23
Eh	4.65	8.94
Dh	9.30	17.88
Ch	18.59	35.76
Bh	37.19	71.52
Ah	74.38	143.04
9h	148.76	286.07
8h	297.51	572.14
7h	595.03	1144.25
6h	1190.05	2288.56
5h	2380.10	4577.12
4h	4760.21	9154.25
3h	9520.42	18308.50
2h	19040.84	36617.00
1h	∞	∞
0h	∞	∞

TL5 - TL0 : Total level setting

This function is used to set the envelope level.

TL	TL5	TL4	TL3	TL2	TL1	TL0
Weighted bit (dB)	-24	-12	-6	-3	-1.5	-0.75

SUS : Sustain On/OFF setting

"0" : OFF

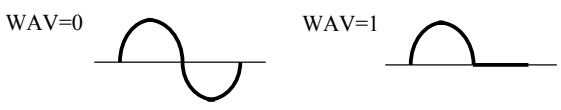
"1" : ON The Release Rate changes to "6" (2.29s) when the sound length comes to the end.

WAV : Waveform selection

The modulator and carrier can generate a sine wave; however, can generate a half-wave rectified waveform by setting this bit. Setting this bit allows creation using wider timbres.

"0" : Sine wave

"1" : Half-wave rectified waveform of a sine wave.



FL2 - FL0 : Feed-back setting

This function is available only for the operator of Modulator. These bits specify the feedback modulation depth. Be sure to set "0" to the operator of the carrier side. This is effective function for generating the strings timbres.

FL [2:0]	0	1	2	3	4	5	6	7
Modulation rate	0	π/16	π/ 8	π/ 4	π/ 2	π	2π	4π

□**Other control data**

$30h Timbre allocation data

One piece can be generated at the same time up to four parts, and timbre can be assigned for each part. The data is used by allocating four timbres out of eight timbres registered in the timbre data register to each part.

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$30h	0	V32	V31	V30	0	V22	V21	V20	0	V12	V11	V10	0	V02	V01	V00

"x" of Vx[2:0] indicates the part No.

Vx[2:0] and timbre data are as follows.

Vx[2:0]	Timbre data to use
0h	Timbre set in the Index of 10 to 13h is used.
1h	Timbre set in the Index of 14 to 17h is used.
2h	Timbre set in the Index of 18 to 1Bh is used.
3h	Timbre set in the Index of 1C to 1Fh is used.
4h	Timbre set in the Index of 20 to 23h is used.
5h	Timbre set in the Index of 24 to 27h is used.
6h	Timbre set in the Index of 28 to 2Bh is used.
7h	Timbre set in the Index of 2C to 2Fh is used.

$31h Tempo data

This register sets "tempo" for reproduction of a piece. Setting data is equal to (8739/TEMPO)-1. TEMPO is the number of crotchets that can be reproduced in one minute.

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$31h	0	0	0	0	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

$32h FM section control

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$32h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLR	ST

ST : This bit is used to control start/stop of a piece. "1" for start and "0" for stop.
FIFO becomes empty when ST is set to "0."

CLR : This bit is used to initialize the whole LSI by the software. All the registers except " Timbre data register" of Index 10 to 2Fh are initialized. Bit CLR itself is not cleared even if setting to "1." In normal operation, write "0" into the bit CLR..

$33h Clock selection

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$33h	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKSEL		

This register is used to set the clock frequency inputted through CLK_I pin when making the clock setting in the preset mode.

A clock with any frequency can be input during the reset period.

(For details of the clock setting, see "On clock frequency setting" (page 24)).

CKSEL [2:0]	Clock frequency (MHz)
0h(*)	2.688
1h	19.200
2h	19.680
3h	19.800
4h	8.400
5h	14.400
6h	27.821
7h	12.600

(*)When clock is set in the programmable mode, set CLKSEL[2:0] to "0h".

$34h Interrupt control

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$34h	0	0	0	0	0	0	0	0	0	0	IRQE	IRQ point				

The musical score data is taken into the FIFO which has a capacity for 32 data. As the sounds are reproduced, the data in FIFO are processed and deleted. And when the amount of data remaining in FIFO becomes less than the setting value of IRQ point, an interrupt signal is generated. At this point, set "0" to IRQE and then write the subsequent musical score data into FIFO.

Be sure to write data in excess of the IRQ point. After writing the data, reset IRQE to "1" and wait another interrupt signal.

IRQ point can be set in 32 ways from 0 (empty) to 31 (1 data vacancy).

IRQE is the interrupt enable bit. "1" indicates Enable.

$35h Speaker volume control

$36h FM volume control

$37h Earphone output volume control

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$35-7h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0

These bits are used to set the volume of each source. The volume setting consists of 31 steps and MUTE state, and can be set in 1dB steps. As the MUTE is selected in the default state, cancel and use the MUTE state before sound generation. And, be sure to power down the volume after muting it.

Relation between register setting value and volume.

V[4:0]	Volume(dB)	V[4:0]	Volume(dB)	V[4:0]	Volume(dB)	V[4:0]	Volume(dB)
00h	MUTE	08h	-23	10h	-15	18h	-7
01h	-30	09h	-22	11h	-14	19h	-6
02h	-29	0Ah	-21	12h	-13	1Ah	-5
03h	-28	0Bh	-20	13h	-12	1Bh	-4
04h	-27	0Ch	-19	14h	-11	1Ch	-3
05h	-26	0Dh	-18	15h	-10	1Dh	-2
06h	-25	0Eh	-17	16h	- 9	1Eh	-1
07h	-24	0Fh	-16	17h	- 8	1Fh	0

$38h Power Management control

Default: 001Eh

Index	b15	b14	b13	b12	b11	B10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$38h	0	0	0	0	0	0	0	0	0	0	0	AP4	AP3	AP2	AP1	DP

These bits are used to control the power-down. 1 digital line and 4 analog lines can be independently controlled. (For details, refer to "■Power-down control division diagram".)
Setting all bits to "1" will minimize the power of the entire LSI.

DP : Setting of "1" can power down the entire digital section.

AP1 : Setting of "1" can power down the VREF circuit in the analog section.

AP2 : Setting of "1" can power down the FM volume, speaker volume, equalizer circuit, and the non-inverted amplifier side of speaker output section.

AP3 : Setting of "1" can power down the inverted amplifier side of the speaker output section.

AP4 : Setting of "1" can power down the DAC and earphone output volume.

After initialization, the analog section (AP1 to AP4) is in the power-down state.

$39h Clock setting

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$39h	0	0	0	0	0	0	0	CLKSET								

The register is used to set the clock frequency that is input through the CLK_I pin when the setting is made in the programmable mode. Be sure to complete the setting before its sound generation.

A clock with any frequency can be input during the reset period.

For details of the clock setting, see “Clock Frequency Setting” (page 24).

CLKSET [8:0]	Clock frequency(MHz)
000000000b	(Preset mode)
000000001b	Prohibition
:	:
000101111b	Prohibition
000110000b	2.684658000
000110001b	2.740588375
:	:
111110001b	27.797396375
111110010b	27.853326750
111110011b	Prohibition
:	:
111111111b	Prohibition

The values that can be set to CLKSET are “000000000b”, and “000110000b” to “111110010b.”

When other value is set, the operation is not guaranteed.

A value to set to CLKSET can be found by using the following formula.

CLKSET = Clock frequency [KHz] / 447.443 × 8

For example, when the clock frequency is 3 MHz:

CLKSET = 3000 / 447.443 × 8 is about 54 = 000110110b

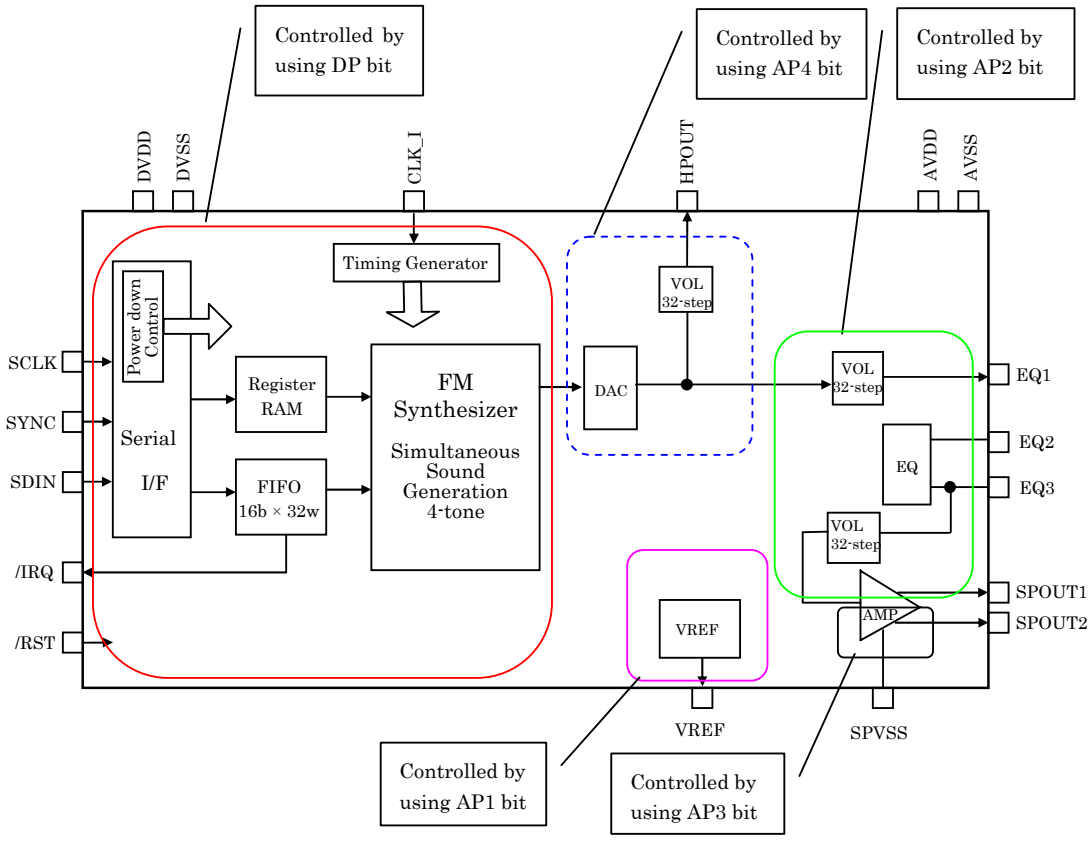
And, actual clock frequency to be set is as follows.

Clock frequency [kHz] = 54 × 447.443 / 8 = 3020.24[kHz] = 3.02024[MHz]

■Power-down control division diagram

Power-down of the LSI can be controlled for each divided internal function.

The power-down is controlled by Index 38h.



■Explanation of each bit

DP0

This is the bit to power off the whole digital section.
Consumption current of the digital part can be minimized because internal clock stops.
Contents of the registers are held but data in the FIFO are cleared.

AP1

This is the bit to power off the VREF circuit.
If AP1 is set to “1”, the whole analog section stops. Because an analog center voltage is made by VREF circuit.

AP2

This is the bit to power off the FM volume section, EQ circuit, speaker volume, and non-inverted amplifier side of speaker output section.

AP3

This is the bit to power off the inverted amplifier side of the speaker output section.
Turning the inverted amplifier side power on after turning the VREF circuit and a non-inverted amplifier power on can reduce pop noise.

AP4

This is the bit to power off the DAC and the HP Volume section.

Cautions for transition to the power-down

1. Be sure to shift a state to the power-down after the sound generation stops.
2. Power-down of the digital and analog section can be made at the same time.
   Be sure to mute FM Volume and HP Volume in advance for the reduction of noise during power-down transition.

The registers to which the digital section cannot access during the power-down are as follows.

Index	Register functions
$00h	Musical score data
$10-2Fh	Timbre data
$30h	Timbre allocation
$31h	Tempo data
$34h	IRQ Control

Cautions for cancellation of the power-down

1. The time of 64×CLK_I is necessary from the setting of DP=0 until the digital section returns to the normal operation. Be sure to access the registers after waiting for the time.
2. Perform the return procedure in this order when the whole analog section was powered off or the analog power supply is OFF.
   - Set AP1 to “0.” VREF goes up at the maximum of 50ms.
     Do not set AP2 to AP4 to “0” until VREF goes up.
   - Set AP2 to “0.”
   - Set AP3 and AP4 to “0” after at least 10µs.
   - Here, analog section is made available.
     Consumption current can be reduced more, by setting AP4 to “1” when only speaker amplifier section is used, and by setting AP2 and AP3 to “1” when only headphone is used without speaker amplifier.

Analog power supply OFF mode

Analog power supply can be powered off only when sound generation is being stopped.
Be sure to set AP1 to AP4 to “1” before powering off the analog power supply.
Or, pop noise may occur.

Example of the setting in each case.

Depending on how the function is used, bit settings can be combined as shown below.

	AP1	AP2	AP3	AP4	Caution
Analog section whole power-down	1	1	1	1	Be sure to set all volumes to “MUTE” first, then set all bits to “1” simultaneously.
Use of only earphone output.	0	1	1	0	Set the FM and speaker volumes to “MUTE.”
Use of only speaker.	0	0	0	1	Set the HP and FM volumes to “MUTE.”

■On Reset

This LSI can be initialized by setting /RST pin to "L." And, CLR bit is provided in $32h to allow the software to initialize the LSI.

Hardware reset initializes the LSI and returns it to the default condition.

All the registers except the timbre data register of Index 10h to 2Fh are initialized by the software reset.

A counter for the amount of FIFO data is cleared to "Empty" state.

Input of CLK_I is required during reset. Be sure to control so that CLK_I is input at least more than 100 clocks during the reset.

After the reset cancellation, access a register after waiting at least 64 clocks of CLK_I.

■Settings and Procedure required for a piece generation

Necessary settings and procedure are as follows.

1. Set the CLKSEL ($33h) or CLKSEL ($39h) according to the clock frequency inputted for CLK_I.
2. Cancel the power-down mode of the analog section. (See "Cautions for cancellation of the power-down" (page22).
3. Set the timbre data ($10-2Fh), timbre allocation data ($30h), tempo data ($31h) and volumes ($35-37h) as required.
4. Write musical score data ($00h) for 32 data (that is, to FIFO_FULL).
5. Set the IRQ point value of $34h.
6. Set the IRQE of $34h to "1."
7. Set the ST bit of $32h to "1" to start the melody.

■Clock Frequency Setting

Two modes for clock frequency setting are supported: "Preset mode" and "Programmable Mode."

Preset mode: a clock is selected from 2.688 / 8.4 / 12.6 / 14.4 /19.2 / 19.68 / 19.8 / 27.82 MHz.

Programmable mode: a clock is selected from 2.685 MHz to 27.853 MHz in 55.93 kHz steps.

1) When the preset mode is used:

Clock frequency setting can be made in the preset mode by setting a value to $33h.

In this case, set $39h to "000000000b." Operation is not guaranteed if other value is set.

When a value is not set to both $33h and $39h (default condition), a condition that 2.688 MHz is set in the preset mode is given.

2) When the programmable mode is used:

Clock frequency setting can be made in the programmable mode by setting a value to $39h.

In this case, set $33h to "000b." Operation is not guaranteed if other value is set.

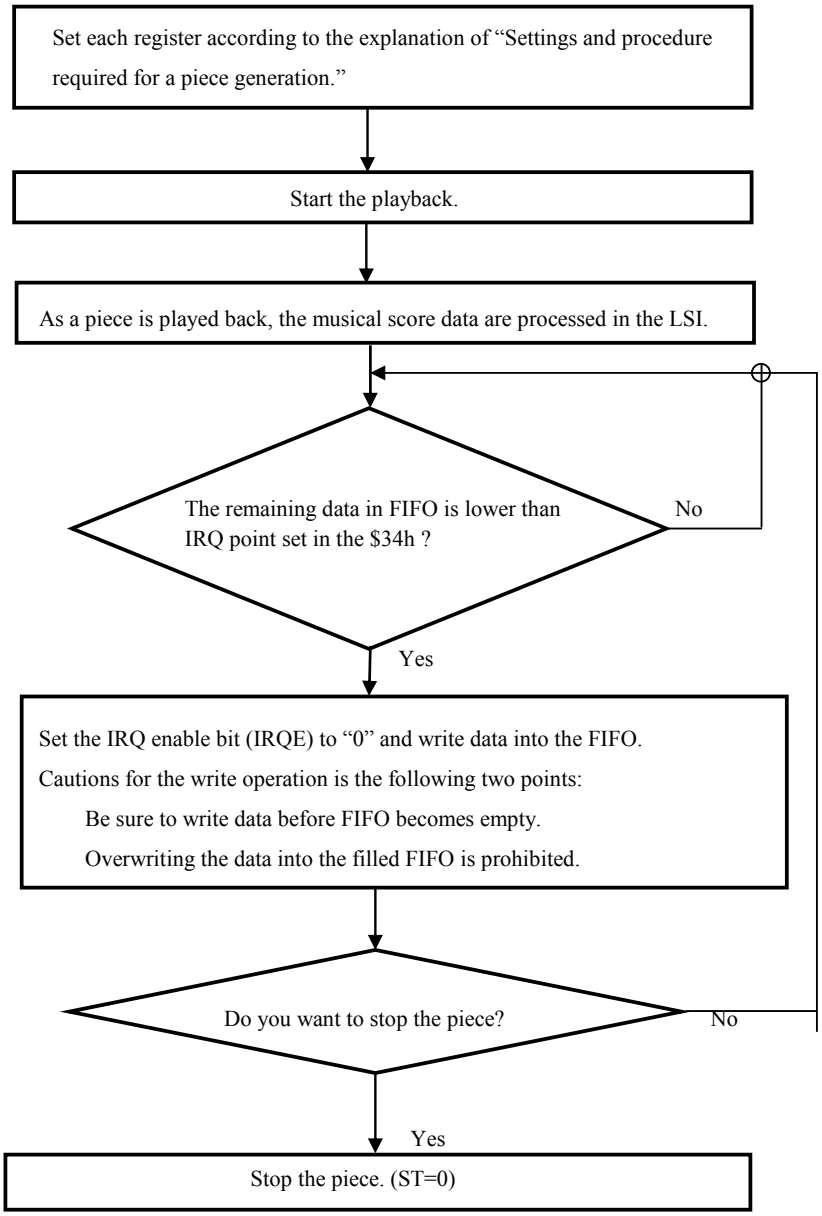
A value that can be set to $39h is "000000000b" and "000110000b" to "111110010b."

Operation is not guaranteed if other value is set.

■On Interrupt Sequence

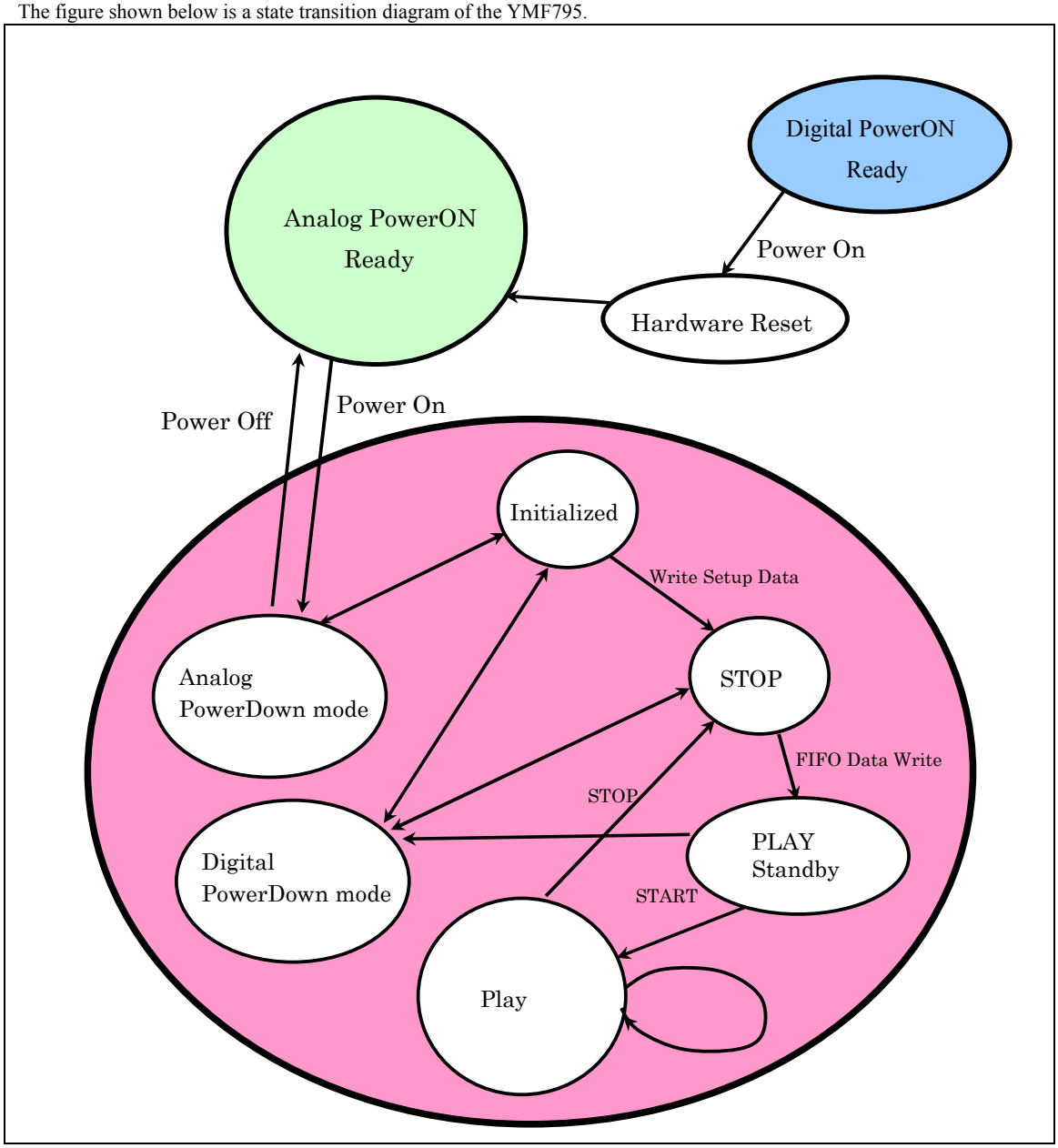
An interrupt from LSI (/IRQ-"L") occurs when the amount of data in the FIFO becomes less than the setting value.
For example, supposing that 10h (16b) is set to the IRQ point of $34h, the FIFO becomes full before starting a piece as described in "Settings and procedure required for a piece generation."
Once a piece is started, the data in the FIFO decreases as the musical score data is processed. When the amount of remaining data becomes 16 bytes or less, /IRQ pin becomes "L" and occurrence of an interrupt is sent to the external microprocessor.
When an interrupt signal is detected, set IRQE to "0" and write the musical score data into the FIFO before it becomes empty. As overwriting the data into the filled FIFO is prohibited, write the data into FIFO by the amount not causing the overwriting (16 data in this case).

Flow chart



■State Transition

The figure shown below is a state transition diagram of the YMF795.



Sequence to turn the power supply on.

A way to turn the analog side power on after turning the digital side power on to initialize the hardware is ideal. If the analog power supply is turned on before the hardware is initialized, noise may be generated.

Description of each state

Digital Power ON Ready

This is a state before turning on the digital power supply.

Hardware Reset

Input the hardware reset to the LSI in conjunction with the power-on of the digital power supply.

Analog Power ON Ready

This is a state before turning on the analog power supply. Turn on the analog power supply after the initialization of the digital section.

Analog Power Down mode

This is a state in which power consumption of the analog section is the minimum.

Operation state is shifted to this operation mode after the analog power supply is turned on. In order to proceed to the next step "Initialized" state, follow the procedure described on page 22.

Be sure to shift from the "Initialized" state in order to shift to this operation mode from a state except Analog Power ON. (That is, each volume must be set to "MUITE.")

A point to power down can be selected according to the usage. For details, refer to the description of Power-down on pages of 21, 22, and 23. Be sure to power off the analog power supply from this state.

Initialized

This state is given after the Power Down mode of the analog and the digital section.

And, shift to the power-down mode from this state.

STOP

This is a state in which volume mute cancellation and the timbre data setting has been completed. In this state, the FIFO is empty. This state returns when the melody reproduction is stopped.

And, transition to the power-down of the digital section is possible from this state. This state will return when the power-down is cancelled.

PLAY Standby

This is a state that is given immediately before the playback of a piece after the write of musical score data into FIFO. Setting bit ST to "1" will shift to the next "PLAY" state. Transition to the power-down of the digital section is possible from this state. However, the state will return to "STOP" state after the power-down cancellation.

PLAY

This is a state in which a piece is being played back. Setting bit ST to "0" will shift to the "STOP" state. Transition to the power-down of the digital section from this state is prohibited. (Noise may be generated.)

Digital Power Down mode

This is a state in which the digital section is in the power-down state. (DP bit = "1")

This state can reduce the power consumption of the digital section because a clock is not input to the LSI even if it is input to CLK_I pin. Make the HP Volume and FM Volume mute state before shifting to this mode.

■Operation in FIFO empty condition

If FIFO become empty during reproduction the musical score data written last is processed continuously until the next data is written.

If the last data written is a note data, that note is reproduced continuously.

If the last data written is a rest data, the rest state is held.

■Reproduction method assuming occurrence of empty state

In the normal reproduction, occurrence of FIFO Empty is prohibited; however, even simple processing can generate a short tone if the above features are effectively used. Processing for interrupt is not required.

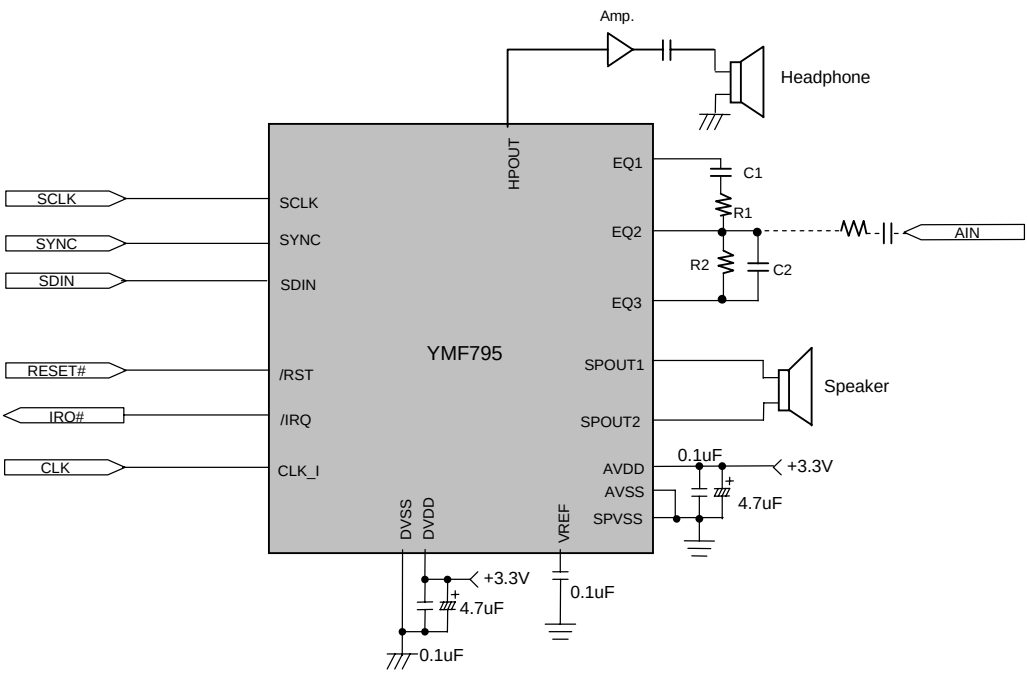
Make the processing according to the following flow.

Short tone is 1 to 32 word data block.

If data block exceeds 33 words, make the processing by the usual reproduction flow using interrupt.

1) Complete the following procedure in advance: Power ON → Analog Power Down mode → Initialized → STOP (See the figure of "■State Transition" (page 26).
2) Start the reproduction in the FIFO Empty state.
3) Write the data block to be reproduced into FIFO.
4) Immediately after writing (after 0 to 20μs), the musical score data are internally processed and its reproduction starts.
   As reproduction goes on, the data in FIFO are processed and cleared.
5) When FIFO becomes empty, if the last data in the data block is a note data, that note is reproduced continuously and if it is a rest data, the rest state is held until the next data block is written into FIFO.
6) When reproducing the next data block, go to step 3).
   To stop the reproduction set ST to "0." Then, the data counter of FIFO will be cleared and the state returns to a state of step 1).

■Example of peripheral circuit



On /RST pin

A schmitt circuit is not used for /RST pin in this device; therefore, please design a board in consideration of noise to the /RST line.

Precautions for the use of separate power supplies:

A LSI with multiple power supply inputs needs to pay attention to the followings for [Power supply connection] and [Ground connection].
We explain it here by giving an analog circuit power supply and a digital circuit power supply as an example.

[Power supply connection]

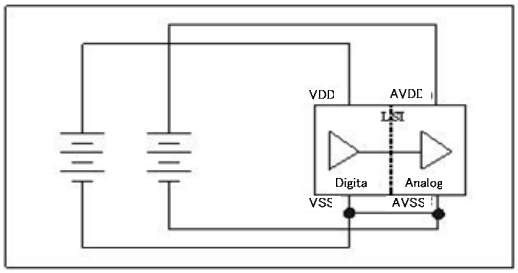
When a power supply for analog circuits of this LSI and a power supply for digital circuits of this LSI can be separately prepared (including a case where a power supply for the LSI's analog circuits is shared with analog circuits of the later stage) please refer to "(1) Circuit diagram and wiring diagram when two power supplies are used:" On the contrary, when multiple power supplies cannot be prepared, please refer to "(2) Circuit diagram and wiring diagram when one power supply and one voltage regulator IC are used:"

And, when "(1) Circuit diagram and wiring diagram when two power supplies are used:" is selected, room for improvement of analog performance becomes big, but you need to consider avoidance of time interval difference between power supplies at the time of power-on (power-off).

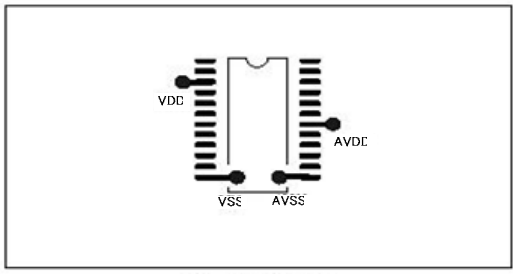
[Ground connection]

The ground connection is common to "(1) Circuit diagram and wiring diagram when two power supplies are used:" and "(2) Circuit diagram and wiring diagram when one power supply and one voltage regulator IC are used:" In each case, grounds must not be separated.

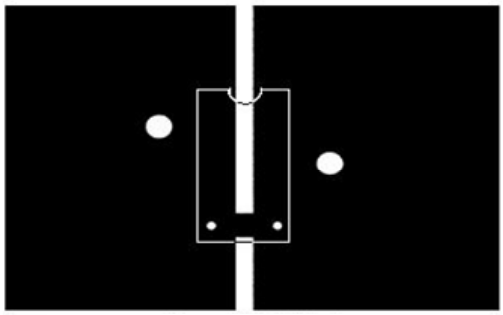
(1) Circuit diagram and wiring diagram when two power supplies are used:



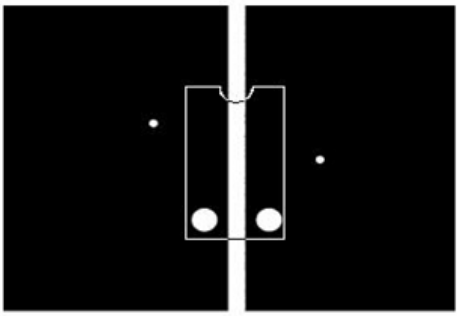
Circuit Diagram



Component Side Wiring Diagram



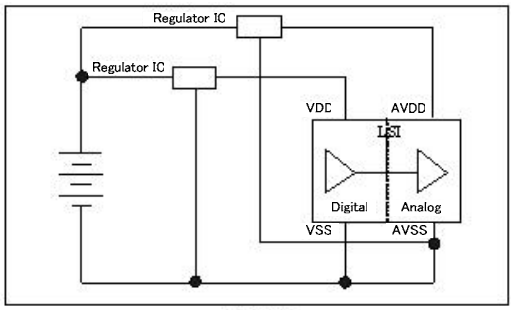
Ground Layer Wiring Diagram



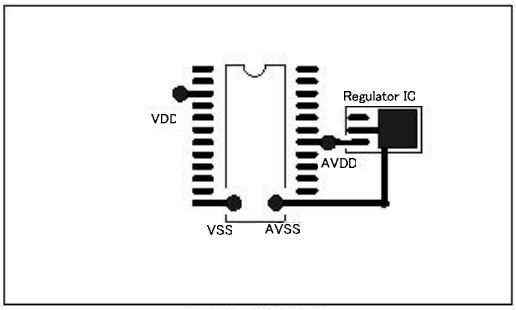
Power Supply Layer Wiring Diagram

・Be sure to connect VSS pin to AVSS pin near the LSI. Excessive inductance between VSS pin and AVSS pin may cause malfunctions and failures.

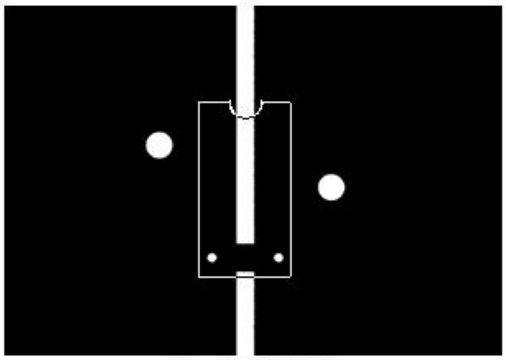
(2) Circuit diagram and wiring diagram when one power supply and one voltage regulator IC are used:



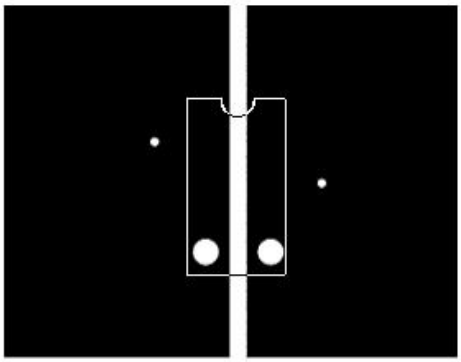
Circuit Diagram



Component Side Wiring Diagram



Ground Layer Wiring Diagram



Power Supply Layer Wiring Diagram

・Be sure to connect VSS pin to AVSS pin near the LSI. Excessive inductance between VSS pin and AVSS pin may cause malfunctions and failures.

・Connect the ground pin of the voltage regulator IC used for analog circuits near AVSS pin to prevent influence of digital circuit's current change.

・The later analog circuits shall consider the AVSS pin as a reference potential.

Warning for the device which makes sound through speaker

A speaker radiates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When DC signal (several Hz or less) is input, heat radiation characteristics falls rapidly.
In addition, even if it is used lower than the rated input, it may lead to voice-coil burnout, smoke, or ignition of a speaker.
In order to avoid such situations, be sure to implement one or more preventive measures from the followings.

1. Don't select settings (sound creation) which may generate DC signal.
   (Since thoroughness of this preventive measure is generally difficult, we recommend the combined use with the following 2, 3, and 4)
2. Add the equivalent of DC cut digital filter for cutting DC signal into a digital section.
   (As long as "Built-in" is not mentioned in the manual, there is no such built-in circuit inside of a device).
3. Add a DC cut capacitor for cutting DC signal into an analog section.
   (When addition is specified in the example of a recommended circuit diagram, be sure to add)
4. When a latter stage device exists in the signal path from this device to speaker, be sure to realize the DC cut is realized in a latter stage device.

In addition, the above-mentioned measures are based on the assumption that the device itself, DC cut capacitor, and a latter stage device will be in a normal operation. Therefore, it is also necessary to implement measures based on the assumption of these part failures.

Warning for short circuit at speaker pins

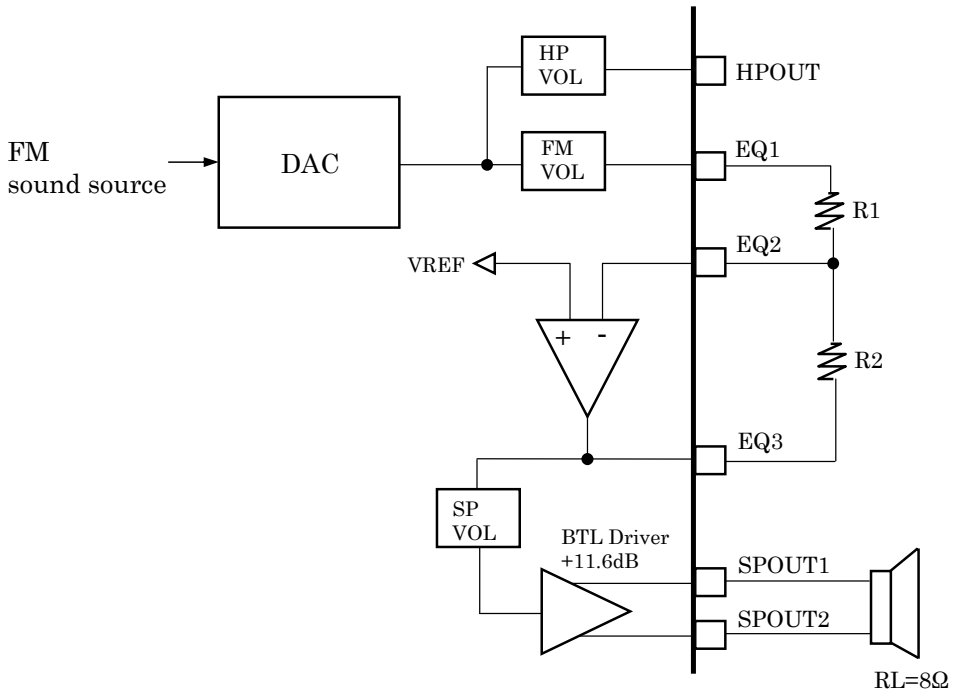
Overcurrent breakdown, extraordinary heat, or package melting is caused if a short circuit is made between two outputs, between output and power supply, and between output and Ground, because of high drive performance of the speaker amplifier output.
In order to avoid such situations, be sure to implement one or more preventive measures from the followings.

1. Adoption of a power supply with overcurrent protection circuit for the speaker amplifier.
2. Provision of an overcurrent protection circuit in the speaker amplifier circuit.
   (This device does not have the circuit)
3. Provision of a thermal shutdown circuit in the speaker amplifier section.
   (This device does not have the circuit)

In addition, the above-mentioned measures are based on the assumption that overcurrent circuit or thermal shutdown circuit will work normally. Therefore, it is also necessary to take measures based on the assumption of these part failures.
Moreover, consider the followings as well.
- Design the board so that speaker amplifier output is not short-circuited easily even if foreign body or solder bridge is present.
- Warning to customers of risk that may be caused by a short circuit of the speaker amplifier output.

■Volume level Adjustment in monophonic sound and 4-sound generation

The volume level outputted from DAC varies depending on the number of the pronunciation.
When one tone (*) is output from the FM sound source, output voltage amplitude from DAC becomes 0.4125 Vp-p.
When multiple sounds are pronounced at the same time, output voltage amplitude varies depending on phase of each waveform, but when the waveforms with the same phase are overlapped, it becomes 0.825 Vp-p in 2-tone, 1.2375 Vp-p in 3-tone, and 1.65 Vp-p in 4-tone.
(*: This explanation is made on the assumption that volume adjustment (Total Level of Carrier) of one tone is 0 dB.)



An assumption of 300 mW output.

Output power of 300 mW can be obtained from the speaker when RL is 8 Ω and a voltage between SPOUT1 and 2 is 1.55 Vrms.

At this time, BTL output amplitude becomes 1.55×2×1.414=4.38 Vp-p, and EQ3 pin is 4.38/3.8=1.15 Vp-p.
(Gain with the speaker amplifier is +11.6 dB= 3.8 times.)

Assurance of volume level in monophonic sound.

"Gain adjustment in the EQ amplifier section" is recommended as a way to assure the volume level in monophonic sound.

The Gain depends on the resistance ratio between R1 and R2, and Gain is equal to R2/R1.

The Gain of 3 times to 4 times is recommended.

Example of the recommended level adjustment in all the system

Turn down either FM or SP volume a little as a default (-3 dB to -6 dB or so).

This is made for previously assuring a volume of which Gain is increased, because either volume may be controlled by user

EQ amplifier Gain of 3 times to 4 times or so is recommended to secure the output level to some extent in monophonic sound. (For example, R1=22 kΩ, R2=82 kΩ).

When monophonic sound is generated in this condition (FM volume as 0dB), EQ1 is 0.4125 Vp-p, and if Gain of the EQ amplifier is four times, EQ3 becomes 1.65 Vp-p.

When -4 dB is given by SPVOL, voltage between SPOUT1 and 2 becomes 3.96 Vp-p, and resultantly 245 mW output power can be obtained with the speaker (RL=8Ω).

A level adjustment of 4-sound simultaneous generation

When normal music is played back, the amplitude of DAC seldom swings to 1.65 Vp-p.

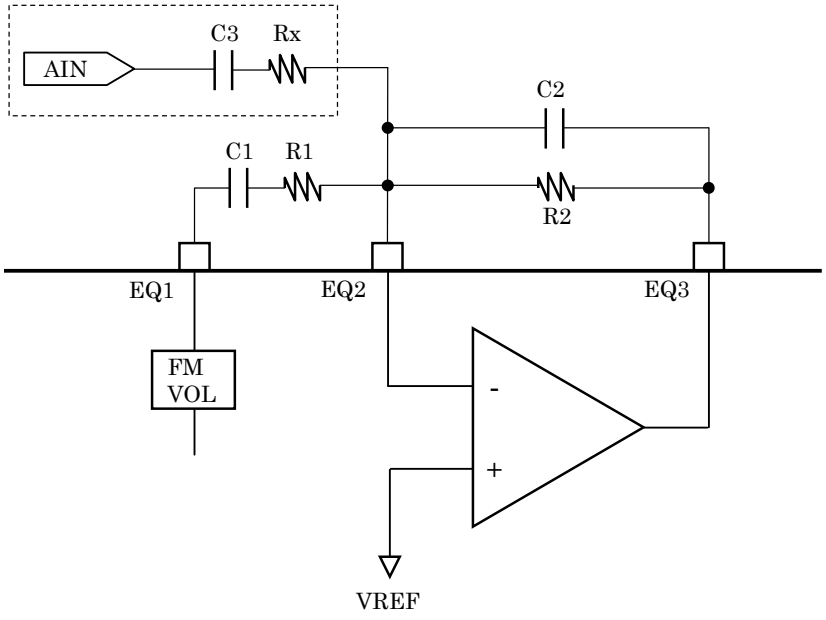
Therefore, the same Gain settings as that of monophonic sound can be made but if distortion of its sound is a little significant, turn down the Gain of EQ amplifier or adjust the FM and/or SP volume.

A level adjustment of HPOUT

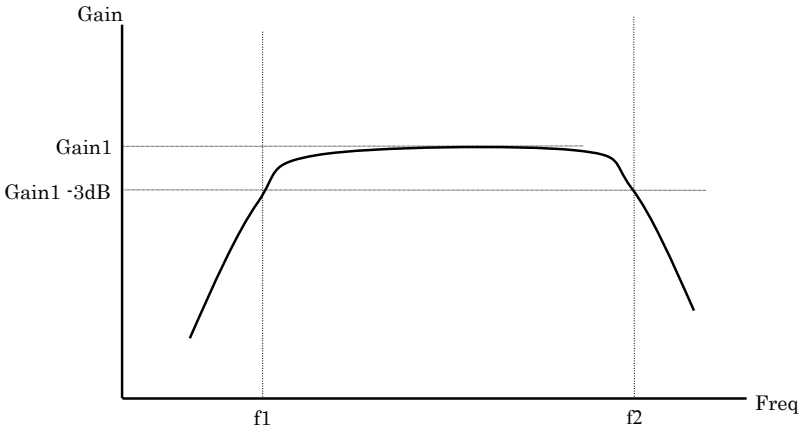
Adjust the GAIN outside the LSI to increase Gain of the HPOUT side.

■Sound Quality Correction Circuit

Sound quality and Gain can be corrected by using an external circuit connected to EQ1 to 3 pins.
The internal circuit configuration of EQ1 to 3 pin and example of the external circuit are as follows.

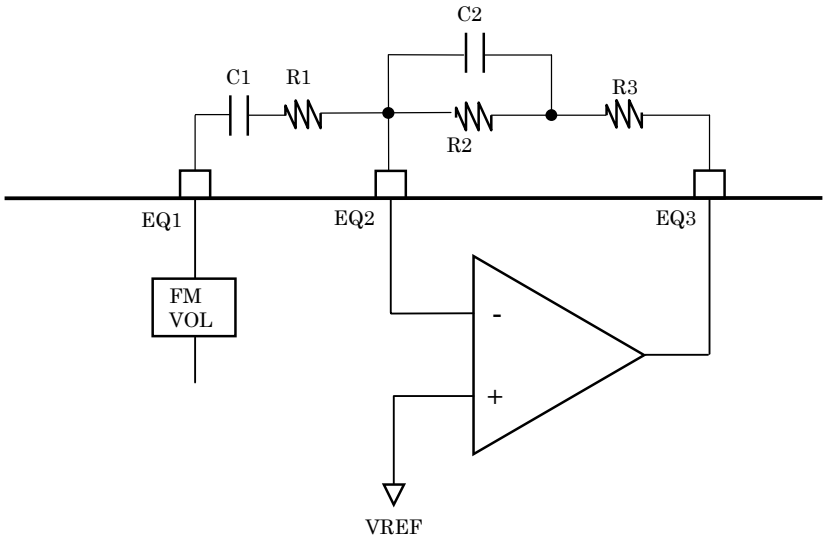


Gain and filter characteristic can be controlled by a value of C1, C2, R1, and R2.
Gain = R2 / R1. The recommended values: R1 = 22 kΩ and R2 = 82 kΩ (Gain = 3.7 times).
Filter cutoff frequency of f1 and f2 is:
f1 = 1/ (2π×R1×C1).
f2 = 1/ (2π×R2×C2).
If C1 = 0.022 µF and C2 = 120 pF, the cutoff frequency of f1 = 330 Hz and f2 = 16 kHz.



Moreover, the circuit enclosed with the dotted line is required when mixing with analog signal from AIN is desired.
The level adjustment for mixing depends on the resistance ratio R2/Rx of Rx and R2.
The value of Rx should be 82 kΩ when mixing of amplitude of one time is required.

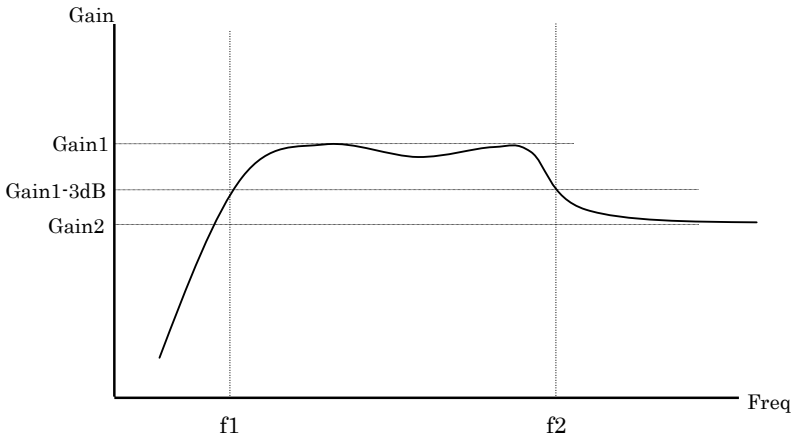
Using a resister R3 can obtain the following frequency characteristic.



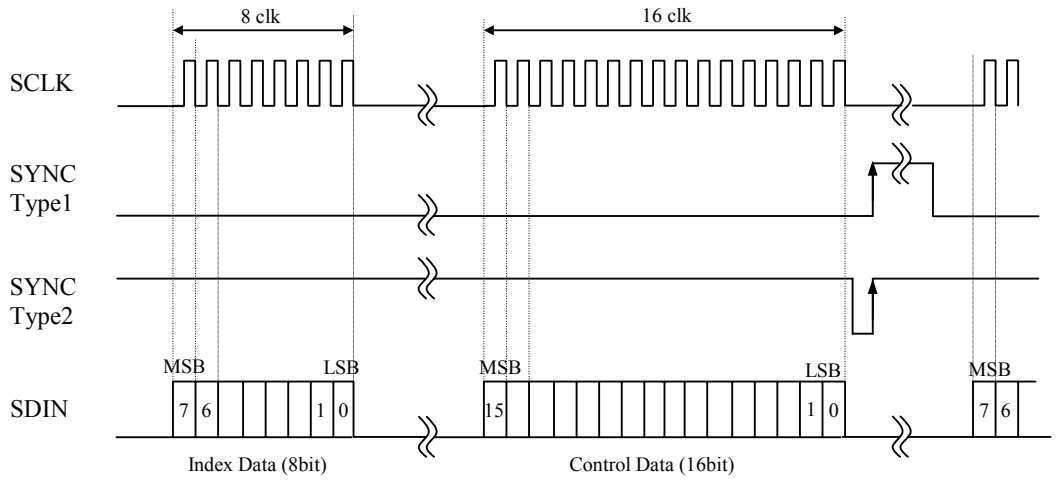
Gain1= (R2+R3) /R1. Gain2=R3/R1.
Filter cutoff frequency of f1 and f2 is:

f1=1/ (2π×R1×C1).

f2=1/ (2π×R2×C2).



■Serial I/F Specifications



YMF795 is controlled by the three serial interface lines of SCLK, SYNC, and SDIN.

Relation between SDIN and SCLK

The LSI takes in the value of SDIN at the rising edge of SCLK.
Input the SDIN so that Setup/Hold time is assured with respect to the rising edge of SCLK.
(For details of timing specification, see "4. AC characteristics" in "Electric Characteristics")

About SDIN

The above figure has the period at which no data is transferred between Index data and Control data, but this period is not necessarily required. Data of 24-bit can be transferred in succession.
When transfer in 8 bits is required, divide the Control data in two of high-order 8 bits and low-order 8 bits. The interval between the first high-order 8 bits and the next low-order 8 bits transfer is not especially defined. However, if excessive interval is given, time taken to complete one transfer becomes long. Pay attention so that FIFO does not become empty when writing the musical score data into the FIFO.

About SYNC

Both Type1 and Type2 in the above figure are available.
The LSI considers the rising edge of SYNC as the completion of one data transfer..
The LSI sees SDIN for 24×SCLK before the rising edge of SYNC as valid data.
(SDIN for 16×SCLK are valid data when only Control Data is transferred.)
The length of the period of "H" is not especially defined, but for the waveform of Type 2, control so that the period of "L" is assured at least 100 ns.
Malfunction may be caused when a rising edge of SYNC comes close to a rising edge of SCLK.
Consider so that a rising edge of SCLK does not generate within 50ns with respect to a rising edge of SYNC.

About the data transfer only Control Data.

When the SDIN for SCLK×16 is input between a rising edge of SYNC and the next rising edge of SYNC, the LSI judges it as the musical score data ($00h) to take it in.
Use this transfer when transferring musical score data fast.

■Electrical Characteristics

1. Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (analog)	AVDD	-0.3	4.6	V
Supply voltage (digital)	DVDD	-0.3	4.6	V
Analog input voltage	V_{INA}	-0.3	AVDD+0.3	V
Digital input voltage	V_{IND}	-0.3	DVDD+0.3	V
Storage temperature	T_{STG}	-50	125	°C

Note) DVSS = AVSS= SPVSS = 0V

2. Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating voltage (analog)	AVDD	3.0	3.3	3.6	V
Operating voltage (digital)	DVDD	3.0	3.3	3.6	V
Operating ambient temperature	T_{OP}	-40	25	85	°C

Note) DVSS = AVSS = SPVSS = 0V

3. DC characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}		0.7 × DVDD	-	-	V
Low-level input voltage	V_{IL}		-	-	0.2 × DVDD	V
High-level output voltage	V_{OH}	I_{OUT} = -1mA	0.8 × DVDD	-	-	V
Low-level output voltage	V_{OL}	I_{OUT} = 1mA	-	-	0.4	V
Schmitt width	Vsh			1.0		V
Input leakage current	IL		-10		10	μA
Input capacity	CI				10	pF

Note) T_{OP}=-40 to 85°C, DVDD=3.3±0.3V, Capacitor load=50pF

4. AC characteristics

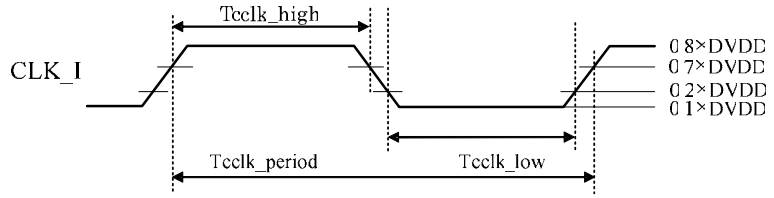
Conditions: Input signal of V_{IH}=0.8×DVDD, V_{IL}=0.1×DVDD.
Timing measurement at V_{IH}=0.7×DVDD, V_{IL}=0.2×DVDD.

4-1. CLK_I ,Reset

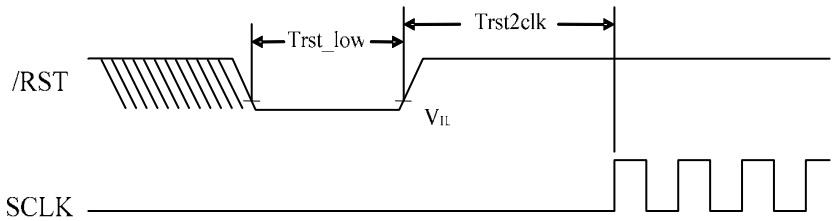
Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK_I clock period	Tcclk_period	35.8			ns
CLK_I "L" pulse width	Tcclk_low	12			ns
CLK_I "H" pulse width	Tcclk_high	12			ns
/RST active "L" pulse width	Trst_low	100			× CLK_I
SCLK start delay time (after /RST inactive)	Trst2clk	64			× CLK_I

Note) T_{OP}=-40 to 85°C, DVDD=3.3±0.3V, Capacitor load=50pF
"× CLK_I" indicates the number of clocks inputted through the CLK_I pin.

CLK_I Duty



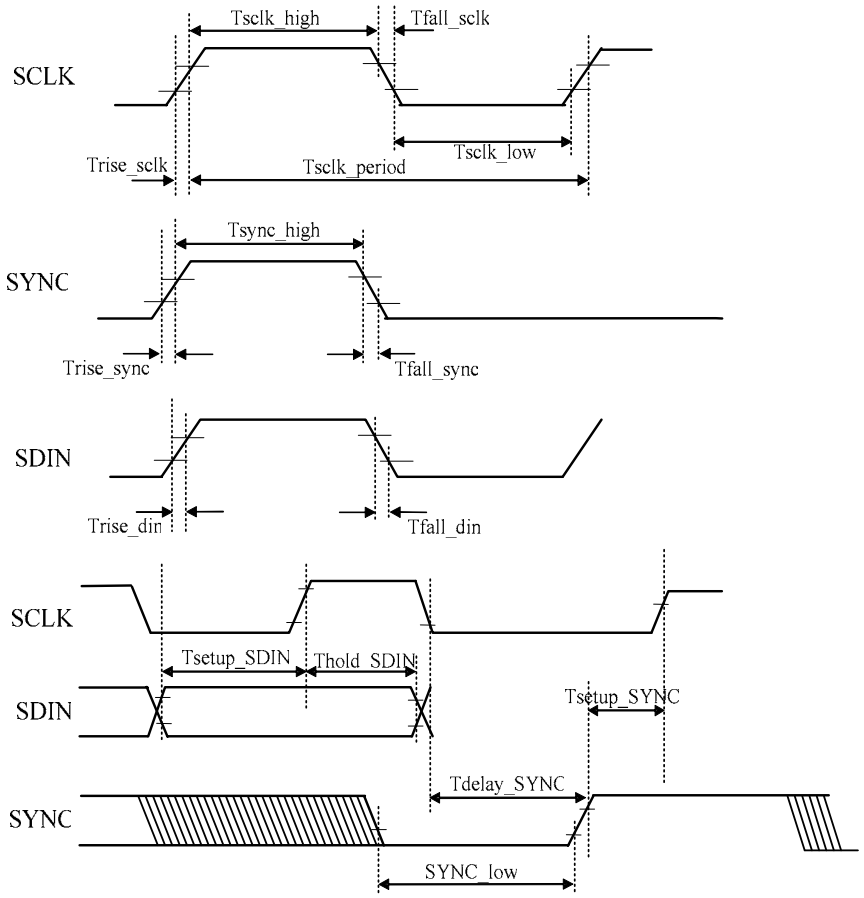
Hardware Reset



4-2. Serial Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK clock period	Tsclk_period	430			ns
SCLK "L" pulse width	Tsclk_low	200			ns
SCLK "H" pulse width	Tsclk_high	200			ns
SCLK rise time	Trise_sclk			20	ns
SCLK fall time	Tfall_sclk			20	ns
SYNC "H" pulse width	Tsync_high	100		-	ns
SYNC rise time	Trise_sync			20	ns
SYNC fall time	Tfall_sync			20	ns
SYNC delay time	Tdelay_SYNC	0			ns
SYNC "L" pulse width	SYNC_low	100			ns
SYNC → SCLK setup time	Tsetup_SYNC	50			ns
SDIN setup time	Tsetup_SDIN	50			ns
SDIN hold time	Thold_SDIN	50			ns
SDIN rise time	Trise_din			20	ns
SDIN fall time	Tfall_din			20	ns

Note) T_{OP}=-40 to 85°C, DVDD=3.3±0.3V, Capacitor load=50pF



5. Power consumption

Parameter	Min.	Typ.	Max.	Unit
Digital part in normal operation		550	2200	μA
Analog part without sound generation		10	13	mA
Analog part at output 300mW, 8Ω load		186		mA
In power-down mode		0.1	1	μA

Note) T_{OP}=-40 to 85°C, DVDD= AVDD = 3.3±0.3V, Capacitor load=50pF

6. Analog characteristics

SP Amplifier

Parameter	Min.	Typ.	Max.	Unit
Gain setting (fixed)		±1.9		times
Minimum resister load (RL)		8		Ω
Maximum output voltage amplitude (RL=8Ω)		5.5		Vp-p
Maximum output power (RL=8Ω, THD+N≤1.0%)		500		mW
THD + N (RL=8Ω, f=1kHz, 300mW output)		0.025		%
Noise level without signal (A-filter)		-90		dBV

Note) T_{OP}=25°C, DVDD = AVDD = 3.3V

EQ Amplifier

Parameter	Min	Typ	Max.	Unit
Gain setting range			30	dB
Maximum output voltage amplitude		3.0		Vp-p
THD + N (f=1kHz)			0.05	%
Noise level without signal (A-filter)		-90		dBV
Input impedance	10			MΩ
Feedback resistance EQ2-EQ3	20			kΩ

Note) T_{OP}=25°C, DVDD = AVDD = 3.3V

SP Volume

Parameter	Min	Typ	Max	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Decay rate in MUTE	80			dB

Note) T_{OP}=25°C, DVDD = AVDD = 3.3V

FM Volume

Parameter	Min	Typ	Max	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Decay rate in MUTE	80			dB
Minimum load resistance		20		kΩ
Maximum output voltage amplitude		3.0		Vp-p
Output impedance		300	600	Ω

Note) T_{OP}=25°C, DVDD = AVDD = 3.3V

HP Volume

Parameter	Min	Typ	Max	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Decay rate in MUTE	80			dB
Minimum load resistance		20		kΩ
Maximum output voltage amplitude		3.0		Vp-p
Output impedance		300	600	Ω

Note) T_{OP}=25°C, DVDD = AVDD = 3.3V

VREF

Parameter	Min	Typ	Max	Unit
VREF voltage		0.5×AVDD		V

Note) T_{OP}=25°C, DVDD = AVDD = 3.3V

DAC

Parameter	Min	Typ	Max	Unit
Resolution		12		Bit
Full-scale analog output (*1)		1.65		Vp-p
THD+N (f= 1kHz)			0.5	%
Noise level without signal (f=400Hz to 20kHz)		-90		dBV
Frequency characteristic (f=50Hz to 20kHz)	-3.0 (2*)		+0.5	dB

Note) T_{OP}=25°C, DVDD = AVDD = 3.3V

*1: When four FM tones are simultaneously generated in the same phase.

*2: Degradation of high-frequency response due to aperture effect.

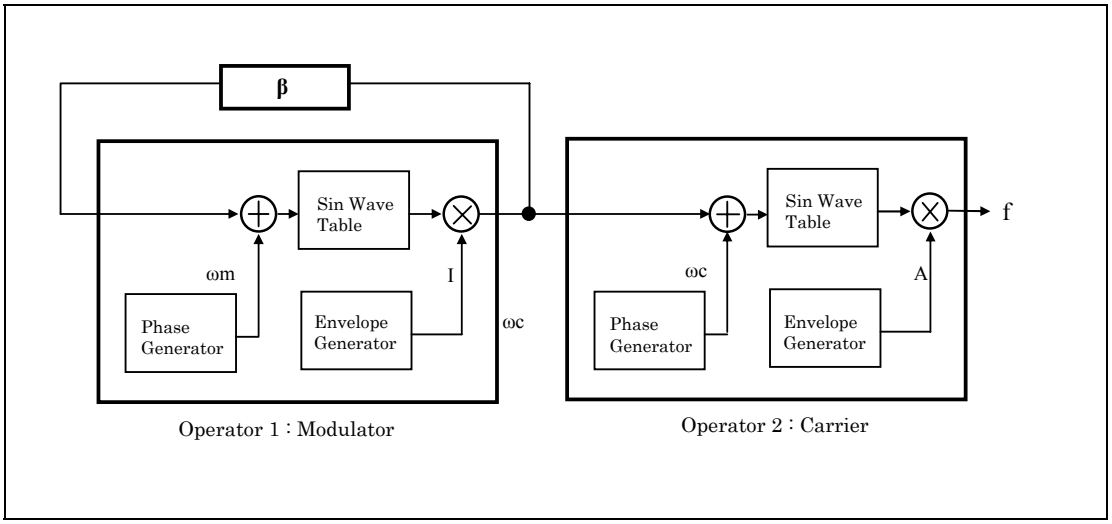
■General description of FM sound generator

"FM" stands for Frequency Modulation.

The FM sound generator utilizes the higher harmonic wave produced by the frequency modulation for synthesis of the musical sounds

With the use of this FM system enables a comparatively simple circuit to produce such waveform that has a harmonic wave including disharmonious sounds, it is possible to create a wide range of sounds from the synthesized sounds of the natural musical instruments to the electronic sounds.

The diagram below shows the most basic configuration of the FM system.



The "Operator" refers to the section where a sine wave is generated and the combination of the operators is called "algorithm". The operator in the front stage is called "modulator" and that in the rear stage "carrier".

Each operator is capable of setting the frequency and the envelope waveform.

The configuration in the above diagram can be expressed in the formula as follows.

$$FM(t) = A \sin(\omega c t + B \sin \omega m t)$$

A : Amplitude of the carrier. B : Amplitude of the modulator. ωc : Angle frequency of the carrier

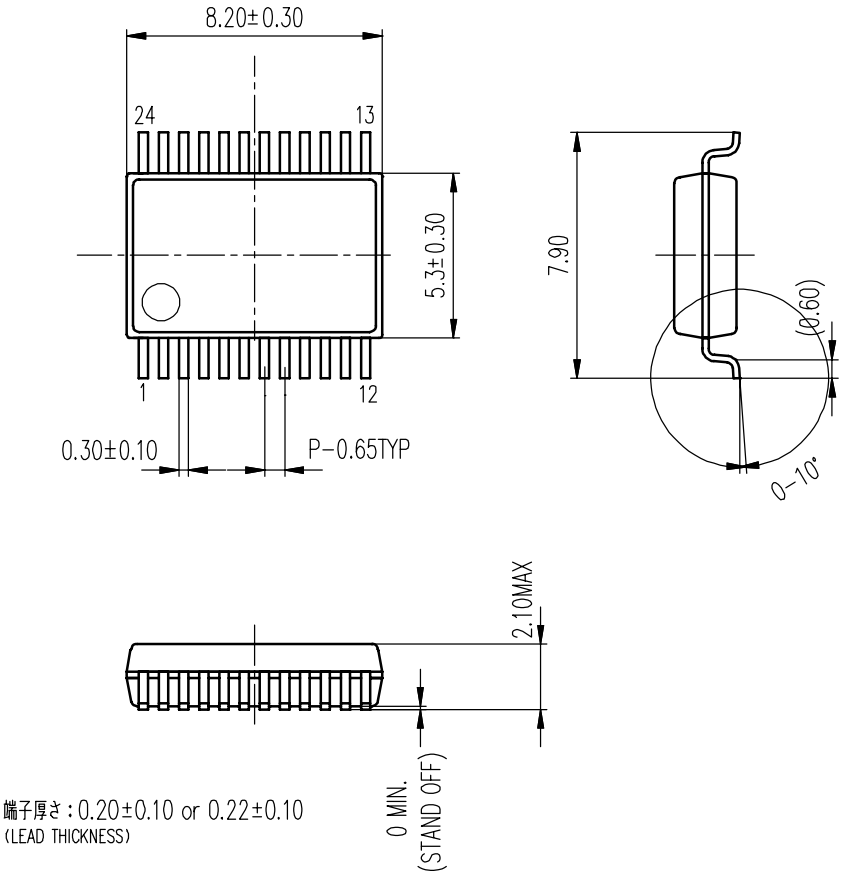
ωm : Angle frequency of the modulator

In addition, a system called "feedback FM" is available to create a wider range of sounds. In this system, the frequency modulation is fed back as shown in the diagram in the following page.

B is called "feed-back ratio". Using the feed-back FM function, it is possible to produce the strings type sounds.

■**External dimensions**

C-PK24EP-1



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
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