Chrontel

CH7021A
Brief Datasheet

CH7021A SDTV / HDTV Encoder

Features

- VGA to SDTV/EDTV/HDTV conversion supporting graphics resolutions up to 1600x1200
- HDTV support for 480p, 576p, 720p, 1080i and 1080p
- Support for NTSC, PAL, SECAM color modulation.
- Macrovision™ 7.1.L1 copy protection support for SDTV
- Macrovision™ copy protection support for progressive scan TV (480p, 576p)
- CGMS-A support for SDTV and HDTV
- High-speed SDVO◊ (1G~2Gbps) AC-coupled serial differential RGB inputs
- Flexible TrueScale™ rendering engine supports overscan compensation in all SDTV/EDTV and HDTV output resolutions †¥
- Text enhancement filter in scan conversion¥
- Adaptive de-flicker filter with up to 7 lines of filtering in scan conversion¥
- Contrast/Brightness/Sharpness control for TV output.
- Hue/Saturation Control for TV output.
- Support for SCART connector
- Support for HDTV D-Connector
- Outputs CVBS, S-Video, RGB and YPbPr
- Support for VGA RGB bypass
- TV / Monitor connection detect
- Programmable power management
- Four 10-bit video DAC outputs
- Three sets of DAC outputs supporting SDTV / HDTV / CRT RGB connectors
- Fully programmable through serial port
- Configuration through Intel® SDVO OpCode◊
- Complete Windows driver support
- Offered in a 64-pin LQFP package

† Patent number 5,781,241
¥ Patent number 5,914,753
◊ Intel Proprietary.

General Description

The CH7021A is a Display Controller device which accepts a digital graphics input signal, and encodes and transmits data through analog SDTV ports (analog composite, s-video, RGB or YPrPb) or an analog HDTV port (YPrPb). The device is able to encode the video signals and generate synchronization signals for NTSC, PAL and SECAM SDTV standards, as well as analog HDTV interface standards and graphics standards up to UXGA. The device accepts one channel of RGB data over three pairs of serial data ports.

The TV-Out processor will perform scaling to convert VGA frames to supported SDTV and HDTV output standards. Adaptive de-flicker filter provides superior text display. Large numbers of input graphics resolutions are supported up to 1600 by 1200 with full vertical and horizontal overscan compensation in all output standards. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality.

In addition to scaling modes, bypass modes are included which perform color space conversion to SDTV or HDTV standards and generate and insert SDTV or HDTV sync signals, or output VGA style analog RGB for use as a CRT DAC.

Different analog video connectors are supported including composite, s-video, YPrPb, SCART, D-connector and VGA connector.

Content protection support is provided for Macrovision™ in SDTV and EDTV modes. CGMS-A is also provided up to 1080i resolution.

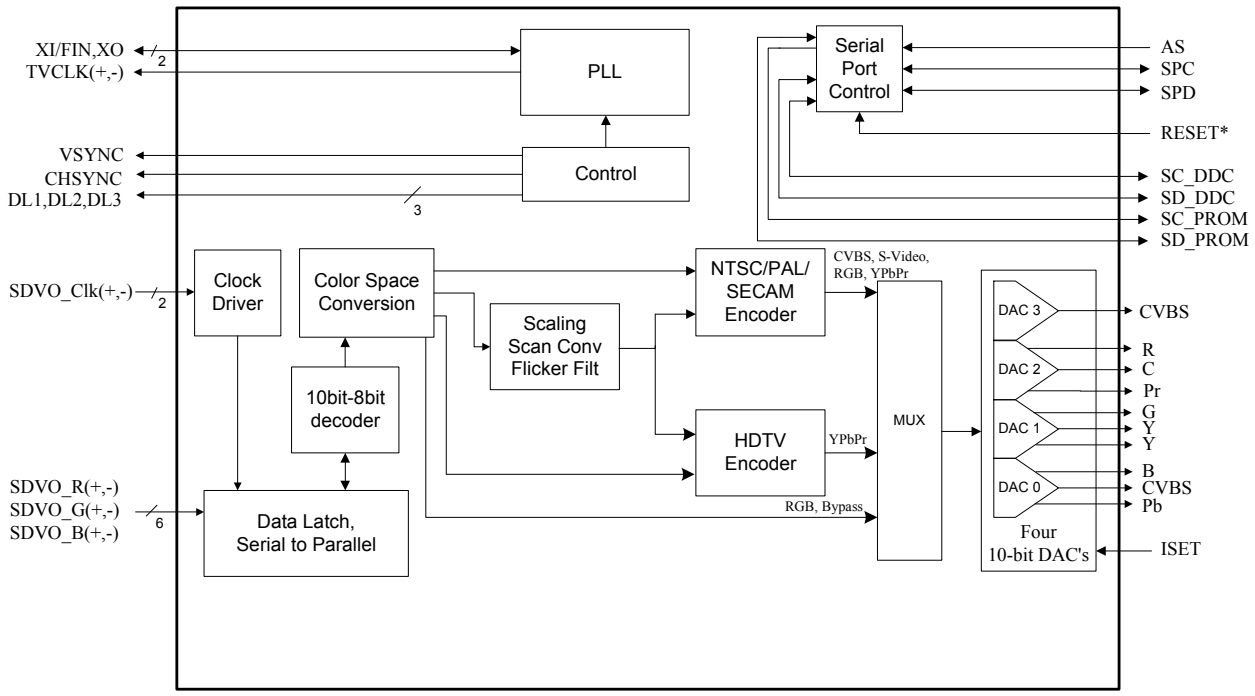

Figure 1: Functional Block Diagram

1.0 Pin-Out

1.1 Package Diagram

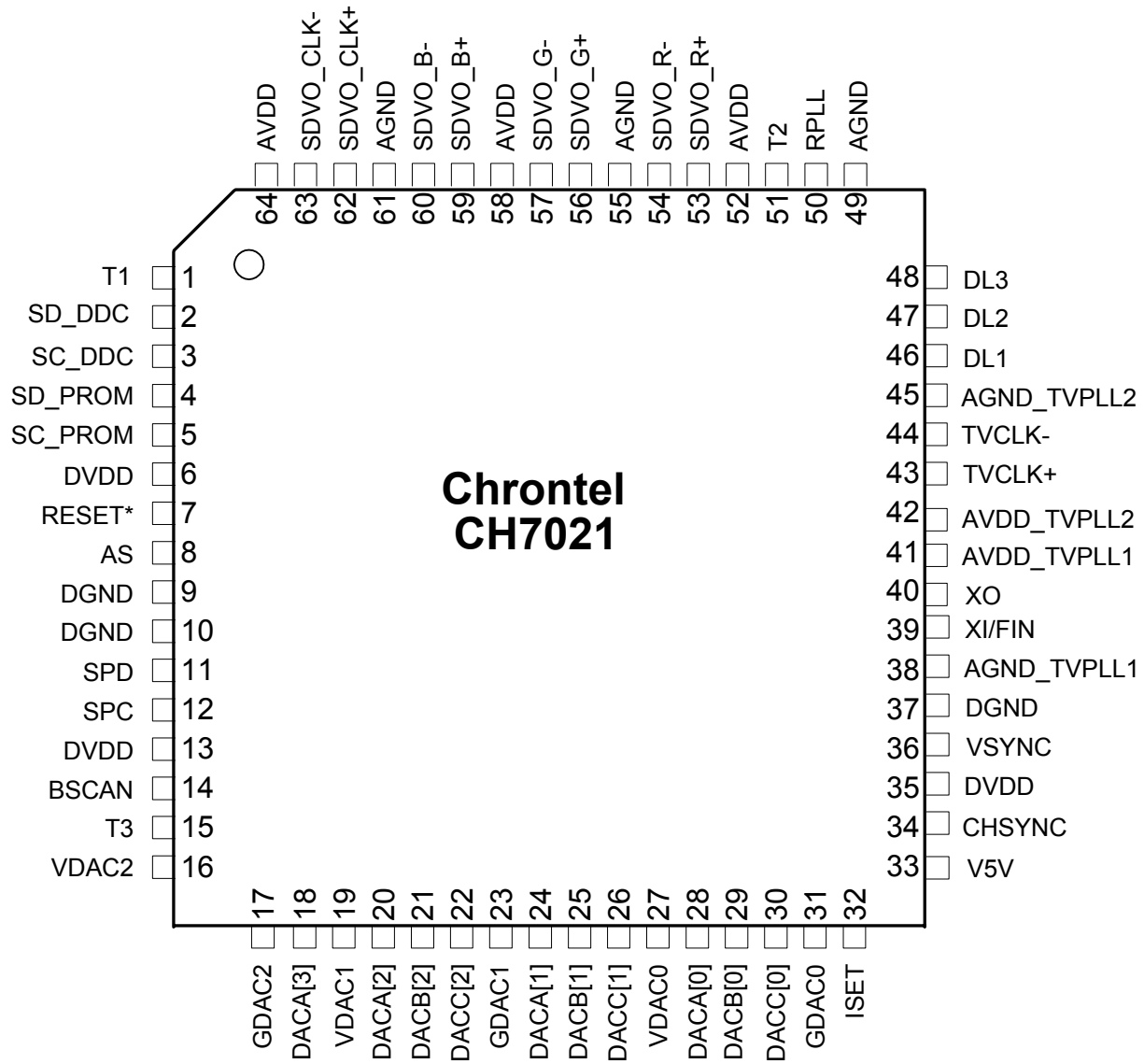

Figure 2: 64-Pin LQFP Package

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1,51	Out	T1,T2	**Test** These pins are reserved for factory test.
2	In/Out	SD_DDC	**Routed Serial Port Data Output to DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
3	In/Out	SC_DDC	**Routed Serial Port Clock Output to DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
4	In/Out	SD_PROM	**Routed Data Output to PROM** This pin functions as the bi-directional data pin of the serial port for PROM on ADD2◊ card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
5	Out	SC_PROM	**Routed Clock Output to PROM** This pin functions as the clock bus of the serial port to PROM on ADD2 card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
7	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register. This pin is 3.3V compliant.
8	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (0,1,1,1,0,0,AS*,0). When AS is low the address is 72h, when high the address is 70h.
11	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 2.5V. Outputs are driven from 0 to 2.5V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 2.5V.
12	In/Out	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and operates with inputs from 0 to 2.5V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 2.5V.
14	In	BSCAN	**BSCAN** (internal pull low) This pin should be left open or pulled low with a 10k resistor in the application. This pin enables the boundary scan for in-circuit testing. Voltage level is 0 to DVDD. This pin should be pulled low during normal operation.
15	In	T3	**Test** (internal pull-down) This pin should be left open or pulled low with a 10k resistor in the application.
18,20,24,28	Out	DACA[3:0]	**DAC Output A** Video Digital-to-Analog outputs. Refer to section **Error! Reference source not found.** for information regarding support for Composite Video, S-Video, SCART, YPrPb and RGB Bypass outputs. Each output is capable of driving a 75-ohm doubly terminated load.
21,25,29	Out	DACB[2:0]	**DAC Output B** Video Digital-to-Analog outputs. Refer to section **Error! Reference source not found.** for information regarding supports for Composite Video, S-Video, SCART, YPrPb and RGB Bypass outputs. Each output is capable of driving a 75-ohm doubly terminated load.

◊ Intel Proprietary.

Table 1: Pin Description (contd.)

Pin #	Type	Symbol	Description
22,26,30	Out	DACC[2:0]	**DAC Output C** Video Digital-to-Analog outputs. Refer to section **Error! Reference source not found.** for information regarding supports for Composite Video, S-Video, SCART, YPrPb and RGB Bypass outputs. Each output is capable of driving a 75-ohm doubly terminated load.
32	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 1.2Kohm resistor should be connected between this pin and DAC ground (pin 31) using short and wide traces.
34	Out	CHSYNC	**Composite / Horizontal Sync Output** A buffered version of VGA composite sync as well as horizontal sync can be acquired from this pin.
36	Out	VSYNC	**VSYNC** A buffered version of VGA vertical sync can be acquired from this pin.
39	In	XI/FIN	**Crystal Input / External Reference Input** A parallel resonant 27MHz crystal (±20 ppm) should be attached between this pin and XO. However, an external CMOS clock can drive the XI/FIN input.
40	Out	XO	**Crystal Output** A parallel resonance 27MHz crystal (±20 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to the XI/FIN input, XO should be left open.
43,44	Out	TVCLK+/-	**Pixel Clock Output** When the chip is operating as a TV encoder in master clock mode, this pair outputs a differential clock to the VGA controller. The VGA controller uses this as a reference frequency to generate SDVO_CLK+/- to the chip. The clock frequency is between 100MHz ~ 200MHz. This clock pair will run at an integer multiple of the desired input pixel rate. Refer to section **Error! Reference source not found.** for details.
46	Out	DL1	**D-Connector Line 1** Video format identification line for HDTV D-Connector. See section **Error! Reference source not found.**.
47	Out	DL2	**D-Connector Line 2** Video format identification line for HDTV D-Connector. See section **Error! Reference source not found.**.
48	Out	DL3	**D-Connector Line 3** Video format identification line for HDTV D-Connector. See section **Error! Reference source not found.**.
50	In	RPLL	**PLL Resistor Input** External resistor 10Kohm should be connected between this pin and pin 49.
53,54,56,57 59,60	In	SDVO_R+/-, SDVO_G+/-, SDVO_B+/-	**SDVO Data Channel Inputs** These pins accept 3 AC-coupled differential pair of RGB inputs from a digital video port of a graphics controller.
62,63	In	SDVO_CLK+/-	**Differential Clock Input associated with SDVO Data channel (SDVO_R+/-, SDVO_G+/-, SDVO_B+/-)** The range of this clock pair is 100~200MHz. For specified pixel rates in specified modes this clock pair will run at an integer multiple of the pixel rate. Refer to section **Error! Reference source not found.** for details.

Table 1: Pin Description (contd.)

Pin #	Type	Symbol	Description
6,13,35	Power	DVDD	**Digital Supply Voltage** (2.5V)
9,10,37	Power	DGND	**Digital Ground**
16	Power	VDAC2	**DAC Supply Voltage** (3.3V)
17	Power	GDAC2	**DAC Ground**
19	Power	VDAC1	**DAC Supply Voltage** (3.3V)
23	Power	GDAC1	**DAC Ground**
27	Power	VDAC0	**DAC Supply Voltage** (3.3V)
31	Power	GDAC0	**DAC Ground**
41	Power	AVDD_TVPLL1	**TV PLL1 Supply Voltage** (2.5V)
38	Power	AGND_TVPLL1	**TV PLL1 Ground**
42	Power	AVDD_TVPLL2	**TV PLL2 Supply Voltage** (2.5V)
45	Power	AGND_TVPLL2	**TV PLL2 Ground**
52,58,64	Power	AVDD	**Analog Supply Voltage** (2.5V)
49,55,61	Power	AGND	**Analog Ground**
33	Power	V5V	**D-Connector Supply Voltage** (5V)

2.0 Package Dimensions

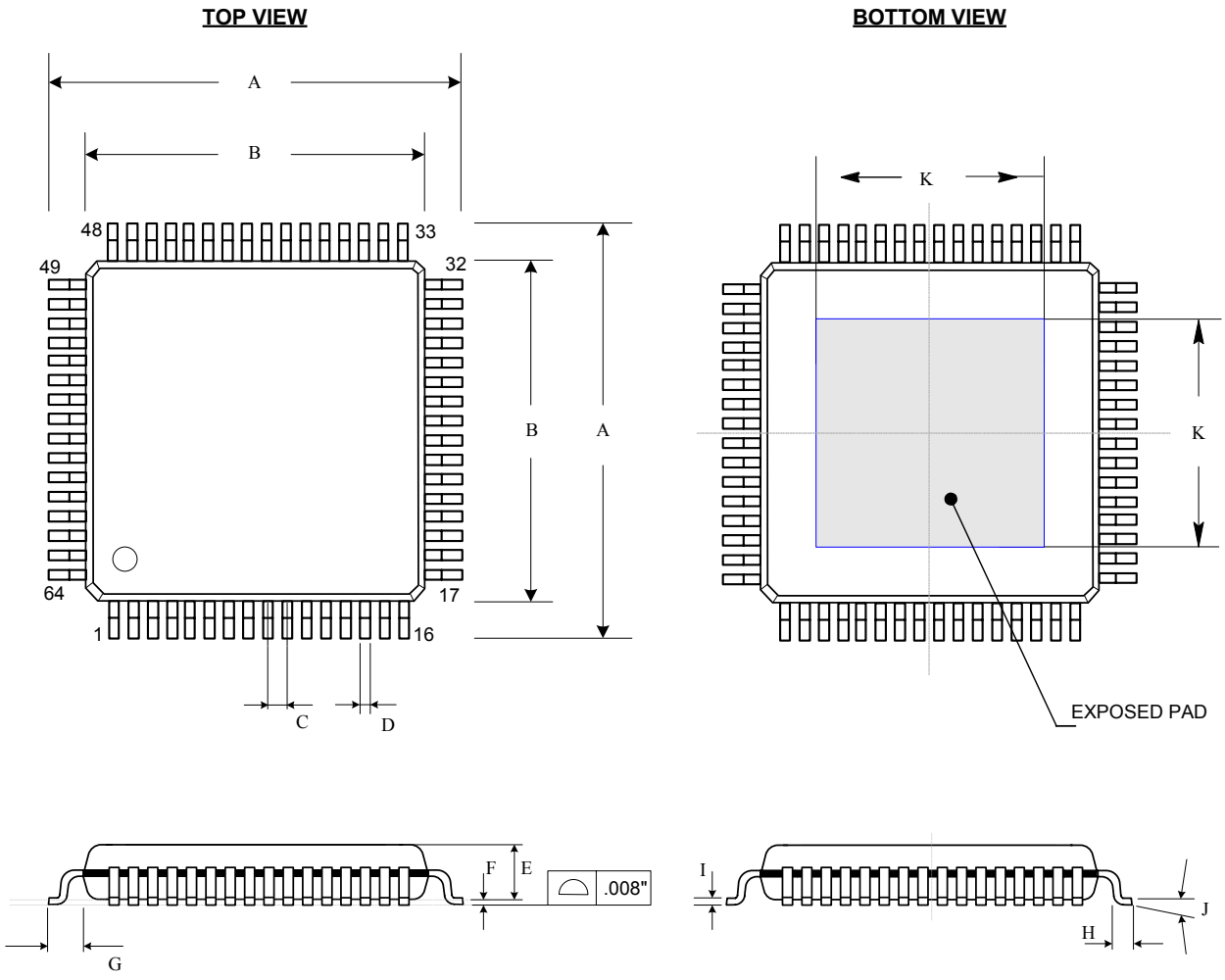

Figure 3: 64 Pin LQFP (Exposed Pad) Package

Table of Dimensions

No. of Leads		SYMBOL										
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°	5.85
	MAX				0.27	1.45	0.15		0.75	0.20	7°	7

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply
CH7021A-TE	LQFP with exposed pad	64	2.5V & 3.3V
CH7021A-TE-TR	LQFP with exposed pad in Tape & Reel	64	2.5V & 3.3V
CH7021A-TEF	Lead Free LQFP with exposed pad	64	2.5V & 3.3V
CH7021A-TEF-TR	Lead Free LQFP with exposed pad in Tape & Reel	64	2.5V & 3.3V

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