
Chrontel CH7028B SDTV Encoder

Features

- TV encoder targets the handheld devices and other appropriate display devices used in consumer products. (i.e. automobile).
- Support TV output format (NTSC, PAL).
- Two on-chip 10-bit high speed DACs providing flexible output capabilities. Such as single, double CVBS outputs, and S-video output.
- Internal embedded 16Mbits SDRAM is used as frame buffer supporting for frame rate conversion.
- Flexible up and down scaling engine is embedded including de-flickering capability.
- Programmable 18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supports various RGB (RGB666, RGB565 and etc), YCbCr (4:2:2 YCbCr, ITU656) and 2x or 3x multiplexed input. CPU/MEMORY interface is also supported.
- Support for flexible input resolution up to 800x800 and 1024x680. (i.e. 220x176, 320x240, 640x480 720x480, 720x576, 800x480, 800x600 480x800, 600x800 and etc)
- Pixel by pixel brightness, contrast, hue and saturation adjustment for each output is supported.
- Pixel by pixel horizontal position adjustment and line by line vertical position adjustment are supported.
- 90/180/270 degree image rotation and vertical or horizontal flip functions are supported.
- TV connection detection capability. DAC can be switched off based on detection result. (Driver support is required)
- Programmable power management.
- Flexible pixel clock frequency from graphics controller is supported (2.3MHz –120MHz).
- Flexible input clock from crystal or oscillator is supported (2.3MHz – 64MHz).
- Only slave mode supported.
- Offered in LQFP package and BGA package.
- Fully programmable through serial port.
- IO and SPC/SPD voltage supported is from 1.2V to 3.3V.

General Description

The CH7028B is a device targeting handheld and similar systems which accept digital input signal, and encodes and transmits data through 10-bit DACs. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards. The device accepts different data formats including RGB and YCbCr (e.g. RGB565, RGB666, ITU656 like YCbCr, etc.). 16Mbit SDRAM is embedded in package. Frame rate conversion and Image rotation are possible.

Note: the above feature list is subject to change without notice. Please contact Chrontel for more information and current updates.

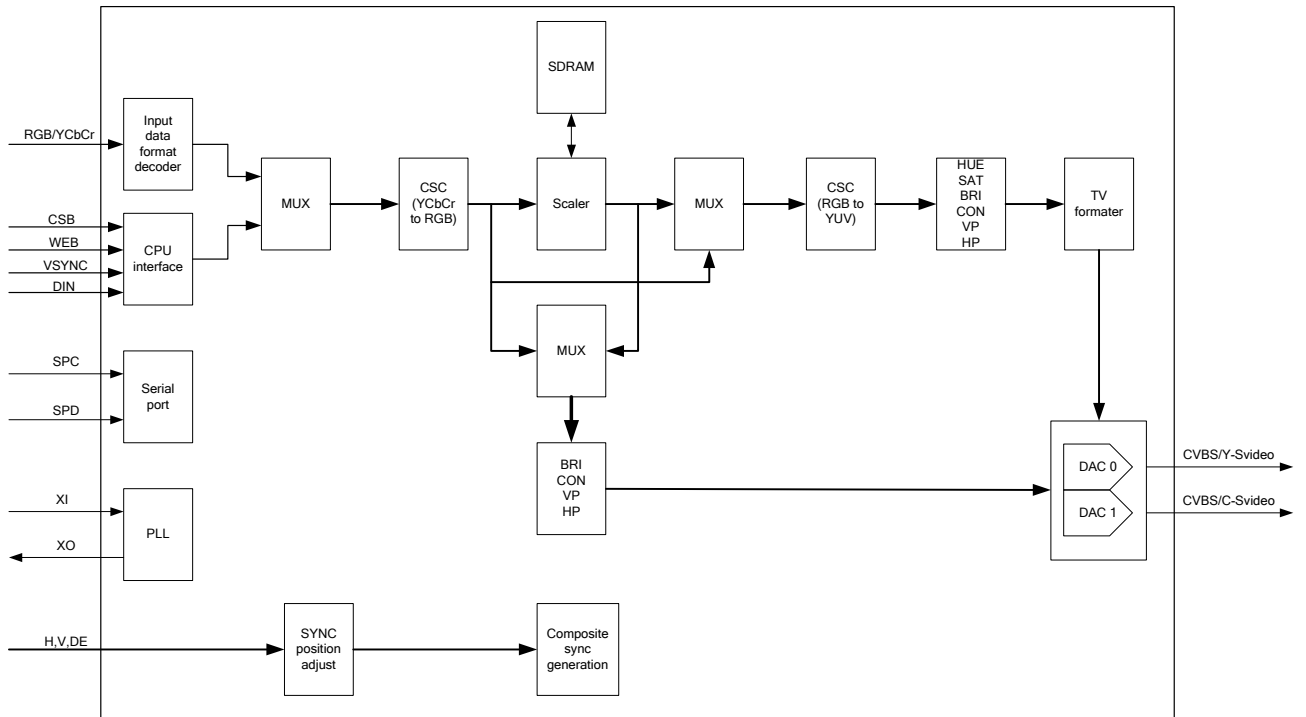


Figure 1: CH7028B Block Diagram

Table of Contents

1.0 Pin-out 5

 1.1 Package Diagram 5

 1.2 Pin Description 7

2.0 Functional Description..... 11

 2.1 Input Interface..... 11

 2.1.1 Overview..... 11

 2.1.2 Input Clock and Data Timing Diagram..... 11

 2.1.3 Input Data Voltage..... 12

 2.1.4 Input Data Format 12

 2.2 Chip Output 14

 2.2.1 TV Output 14

 2.2.2 Video DAC Output 14

 2.2.3 DAC Single/Double Termination 14

 2.2.4 TV Connection Detect 14

 2.2.5 Picture Enhancement..... 14

 2.2.6 Color Sub-Carrier Generation..... 15

 2.2.7 ITU-R BT.470 Compliance..... 15

 2.2.8 SDRAM Power Down 15

 2.2.9 Test Pattern Select..... 15

3.0 Electrical Specifications 16

 3.1 Absolute Maximum Ratings 16

 3.2 Recommended Operating Conditions 16

 3.3 Electrical Characteristics 17

 3.4 Digital Inputs / Outputs..... 17

 3.5 AC Specifications 18

4.0 Package Dimensions 19

5.0 Revision History 21

Figures and Tables

LIST OF FIGURES

Figure 1: CH7028B Block Diagram2
 Figure 2: 80 pin BGA Package(Top view)5
 Figure 3: 64 pin LQFP Package.....6
 Figure 4: SDR and DDR Input Data Formats11
 Figure 5: Horizontal Input Timing11
 Figure 6: Vertical Input Timing.....12
 Figure 7: CPU/MEMERY Interface Timing.....12
 Figure 8: 80 Pin BGA Package.....19
 Figure 9: 64 Pin LQFP Package20

LIST OF TABLES

Table 1: Pin Name Description (BGA Package)7
 Table 2: Pin Name Descriptions (LQFP64 Package).....9
 Table 3: Input Data Format.....13
 Table 4: Supported SDTV Standards.....14
 Table 5: Video DAC Configurations for CH7028B14
 Table 6: Test Pattern Selection.....15

1.0 Pin-out

1.1 Package Diagram

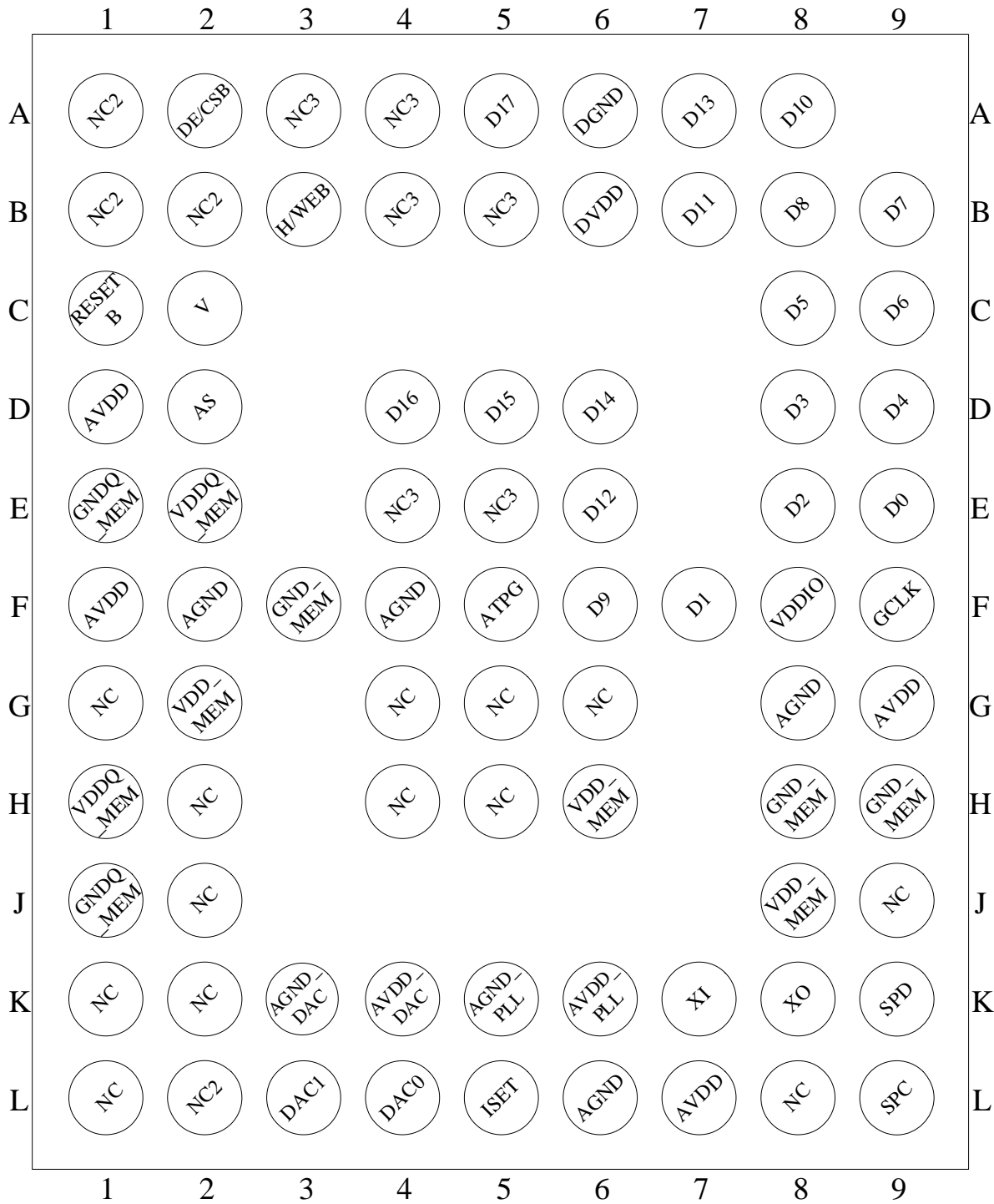


Figure 2: 80 pin BGA Package(Top view)

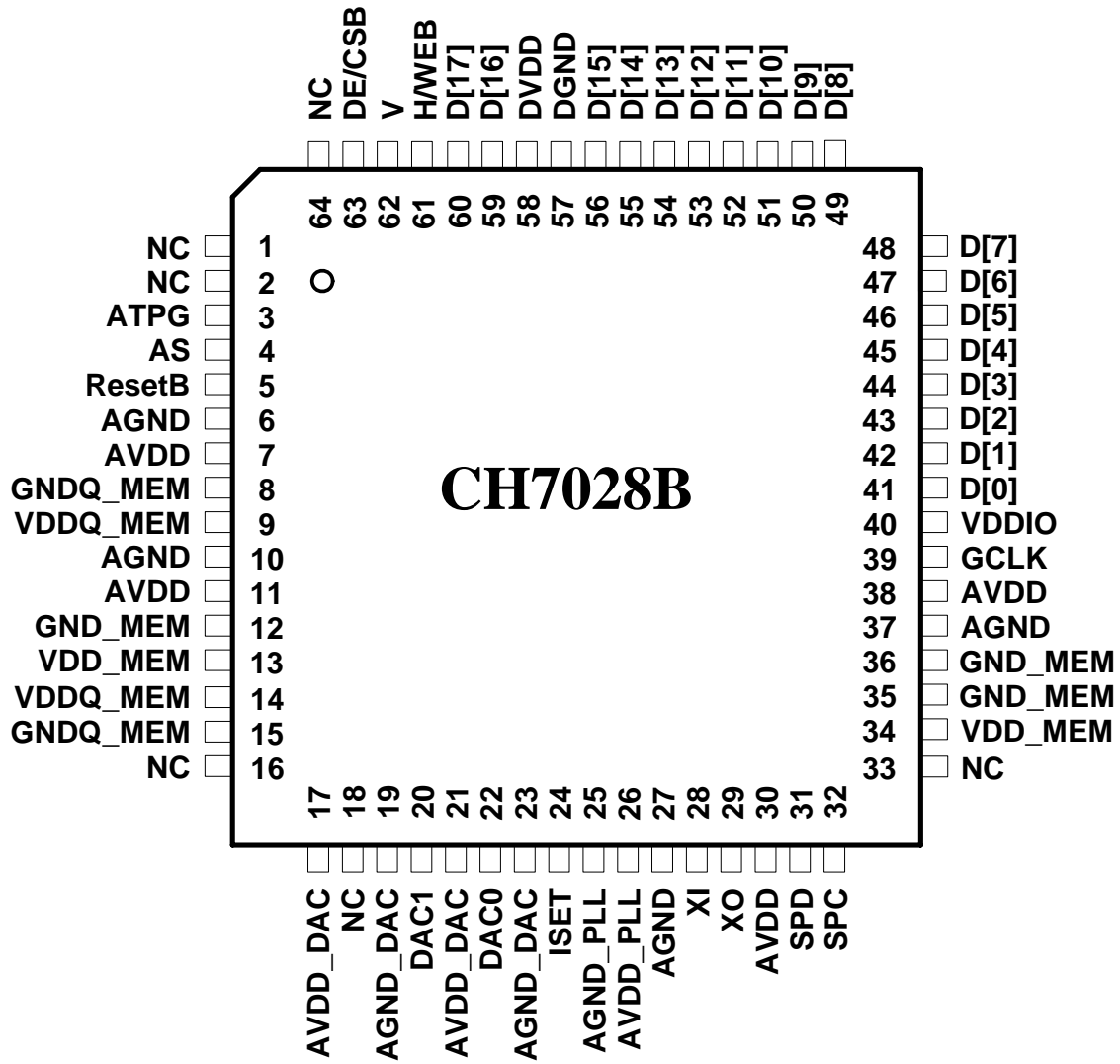


Figure 3: 64 pin LQFP Package

1.2 Pin Description

Table 1: Pin Name Description (BGA Package)

Pin #	Type	Symbol	Description
A5, D4, F7, E9, D5, D6, A7, E6, B7, A8, F6, B8, B9, C9, C8, D9, D8, E8	In	D[17:0] ^[1]	Data[0] through Data[17] Inputs These pins accept the 18 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
C2	In/Out	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
B3	In/Out	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU/MEMORY interface.
A2	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also the CSB signal of CPU/MEMORY interface.
D2	In	AS	Serial Port Device Address Select 0: 76h 1: 75h
F5	In	ATPG	ATPG Enable (Internally pull-low) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be pulled low. Voltage level is 0 to 3.3V.
C1	In	RESETB	Active low reset. When RESETB is low, the device is held in the hardware reset condition. When RESETB is high, reset is controlled through the serial port.
K9	In/Out	SPD	Serial Port Data Input / Output (open drain) This pin functions as the bi-directional data pin of the serial port. External pull-up resistor is required.
L9	In	SPC	Serial Port Clock Input (open drain) This pin functions as the clock pin of the serial port. External pull-up resistor is required.
L4	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3 V.
L3	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3 V.
L5	In	ISET	Current Set This pin sets the DAC current. A 1.2k Ω , 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide trace.

Pin #	Type	Symbol	Description
K7	In	XI	Crystal Input / External Input For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI input.
K8	Out	XO	Crystal Output For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI. However, if an external CMOS clock is attached to XI, XO should be left open.
F9	In	GCLK	Graphics Controller Clock Input
F8	Power	VDDIO	IO supply voltage (1.2-3.3V)
B6	Power	DVDD	Digital supply voltage (1.8V)
D1, F1, L7, G9	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
K6	Power	AVDD_PLL	PLL supply voltage (1.8V)
K4	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
E2, H1	Power	VDDQ_MEM	SDRAM output buffer supply voltage (2.5V)
G2, J8, H6	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
A6	Power	DGND	Digital supply ground
F4, F2, L6, G8	Power	AGND	Analog supply ground
K5	Power	AGND_PLL	PLL supply ground
K3	Power	AGND_DAC	DAC supply ground
E1, J1	Power	GNDQ_MEM	SDRAM output buffer supply ground
F3, H9, H8	Power	GND_MEM	SDRAM device supply ground
		NC	All the NC pins should be left open.

Notes:

1. All the unused Data input pins should be pulled low with 10k Ω resistors or shorted to Ground directly.
2. All the NC pins should be left open.

Table 2: Pin Name Descriptions (LQFP64 Package)

Pin #	Type	Symbol	Description
41 - 56 59 - 60	In	D[17:0] ^[1]	Data[0] through Data[17] Inputs These pins accept the 18 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
62	I/O	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
61	I/O	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU/MEMERY interface.
63	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. CSB signal input of CPU/MEMERY interface.
4	In	AS	Serial Port Device Address Select 0: 76h 1: 75h
3	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be pulled low. Voltage level is 0 to 3.3V.
5	In	ResetB	Reset * Input When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
31	I/O	SPD	Serial Port Data Input / Output (open drain) This pin functions as the bi-directional data pin of the serial port. External pull-up resistor is required.
32	In	SPC	Serial Port Clock Input (open drain) This pin functions as the clock pin of the serial port. External pull-up resistor is required.
22	Out	DAC0	CVBS or S-video output Full swing is up to 1.3v.
20	Out	DAC1	CVBS or S-video output Full swing is up to 1.3v.
24	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k Ω , 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
28	In	XI	Crystal Input / External Input For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
29	Out	XO	Crystal Output For some situation of the slave mode, a parallel resonance crystal (± 20

Pin #	Type	Symbol	Description
			ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
39	In	GCLK	Graphics Controller Clock Input
40	Power	VDDIO	IO supply voltage (1.2-3.3V).
58	Power	DVDD	Digital supply voltage (1.8V).
7,11,30,38	Power	AVDD	Analog supply voltage (2.5-3.3V).
26	Power	AVDD_PLL	PLL supply voltage (1.8V).
17,21	Power	AVDD_DAC	DAC power supply (2.5-3.3V).
9,14	Power	VDDQ_MEM	SDRAM output buffer supply voltage (2.5V).
13,34	Power	VDD_MEM	SDRAM device supply voltage (2.5V).
57	Power	DGND	Digital supply ground.
6,10,27,37	Power	AGND	Analog supply ground.
25	Power	AGND_PLL	PLL supply ground.
19,23	Power	AGND_DAC	DAC supply ground.
8,15	Power	GNDQ_MEM	SDRAM output buffer supply ground.
12,35,36	Power	GND_MEM	SDRAM device supply ground.

Notes:

1. All the unused Data input pins should be pulled low with 10kΩ resistors or shorted to Ground directly.

2.0 Functional Description

2.1 Input Interface

2.1.1 Overview

Five distinct methods of transferring data to the CH7028B are described below.

1. Unitary data, clock input at 1X the pixel rate (SDR mode)
2. Multiplexed data, clock input at 1X of pixel rate (DDR mode)
3. Multiplexed data, clock input at 2X of pixel rate
4. Multiplexed data, clock input at 3X of pixel rate
5. 16 bit CPU/MEMERY interface

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7028B is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X or 3X pixel rate the data applied to the CH7028B is latched with one edge of the clock (also known as single edge transfer mode or SDR). For the unitary data, clock at 1X pixel rate, the data applied to the CH7028B is latched with one edge of the clock. The polarity of the pixel clock can be reversed under serial port control. Hsync and Vsync can be input individually or embedded into data signal such as BT656 input format.

2.1.2 Input Clock and Data Timing Diagram

Figure 3 to Figure 6 below shows the timing diagram for input data and clocks. The timing requirements are given in later section.

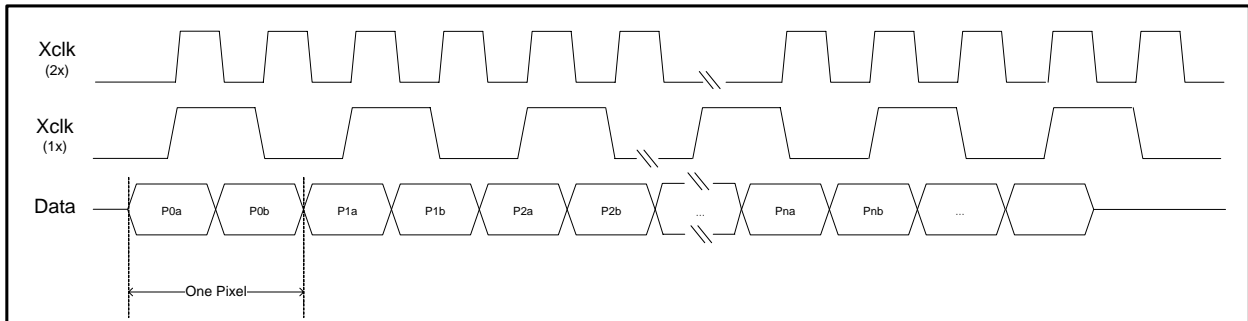


Figure 4: SDR and DDR Input Data Formats

(Note: In Figure 3, the first XCLK waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK waveform represents the input clock for the dual edge transfer (DDR) method.)

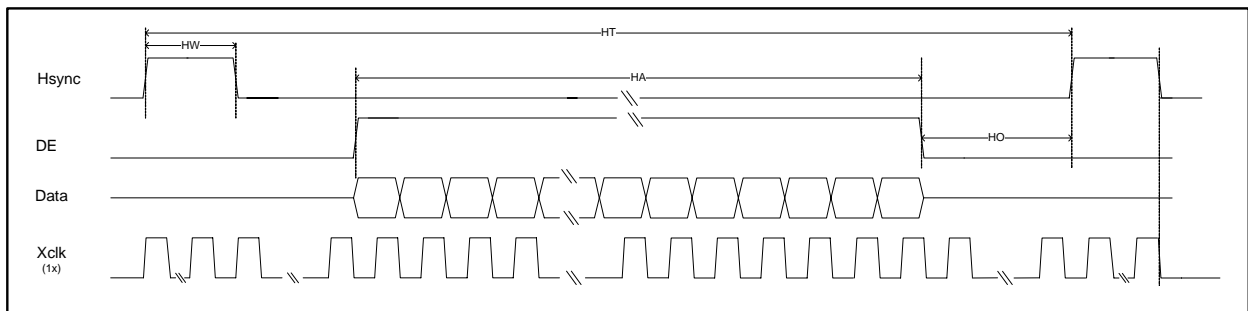


Figure 5: Horizontal Input Timing

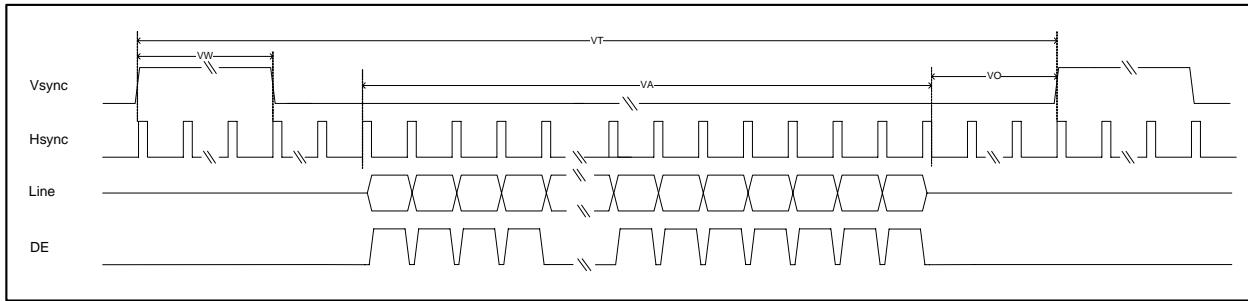


Figure 6: Vertical Input Timing

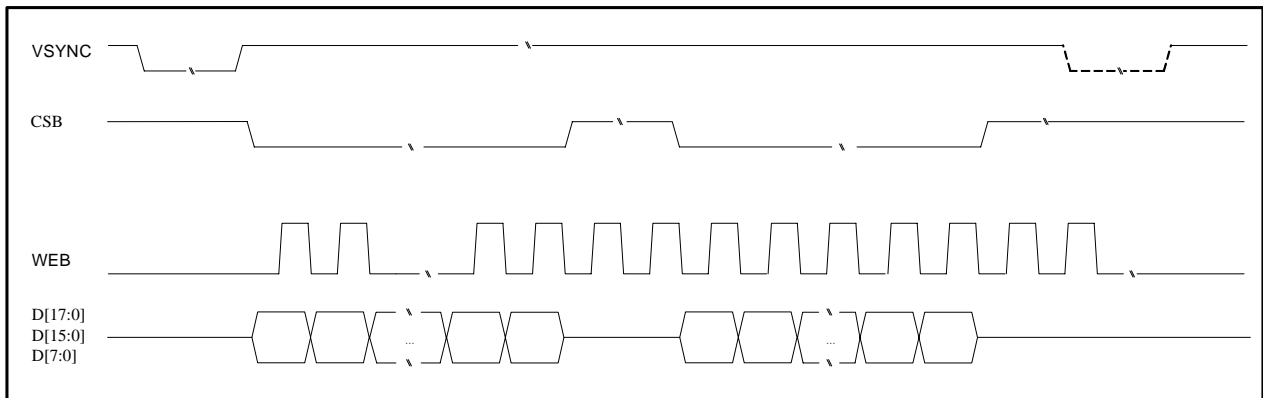


Figure 7: CPU/MEMERY Interface Timing

(Note: VSYNC pulse of CPU/MEMERY interface is not necessary for each input frame, it is required to appear at least one time at any input frame blank period.)

2.1.3 Input Data Voltage

The voltage level of input pins D[17:0], H, V, DE, are from 0 to VDDIO. These pins support two input mode, one is CMOS mode, and the other is pseudo differential mode. The default is CMOS mode with CMOS level on these pins. When control bit **DIFFEN** is high, the input is pseudo differential mode that uses a reference voltage (VREF) to compare with input voltage and decide input logic value. The VREF value can be 80%, 70%, 60% and 50% of VDDIO value, referring to **VRTM[1:0]**. The pseudo differential mode can accept the wide range of the input voltage level from 1.2v to 3.3v, while the CMOS mode can accept 1.8v to 3.3v input voltage.

2.1.4 Input Data Format

The following table indicates the supported input data format by CH7028B.

Table 3: Input Data Format

MULTI	IDF	D[17:16]	D[15:8]	D[7:0]	
0	5	8'h00	Y[7:0]	C[7:0]	
	9	6'h00, R[5:4]	R[3:0],G[5:2]	G[1:0],B[5:0]	
	10	8'h00	R[4:0],G[5:3]	G[2:0],B[4:0]	
	11	8'h00	1'b0, R[4:0],G[4:3]	G[2:0],B[4:0]	
1	PA	0		4'h0, R[7:4]	R[3:0],G[7:4]
			PB		4'h0, G[3:0]
	PA	1			7'h00, R[5]
			PB		7'h00, G[2]
	PA	2			
			PB		
	PA	3			
			PB		
	PA	4			4'h0, R[7:4]
			PB		4'h0, G[4:2], [7]
	PA	5			
			PB		
	PA	6			6'h00, Y[9:8]
			PB		6'h00, C[9:8]
	PA	7			4'h0, Y[7:4]
			PB		4'h0, Cb[3:0]
2	PA	0			R[7:0]
			PB		G[7:0]
				PC	
	PA	7			Y[7:0]
			PB		Cb[7:0]
				PC	

(PA,PB,PC represent the parts of one pixel data)

IDF[3:0] describes the major input data format that CH7028B accepts. They are: (Table 10)

- IDF = 0: Multiplexed 888 RGB input
- IDF = 1: Multiplexed 666 RGB input
- IDF = 2: Multiplexed 565 RGB input
- IDF = 3: Multiplexed 555 RGB input
- IDF = 4: DVO input
- IDF = 5: 8-bit YCbCr4:2:2 input
- IDF = 6: 10-bit YCbCr4:2:2 input
- IDF = 7: 8-bit YCbCr4:4:4 input
- IDF = 8: Reserved
- IDF = 9: 666 RGB input
- IDF = 10: 565 RGB input
- IDF = 11: 555 RGB input

Table 2 above describes the 18-bit input data format under unitary mode. For multiplexed input, input data need to be de-multiplexed to unitary input first then this table can be applied. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g. PA and PB) will contain a complete pixel. (3X input has the similar feature)

When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). In YCbCr 4:2:2 with embedded sync mode, the hardware can detect the connection error and correct it automatically. All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

2.2 Chip Output

2.2.1 TV Output

The CH7028B support the following output formats:

Table 4: Supported SDTV Standards

No.	Standards	Field Rate (Hz)	Total	Scan Type
0	NTSC-M	60/1.001	858x525	Interlaced
1	NTSC-J	60/1.001	858x525	Interlaced
2	NTSC-443	60/1.001	858x525	Interlaced
3	PAL-B/D/G/H/I	50	864x625	Interlaced
4	PAL-M	60/1.001	858x525	Interlaced
5	PAL_N	50	864x625	Interlaced
6	PAL-Nc	50	864x625	Interlaced
7	PAL_60	60/1.001	858x525	Interlaced

CVBS, S-video output are supported.

2.2.2 Video DAC Output

The DAC output is configured by the register bits **VFMT[2:0]**. **DACS[1:0]** bits are used to control the multiple output format i.e. dual CVBS or S-Video output. **DACSP[2:0]** bits are to swap the DAC output sequence such as CVBS, S-Video or S-Video, CVBS. Detailed information of these bits are described in register bits description section of this document. **Table 4** below lists the DAC output configurations of the CH7028B:

Table 5: Video DAC Configurations for CH7028B

DAC0	DAC1
CVBS	
CVBS	CVBS
C	Y

2.2.3 DAC Single/Double Termination

The DAC output of CH7028B can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the reflection from the cable. Refer to the description of register bit **SEL_R**.

2.2.4 TV Connection Detect

CH7028B can detect the TV connection by setting register **SPPSNS**. It can detect which DAC is connected, short to ground or not connected.

2.2.5 Picture Enhancement

The CH7028B has the capability of vertical and horizontal output picture position adjustment. It can automatically put the picture in the display center, and the vertical or horizontal position is also programmable through user input. And also it can provide brightness, contrast, hue, saturation adjustment and text enhancement functions.

CH7028B also supports vertical or horizontal flip and rotation (0, 90, 180 and 270 degree) functions.

2.2.6 Color Sub-Carrier Generation

CH7028B has two ways to generate the color sub-carrier frequency. If the **GCLK** from the graphics controller has a steady center frequency and very small jitters, the sub-carrier can be derived from the **GCLK**. However, since even a $\pm 0.01\%$ sub-carrier frequency variation is enough to cause some TV to lose color lock, CH7028B has the ability to generate the sub-carrier frequency from the crystal when the **GCLK** from the graphics device cannot meet the requirement. In this case, the crystal has to be present.

In addition, CH7028B has the capability to gen-lock the color sub-carrier with Vsync. Also, it has the ability to operate in a “stop dot crawl” mode for NTSC CVBS output when the first sub-carrier generation method is used.

2.2.7 ITU-R BT.470 Compliance

The CH7028B is mostly compliant with ITU-R BT.470 standard except for the items below.

- The frequencies of horizontal sync, vertical sync, and color sub-carrier depend on the quality of **GCLK** from graphics controller and/or the off-chip crystal.
- It is assumed that gamma correction, if required, is performed in the graphics device.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements. However, they may have a small variation depending on the actual input and output format.
- The actual bandwidths of the luminance and chrominance signals depend on the input resolution and the filter selection.

2.2.8 SDRAM Power Down

SDRAM have two kinds of power down modes. One is power down mode, the other is deep power down mode. For power down mode, all data contents will be held in the bank. For deep power down mode, a command is required to issued. There is a bit called MEMPD in register map. It can be used to enable the deep power mode. During deep power mode, all the data in memory banks will be lost, and the SDRAM leakage current is less than $1\mu A$. **A very important thing required to be noted here is that not all the SDRAM parts support either power down or deep power down mode.** In these cases, even CH7028B enters into power down, the current consumption is still large ($> 100\mu A$). This current is primarily derived from the SDRAM die.

2.2.9 Test Pattern Select

Setting TSTP[3:0] bit[3:0] of 04h on the second page of register map(refer to PG register bit0 of 03h on the first page) can select different video patterns that go through datapath, according to the following table. TEST(bit5 of 04h on the second page) is the test pattern selection enable. It has to be 1 to enable test mode. TSYNC(bit4 of 04h on the second page) is to select which sync will be used internally generated sync or external input sync.

Table 6: Test Pattern Selection

TSTP[3:0]	Test pattern
0	Black
1	White
2	Vertical ramp
3	Horizontal ramp
4	Color bar
5	One pixel wide color bar
6	Zigzag

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All 1.8V power supplies relative to GND ^[1] All 3.3V power supplies relative to GND ^[2]	-0.5 -0.5		2.5 5.0	V
	Input voltage of all digital pins ^[3]	GND – 0.5		VDDIO+0.5	V
T _{AMB}	Ambient operating temperature	-40		85	°C
T _{STOR}	Storage temperature	-40		150	°C
T _J	Junction temperature			150	°C
TVPS	Vapor phase soldering (5 second) Vapor phase soldering (11 second) Vapor phase soldering (1 minute)			260 245 225	°C

Note:

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce permanent damage.
- The digital input voltage will follow the I/O supply voltage (VDDIO), the I/O supply voltage range is from 1.2V to 3.3V.

3.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Crystal and I/O Power Supply Voltage	2.5	3.3	3.5	V
AVDD_DAC	DAC Power Supply Voltage	2.5	3.3	3.5	V
AVDD_PLL	PLL Power Supply Voltage	1.71	1.8	1.89	V
DVDD	Digital Power Supply Voltage	1.71	1.8	1.89	V
VDDIO	Data I/O supply voltage	1.14		3.5	V
R _{L1}	Output load to DAC Current Reference		1.2k		Ω
R _{L2}	Output load to DAC Outputs		37.5		Ω
VDDQ_MEM	Memory data interface supply	2.375	2.5	2.625	V
VDD_MEM	Memory core supply	2.375	2.5	2.625	V
VDD18	Generic for all 1.8V supplies	1.71	1.8	1.89	V
VDD33	Generic for all 3.3V supplies	2.5	3.3	3.5	V
	Ambient operating temperature	-20		70	°C

3.3 Electrical Characteristics

(Operating Conditions: $T_A = -20^{\circ}\text{C} - 70^{\circ}\text{C}$, $V_{DD18}=1.8\text{V} \pm 5\%$, $V_{DD33}=2.5\text{V} - 3.5\text{V}$)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		38		mA
	Video level error			10	%
I_{VDD18}	Total VDD18 supply current (1.8V supplies)		30		mA
$I_{VDD33}^{(1)}$	Total VDD33 supply current (3.3V supplies) ^[1]		30		mA
I_{VDDQ}	Memory data interface supply current		0.1		mA
I_{VDD_MEM}	Memory core supply current		20		mA
I_{PD}	Total Power Down Current ^[2]		<20		μA

Notes:

1. Applies for one DAC and single 75 Ω termination. The current of every DAC is less than 25mA for single termination and less than 50mA for double termination.
2. If the chip is not in deep power down mode, the total power down current will be about 6mA. Most of the leakage current is come from the SDRAM.

3.4 Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	$I_{OL} = 3.0 \text{ mA}$	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		$V_{DD33} + 0.5$	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{DATAIH}	Data I/O ^[1] High Voltage		$V_{DDIO}/2 + 0.25$		$V_{DDIO} + 0.5$	V
V_{DATAIL}	Data I/O Low Voltage		GND-0.5		$V_{DDIO}/2 - 0.25$	V
V_{MISCIH}	Miscellaneous Input High Voltage ^[2]		$V_{DD33} - 0.5$		$V_{DD33} + 0.5$	V
V_{MISCIL}	Miscellaneous Input Low Voltage ^[2]		GND-0.5		0.6	V
V_{SYNCOH}	Miscellaneous Output High Voltage ^[3]		$V_{DD33} \times 0.8$			V
V_{SYNCOL}	Miscellaneous Output Low Voltage ^[3]				0.3	V
I_{MISCPU}	Miscellaneous Input Pull Up Current ^[2]	$V_{IN} = 0$	0.5		5.0	μA
I_{MISCPD}	Miscellaneous Input Pull Down Current ^[2]	$V_{IN} = V_{DD33}$	0.1		1.1	μA

Notes:

1. Applies to D[17:0], GCLK, H, V and DE. VDDIO is the I/O supply, ranging from 1.2V to 3.3V.
2. Applies to AS, RESETB and ATPG.
3. Applies to HSO, VSO, CSYNC.

3.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{CRYSTAL}	Input (CRYSTAL) frequency		2.3		64	MHz
f_{GCLK}	Input (GCLK) frequency		1.5		120	MHz
DC_{GCLK}	Input (GCLK) Duty Cycle	$T_S + T_H < 1.2\text{ns}$	30		70	%
t_{GJT}	GCLK clock jitter tolerance			10		ns
t_S	Setup Time: D[17:0], H, V and DE to GCLK	GCLK to D[17:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[17:0], H, V and DE to GCLK	D[17:0], H, V, DE = Vref to GCLK	0.5			ns
t_{STEP}	De-skew time increment		50		80	ps

4.0 Package Dimensions

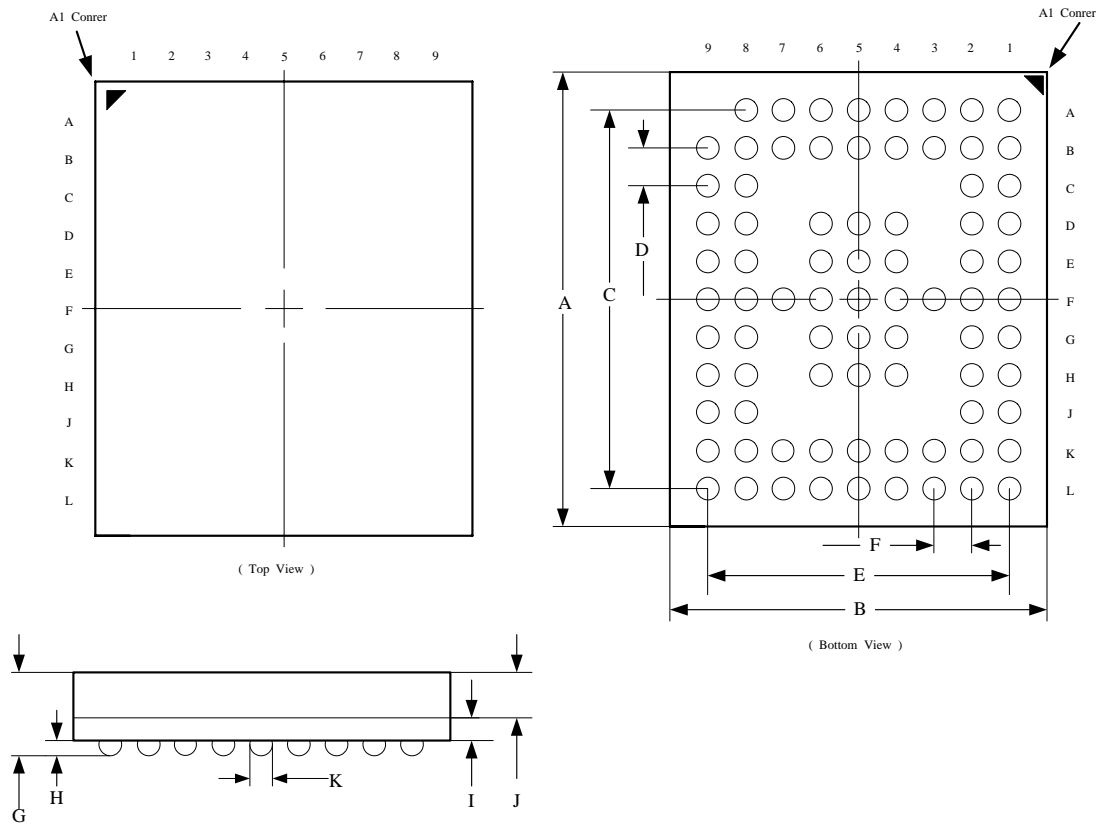


Figure 8: 80 Pin BGA Package

Table of Dimensions

No. of Leads		SYMBOL										
80 (5 X 6 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	Min	6.00	5.00	5.00	0.50	4.00	0.50		0.22	0.30	0.60	0.30
	Max							1.20	0.30			

Notes:

All dimensions conform to JEDEC standard MO-216.

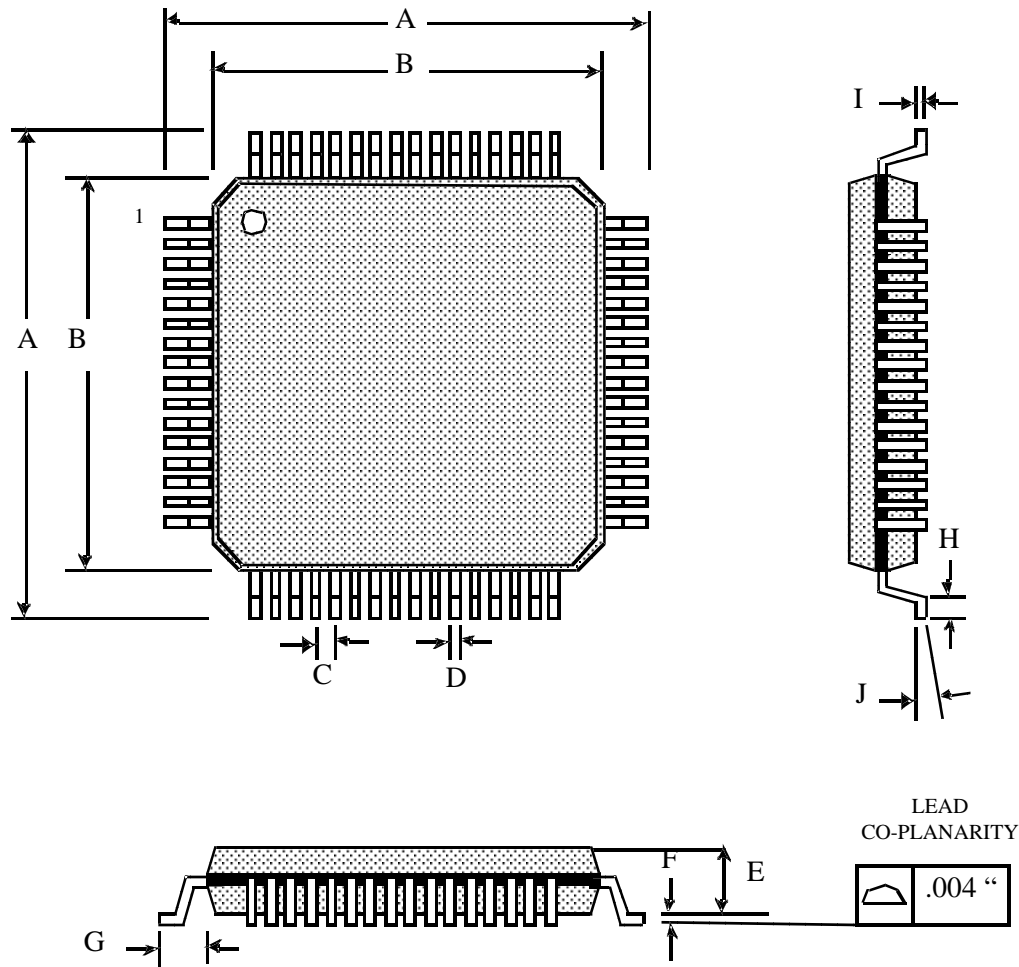


Figure 9: 64 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	K
Milli-meters	Min	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	Max				0.27	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

5.0 Revision History

Rev. #	Date	Section	Description
1.0	11/04/2007	All	Initial preliminary release.
1.1	08/21/2008	2.1	Add input timing figure. Add BGA package.

Disclaimer

This document provides technical information for the user. Chrontel reserves the right to make changes at any time without notice to improve and supply the best possible product and is not responsible and does not assume any liability for misapplication or use outside the limits specified in this document. We provide no warranty for the use of our products and assume no liability for errors contained in this document. The customer should make sure that they have the most recent data sheet version. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Chrontel, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Chrontel PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF Chrontel. Life support systems are those intended to support or sustain life and whose failure to perform when used as directed can reasonably expect to result in personal injury or death.

ORDERING INFORMATION			
Part Number	Package Type	Copy Protection	Operating Temperature Range
CH7028B-TF	64 LQFP, Lead-free	None	Commercial : -20 to 70°C
CH7028B-TF-TR	64 LQFP, Lead-free, Tape & reel	None	Commercial : -20 to 70°C
CH7028B-TFI	64 LQFP, Lead-free	None	Industrial : -40 to 85°C
CH7028B-TFI-TR	64 LQFP, Lead-free, Tape & reel	None	Industrial : -40 to 85°C
CH7028B-GF	80BGA, Lead-free	None	Commercial : -20 to 70°C
CH7028B-GF-TR	80BGA, Lead-free, Tape & reel	None	Commercial : -20 to 70°C

Chrontel

Chrontel International Limited

129 Front Street, 5th floor,

Hamilton, Bermuda HM12

www.chrontel.com

E-mail: sales@chrontel.com