Document No: AX88782_783/V1.00/04/30/09

Features

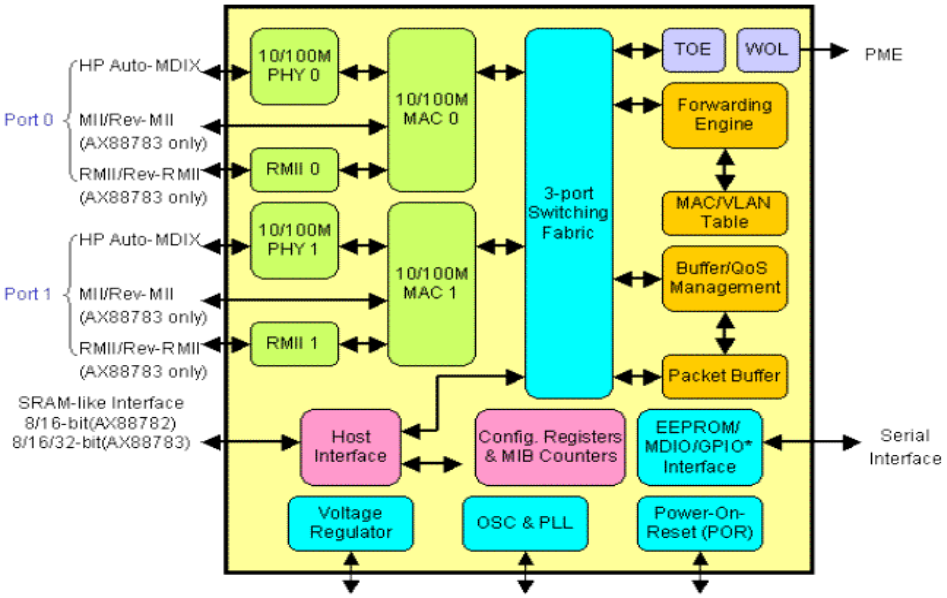
- **High Performance Non-PCI Interface**
  - Configurable 8/16/32-bit SRAM-like host interface, easily interfaces with most common embedded MCUs (AX88782: 8/16-bit, AX88783: 8/16/32-bit)
  - Supports PPPoE/IPv4 IP/TCP/UDP/ICMP/ IGMP checksum offload to relieve CPU loading
  - Supports burst-mode access, minimizing CPU overhead
- **Fast Ethernet MAC + PHY**
  - IEEE 802.3 10Base-T/100Base-TX compatible
  - Supports Full Duplex operation with IEEE 802.3x flow control and Half Duplex with backpressure
  - 10/100M PHY supports twisted pair crossover detection and auto-correction (HP Auto-MDIX)
  - Supports Wake-on-LAN by Microsoft Wakeup Frame, Magic Packet and link status change detection
- **Switching Fabric**
  - Performs non-blocking wire-speed forwarding and filtering
  - Embeds 32KB SRAM for packet buffering
  - Supports broadcast storm filtering
  - Supports per queue and per port ingress and egress programmable rate limit control
  - Integrates two-way Address-Lookup engine and table for 1K MAC addresses
  - Supports Routing Table/IGMP/VLAN Table access through CPU read/write operation
  - Supports 802.1D Spanning Tree Protocol and 802.1w Rapid Spanning Tree Protocol
- **QoS**
  - Supports Quality-of-Service for Port-Based, 802.1p VLAN and IPv4 TOS/IPv6 COS packets with four priority queues
  - Supports RFC2475 DiffServ-based
- **VLAN**
  - Supports up to 3 VLAN groups for port-based VLAN and 16 VLAN entries for 802.1Q tag-based VLAN functions
  - Supports the Double tagging 802.1Q-in-802.1Q Function for WAN access
- **Security**
  - Supports ingress port security mode, incoming packets with unknown source MAC address could be dropped
  - Supports eight Security MAC Registrations
  - Supports 802.1X port-based Authorization
- **Multicast**
  - Supports GMRP/GVRP/GARP packet snooping
  - Support IPv4 IGMP and IPv6 ICMP/MLD (Multicast Listener Discovery) Snooping
  - Supports up to 1K Multicast Group (shared with L2 MAC table)
  - Supports eight IGMP Multicast IP address snooping
- **Monitoring**
  - Supports RMON group 1, 2, 3 and 9 counter (RFC1213)
  - Supports Ethernet-like MIB counter (RFC 1643)
  - Supports Bridge MIB counter (RFC 1493)
  - Egress/Ingress Port Mirroring
  - Sniffer functions:
    - Source/Destination Port
    - DA/SA
    - VLAN ID
    - Ethernet Packet Type
    - IPv4/IPv6 Protocol
    - IPv4/IPv6 TCP/UDP Port Number
- **Optional Interfaces Supported:**
  - MII or Reverse-MII
  - RMII or Reverse-RMII
  - Optional serial EEPROM
  - Optional GPIO/GPI/GPO (AX88783)
- Single 3.3V power supply with options for 1.8V, 2.5V and 3.3V I/O voltage support
- Integrated an on-chip voltage regulator requiring only a single power supply of 3.3V
- Integrates an on-chip oscillator and PLL requiring only a 25MHz crystal to operate
- Integrates on-chip power-on reset circuit
- Small form factor: 80-pin E-PAD LQFP (AX88782) or 128-pin E-PAD LQFP (AX88783) RoHS compliant package
- Operating temperature range: 0˚C to 70˚C

Product Description

The AX88782/AX88783 is a non-PCI 2-port 10/100M Ethernet controller with an integrated 3-port switching fabric, three 10/100M MACs, two 10/100M PHYs, and an 8/16/32-bit SRAM-like host interface. This controller is targeted at embedded system applications that need to support two Ethernet ports, typically one for a LAN port and one for a WAN port. The AX88782/AX88783 supports simple a SRAM-like host interface, routine packet checksum calculation, and burst-mode access which make it easy to provide high performance 2-port Ethernet connectivity solutions for any

embedded MCU. The built-in switching fabric supports non-blocking wire-speed forwarding and provides four priority queues for advanced QoS functions including Port-Based, 802.1p VLAN, IPv4 TOS/IPv6 COS for voice, video, audio and data traffic classification. The AX88782/AX88783 combines the benefits of high integration and flexibility which makes it an ideal single-chip solution for designing high performance, QoS-aware, cost effective and small form factor 2-port Ethernet function for any embedded system application.

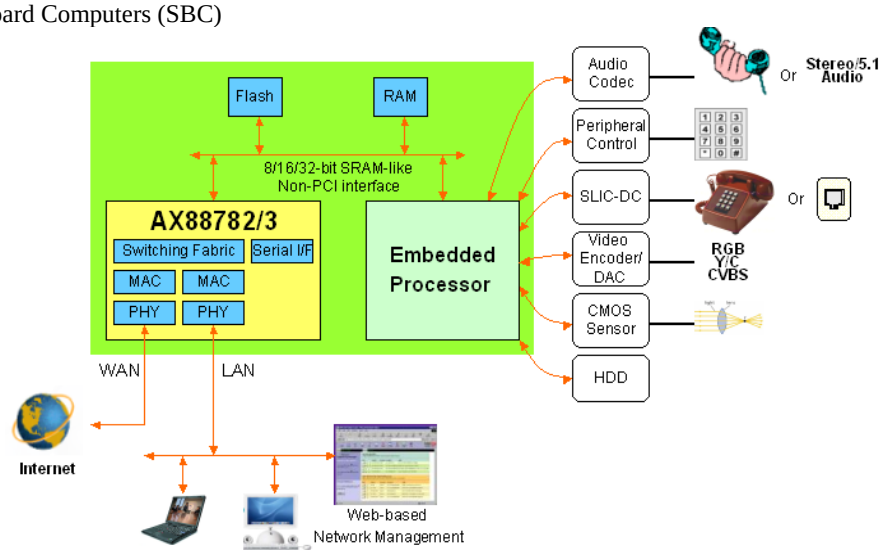
Block Diagram



*Optional GPIO Interface only for AX88783

Target Applications

- VoIP Phone, VoIP ATA Adapter
- IP Camera for Remote Surveillance
- Next Generation IP-STB and IPTV
- Industrial Controller and Networked Sensor
- Port Redundancy and Port Monitoring
- Single Board Computers (SBC)



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1.0 Overview

1.1 General Description

The AX88782/AX88783 is a non-PCI 2-port 10/100M Ethernet controller with an integrated 3-port switching fabric, three 10/100M MACs, two 10/100M PHYs, and the 8/16/32-bit SRAM-like host interface targeted for embedded system applications that need support of two Ethernet ports, typically one for LAN port and one for WAN port.

The AX88782/AX887833 supports the simple SRAM-like host interface, the routine packet checksum calculation, and the burst read and write access through host port which make it easy to provide 2-port Ethernet connectivity solutions for any embedded MCU with reasonable performance. The built-in switching fabric supports non-blocking wire-speed forwarding and provides four priority queues for advanced QoS functions including Port-Based, 802.1P VLAN, IPv4 TOS/IPv6 COS for voice, video, audio and data traffic classification. The AX88782/AX88783 combines the benefits of high integration and flexibility which makes it a ideal single-chip solution for designing high performance, QoS-aware, cost effective and small form factor 2-port Ethernet function for any embedded system applications.

The AX88782/AX88783 supports non-blocking wire speed forwarding rate and no Head-of-Line (HOL) blocking issue. The AX88782/AX88783 provides two flow-control mechanisms to avoid loss of data: an optional jamming-based backpressure flow control in the half-duplex operation and IEEE 802.3x in the full-duplex mode.

To support Quality of Service (QoS), each output port has four priority queues and their assignment can be based on the 802.1P priority field, TOS/COS/DiffServ field or Port-Pair setting. Each output port retrieves the Ethernet frames from the shared buffer based on queuing and sends them to the transmitting (Tx) FIFO.

1.2 Block Diagram

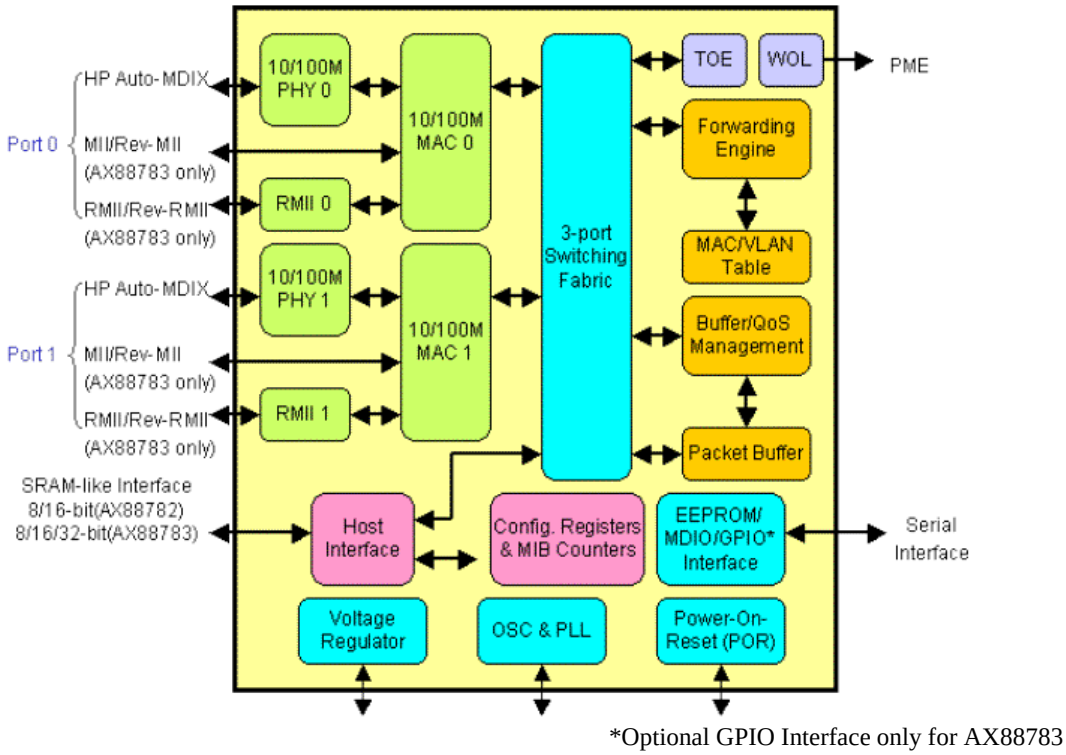


Fig 1 The AX88782/AX88783 Block Diagram

1.3 Pinout Diagram

1.3.1 AX88782: Port 0/Port 1 PHY Mode

Port 0: Built-in PHY
Port 1: Built-in PHY
Port 2: 8 / 16 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode

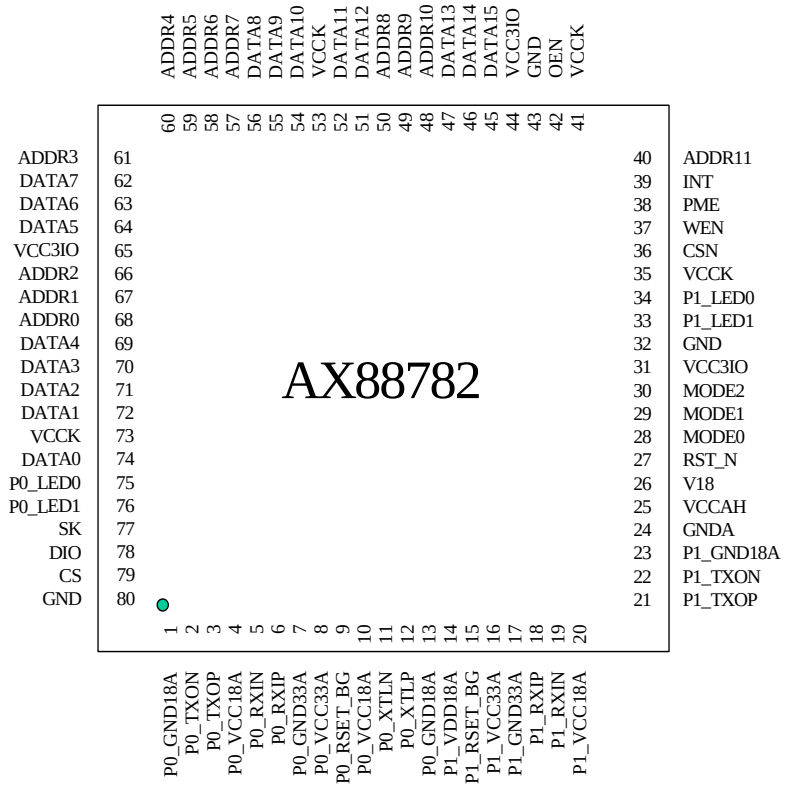


Fig 2 The AX88782 Default Pinout Diagram

1.3.2 AX88783 : Port 0/Port 1 PHY Mode (Default)

Port 0: Built-in PHY
Port 1: Built-in PHY
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

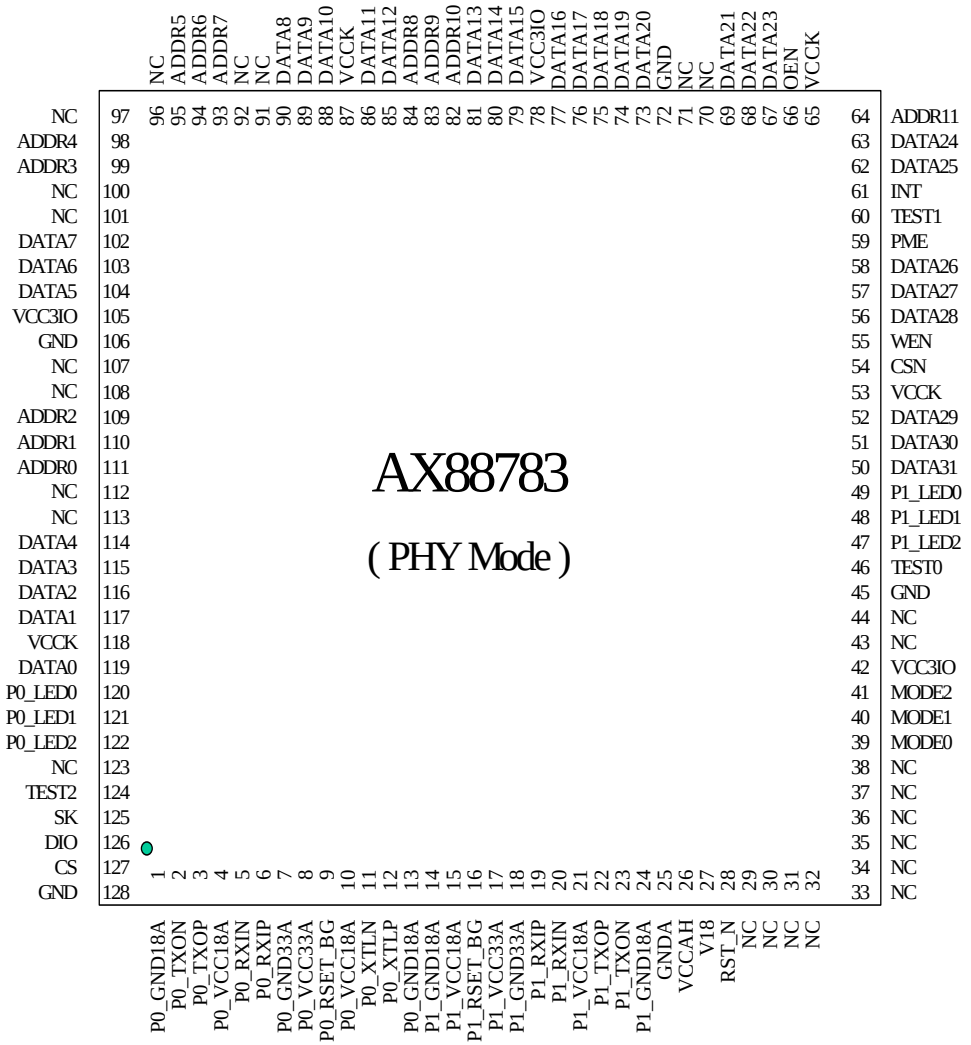


Fig 3 The AX88783 PHY Mode Pinout Diagram

1.3.3 AX88783 : Port 0/Port 1 MII Mode

Port 0 : MII Interface
Port 1 : MII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

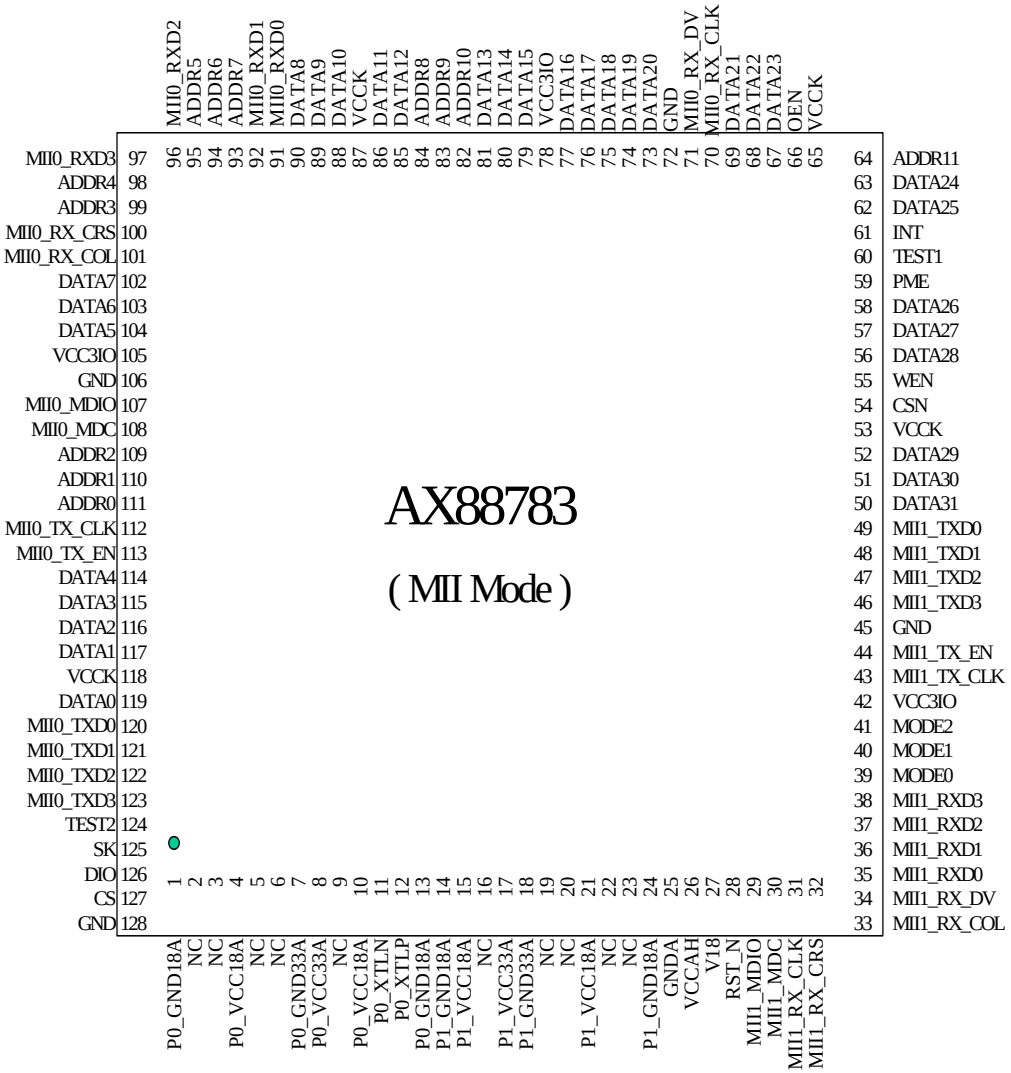


Fig 4 The AX88783 Port0/Port1 in MII Mode

1.3.4 AX88783: Port 0/Port 1 Reverse MII Mode

Port 0 : Reverse MII Interface
Port 1 : Reverse MII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

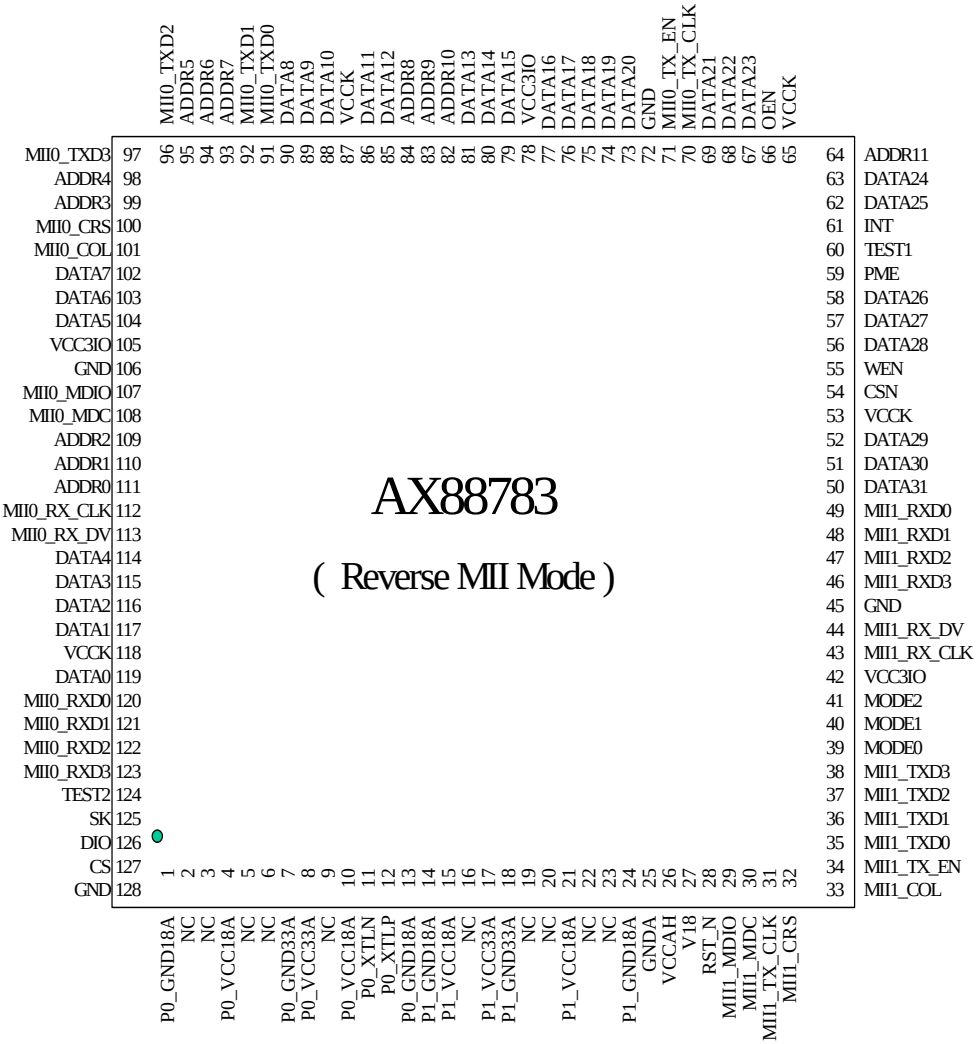


Fig 5 The AX88783 Port0/Port1 in Reverse MII Mode

1.3.5 AX88783: Port 0/Port 1 RMII Mode

Port 0 : RMII Interface
Port 1 : RMII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

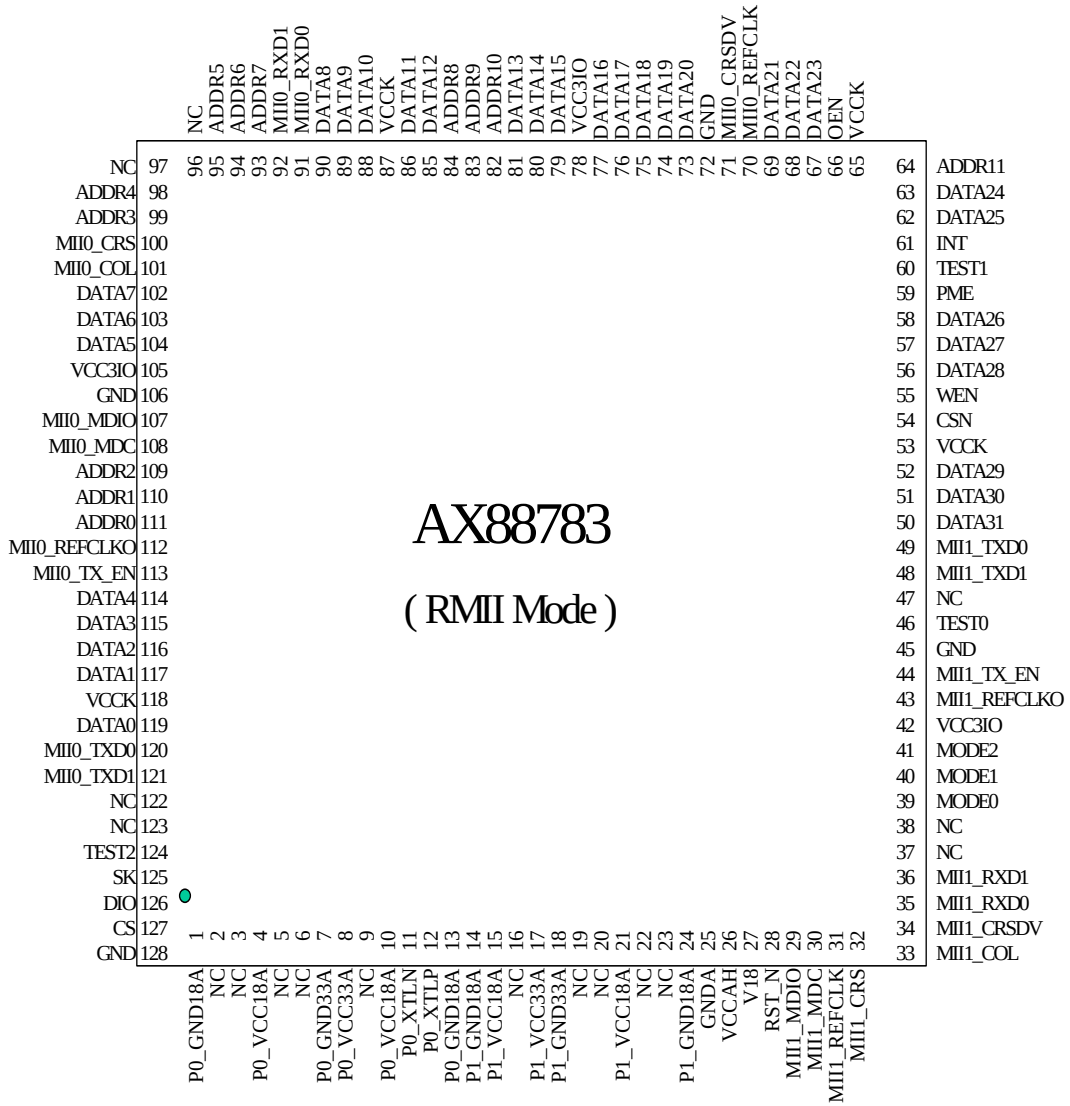


Fig 6 The AX88783 Port0/Port1 in RMII Mode

1.3.6 AX88783: Port 0/Port 1 Reverse RMII Mode

Port 0 : Reverse RMII Interface
Port 1 : Reverse RMII Interface
Port 2: 8/16/32 Bit SRAM-like Host Interface
{Mode2, Mode1, Mode0} = 000: 8 Bit Interface Mode
{Mode2, Mode1, Mode0} = 001: 16 Bit Interface Mode
{Mode2, Mode1, Mode0} = 010: 32 Bit Interface Mode

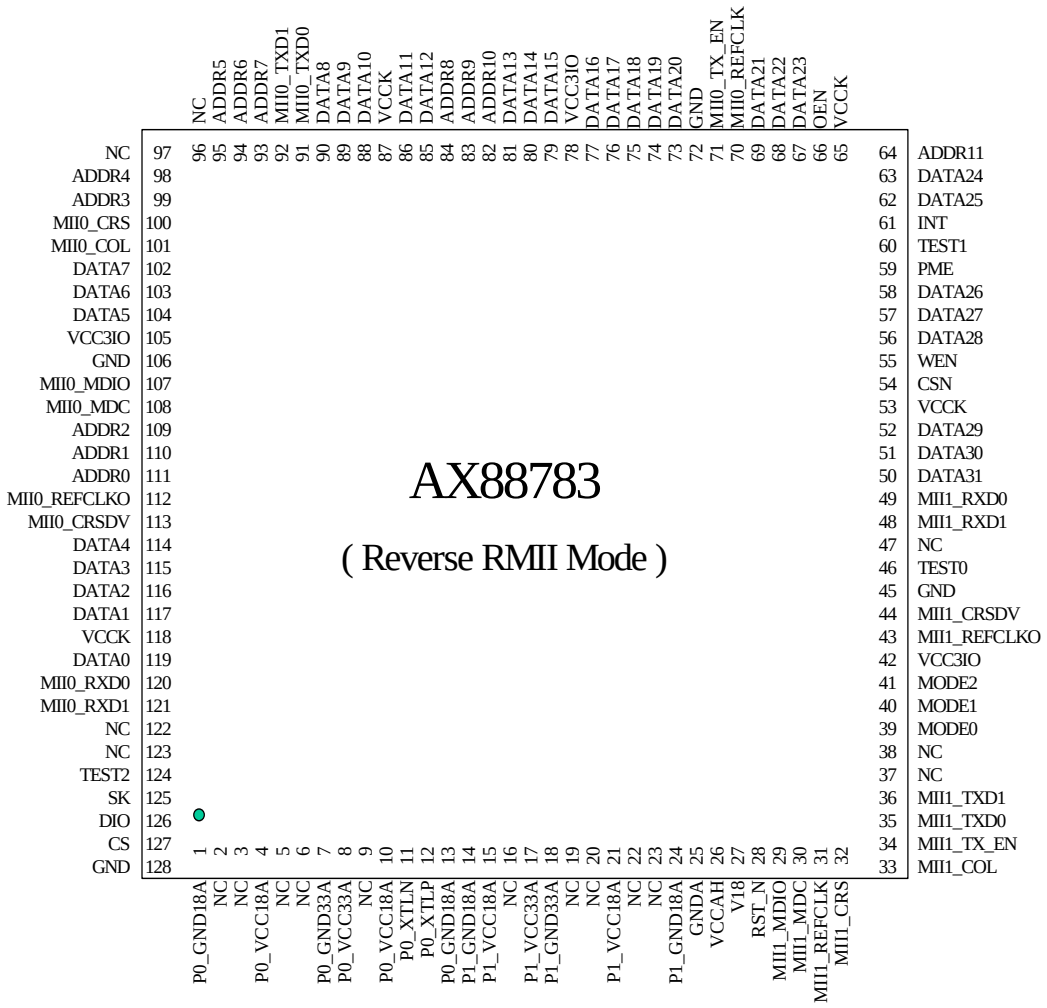


Fig 7 The AX88783 Port0/Port1 in Reverse RMII Mode

Note: The AX88783 also supports following mix-mode operations. Please refer to corresponding pin-out diagrams above. The AX88782 only support PHY mode with either 8 or 16-bit SRAM-like CPU interface.

Port 0	Port 1	Port 2
Built-in PHY	Built-in PHY	8-Bit Interface
MII Interface	MII Interface	16-Bit Interface
Reverse MII Interface	Reverse MII Interface	32-Bit Interface
RMII Interface	RMII Interface	
Reverse RMII Interface	Reverse RMII Interface	

2.0 Pin Descriptions

I/O Definition: The following terms describe the AX88782/AX88783 pin-out. The following abbreviations are used in following Tables. (Assume VCC3IO = 3.3V)

I18	**Input 1.8V**	**PU**	**Pull Up**
I3	**Input 3.3V**	**PD**	**Pull Down**
O18	**Output 1.8V**	**P**	**Power Pin**
O3	**Output 3.3V**	**NC**	**No Connect**
B18	**Bi-directional 1.8V**	**OD**	**Open Drain**
B3	**Bi-directional 3.3V**	**T**	**Tri-state**
AB	**Analog Bi-directional**	**8mA**	**8 mA drive strength**
A	**Analog**	**16mA**	**16 mA drive strength**

2.1 Port 0 Interface

2.1.1 PHY Mode

Signal Name	I/O	AX88782 Pin No.	AX88783 Pin No.	Description
P0_TXOP, P0_TXON	AB	3 2	3 2	Transmit Differential Data Pair for PHY0. The differential data is transmitted to the media on the TXOP/TXON signal pair in MDI mode or received differential data input positive pin in MDIX mode.
P0_RXIP, P0_RXIN	AB	6 5	6 5	Receive Differential Data Pair for PHY0. The differential data is received from the media on the RXIP/RXIN signal pair in MDI mode or transmitted differential data output negative pin in MDIX mode.
P0_XTLN,	I18	11	11	25Mhz ± 50 PPM crystal or oscillator clock input. A 25 MHz parallel-resonant crystal may be connected between these pins to stabilize the internal oscillator. This clock is needed for the embedded 10/100M Ethernet PHY to operate.
P0_XTLP	O18	12	12	25MHz Crystal Feedback Output. This output is used in crystal connection only. It must be left open when P0_XTLN is driven with an external 25MHz oscillator.
P0_RSET_BG	AO	9	9	Off-chip resistor. Connect 12.1Kohm ± 1% resistor to analog ground.
P0_LED0	B3/8mA	75	120	Port 0 PHY LED 0 signal output. Please configure LCR [7:0] to select LED output function.
P0_LED1	B3/8mA	76	121	Port 0 PHY LED 1 signal output. Please configure LCR [15:8] to select LED output function.
P0_LED2	O3/8mA	N/A*	122	Port 0 PHY LED 2 signal output. Please configure LCR [23:16] to select LED output function.
P0_VCC18A	P/A	4, 10	4, 10	1.8V power supply for internal PHY Analog circuit
P0_VCC33A	P/A	8	8	3.3V power supply for internal PHY Analog circuit.
P0_GND18A	P/A	1, 13	1, 13	1.8V Ground for internal PHY Analog circuit
P0_GND33A	P/A	7	7	3.3V Ground for internal PHY Analog circuit.

* The AX88782 Only supports P0_LED0 and P0_LED1 LED output function.

2.1.2 MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_RX_CLK	I3	70	Port 0 Receive clock input
MII0_RX_COL	I3	101	Port 0 Receive collision signal. Collision signal is driven high by PHY when the collision is detected.
MII0_RX_CRS	I3	100	Port 0 Receive carrier sense. Carrier sense signal is asserted high asynchronously by the PHY when either transmit or receive medium is non-idle.
MII0_RX_DV	I3	71	Port 0 Receive data valid. MII0_RX_DV is asserted high when valid data is present on receive data bus [3:0].
MII0_RXD0	I3	91	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD1	I3	92	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD2	I3	96	Port 0 Receive data bit 2 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD3	I3	97	Port 0 Receive data bit 3 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_TX_CLK	I3	112	Port 0 Transmit clock input
MII0_TX_EN	O3/8mA	113	Port 0 Transmit data enable. MII0_TX_EN is asserted high to indicate a valid transmit data bus [3:0]
MII0_TXD0	O3/8mA	120	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD1	O3/8mA	121	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD2	O3/8mA	122	Port 0 Transmit data bit 2 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD3	O3/8mA	123	Port 0 Transmit data bit 3 synchronously with respect to the rising edge of MII0_TX_CLK. Note: Pull-Down with a 4.7K ohm resistor to ground
MII0_MDIO	B3/8mA	107	MII management Data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	O3/8mA	108	MII management clock output to PHY. All data transferred on MII0_MDIO are synchronized to the rising edge of this clock. The frequency of MII0_MDC is 1MHz.

2.1.3 Reverse MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_TX_CLK	O3/8mA	70	Port 0 Transmit clock output
MII0_CRS	I3	100	Port 0 Carrier Sense. Please connect this signal to MII0_TX_EN enable signal.
MII0_COL	I3	101	Pull-Down with a 4.7KOhm resistor to ground. (Reverse MII mode only support full duplex mode)
MII0_TX_EN	I3	71	Port 0 Transmit data valid. MII0_TX_EN is asserted high when valid data is present on transmit data bus [3:0].
MII0_TXD0	I3	91	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD1	I3	92	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD2	I3	96	Port 0 Transmit data bit 2 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_TXD3	I3	97	Port 0 Transmit data bit 3 synchronously with respect to the rising edge of MII0_TX_CLK.
MII0_RX_CLK	O3/8mA	112	Port 0 Transmit clock output
MII0_RX_DV	O3/8mA	113	Port 0 Receive data enable. MII0_RX_DV is asserted high to indicate a valid receive data bus [3:0]
MII0_RXD0	O3	120	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD1	O3	121	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD2	O3	122	Port 0 Receive data bit 2 synchronously with respect to the rising edge of MII0_RX_CLK.
MII0_RXD3	O3/8mA	123	Port 0 Receive data bit 3 synchronously with respect to the rising edge of MII0_RX_CLK. Note: Pull-Down with a 4.7K ohm resistor to ground
MII0_MDIO	B3/8mA	107	MII management Data. Serial data input/output transferred from/to the external connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	I3	108	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MII0_MDIO are synchronized to the rising edge of this clock. Note: P0SMR0 Slave MDIO Register need to be programmed.

2.1.4 RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_REFCLK	I3	70	Port 0 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII0_CRSDV	I3	71	Port 0 Receive data valid synchronously with respect to the rising edge of MII0_REFCLK. MII0_CRSDV is asserted high when valid data is present on receive data bus [1:0].
MII0_RXD0	I3	91	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_RXD1	I3	92	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_REFCLKO	O3/8mA	112	Port 0 50MHz reference clock output if ICR [12] is set to one.
MII0_TX_EN	O3/8mA	113	Port 0 Transmit data enable synchronously with respect to the rising edge of MII0_REFCLK. MII0_TX_EN is asserted high to indicate a valid transmit data bus [1:0]
MII0_TXD0	O3/8mA	120	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_TXD1	O3/8mA	121	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_MDIO	B3/8mA	107	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	O3/8mA	108	MII management clock output to PHY. All data transferred on MDIO are synchronized to the rising edge of this clock. The frequency of MII0_MDC is 1MHz.
MII0_CRS	I3	100	Pull-Down with a 4.7K ohm resistor to ground
MII0_COL	I3	101	Pull-Down with a 4.7K ohm resistor to ground

2.1.5 Reverse RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII0_REFCLK	I3	70	Port 0 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII0_TX_EN	I3	71	Port 0 Transmit data valid synchronously with respect to the rising edge of MII0_REFCLK. MII0_TX_EN is asserted high when valid data is present on transmit data bus [1:0].
MII0_TXD0	I3	91	Port 0 Transmit data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_TXD1	I3	92	Port 0 Transmit data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_REFCLKO	O3/8mA	112	Port 0 50 MHz Reference clock output if ICR [12] is set to one.
MII0_CRSDV	O3/8mA	113	Port 0 Receive data enable synchronously with respect to the rising edge of MII0_REFCLK. MII0_CRSDV is asserted high to indicate a valid receive data bus [1:0]
MII0_RXD0	O3/8mA	120	Port 0 Receive data bit 0 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_RXD1	O3/8mA	121	Port 0 Receive data bit 1 synchronously with respect to the rising edge of MII0_REFCLK.
MII0_MDIO	B3/8mA	107	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII0_MDC	I3	108	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MII0_MDIO are synchronized to the rising edge of this clock. Note: P0SMR0 Slave MDIO Register need to be programmed.
MII0_CRS	I3	100	Pull-Down with a 4.7K ohm resistor to ground
MII0_COL	I3	101	Pull-Down with a 4.7K ohm resistor to ground

2.1.6 GPIO Mode (AX88783)

Signal Name	I/O	AX88783 Pin No.	Description
GPIO0	B3	101	Generous Purpose IO Pin #0
GPIO1	B3	100	Generous Purpose IO Pin #1
GPIO2	B3	112	Generous Purpose IO Pin #2
GPIO3	B3	70	Generous Purpose IO Pin #3
GPIO4	B3	107	Generous Purpose IO Pin #4
GPIO5	B3	108	Generous Purpose IO Pin #5
GPI0	I3	91	Generous Purpose Input Pin #0
GPI1	I3	92	Generous Purpose Input Pin #1
GPI2	I3	96	Generous Purpose Input Pin #2
GPI3	I3	97	Generous Purpose Input Pin #3
GPI4	I3	71	Generous Purpose Input Pin #4
GPO	O3	113	Generous Purpose Output Pin

2.1.7 Port 0 Multi-Function Pin Summary

AX88783 Pin #	MII Mode	Reverse MII Mode	RMII Mode	Reverse RMII Mode	PHY Mode	GPIO Mode
70	MII0_RX_CLK	MII0_TX_CLK	MII0_REFCLK	MII0_REFCLK	NC	GPIO3
101	MII0_RX_COL	Pull-Down	Pull-Down	Pull-Down	NC	GPIO0
100	MII0_RX_CRS	MII0_CRS	Pull-Down	Pull-Down	NC	GPIO1
71	MII0_RX_DV	MII0_TX_EN	MII0_CRSDV	MII0_TX_EN	NC	GPI4
91	MII0_RXD0	MII0_TXD0	MII0_RXD0	MII0_TXD0	NC	GPI0
92	MII0_RXD1	MII0_TXD1	MII0_RXD1	MII0_TXD1	NC	GPI1
96	MII0_RXD2	MII0_TXD2	NC	NC	NC	GPI2
97	MII0_RXD3	MII0_TXD3	NC	NC	NC	GPI3
112	MII0_TX_CLK	MII0_RX_CLK	MII0_REFCLKO	MII0_REFCLKO	NC	GPIO2
113	MII0_TX_EN	MII0_RX_DV	MII0_TX_EN	MII0_CRSDV	NC	GPO
120	MII0_TXD0	MII0_RXD0	MII0_TXD0	MII0_RXD0	P0_LED0	
121	MII0_TXD1	MII0_RXD1	MII0_TXD1	MII0_RXD1	P0_LED1	
122	MII0_TXD2	MII0_RXD2	NC	NC	P0_LED2	
123	MII0_TXD3	MII0_RXD3	NC	NC	NC	
107	MII0_MDIO	MII0_MDIO	MII0_MDIO	MII0_MDIO	NC	GPIO4
108	MII0_MDC	MII0_MDC	MII0_MDC	MII0_MDC	NC	GPIO5

Note1: The AX88782 can only support PHY Mode
Note2: GPIO mode and PHY mode can active at the same time without any conflict.

2.2 Port 1 Interface

2.2.1 PHY Mode

Signal Name	I/O	Pin No. AX88782	Pin No. AX88783	Description
P1_TXOP, P1_TXON	AB AB	21 22	22 23	Transmit Differential Data Pair for PHY0. The differential data is transmitted to the media on the TXOP/TXON signal pair in MDI mode or received differential data input positive pin in MDIX mode.
P1_RXIP, P1_RXIN	AB AB	18 19	19 20	Receive Differential Data Pair for PHY0. The differential data is received from the media on the RXIP/RXIN signal pair in MDI mode or transmitted differential data input positive pin in MDIX mode.
P1_RSET_BG	AO	15	16	Off-chip resistor. Connect 12.3±1%Kohm resistor to ground.
P1_LED0	B3/8mA	34	49	Port 1 PHY LED 0 signal output. Please configure LCR [7:0] to select LED output function.
P1_LED1	B3/8mA	33	48	Port 1 PHY LED 1 signal output. Please configure LCR [15:8] to select LED output function.
P1_LED2	O3/8mA	N/A	47	Port 1 PHY LED 2 signal output. Please configure LCR [23:16] to select LED output function.
P1_VCC18A	P/A	14, 20	15, 21	1.8V power supply for internal PHY Analog circuit
P1_VCC33A	P/A	16	17	3.3V power supply for internal PHY Analog circuit.
P1_GND18A	P/A	23	14, 24	1.8V Ground for internal PHY Analog circuit
P1_GND33A	P/A	17	18	3.3V Ground for internal PHY Analog circuit.

2.2.2 MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_RX_CLK	I3	31	Port 1 Receive clock input
MII1_RX_COL	I3	33	Port 1 Receive collision signal. Collision signal is driven high by PHY when the collision is detected.
MII1_RX_CRS	I3	32	Port 1 Receive carrier sense. Carrier sense signal is asserted high asynchronously by the PHY when either transmit or receive medium is non-idle.
MII1_RX_DV	I3	34	Port 1 Receive data valid. MII1_RX_DV is asserted high when valid data is present on receive data bus [3:0].
MII1_RXD0	I3	35	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD1	I3	36	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD2	I3	37	Port 1 Receive data bit 2 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD3	I3	38	Port 1 Receive data bit 3 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_TX_CLK	O3/8mA	43	Port 1 Transmit clock input
MII1_TX_EN	O3/8mA	44	Port 1 Transmit data enable. MII1_TX_EN is asserted high to indicate a valid transmit data bus [3:0]
MII1_TXD0	O3/8mA	49	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD1	O3/8mA	48	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD2	O3/8mA	47	Port 1 Transmit data bit 2 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD3	O3/8mA/PD	46	Port 1 Transmit data bit 3 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII1_MDC	O3/8mA	30	MII management clock output to PHY. All data transferred on MII1_MDIO are synchronized to the rising edge of this clock. The frequency of MII1_MDC is 1MHz.

2.2.3 Reverse MII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_TX_CLK	O3/8mA	31	Port 1 Transmit clock output
MII1_CRS	I3	32	Port 1 Carrier Sense. Please connect this signal to MII1_TX_EN enable signal.
MII1_COL	I3	33	Pull-Down with a 4.7KOhm resistor to ground. Reverse MII mode only support full duplex.
MII1_TX_EN	I3	34	Port 1 Transmit data valid. MII1_TX_EN is asserted high when valid data is present on transmit data bus [3:0].
MII1_TXD0	I3	35	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD1	I3	36	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD2	I3	37	Port 1 Transmit data bit 2 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_TXD3	I3	38	Port 1 Transmit data bit 3 synchronously with respect to the rising edge of MII1_TX_CLK.
MII1_RX_CLK	O3/8mA	43	Port 1 Receive clock output
MII1_RX_DV	O3/8mA	44	Port 1 Receive data enable. MII1_RX_DV is asserted high to indicate a valid receive data bus [3:0]
MII1_RXD0	O3/8mA	49	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD1	O3/8mA	48	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD2	O3/8mA	47	Port 1 Receive data bit 2 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_RXD3	O3/8mA	46	Port 1 Receive data bit 3 synchronously with respect to the rising edge of MII1_RX_CLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII1_MDC	I3	30	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MDIO are synchronized to the rising edge of this clock. Note: P1SMR0 Slave MDIO Register need to be programmed

2.2.4 RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_REFCLK	I3	31	Port 1 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII1_CRSDV	I3	34	Port 1 Receive data valid synchronously with respect to the rising edge of MII1_REFCLK. MII1_CRSDV is asserted high when valid data is present on receive data bus [1:0].
MII1_RXD0	I3	35	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_RXD1	I3	36	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_REFCLKO	O3/8mA	43	Port 1 50MHz clock output if ICR [13] is set to one.
MII1_TX_EN	O3/8mA	44	Port 1 Transmit data enable synchronously with respect to the rising edge of MII1_REFCLK. MII1_TX_EN is asserted high to indicate a valid transmit data bus [1:0]
MII1_TXD0	O3/8mA	49	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_TXD1	O3/8mA	48	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII1_MDC	O3/8mA	30	MII management clock output to PHY. All data transferred on MDIO are synchronized to the rising edge of this clock. The frequency of MDC is 1MHz.
MII1_CRS	I3	32	Pull-Down with a 4.7K ohm resistor to ground
MII1_COL	I3	33	Pull-Down with a 4.7K ohm resistor to ground

2.2.5 Reverse RMII Mode

Signal Name	I/O	AX88783 Pin No.	Description
MII1_REFCLK	I3	31	Port 1 50MHz RMII reference clock input ± 50 PPM with a duty cycle between 35% and 65% inclusive.
MII1_TX_EN	I3	34	Port 1 Transmit data valid synchronously with respect to the rising edge of MII1_REFCLK. MII1_TX_EN is asserted high when valid data is present on transmit data bus [1:0].
MII1_TXD0	I3	35	Port 1 Transmit data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_TXD1	I3	36	Port 1 Transmit data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_REFCLKO	O3/8mA	43	Port 1 50MHz reference clock output if ICR [13] is set to one.
MII1_CRSDV	O3/8mA	44	Port 1 Receive data enable synchronously with respect to the rising edge of MII1_REFCLK. MII1_CRSDV is asserted high to indicate a valid receive data bus [1:0]
MII1_RXD0	O3/8mA	49	Port 1 Receive data bit 0 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_RXD1	O3/8mA	48	Port 1 Receive data bit 1 synchronously with respect to the rising edge of MII1_REFCLK.
MII1_MDIO	B3/8mA/T	29	MII management data. Serial data input/output transferred from/to the externally connected MAC device. The transfer protocol should conform to the IEEE 802.3u MII spec.
MII1_MDC	I3	30	MII management clock input from the externally connected Ethernet MAC device. All data transferred on MDIO are synchronized to the rising edge of this clock. Note: P1SMR0 Slave MDIO Register need to be programmed
MII1_CRS	I3	32	Pull-Down with a 4.7K ohm resistor to ground
MII1_COL	I3	33	Pull-Down with a 4.7K ohm resistor to ground

2.2.6 Port 1 Multi-Function Pin Summary

AX88783 Pin #	MII Mode	Reverse MII Mode	RMII Mode	Reverse RMII Mode	PHY Mode
31	MII1_RX_CLK	MII1_TX_CLK	MII1_REFCLK	MII1_REFCLK	NC
33	MII1_RX_COL	Pull-Down	Pull-Down	Pull-Down	NC
32	MII1_RX_CRS	MII1_CRS	Pull-Down	Pull-Down	NC
34	MII1_RX_DV	MII1_TX_EN	MII1_CRSDV	MII1_TX_EN	NC
35	MII1_RXD0	MII1_TXD0	MII1_RXD0	MII1_TXD0	NC
36	MII1_RXD1	MII1_TXD1	MII1_RXD1	MII1_TXD1	NC
37	MII1_RXD2	MII1_TXD2	NC	NC	NC
38	MII1_RXD3	MII1_TXD3	NC	NC	NC
43	MII1_TX_CLK	MII1_RX_CLK	MII1_REFCLKO	MII1_REFCLKO	NC
44	MII1_TX_EN	MII1_RX_DV	MII1_TX_EN	MII1_CRSDV	NC
49	MII1_TXD0	MII1_RXD0	MII1_TXD0	MII1_RXD0	P1_LED0
48	MII1_TXD1	MII1_RXD1	MII1_TXD1	MII1_RXD1	P1_LED1
47	MII1_TXD2	MII1_RXD2	NC	NC	P1_LED2
46	MII1_TXD3	MII1_RXD3	NC	NC	NC
29	MII1_MDIO	MII1_MDIO	MII1_MDIO	MII1_MDIO	NC
30	MII1_MDC	MII1_MDC	MII1_MDC	MII1_MDC	NC

2.3 Port 2 SRAM-like Interface

2.3.1 8/16 Bit CPU Interface for the AX88782

Signal Name	I/O	Pin No.	Description
CSN	I3	36	Chip Select, active low.
WEN	I3	37	Write Enable, active low.
OEN	I3	42	Read Enable active low.
INT	O3/T	39	Interrupt output to external CPU. Interrupt polarity can be programmed by setting GMCR register bit [27].
ADDR0	I3	68	CPU Address bus bit [0]
ADDR1	I3	67	CPU Address bus bit [1]
ADDR2	I3	66	CPU Address bus bit [2]
ADDR3	I3	61	CPU Address bus bit [3].
ADDR4	I3	60	CPU Address bus bit [4].
ADDR5	I3	59	CPU Address bus bit [5].
ADDR6	I3	58	CPU Address bus bit [6]
ADDR7	I3	57	CPU Address bus bit [7]
ADDR8	I3	50	CPU Address bus bit [8]
ADDR9	I3	49	CPU Address bus bit [9]
ADDR10	I3	48	CPU Address bus bit [10]
ADDR11	I3	40	CPU Address bus bit [11]
DATA0	B3	74	CPU Data bus bit [0]
DATA1	B3	72	CPU Data bus bit [1]
DATA2	B3	71	CPU Data bus bit [2]
DATA3	B3	70	CPU Data bus bit [3]
DATA4	B3	69	CPU Data bus bit [4]
DATA5	B3	64	CPU Data bus bit [5]
DATA6	B3	63	CPU Data bus bit [6]
DATA7	B3	62	CPU Data bus bit [7]
DATA8	B3	56	CPU Data bus bit [8]
DATA9	B3	55	CPU Data bus bit [9]
DATA10	B3	54	CPU Data bus bit [10]
DATA11	B3	52	CPU Data bus bit [11]
DATA12	B3	51	CPU Data bus bit [12] Please Pull-Down with a 4.7K ohm resistor to ground when MODE2, MODE1 and MODE0 is configured to 8-bit bus mode.
DATA13	B3	47	CPU Data bus bit [13]
DATA14	B3	46	CPU Data bus bit [14]
DATA15	B3	45	CPU Data bus bit [15]

2.3.2 8/16/32 Bit CPU Interface for the AX88783

Signal Name	I/O	Pin No.	Description
CSN	I3	54	Chip Select, active low.
WEN	I3	55	Write Enable, active low.
OEN	I3	66	Read Enable active low.
INT	O3/T	61	Interrupt output to external CPU. Interrupt polarity can be programmed by setting GMCR register bit [27].
ADDR0	I3	111	CPU Address bus bit [0]
ADDR1	I3	110	CPU Address bus bit [1]
ADDR2	I3	109	CPU Address bus bit [2]
ADDR3	I3	99	CPU Address bus bit [3].
ADDR4	I3	98	CPU Address bus bit [4].
ADDR5	I3	95	CPU Address bus bit [5].
ADDR6	I3	94	CPU Address bus bit [6]
ADDR7	I3	93	CPU Address bus bit [7]
ADDR8	I3	84	CPU Address bus bit [8]
ADDR9	I3	83	CPU Address bus bit [9]
ADDR10	I3	82	CPU Address bus bit [10]
ADDR11	I3	64	CPU Address bus bit [11]
DATA0	B3	119	CPU Data bus bit [0]
DATA1	B3	117	CPU Data bus bit [1]
DATA2	B3	116	CPU Data bus bit [2]
DATA3	B3	115	CPU Data bus bit [3]
DATA4	B3	114	CPU Data bus bit [4]
DATA5	B3	104	CPU Data bus bit [5]
DATA6	B3	103	CPU Data bus bit [6]
DATA7	B3	102	CPU Data bus bit [7]
DATA8	B3	90	CPU Data bus bit [8]
DATA9	B3	89	CPU Data bus bit [9]
DATA10	B3	88	CPU Data bus bit [10]
DATA11	B3	86	CPU Data bus bit [11]
DATA12	B3	85	CPU Data bus bit [12] Please Pull-Down with a 4.7K ohm resistor to ground when MODE2, MODE1 and MODE0 is configured to 8-bit bus mode.
DATA13	B3	81	CPU Data bus bit [13]
DATA14	B3	80	CPU Data bus bit [14]
DATA15	B3	79	CPU Data bus bit [15]
DATA16	B3	77	CPU Data bus bit [16]
DATA17	B3	76	CPU Data bus bit [17]
DATA18	B3	75	CPU Data bus bit [18]
DATA19	B3	74	CPU Data bus bit [19]
DATA20	B3	73	CPU Data bus bit [20]
DATA21	B3	69	CPU Data bus bit [21]
DATA22	B3	68	CPU Data bus bit [22]
DATA23	B3	67	CPU Data bus bit [23]
DATA24	B3	63	CPU Data bus bit [24]
DATA25	B3	62	CPU Data bus bit [25]
DATA26	B3	58	CPU Data bus bit [26]
DATA27	B3	57	CPU Data bus bit [27]
DATA28	B3	56	CPU Data bus bit [28]
DATA29	B3	52	CPU Data bus bit [29]
DATA30	B3	51	CPU Data bus bit [30]
DATA31	B3	50	CPU Data bus bit [31]

2.4 EEROM Interface

Signal Name	I/O	AX88782 Pin No.	AX88783 Pin No.	Description
CS	B3/8mA/ PD	79	127	EEPROM chip select signal PU: Pull-Up with a 4.7K ohm resistor to VCC PD: Pull-Down with a 4.7K ohm resistor to ground **EEPROM size / SK / CS** N/A (default) PD PD 1K(93C46) PD PU 2K(93C56) PU PD 4K(93C66) PU PU
DIO	B3/8mA/ T	78	126	EEPROM bi-direction data signal. This pin should connect to EEPROM's DO and DI pin.
SK	B3/8mA/ PD	77	125	EEPROM clock (1MHz)

2.5 Miscellaneous IO Pin Function

Signal Name	I/O	AX88782 Pin No.	AX88783 Pin No.	Description
MODE2, MODE1, MODE0	I3 I3 I3	30 29 28	41 40 39	Chip Bus Mode Select MODE2 / MODE1 / MODE0 / Chip Mode PD / PD / PD / 8-Bit CPU Bus Mode PD / PD / PU / 16-Bit CPU Bus Mode PD / PU / PD / 32-Bit CPU Bus Mode PU: Pull-Up with a 4.7K ohm resistor to VCC PD: Pull-Down with a 4.7K ohm resistor to ground
TEST0	I3		46	Pull-Down with a 4.7K ohm resistor to ground when the Port 1 is in the PHY, RMII or reverse RMII mode
TEST1	I3		60	Pull-Down with a 4.7K ohm resistor to ground
TEST2	I3		124	Pull-Down with a 4.7K ohm resistor to ground
RST_N	I3	27	28	Chip Reset pin. Default is active low.
PME	O3	38	59	Power Management Event. This pin is used to indicate that a power management event has occurred.
VCCAH	P	25	26	Internal Regulator 3.3 Volt DC power input
V18	P	26	27	Internal Regulator 1.8 Volt DC power output.
GNDA	P	24	25	Internal Regulator analog ground pin
VCCK	P	35,41,53,73	53,65,87,118	1.8 Volt. DC Power Supply for core logic
VCC3IO	P	31,44,65	42,78,105	Support 1.8V, 2.5V or 3.3 multi voltage DC Power Supply for IO pad
GND	P	32,43,80	45,72, 106,128	Ground

3.0 Functional Description

Please contact ASIX's Sales (sales@asix.com.tw) for receiving "AX88782/AX88783 Full Datasheet" which contains the detailed descriptions of section 3, 4, and 5.

3.1 Overview

3.2 Clock

3.3 Built-in Power-On-Reset

3.4 Built-in Voltage Regulator

3.5 Two Built-in 10/100M Base-TX Fast Ethernet DSP-Based PHY

3.6 Basic MAC Function

3.7 Basic Switch Function

3.8 VLAN Support

3.9 IEEE 802.1D Spanning Tree

3.10 QoS and Ingress/Egress Rate Limit Operation

3.11 Security Operation

3.12 PPPoE/TCP/UDP/ICMP/IGMP/IPv4 Checksum Off-load Support

3.13 RMON Counter Support

3.13 Layer 2/3/4 Sniffer Function Support

3.14 IPv4 IGMP and IPv6 ICMP/MLD Snooping

3.15 Wake-On-LAN Function Support

3.16 Power Management

3.17 Auto-Polling Function

3.18 Port Mirroring

3.19 Serial EEPROM Protocol

3.20 GPIO Interface Support (Only for AX88783)

3.21 CPU Interface Protocol

4.0 Interface

4.1 MII Interface

4.1.1 MII Interface Set-Up Procedure

4.2 Reverse MII Interface (Only Support 100M Full Duplex Mode)

4.2.1 Reverse MII Interface Set-Up Procedure

4.3 RMII and Reverse RMII Interface

4.3.1 RMII Mode Reference connection

4.3.2 RMII Interface Set-Up Procedure

4.3.3 Reverse RMII Mode Reference connection: (Only support 100 Full Duplex mode)

4.3.4 Reverse RMII Interface Set-Up Procedure

4.4 CPU Read/Write Operation

4.4.1 8-Bit CPU Burst Read/Write Operation

4.4.2 16-Bit CPU Burst Read/Write Operation

4.4.3 32-Bit CPU Burst Read/Write Operation

5.0 Internal Register Configuration

5.1 MAC Register Definition

5.1.1 Chip revision ID and Reset Register (CIRR)

5.1.2 PHY0 /PHY1 Configuration Register (PCR)

5.1.3 PHY0/PHY1 Status Register (PSR)

5.1.4 Global MAC Configuration Register (GMCR)

5.1.5 Layer 2 Global Configuration Register (LGCR)

5.1.6 Layer 2 Learning/Aging/OneSA Control Register (LLCR)

5.1.7 Layer 2 Routing Table Entry Read/Write Register (LRCR0 and LRCR1)

5.1.8 802.1D and Port-based VLAN Configuration Register (PVCR)

5.1.9 Sniffer Function Configuration Register (SFCR0, SFCR1, SFCR2)

5.1.9.1 Sniffer Function Configuration Register 0 (SFCR0)

5.1.9.2 Sniffer Function Configuration Register 1 (SFCR1)

5.1.9.3 Sniffer Function Configuration Register 2 (SFCR2)

5.1.10 QoS Priority Mapping Table Register (QPTR)

5.1.11 802.1Q-in-1Q (Double-Tagging) Configuration Register (QCR)

5.1.12 Port Pair and MDC Control Register (PPMR)

5.1.13 MDIO Read/Write Control Register (MRCR)

5.1.14 TCP/IP Offload Control Register (TOCR)

5.1.15 CPIO Control Register (CCR)

5.1.16 Security Mac Control Registers

5.1.16.1 Security Mac 0 Control Register (SM0CR0, SM0CMR1)

5.1.16.2 Security Mac 1 Control Register (SM1CR0, SM1CR1)

5.1.16.3 Security Mac 2 Control Register (SM2CR0, SM2CR1)

5.1.16.4 Security Mac 3 Control Register (SM3CR0, SM3CR1)

5.1.16.5 Security Mac 4 Control Register (SM4CR0, SM4CR1)

5.1.16.6 Security Mac 5 Control Register (SM5CR0, SM5CR1)

5.1.16.7 Security Mac 6 Control Register (SM6CR0, SM6CR1)

5.1.16.8 Security Mac 7 Control Register (SM7CR0, SM7CR1)

5.1.17 VLAN Entry Registers

5.1.17.1 VLAN Entry 0 Register (VER0)

5.1.17.2 VLAN Entry 1 Register (VER1)

5.1.17.3 VLAN Entry 2 Register (VER2)

5.1.17.4 VLAN Entry 3 Register (VER3)

5.1.17.5 VLAN Entry 4 Register (VER4)

5.1.17.6 VLAN Entry 5 Register (VER5)

5.1.17.7 VLAN Entry 6 Register (VER6)

5.1.17.8 VLAN Entry 7 Register (VER7)

5.1.17.9 VLAN Entry 8 Register (VER8)

5.1.17.10 VLAN Entry 9 Register (VER9)

5.1.17.11 VLAN Entry 10 Register (VER10)

5.1.17.12 VLAN Entry 11 Register (VER11)

5.1.17.13 VLAN Entry 12 Register (VER12)

5.1.17.14 VLAN Entry 13 Register (VER13)

5.1.17.15 VLAN Entry 14 Register (VER14)

5.1.17.16 VLAN Entry 15 Register (VER15)

5.1.18 CPIO Byte Order Register (CBOR)

5.1.19 CPIO Start Command Register (CSCR)

5.1.20 IGMP Table Read/Write Control Register (ITCR)

5.1.21 LED Control Register (LCR)

5.1.22 RMON Control Register (RCR)

5.1.23 RMON Data Register (RDR)

5.1.24 DSCP QoS mapping table Register (DQR0, DQR1, DQR2, DQR3)

5.1.25 Interrupt Status and Mask Register (ISMR)

5.1.26 User-Defined Sniffer Packet Type Register (USTR)

5.1.27 Wake-On-LAN Configuration Register (WCR)

5.1.28 Wake-ON-LAN Setup Register (WSR)

5.1.29 Port 0 Wakeup Frame Mask0 ~ 2 Register (P0WMR0, P0WMR1, P0WMR2)

5.1.30 Port 0 Wakeup Frame CRC Mask 0 ~ 3 Register (P0WCR0, P0WCR1, P0WCR2)

5.1.31 Port 1 Wakeup Frame Mask0 ~ 2 Register (P1WMR0, P1WMR1, P1WMR2)

5.1.32 Port 1 Wakeup Frame CRC Mask 0 ~ 3 Register (P1WCR0, P1WCR1, P1WCR2)

5.1.33 Auto-Polling Control Register (ACR)

5.1.34 EEROM Control Register (ECR)

5.1.35 Boot Loader Control Register (BLCR)

5.1.36 IO Pad Pull-Up/Pull-Down Control Register (IOCR)

5.1.37 Multicast IP for IGMP Snooping Entry 0 - 7 Register (IER0~IER7)

5.1.37.1 Multicast IP Entry 0 Register (IER0)

5.1.37.2 Multicast IP Entry 1 Register (IER1)

5.1.37.3 Multicast IP Entry 2 Register (IER2)

5.1.37.4 Multicast IP Entry 3 Register (IER3)

5.1.37.5 Multicast IP Entry 4 Register (IER4)

5.1.37.6 Multicast IP Entry 5 Register (IER5)

5.1.37.7 Multicast IP Entry 6 Register (IER6)

5.1.37.8 Multicast IP Entry 7 Register (IER7)

5.1.38 GPIO Control Register 1 (GPIOCR1)

5.1.39 GPIO Control Register 2 (GPIOCR2)

5.1.40 GPIO Control Register 3 (GPIOCR3)

5.1.41 GPIO Control Register 4 (GPIOCR4)

5.1.42 Port 0 Slave MDC/MDIO Register 0 (P0SMR0)

5.1.43 Port 0 Slave MDC/MDIO Register 1 (P0SMR1)

5.1.44 Port 0 Slave MDC/MDIO Register 2 (P0SMR2)

5.1.45 Port 0 Slave MDC/MDIO Register 3 (P0SMR3)

5.1.46 Port 1 Slave MDC/MDIO Register 0 (P1SMR0)

5.1.47 Port 1 Slave MDC/MDIO Register 1 (P1SMR1)

5.1.48 Port 1 Slave MDC/MDIO Register 2 (P1SMR2)

5.1.49 Port 1 Slave MDC/MDIO Register 3 (P1SMR3)

5.1.50 Port 2 Multicast MAC Filters Register (P2MFR0 ~ P2MFR15)

5.1.50.1 Port 2 Multicast MAC Filters Register 0 (P2MFR0)

5.1.50.2 Port 2 Multicast MAC Filters Register 1 (P2MFR1)

5.1.50.3 Port 2 Multicast MAC Filters Register 2 (P2MFR2)

5.1.50.4 Port 2 Multicast MAC Filters Register 3 (P2MFR3)

5.1.50.5 Port 2 Multicast MAC Filters Register 4 (P2MFR4)

5.1.50.6 Port 2 Multicast MAC Filters Register 5 (P2MFR5)

5.1.50.7 Port 2 Multicast MAC Filters Register 6 (P2MFR6)

5.1.50.8 Port 2 Multicast MAC Filters Register 7 (P2MFR7)

5.1.50.9 Port 2 Multicast MAC Filters Register 8 (P2MFR8)

5.1.50.10 Port 2 Multicast MAC Filters Register 9 (P2MFR9)

5.1.50.11 Port 2 Multicast MAC Filters Register 10 (P2MFR10)

5.1.50.12 Port 2 Multicast MAC Filters Register 11 (P2MFR11)

5.1.50.13 Port 2 Multicast MAC Filters Register 12 (P2MFR12)

5.1.50.14 Port 2 Multicast MAC Filters Register 13 (P2MFR13)

5.1.50.15 Port 2 Multicast MAC Filters Register 14 (P2MFR14)

5.1.50.16 Port 2 Multicast MAC Filters Register 15 (P2MFR15)

5.1.51 Interface Configuration Register (ICR)

5.1.52 Sleep Mode Exit Register (SMER)

5.1.53 Endian Configuration Register (ECR)

5.1.54 General Purpose Timer Configuration Register (GTCR)

5.1.55 Port 0 MAC Configuration Register (P0MCR)

5.1.56 Port 0 802.1p QoS Mapping Table Register (P0QMTR)

5.1.57 Port 0 802.1Q Configuration for UnTag Frame Register (P0QCR)

5.1.58 Port 0 RX per Queue Rate Limit Control Register 0 (P0RQR0)

5.1.59 Port 0 RX per Queue Rate Limit Control Register 1 (P0RQR1)

5.1.60 Port 0 TX per Queue Rate Limit Control Register 0 (P0TQR0)

5.1.61 Port 0 TX per Queue Rate Limit Control Register 1 (P0TQR1)

5.1.62 Port 0 Rate Limit Control Register (P0RLR)

5.1.63 Port 0 Rate Limit Timer Register (P0RLTR)

5.1.64 Port 0 Flow Control High/Low Watermark Register (P0FCR)

5.1.65 Port 0 Queue Weighting Configuration Register (P0QWR)

5.1.66 Port 0 RX Bad Check-sum Drop Counter Register (P0RDCR)

5.1.67 Port 0 DA MAC Address Register (P0DAR0, P0DAR1)

5.1.68 Port 1 MAC Configuration Register (P1MCR)

5.1.69 Port 1 802.1p QoS Mapping Table Register (P1QMTR)

5.1.70 Port 1 802.1Q Configuration for UnTag Frame Register (P1QCR)

5.1.71 Port 1 RX per Queue Rate Limit Control Register 0 (P1RQR0)

5.1.72 Port 1 RX per Queue Rate Limit Control Register 1 (P1RQR1)

5.1.73 Port 1 TX per Queue Rate Limit Control Register 0 (P1TQR0)

5.1.74 Port 1 TX per Queue Rate Limit Control Register 1 (P1TQR1)

5.1.75 Port 1 Rate Limit Control Register (P1RLR)

5.1.76 Port 1 Rate Limit Timer Register (P1RLTR)

5.1.77 Port 1 Flow Control High/Low Watermark Register (P1FCR)

5.1.78 Port 1 Queue Weighting Configuration Register (P1QWR)

5.1.79 Port 1 RX Bad Checksum Drop Counter Register (P1RDCR)

5.1.80 Port 1 DA MAC Address Register (P1DAR0, P1DAR1)

5.1.81 Port 2 MAC Configuration Register (P2MCR)

5.1.82 Port 2 802.1p QoS Mapping Table Register (P2QMTR)

5.1.83 Port 2 802.1 Q Configuration for UnTag Frame Register (P2QCR)

5.1.84 Port 2 RX per Queue Rate Limit Control Register 0 (P2RQR0)

5.1.85 Port 2 RX per Queue Rate Limit Control Register 1 (P2RQR1)

5.1.86 Port 2 TX per Queue Rate Limit Control Register 0 (P2TQR0)

5.1.87 Port 2 TX per Queue Rate Limit Control Register 1 (P2TQR1)

5.1.88 Port 2 Rate Limit Control Register (P2RLR)

5.1.89 Port 2 Rate Limit Timer Register (P2RLTR)

5.1.90 Port 2 Flow Control High/Low Watermark Register (P2FCR)

5.1.91 Port 2 Queue Weighting Configuration Register (P2QWR)

5.1.92 Port 2 DA MAC Address Register (P2DAR0, P2DAR1)

5.1.93 GPIO Wakeup Register (GPIOWR)

5.2 PHY Register Description

5.2.1 Basic Mode Control Register (BMCR)

5.2.2 Basic Mode Status Register (BMSR)

5.2.3 PHY Identifier Register 1 (PHYIDR1)

5.2.4 PHY Identifier Register 2 (PHYIDR2)

5.2.5 Auto-Negotiation Advertisement Register (ANAR)

5.2.6 Auto-Negotiation Link Partner Ability Register (ANLPAR)

5.2.7 Auto-Negotiation Expansion Register (ANER)

5.3 Reverse Mode PHY Register Description

5.3.1 Basic Mode Control Register (Rev_BMCR)

5.3.2 Basic Mode Status Register (Rev_BMSR)

5.3.3 Auto-Negotiation Advertisement Register (Rev_ANAR)

5.3.4 Auto-Negotiation Link Partner Ability Register (Rev_ANLPAR)

5.3.5 Local User-Defined Control Register (Rev_LUCR)

5.3.6 Remote User-Defined Control Register (Rev_RUCR)

6.0 ELECTRICAL SPECIFICATION AND TIMING

6.1 DC Characteristics

6.1.1 Absolute Maximum Ratings

Description	Rating	Units
VCCK (Core power supply), V18(voltage regulator), P0_VCC18A, P1_VCC18A (analog power supply for oscillator, PLL, PHY)	-0.3 to 2.16	V
VCC3IO (power supply for 3.3V I/O), VCCAH(voltage regulator), P0_VCC33A, P1_VCC33A(analog power supply for bandgap)	-0.3 to 4.0	V
Storage Temperature	-40 to 150	°C
I_{IN} (DC input current)	20	mA
I_{OUT} (Output short circuit current)	20	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the recommended operating condition section of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability

6.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.62	1.8	1.98	V
P0_VCC18A, P1_VCC18A	Analog core power supply	1.62	1.8	1.98	V
VCCAH	Power supply of on-chip voltage regulator	2.97	3.3	3.63	V
VCC3IO	Power supply of 3.3V I/O	2.97	3.3	3.63	V
P0_VCC33A, P1_VCC33A	Analog power supply for bandgap	2.97	3.3	3.63	V
V_{IN18}	Input voltage of 1.8 V I/O	0	1.8	1.98	V
V_{IN3}	Input voltage of 3.3 V I/O	0	3.3	3.63	V
T_j	Commercial junction operating temperature	-40	25	125	℃
T_a	Commercial operating temperature	0	-	70	℃

6.1.3 DC Characteristics of 3.3V I/O (VCC3IO = 3.3V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	LVTTL spec.			0.8	V
Vih	Input high voltage		2.0			V
Vt-	Schmitt-trigger negative threshold voltage	LVTTL spec.	0.8			V
Vt+	Schmitt-trigger negative threshold voltage				2.0	
Vol	Output low voltage	Iol = 2 ~ 12 mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -2 ~ -12 mA	2.4	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0V	40	75	190	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	75	190	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-15	-45	-90	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	15	45	90	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

6.1.4 DC Characteristics of 2.5V I/O (VCC3IO = 2.5V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 2.5V I/O	2.5V I/O	2.25	2.5	2.75	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	CMOS spec.			0.25* VCC3IO	V
Vih	Input high voltage		0.625* VCC3IO			V
Vt-	Schmitt-trigger negative threshold voltage	CMOS spec.	0.25* VCC3IO			V
Vt+	Schmitt-trigger negative threshold voltage				0.625* VCC3IO	
Vol	Output low voltage	Iol =1.1 ~ 6.68mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -1.1 ~ -6.6mA	1.85	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0V	40	110	290	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	40	110	290	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-7	-23	-62	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	7	23	62	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

6.1.5 DC Characteristics of 1.8 V I/O (VCC3IO = 1.8V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC3IO	Power supply of 1.8V I/O	1.8V I/O	1.62	1.8	1.98	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	CMOS spec.			0.3* VCC3IO	V
Vih	Input high voltage		0.7* VCC3IO			V
Vt-	Schmitt-trigger negative threshold voltage	CMOS spec.	0.3* VCC3IO			V
Vt+	Schmitt-trigger negative threshold voltage				0.7* VCC3IO	
Vol	Output low voltage	Iol = 0.7 ~ 4.2mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -0.7 ~ -4.2mA	0.7* VCC3IO	-	-	V
Rpu	Input pull-up resistance	V_{in} = 0V	80	200	510	KΩ
Rpd	Input pull-down resistance	V_{in} = VCC3IO	80	200	510	KΩ
Iin	Input leakage current	Vin = VCC3IO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-3	-9	-25	μA
	Input leakage current with pull-down resistance	Vin = VCC3IO	3	9	25	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

6.1.6 DC Characteristics of Voltage Regulator

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCCAH	Power supply of on-chip voltage regulator.		2.7	3.3	3.6	V
Tj	Operating junction temperature.		-40	25	125	℃
Iload_v18	Driving current.	Normal operation,	-	-	300	mA
	Driving current.	Standby mode enabled,	-	-	30	mA
V18	Output voltage of on-chip voltage regulator.	VCCAH = 3.3V After trimming	1.71	1.8	1.89	V
		VCCAH = 2.7V Iload_v18=300mA	1.71	1.8	1.89	
		VCCAH=3.6V STB=1 Iload_v18_stb=30 mA Tj=25℃	1.71	1.8	1.89	
		VCCAH=3.3V STB=1 Iload_v18_stb=30 mA Tj=25℃	1.71	1.8	1.89	
Vdrop	Dropout voltage.	△V18 = -1%, Iload_v18 = 10mA	-	0.1	0.2	V
$\frac{\triangle V18}{(\triangle VCCAH \times V18)}$	Line regulation.	VCCAH = 2.7 ~ 3.6V, Iload_v18 = 50mA	-	0.2	0.4	%/V
$\frac{\triangle V18}{(\triangle Iload\_v18 \times V18)}$	Load regulation.	VCCAH = 3.3V, 1mA ≦ Iload_v18 ≦ 300mA	-	0.006	0.012	%/mA
$\frac{\triangle V18}{\triangle Tj}$	Temperature coefficient.	VCCAH = 3.3V, -40℃ ≦ Tj ≦ 125℃ Iload_v18=10mA	-	0.1	0.2	mV/℃
Iq_25℃	Quiescent current at 25 ℃.	VCCAH = 3.3V, STB = 0	-	100	165	μA

		VCCAH = 3.3V, STB = 1	-	70	100	μA
Iq_125℃	Quiescent current at 125℃.	VCCAH = 3.3V, STB = 0	-	125	185	μA
		VCCAH = 3.3V, STB = 1	-	85	115	μA
Idis	Disable current			1	3	μA
Cout	Output external capacitor.		0.1	1	-	μF
△Vtransient	Voltage drop due to current transient effect	VCCAH = 3.3V Cout = 1μF Tr = Tf = 10 ns		0.3		V
ESR	Allowable effective series resistance of external capacitor.		-	0.5	1	Ω

6.2 Thermal Characteristics

A. Junction to ambient thermal resistance, θ_{JA}

Symbol	Min	Typ	Max	Units
θ_{JA}	-	25.2 (AX88782) 24.4(AX88783)	-	°C/W

B. Junction to case thermal resistance, θ_{JC}

Symbol	Min	Typ	Max	Units
θ_{JC}	-	9.6(AX88782) 9.5(AX88783)		°C/W

Note: θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P}, \quad \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature
T_A: ambient or environment temperature
T_C: the top center of compound surface temperature
P: input power (watts)

6.3 Power Consumption

- **Device only**

  Power measurements base on 3.3V/25 °C condition with the help of current probe.

Device	Both Ports @ 10BASE-T Half-Duplex*1			Both Ports @ 100BASE-TX Full-Duplex *1			D1 RemoteWake-up Mode*2			D2 Sleep Mode*3			Both Ports in PHY Power-Down*4			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
AX88782		224			336			78			8			<1		mA
		739			1109			257			26			<1		mW
AX88783		206			328			60			9			<1		mA
		680			1082			198			30			<1		mW

*1: 100% utilization on both ports.
*2: PHY0 Power-On, PHY1 Power-Down, Remote Wake-up function enable for Port 0, core clock ON
*3: Both PHY Power-Down, core clock ON, Write any data to SMER register to go back normal mode
*4: Both PHY Power-Down, core clock OFF
Note: The transformer will consume additional 40mA @3.3V for 100BASE-TX and 100mA @3.3V for 10BASE-T

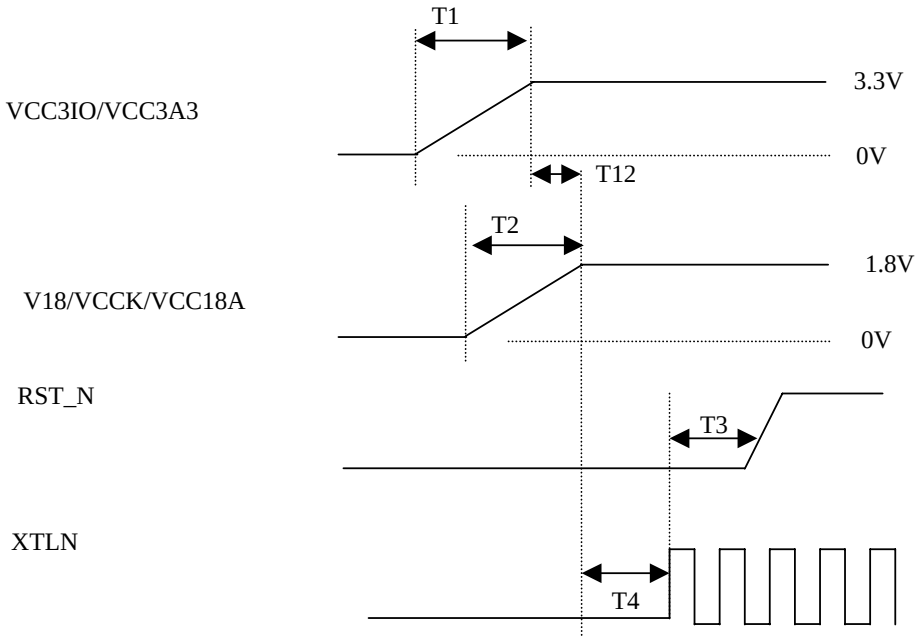
- **Device and system components**

  This is the total of Ethernet connectivity solution, which includes external components such as the Ethernet magnetic, EEPROM, etc.
  Power measurements base on 3.3V/25 °C condition.

Item	Test Conditions (Typical Condition)	AX88782/AX88783			Units
		Min	Typ	Max	
1	10BASE-T operation (Both Ports, Half-Duplex)		1399/1339		mW
2	100BASE-TX operation (Both Ports, Full-Duplex)		1372/1346		mW
3	Cable unplug and non power saving mode (Both Ports)		650/660		mW
4	D1 WOL mode (Port 0 PHY Power-On, Port 1 PHY Power-Down, Remote Wake-up supported for port 0)		587/528		mW
5	D2 Sleep mode (Both Ports, Remote Wake-up not supported)		28/32		mW
6.	PHY power down (Both Ports)		<1		mW

6.4 Power-up Sequence

At power-up, the AX88782/AX88783 requires the VCC3IO/VCC3A3 power supply to rise to nominal operating voltage within Trise3 and the V18/VCCK/VCC18A power supply to rise to nominal operating voltage within Trise2.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_1	3.3V power supply rise time	From 0V to 3.3V	0.5	-	10	ms
T_2	1.8V power supply rise time	From 0V to 1.8V	-	-	10	ms
T_{12}	3.3V rise to 1.8V rise time delay		-5	-	5	ms
T3	System Reset rise time after the clock is stable	From VCCIO = 3.3V and VCCK = 1.8V to RST_N going high	200			us
T4	Oscillator stable time	From VCCK = 1.8V	805			us

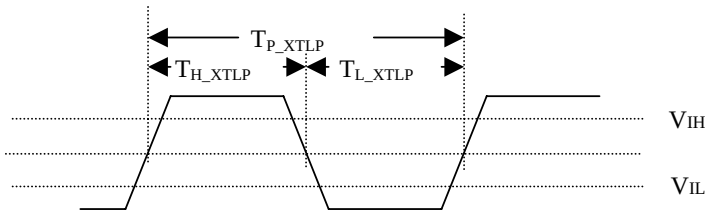
Note: Please read the register 0x000 [16] ChipInitDone to check if the chip has finish initialized process.

6.5 AC specifications

Notice that the following AC timing specifications for output pins are based on CL (Output load) = 50pF.

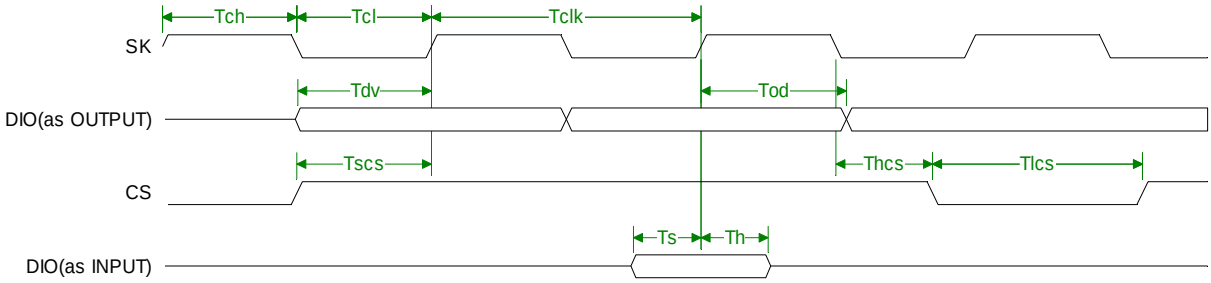
6.5.1 Clock Timing

XTLP



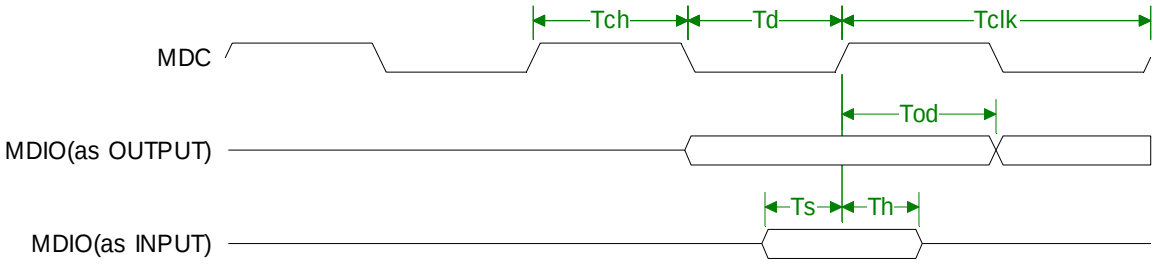
Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTL25P}	XTLP clock cycle time		-	40.0	-	ns
T_{H_XTL25P}	XTLP clock high time		-	20.0	-	ns
T_{L_XTL25P}	XTLP clock low time		-	20.0	-	ns

6.5.2 Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Unit
Tclk	SK clock cycle time	-	1000	-	ns
Tch	SK clock high time	-	500	-	ns
Tcl	SK clock low time	-	500	-	ns
Tdv	DIO output valid to SK rising edge time	500	-	-	ns
Tod	SK rising edge to DIO output delay time	500	-	-	ns
Tscs	CS output valid to SK rising edge time	500	-	-	ns
Thcs	SK falling edge to CS invalid time	510	-	-	ns
Tlcs	Minimum CS low time	2050	-	-	ns
Ts	DIO input setup time	10	-	-	ns
Th	DIO input hold time	30	-	-	ns

6.5.3 Station Management Timing (MDIO)



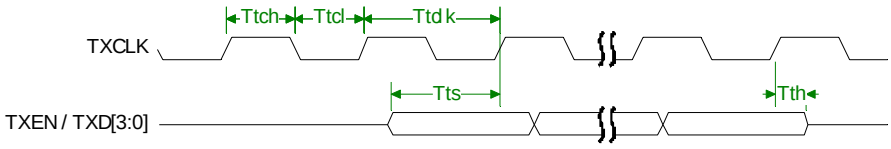
MAC mode with MII: MDC=Output

Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	1000	-	ns
Tch	MDC clock high time	-	500	-	ns
Tcl	MDC clock low time	-	500	-	ns
Tod	MDC clock rising edge to MDIO output delay	0.5	-	-	Tclk
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	30	-	-	ns

PHY/Dual-PHY mode with Reverse MII/RMII: MDC=Input

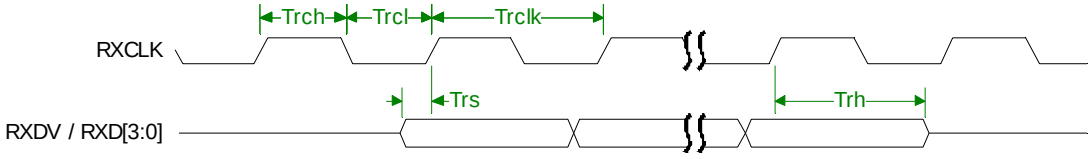
Symbol	Description	Min	Typ	Max	Unit
Tclk	MDC clock cycle time	-	1000	-	ns
Tch	MDC clock high time	-	500	-	ns
Tcl	MDC clock low time	-	500	-	ns
Tod	MDC clock rising edge to MDIO output delay	0	-	300	ns
Ts	MDIO data input setup time	10	-	-	ns
Th	MDIO data input hold time	30	-	-	ns

6.5.4 MII Interface Timing



TXCLK: Port 0 and Port 1 MII Transmit clock. (MII0_TX_CLK, MII1_TX_CLK)
TXD: Port 0 and Port 1 MII TX Data bus include MII0_TXD0, MII0_TXD1, MII0_TXD2, MII0_TXD3, MII1_TXD0, MII1_TXD1, MII1_TXD2, and MII1_TXD3.
TXEN: Port 0 and Port 1 MII Transmit Enable (MII0_TX_EN, MII1_TX_EN)

Symbol	Description	Min	Typ	Max	Unit
Ttclk	TXCLK clock cycle time *1	-	40.0	-	ns
Ttch	TXCLK clock high time *2	-	20.0	-	ns
Ttcl	TXCLK clock low time *2	-	20.0	-	ns
Tts	TXD [3:0], TXEN setup to rising TXCLK	23.0	-	-	ns
Tth	TXD [3:0], TXEN hold from rising TXCLK	7.0	-	-	ns

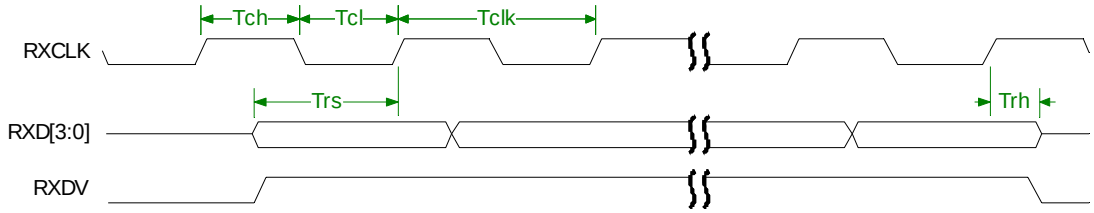


RXCLK: Port 0 and Port 1 MII Receive clock. (MII0_RX_CLK, MII1_RX_CLK)
RXD: Port 0 and Port 1 MII RX Data bus include MII0_RXD0, MII0_RXD1, MII0_RXD2, MII0_RXD3, MII1_RXD0, MII1_RXD1, MII1_RXD2, and MII1_RXD3.
RXDV: Port 0 and Port 1 MII Receive Data Valid (MII0_RX_DV, MII1_RX_DV)

Symbol	Description	Min	Typ	Max	Unit
Trclk	RXCLK clock cycle time *1	-	40.0	-	ns
Trch	RXCLK clock high time *2	-	20.0	-	ns
Trcl	RXCLK clock low time *2	-	20.0	-	ns
Trs	RXD [3:0], RXDV setup to rising RXCLK	5.0	-	-	ns
Trh	RXD [3:0], RXDV hold from rising TXCLK	3.5	-	-	ns

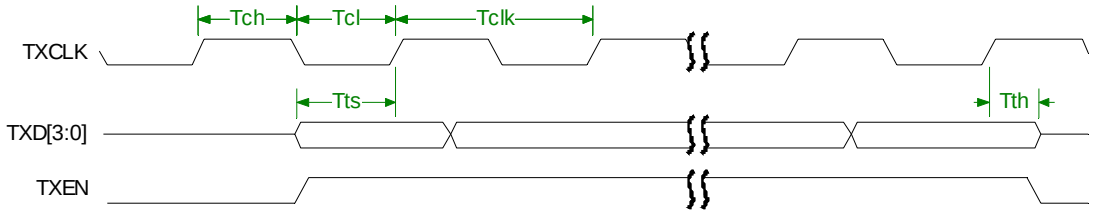
*1: For 10Mbps, the typical value of Ttclk and Trclk shall scale to 400ns.
*2: For 10Mbps, the typical value of Ttch, Ttcl, Trch, and Trcl shall scale to 200ns.

6.5.5 Reverse MII Timing



RXCLK: Port 0 and Port 1 MII Transmit clock. (MII0_RX_CLK, MII1_RX_CLK)
RXD: Port 0 and Port 1 MII Transmit Data bus include MII0_RXD0, MII0_RXD1, MII0_RXD2, MII0_RXD3, MII1_RXD0, MII1_RXD1, MII1_RXD2, and MII1_RXD3.
RXDV: Port 0 and Port 1 MII Transmit Data Valid (MII0_RX_DV, MII1_RX_DV)

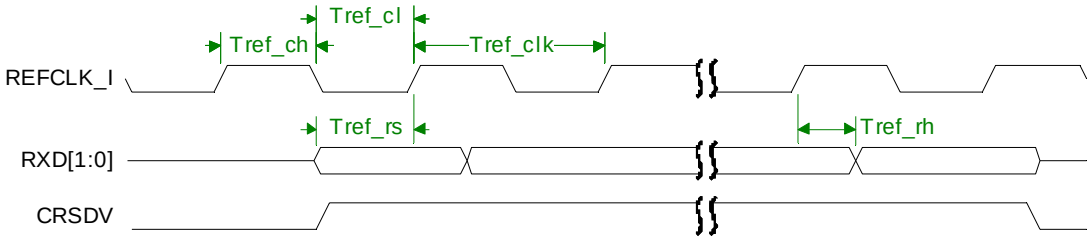
Symbol	Description	Min	Typ	Max	Unit
Tclk	Clock cycle time	-	40.0	-	ns
Tch	Clock high time	-	20.0	-	ns
Tcl	Clock low time	-	20.0	-	ns
Trs	RXD [3:0], RXDV setup to rising RXCLK	10.0	-	-	ns
Trh	RXD [3:0], RXDV hold from rising RXCLK	10.0	-	-	ns



TXCLK: Port 0 and Port 1 MII Receive clock. (MII0_TX_CLK, MII1_TX_CLK)
TXD: Port 0 and Port 1 MII Receive Data bus include MII0_TXD0, MII0_TXD1, MII0_TXD2, MII0_TXD3, MII1_TXD0, MII1_TXD1, MII1_TXD2, and MII1_TXD3.
TXEN: Port 0 and Port 1 MII Receive Data Valid (MII0_TX_EN, MII1_TX_EN)

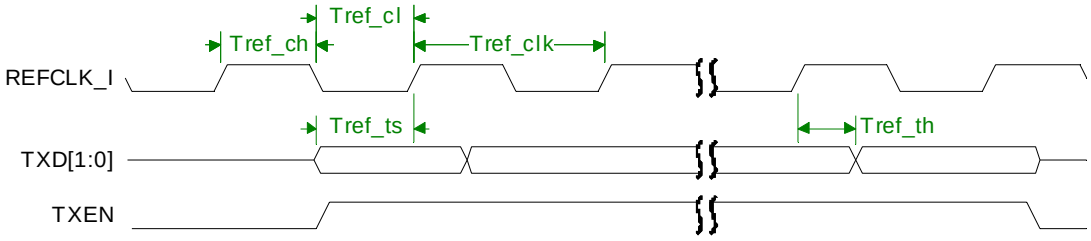
Symbol	Description	Min	Typ	Max	Unit
Tts	TXD [3:0], TXEN setup to rising TXCLK	11.0	-	-	ns
Tth	TXD [3:0], TXEN hold from rising TXCLK	2.0	-	-	ns

6.5.6 RMII and Reverse RMII Timing



RXCLK: Port 0 and Port 1 MII Transmit clock. (MII0_RX_CLK, MII1_RX_CLK)
RXD: Port 0 and Port 1 MII Transmit Data bus include MII0_RXD0, MII0_RXD1, MII1_RXD0, and MII1_RXD1.
RXDV: Port 0 and Port 1 MII Transmit Data Valid (MII0_RX_DV, MII1_RX_DV)

Symbol	Description	Min	Typ	Max	Unit
Tref_clk	Clock cycle time	-	20.0	-	ns
Tref_ch	Clock high time	-	10.0	-	ns
Tref_cl	Clock low time	-	10.0	-	ns
Tref_rs	RXD [1:0], CRSDV setup to rising REFCLK_I	4.0	-	-	ns
Tref_rh	RXD [1:0], CRSDV hold from rising REFCLK_I	2.0	-	-	ns



TXCLK: Port 0 and Port 1 MII Receive clock. (MII0_TX_CLK, MII1_TX_CLK)
TXD: Port 0 and Port 1 MII Receive Data bus include MII0_TXD0, MII0_TXD1, MII1_TXD0, and MII1_TXD1.
TXEN: Port 0 and Port 1 MII Receive Data Valid (MII0_TX_EN, MII1_TX_EN)

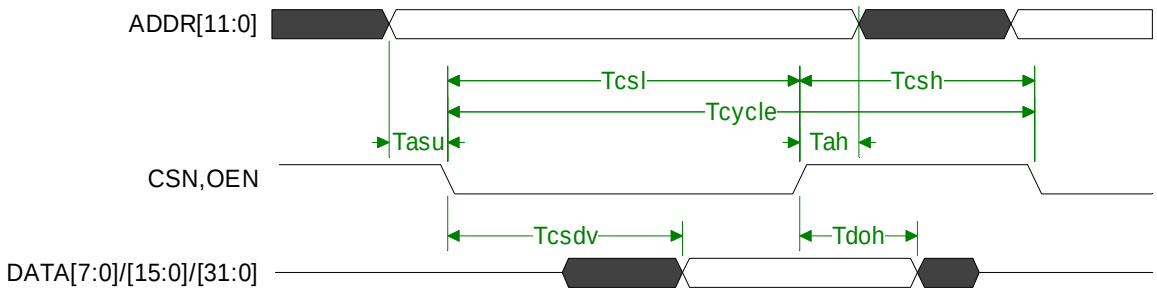
Symbol	Description	Min	Typ	Max	Unit
Tref_ts	TXD [1:0], TXEN setup to rising REFCLK_I	4.0	-	-	ns
Tref_th	TXD [1:0], TXEN hold from rising REFCLK_I	2.0	-	-	ns

6.5.7 CPU Interface Timing

ADDR [11:0]: {CPU_ADDR11, CPU_ADDR10, CPU_ADDR9, CPU_ADDR8, CPU_ADDR7, CPU_ADDR6, CPU_ADDR5, CPU_ADDR4, CPU_ADDR3, CPU_ADDR2, CPU_ADDR1, CPU_ADDR0}

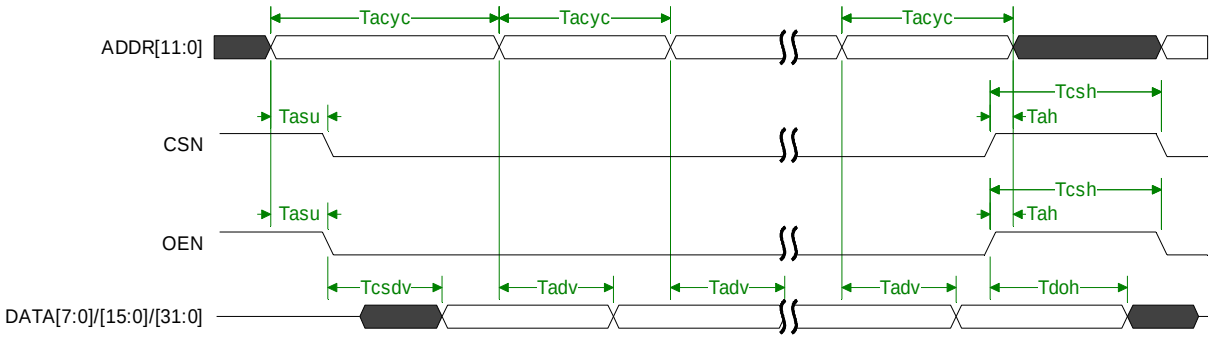
DATA [31:0]: {CPU_DATA31, CPU_DATA30, CPU_DATA29, CPU_DATA28, CPU_DATA27, CPU_DATA26, CPU_DATA25, CPU_DATA24, CPU_DATA23, CPU_DATA22, CPU_DATA21, CPU_DATA20, CPU_DATA19, CPU_DATA18, CPU_DATA17, CPU_DATA16, CPU_DATA15, CPU_DATA14, CPU_DATA13, CPU_DATA12, CPU_DATA11, CPU_DATA10, CPU_DATA9, CPU_DATA8, CPU_DATA7, CPU_DATA6, CPU_DATA5, CPU_DATA4, CPU_DATA3, CPU_DATA2, CPU_DATA1, CPU_DATA0}

CPU Single Read Cycle



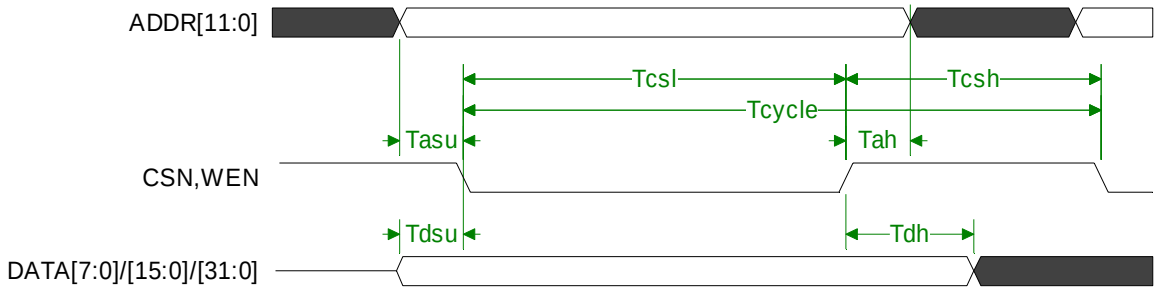
Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	45	-	-	ns
Tcsl	CSN, OEN ASSERT TIME	32	-	-	ns
Tcsh	CSN, OEN DEASSERTION TIME	15	-		ns
Tcsdv	CSN, OEN VALID TO DATA VALID			30	ns
Tasu	ADDRESS SETUP TO CSN, OEN VALID	0			ns
Tah	ADDRESS HOLD TIME	0			ns
Tdoh	DATA OUTPUT HOLD TIME	0			ns

CPU Burst Read Cycle



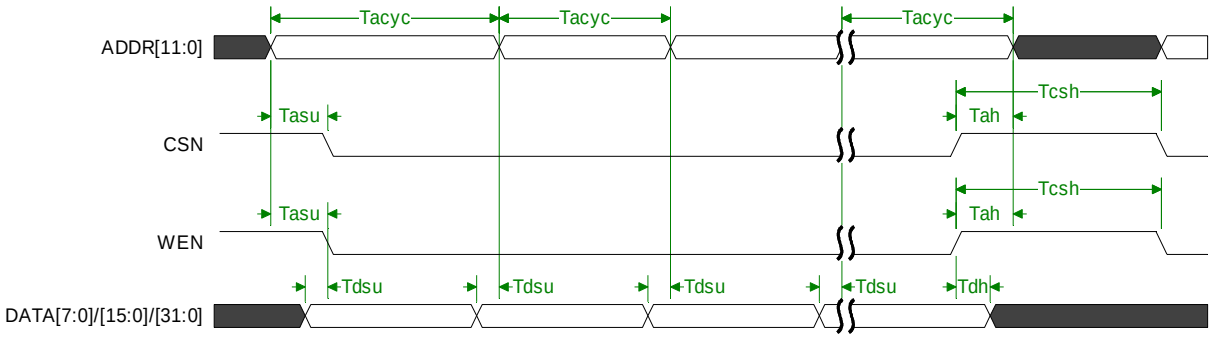
Symbol	Description	Min	Typ.	Max	Units
Tcsh	CSN, OEN DEASSERTION TIME	15			ns
Tcsdv	CSN, OEN VALID TO DATA VALID			30	ns
Tacyc	ADDRESS CYCLE TIME	45			ns
Tasu	ADDRESS SETUP TO CSN, OEN VALID	0			ns
Tadv	ADDRESS STABLE TO DATA VALID			40	ns
Tah	ADDRESS HOLD TIME	0			ns
Tdoh	DATA OUTPUT HOLD TIME	0			ns

CPU Single Write Cycle



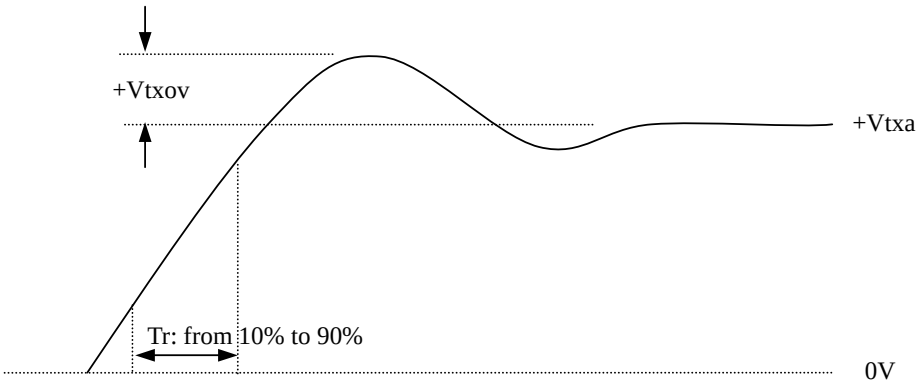
	Description	Min	Typ.	Max	Units
Tasu	ADDRESS SETUP TO CSN, WEN ASSERTION	0	-	-	ns
Tdsu	DATA SETUP TO CSN, WEN ASSERTION	0	-	-	ns
Tcycle	WRITE CYCLE TIME	45	-		ns
Tcsl	CSN, WEN ASSERTION TIME	32	-	-	ns
Tcsh	CSN, WEN DEASSERTION TIME	15			ns
Tah	ADDRESS HOLD TIME	0			ns
Tdh	DATA HOLD TIME	0			ns

CPU Burst Write Cycle



Symbol	Description	Min	Typ.	Max	Units
Tcsh	CSN, WEN DEASSERTION TIME	0	-	-	ns
Tacyc	ADDRESS CYCLE TIME	0	-	-	ns
Tasu	ADDRESS SETUP TO CSN, WEN	45	-		ns
Tah	ADDRESS HOLD TIME	32	-	-	ns
Tdsu	DATA SETUP TO CSN, OEN ASSERTION	15			ns
Tdh	DATA HOLD TIME	0			ns

6.5.8 10/100M Ethernet PHY Interface Timing



10/100M Ethernet PHY Transmitter Waveform and Spec:

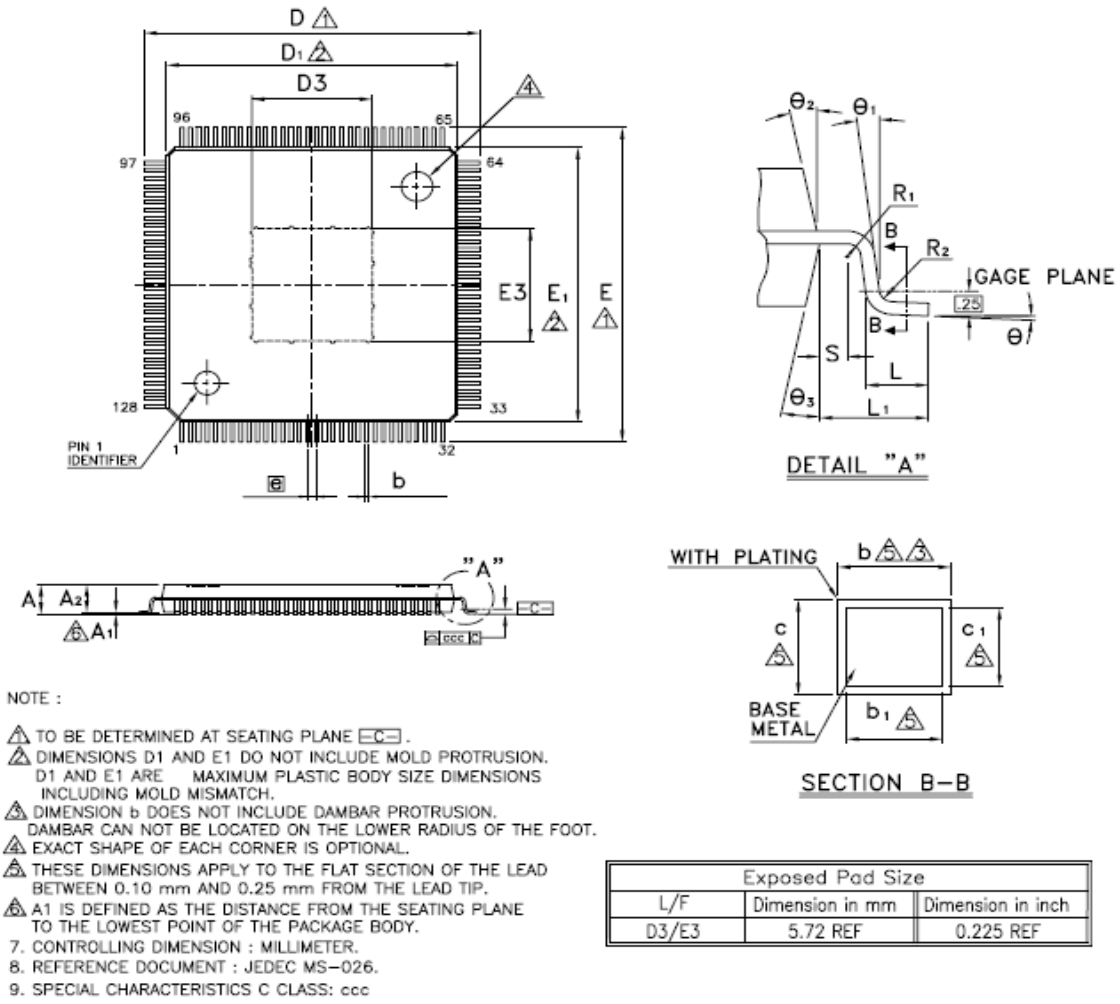
Symbol	Description	Condition	Min	Typ	Max	Units
	Peak-to-peak differential output voltage	10BASE-T mode	4.4	5	5.6	V
Vtxa *2	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2	2.1	V
Tr / Tf	Signal rise / fall time	100BASE-TX mode	3	4	5	ns
	Output jitter	100BASE-TX mode, scrambled idle signal	-	-	1.4	ns
Vtxov	Overshoot	100BASE-TX mode	-	-	5	%

10/100M Ethernet PHY Receiver Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Receiver input impedance		10	-	-	KΩ
	Differential squelch voltage	10BASE-T mode	300	400	500	mV
	Common mode input voltage		2.97	3.3	3.63	V
	Maximum error-free cable length		100	-	-	meter

7 PACKAGE INFORMATION

7.1 The AX88783 128 Pin LQFP/E-PAD Package



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C-.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

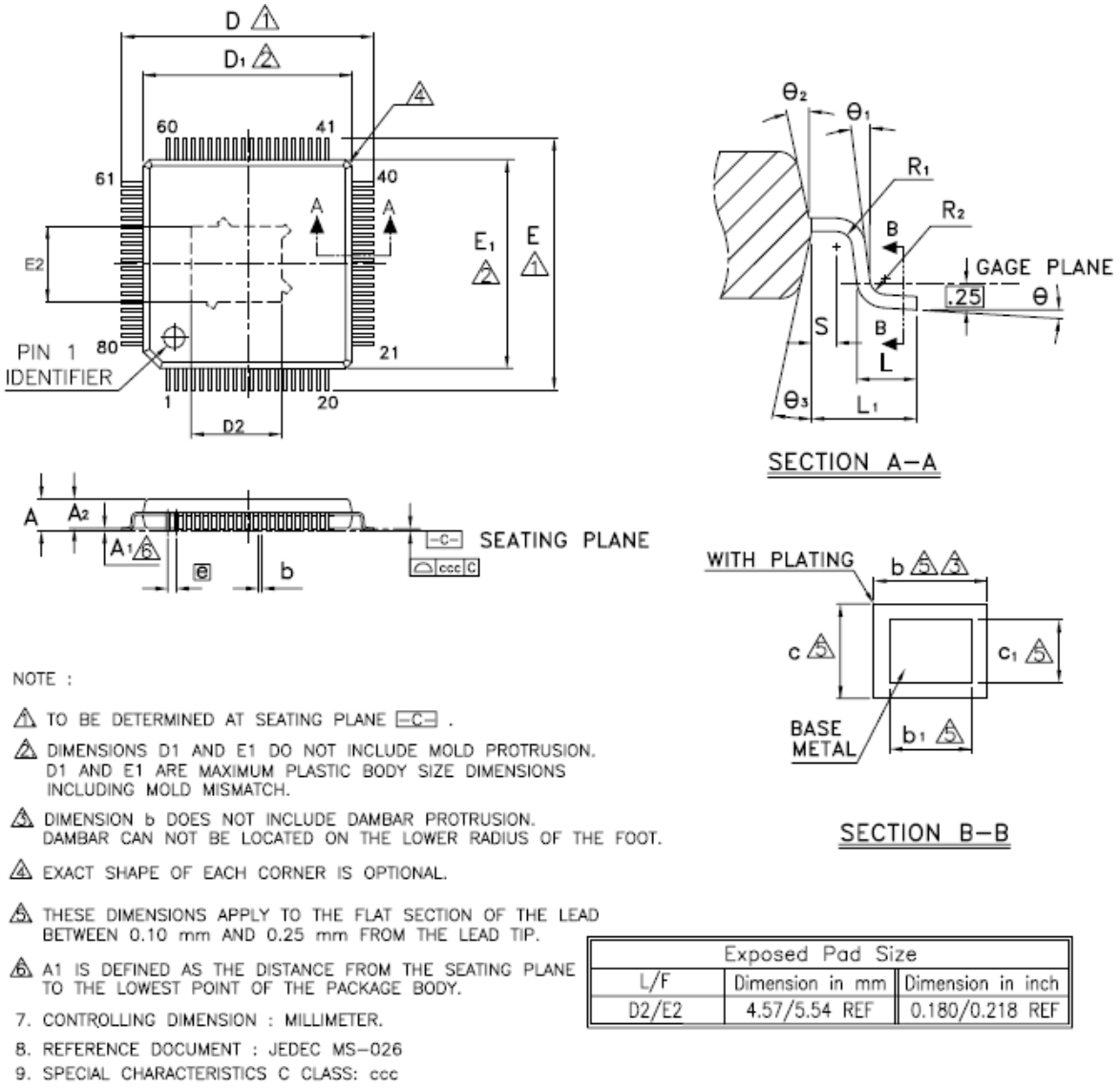
Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D3/E3	5.72 REF	0.225 REF

Exposed Pad (E-PAD) Information:

The AX88783 has an exposed pad to help transfer heat from the silicon wafer to the PCB. This metallic exposed pad should be tied to ground.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		
ccc	0.08			0.003		

7.2 The AX88782 80 Pin LQFP Package



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026
9. SPECIAL CHARACTERISTICS C CLASS: ccc

Exposed Pad Size		
L/F	Dimension in mm	Dimension in inch
D2/E2	4.57/5.54 REF	0.180/0.218 REF

Exposed Pad (E-PAD) Information:

The AX88782 has an exposed pad to help transfer heat from the silicon wafer to the PCB. This metallic exposed pad should be tied to ground.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D_1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E_1	10.00 BSC			0.394 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

8 Ordering Information

Part Number	Description
AX88782 LF	80 PIN, LQFP/E-PAD Package, Commercial Grade 0°C to +70 °C (Green, Lead-Free)
AX88783 LF	128 PIN, LQFP/E-PAD Package, Commercial Grade 0°C to +70 °C (Green, Lead-Free)

Revision History

Revision	Date	Comment
V0.10	2008/04/11	Preliminary Release
V0.20	2009/03/04	*Add MLD Snooping information (3.15) *Add EEPROM information (3.20) *Update pinout information (2.1 ~ 2.3) Rename P0_VCC18D to P0_VCC18A and P1_VCC18D to P1_VCC18A Rename P0_GND18D to P0_VCC18A and P1_GND18D to P1_VCC18A *Add GPIO information (3.21) *Update Power consumption table in 6.4
V1.00	2009/04/30	*Update RMON counter information (5.1.24 and 3.13) Remove unused counter on address 0x12 and 0x13 *Add 3.22 CPU Interface Protocol section *Add thermal characteristics table (6.2) *Add power-saving function description (3.5) *Add IPv6 MLD snooping function (3.15) *Add EEPROM example code (3.20) *Add PHY power-saving control bit (5.1.2) *Add PHY cable-off status information (5.1.3) *Add sniffer register IPv4/IPv6 related information (5.1.9) *Add IO pad pull-up and pull-down control register (5.1.36) *Add Endian Configuration register (5.1.53) *Add GPIO wakeup register (5.1.93) and GPIO control register (5.1.38 ~ 5.1.41) *Add multi-voltage 3.3V, 2.5V and 1.8V I/O support (6.3.1 ~ 6.3.3) *The AX88783 pin 123 MII0_TXD3 need an external pull-down resistor (2.1.2 and 2.1.3) * Change bi-directional IO pad abbreviations to B (2.0) * Add bus mode select table in 2.5 MODE2,1,0 bit description * DATA12 should add a pull-down resistor when configured in 8-bit bus mode (2.3) * Add 50MHz RMII reference clock spec. on 2.1.4 and 2.1.5 MII0_REFCLK 2.2.4 and 2.2.5 MII1_REFCLK pin description.

ASIX Electronics Corporation.

4F, No. 8, Hsin Ann Rd., HsinChu Science Park,
HsinChu, Taiwan, R.O.C.

TEL: 886-3-5799500
FAX: 886-3-5799558

Email: support@asix.com.tw
Web: http://www.asix.com.tw