10/100BASE 3-in-1 PCMCIA Fast Ethernet Controller

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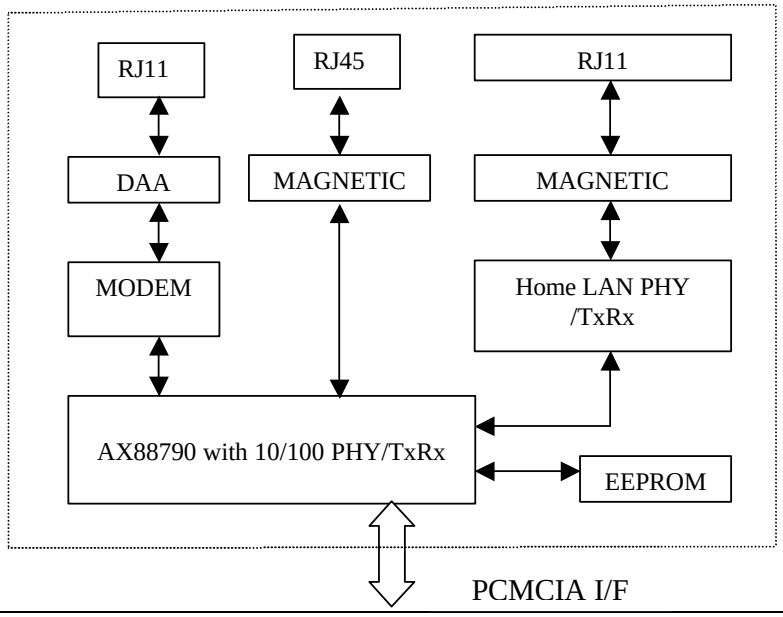
Features

- Highly integrated with embedded 10/100Mbps MAC, PHY and Transceiver
- Compliant with IEEE 802.3/802.3u 100BASE-TX/FX specification
- Single chip PCMCIA bus 10/100Mbps Fast Ethernet MAC Controller
- Embedded 8K * 16 bit SRAM
- NE2000 register level compatible instruction
- Compliant with 16 bit PC Card Standard - February 1995
- Support both 10Mbps and 100Mbps data rate
- Support both full-duplex or half-duplex operation
- Provides FAX/MODEM interface for COMBO AP
- Provides an extra MII port for supporting other media. For example, Home-LAN application
- Support 128/256 bytes EEPROM (used for saving CIS)
- Support automatic loading of Ethernet ID, CIS and Adapter Configuration from EEPROM on power-on initialization
- External and internal loop-back capability
- Support 3 General Purpose Input pins
- Low Power Consumption, typical under 100mA
- 128-pin LQFP low profile package
- 0.25 Micron low power CMOS process. 25MHz Operation, Pure 3.3V operation with 5V I/O tolerance.

Product description

The AX88790 Fast Ethernet Controller is a high performance and highly integrated PCMCIA bus Ethernet Controller with embedded 10/100Mbps PHY/Transceiver and 8K*16 bit SRAM. The AX88790 contains a 16 bit PCMCIA interfaces to host CPU and compliant with PC Card Standard – February 1995. The AX88790 implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard. The AX88790 also provides an extra IEEE802.3u compliant media-independent interface (MII) to support other media applications. Using MII interface, Home LAN PHY type media can be supported. The AX88790 is built in interface to connect FAX/MODEM chipset with parallel bus interface.

Typical System Block Diagram



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1.0 Introduction

1.1 General Description:

The AX88790 provides industrial standard NE2000 registers level compatible instruction set. Various drivers are easy acquired, maintenance and usage with no pain and tears

The AX88790 Fast Ethernet Controller is a high performance and highly integrated PCMCIA bus Ethernet Controller with embedded 10/100Mbps PHY/Transceiver and 8K*16 bit SRAM. The AX88790 contains a 16 bit PCMCIA interfaces to host CPU and compliant with PC Card Standard – February 1995. The AX88790 implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard. The AX88790 also provides an extra IEEE802.3u compliant media-independent interface (MII) to support other media applications. Using MII interface, Home LAN PHY type media can be supported. The AX88790 is also built in interface to connect FAX/MODEM chipset with parallel bus interface.

The main difference between AX88790 and AX88190 are: 1) Embedded packet buffer memory 2) Built-in 10/100Mbps PHY/Transceiver 3) Replace memory I/F with PHY/Transceiver I/F. 4) Fix OE# signal synchronous problem 5) Fix interrupt status can't always clean up problem of AX88190. 6) Add 3 general-purpose input pins.

AX88790 use 128-pin LQFP low profile package, 25MHz operation, and single 3.3V operation with 5V I/O tolerance. The ultra low power consumption is an outstanding feature and enlarges the application field. It is suitable for some power consumption sensitive product like Compact Flash Adapter Card, PDA (Personal Digital Assistant) and Palm size computer …etc.

1.2 AX88790 Block Diagram:

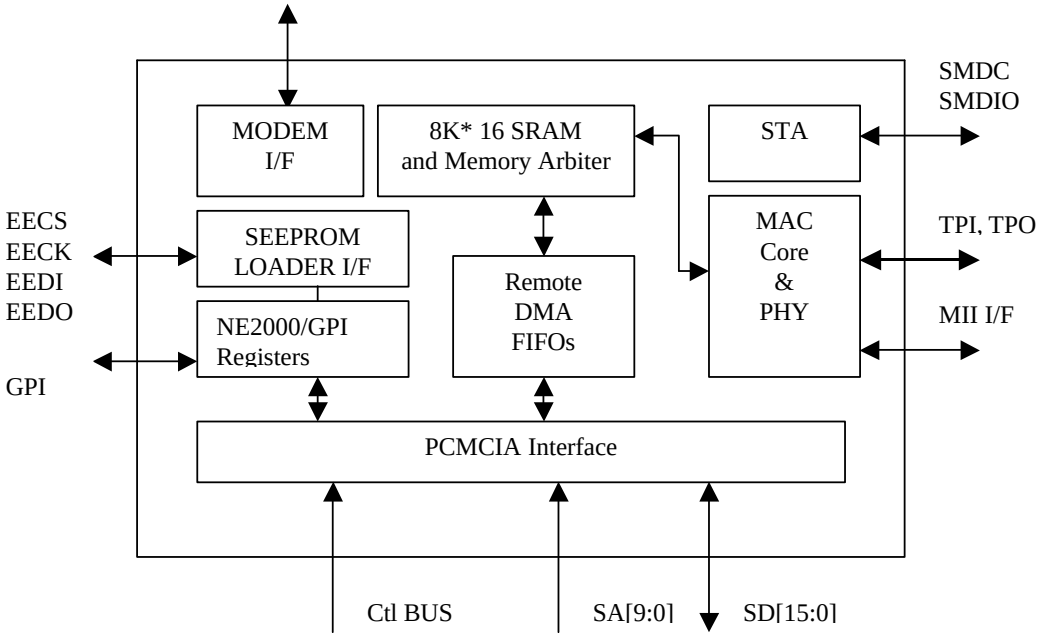

Fig - 1 AX88790 Block Diagram

1.3 AX88790 Pin Connection Diagram

The AX88790 is housed in the 128-pin plastic light quad flat pack. See Fig - 2 AX88790 Pin Connection Diagram.

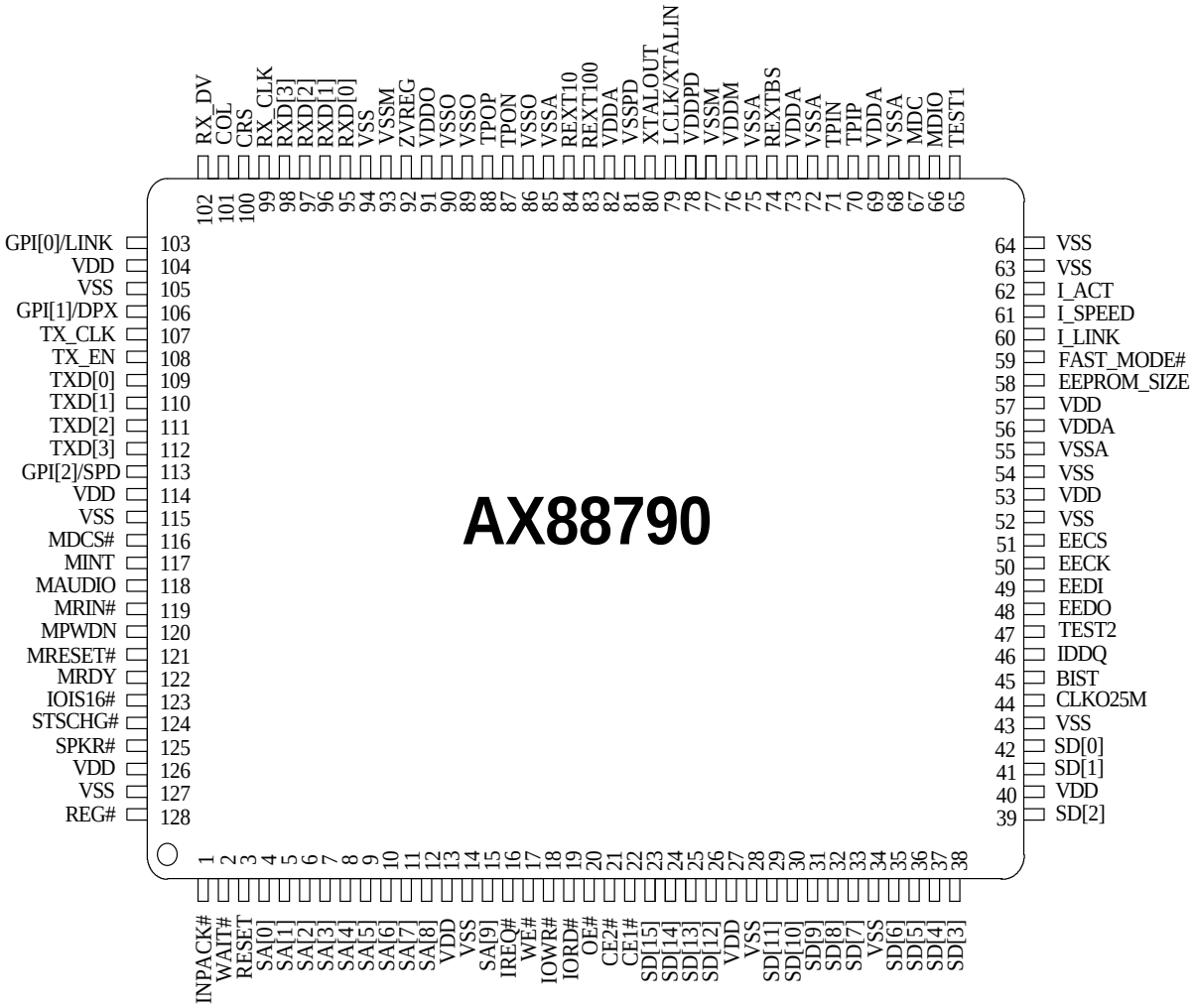

Fig - 2 AX88790 Pin Connection Diagram

2.0 Signal Description

The following terms describe the AX88790 pin-out:
All pin names with the "#" suffix are asserted low.
The following abbreviations are used in following Tables.

I	**Input**	**PU**	**Pull Up**
O	**Output**	**PD**	**Pull Down**
I/O	**Input/Output**	**P**	**Power Pin**
OD	**Open Drain**		

2.1 PCMCIA Bus Interface Signals Group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
SA[9:0]	I/PD	15, 12 – 4	System Address: Signals SA[9:0] are address bus input lines which enable direct address of up to 2K memory and I/O spaces on card.
SD[15:0]	I/O/PD	23 – 26, 29 – 33, 35 – 39, 41 – 42	System Data Bus: Signals SD[15:0] constitute the bi-directional data bus.
IREQ#	O	16	Interrupt Request: IREQ# is asserted to indicate the host system that the PC Card device requires host software service.
WAIT#	O	2	Wait: This signal is set low to insert wait states during Remote DMA transfer.
REG#	I/PU	128	Attribute Memory and I/O Space Select: When the REG# signal is asserted, access is limited to Attribute Memory and to the I/O space.
IORD#	I/PU	19	I/O Read: The host asserts IORD# to read data from AX88790 I/O space.
IOWR#	I/PU	18	I/O Write: The host asserts IOWR# to write data into AX88790 I/O space.
OE#	I/PU	20	Output Enable : The OE# line is used to gate Memory Read data from memory on PC Card
WE#	I/PU	17	Write Enable: The WE# signal is used for strobing Memory Write data into the memory on PC Card.
IOIS16#	O	123	I/O is 16 Bit Port: The IOIS16# is asserted when the address at the socket corresponds to an I/O address to which the card responds, and the I/O port addressed is capable of 16-bit access.
INPACK#	O	1	Input Port Acknowledge: The signal is asserted when the AX88790 is selected and can respond to and I/O read cycle at the address on the address bus.
CE1#-CE2#	I/PU	22, 21	Card Enable : The CE1# enables even numbered address bytes and CE2# enables odd numbered address bytes
STSCHG#	O	124	Battery Voltage Detect 1 / Status Change
SPKR#	O	125	Battery Voltage Detect 2 / Audio speaker out

Tab - 1 PCMCIA bus interface signals group

2.2 EEPROM Signals Group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
EECS	O	51	EEPROM Chip Select: EEPROM chip select signal.
EECK	O/PD	50	EEPROM Clock: Signal connected to EEPROM clock pin.
EEDI	O	49	EEPROM Data In: Signal connected to EEPROM data input pin.
EEDO	I/PU	48	EEPROM Data Out: Signal connected to EEPROM data output pin.

Tab - 2 EEPROM bus interface signals group

2.3 MII interface signals group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
RXD[3:0]	I/PU	98 – 95	Receive Data: RXD[3:0] is driven by the PHY synchronously with respect to RX_CLK.
CRS	I/PD	100	Carrier Sense: Asynchronous signal CRS is asserted by the PHY when either transmit or receive medium is non-idle.
RX_DV	I/PD	102	Receive Data Valid: RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:0].
RX_ER	(Omit)	No Support	Receive Error: RX_ER is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected.
RX_CLK	I/PU	99	Receive Clock: RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD[3:0] and RX_ER signals from the PHY to the MII port.
COL	I/PD	101	Collision: this signal is driven by PHY when collision is detected.
TX_EN	O	108	Transmit Enable: TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
TXD[3:0]	O	112 – 109	Transmit Data: TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] are accepted for transmission by the PHY.
TX_CLK	I/PU	107	Transmit Clock: TX_CLK is a continuous clock from PHY. It provides the timing reference for the transfer of the TX_EN and TXD[3:0] signals from the MII port to the PHY.
MDC	O/PU	67	Station Management Data Clock: The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock. MDC is a 2.5MHz frequency clock output.
MDIO	I/O/PU	66	Station Management Data Input / Output: Serial data input/output transfers from/to the PHYs. The transfer protocol conforms to the IEEE 802.3u MII specification.

Tab - 3 MII interface signals group

2.4 10/100Mbps Twisted-Pair Interface pins group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
TPIP	I	70	Received Data. Positive differential received 125M baud MLT3 or 10M baud Manchester data from magnetic.
			Fiber-Optic Data Input. Positive differential received 125M baud pseudo-ECL data from fiber transceiver.
TPIN	I	71	Received Data. Negative differential received 125M baud MLT3 or 10M baud Manchester data from magnetic.
			Fiber-Optic Data Input. Negative differential received 125M baud pseudo-ECL data from fiber transceiver.
TPOP	O	88	Transmit Data. Positive differential transmit 125M baud MLT3 or 10M baud Manchester data to magnetic.
			Fiber-Optic Data Output. Positive differential transmit 125M baud pseudo-ECL compatible data to fiber transceiver.
TPON	O	87	Transmit Data. Negative differential transmit 125M baud MLT3 or 10M baud Manchester data to magnetic.
			Fiber-Optic Data Output. Negative differential transmit 125M baud pseudo-ECL compatible data to fiber transceiver.
REXT10	I	84	Current Setting 10Mbits/s. An external resistor 20.1k ohm is placed from this signal to ground to set the 10Mbits/s TP driver transmit output level.
REXT100	I	83	Current Setting 100Mbits/s. An external resistor 2.49k ohm is placed from this signal to ground to set the 100Mbits/s TP driver transmit output level.
REXTBS	I	74	External Bias Resistor. Band Gap Reference for the Receive Channel. Connect this signal to a 24.9k ohm +/- 1 percent resistor to ground. The parasitic load capacitance should be less than 15 pF.

Tab - 4 10/100Mbps Twisted-Pair Interface pins group

2.5 Built-in PHY LED indicator pins group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
I_ACT or I_FULL/COL	O	62	Active Status: When I_OP is logic 1. If there is activity, transmit or receive, on the line occurred, the output will be driven low for 0.67 sec and then driven high at least 0.67 sec. Full-Duplex/Collision Status. When I_OP is logic 0. If this signal is low, it indicates full-duplex link established, and if it is high, then the link is in half-duplex mode. When in half-duplex and collision occurrence, the output will be driven low for 0.67 sec and driven high at least 0.67 sec.
I_SPEED	O	61	Speed Status: If this signal is low, it indicates 100Mbps, and if it is high, then the speed is 10Mbps.
I_LINK Or I_LK/ACT	O	60	Link Status: When I_OP is logic 1. If this signal is low, it indicates link, and if it is high, then the link is fail. Link Status/Active: When I_OP is logic 0. If this signal is low, it indicates link, and if it is high, then the link is fail. When in link status and line activity occurrence, the output will be driven low for 0.67 sec and driven high at least 0.67 sec.

Tab - 5 Built-in PHY LED indicator pins group

2.6 Modem interface pins group

Signal Name	Type	Pin No.	Description
MRDY	I/PU	122	Modem Ready: MRDY low indicates that modem is initializing the modem after reset signal asserted or the modem is at SLEEP/STOP mode.
MRESET#	O	121	Modem Reset: This signal asserts low to reset the modem chipset.
MDCS#	O/PU	116	Modem Chip Select: This signal connected to modem chip select pin.
MPWDN	O/PU	120	Modem Power Down: Rockwell modem chipset, this signal asserts low to let modem chipset into power down mode. AT&T modem chipset, this signal asserts high to let modem chipset into power down mode.
MINT	I/PD	117	Modem Interrupt: This signal driven by modem chipset to active interrupt.
MRIN#	I/PU	119	Ring Input: This signal is driven by DAA's ring detect circuit. When a telephone-ringing signal is being received.
MAUDIO	I/PU	118	Modem Audio: This signal is passed to PCMCIA interface via SPKR.

Tab - 6 Modem interface signals group

2.7 General Purpose I/O pins group

Signal Name	Type	Pin No.	Description
GPI[2]/SPD	I/PU	113	Read register offset 17h bit 6 value reflects this input value.
GPI[1]/DPX	I/PU	106	Read register offset 17h bit 5 value reflects this input value.
GPI[0]/LINK	I/PU	103	Read register offset 17h bit 4 value reflects this input value.

Tab – 7 General Purposes I/O pins group

2.8 Miscellaneous pins group

SIGNAL	TYPE	PIN NO.	DESCRIPTION
LCLK/XTALIN	I	79	CMOS Local Clock: Typical a 25Mhz clock, +/- 100 PPM, 40%-60% duty cycle. The signal not supports 5 Volts tolerance (See application note also) Crystal Oscillator Input: Typical a 25Mhz crystal, +/- 25 PPM can be connected across XTALIN and XTALOUT.
XTALOUT	O	80	Crystal Oscillator Output: Typical a 25Mhz crystal, +/- 25 PPM can be connected across XTALIN and XTALOUT. If a single-ended external clock (LCLK) is connected to XTALIN, the crystal output pin should be left floating.
CLKO25M	O	44	Clock Output: This clock is source from LCLK/XTALIN.
RESET	I/PU	3	Reset Reset is active high then place AX88790 into reset mode immediately. During falling edge the AX88790 loads the power on setting data. And, after the falling edge the AX88790 loads the EEPROM data.
TEST[2:1]	I/PD	47, 65	Test Pins **:** Active high These pins are just for test mode setting purpose only. Must be pull down or keep no connection when normal operation.
IDDQ	I	46	For test only. Must be pulled down at normal operation.
BIST	I/PD	45	For test only. Must be pulled down or keep no connection when normal operation.
FAST_MODE#	I/PU	59	FAST_MODE **:** Active LOW The pin is just for test mode only. Must be pulled high or keep no connection when normal operation.
EEPROM_SIZE	I/PU	58	EEPROM SIZE = 0: 93C46 type 128 byte EEPROM is used. EEPROM SIZE = 1: 93C56 type 256 byte EEPROM is used.
ZVREG	O	92	This sets the common mode voltage for 10Base-T and 100Base-TX modes. It should be connected to the center tap of the transmit side of the transformer
VDD	P	13, 27, 40, 53, 57, 104, 114, 126	Power Supply: +3.3V DC.
VSS	P	14, 28, 34, 43, 52, 54, 63, 64, 94, 105,115, 127	Power Supply: +0V DC or Ground.
VDDA	P	56, 69, 73, 82	Power Supply for Analog Circuit: +3.3V DC.
VSSA	P	55, 68, 72, 75, 85,	Power Supply for Analog Circuit: +0V DC or Ground.
VDDM	P	76	Powers the analog block around the transmit/receive area. This should be connected to VDDA: +3.3V DC.
VSSM	P	77, 93	Powers the analog block around the transmit/receive area. This should be connected to VSSA: +0V DC or Ground Power.
VDDPD	P	78	The Phase Detector (or PLL) power. This should be isolated with other power: +3.3V DC.
VSSPD	P	81	The Phase Detector (or PLL) power. This should be isolated with other power: +0V DC or Ground.
VDDO	P	91	Power Supply for Transceiver Output Driver: +3.3V DC.
VSSO	P	86, 89, 90	Power Supply for Transceiver Output Driver: +0V DC or Ground.

Tab – 8 Miscellaneous pins group

2.9 Power on configuration setup signals cross reference table

Signal Name	Share with	Description
MPD_SET	MPWDN	MPD_SET = 0: MPWDN pin active high. MPD_SET = 1: MPWDN pin active low. (default)
PPD_SET	EECK	PPD_SET = 0: Internal PHY in normal mode. (default) PPD_SET = 1: Internal PHY in power down mode.
I_OP	MDCS#	LED Indicator Option: Selection of LED display mode. I_OP = 0: I_LK/ACT, I_SPEED and I_FULL/COL LED display mode. I_OP = 1: I_LINK, I_SPEED and I_ACT LED display mode. (default)

Tab - 9 Power on Configuration Setup Table

3.0 Memory and I/O Mapping

There are four memories or I/O mapping used in AX88790.

1. EEPROM Memory Mapping
2. Attribute Memory Mapping
3. I/O Mapping
4. Local Memory Mapping

3.1 EEPROM Memory Mapping

EEPROM OFFSET	HIGH BYTE	LOW BYTE
00H	RESERVED	WORD COUNT
01H	CFH	CFL
02H	NODE-ID1	NODE ID 0
03H	NODE ID 3	NODE ID 2
04H	NODE ID 5	NODE ID 4
05H	CHECKSUM	RESERVED
06H – 10H	RESERVED	RESERVED
10H – FFH	CIS	CIS

Tab – 10 EEPROM Memory Mapping

Note: bit 3 register of LCOR in AX88190 is replaced by bit 0 of CFL in AX88790
Bit 0 of CFL: Enable Power Down mode
This bit is set to 1; the LAN will go into power down mode. At power down mode AX88790 will disable MAC transmitting and receiving operation. But the host interface will not be affected.

3.2 Attribute Memory Mapping

ATTRIBUTE MEMORY OFFSET	CONTENTS
0000H 03BFH	CIS
03C0H	LCOR
03C2H	LCCSR
03C4H	-
03C6H	-
03CAH	LIOBASE0
03CCH	LIOBASE1
03CEH 03DFH	RESERVED
03E0H	MCOR
03E2H	MCCSR
03E4H	-
03E6H	-
03EAH	MIOBASE0
03ECH	MIOBASE1
03EEH 03FFH	RESERVED

Tab – 11 Attribute Memory Mapping

3.3 I/O Mapping

SYSTEM I/O OFFSET	FUNCTION
0000H 001FH	MAC CORE REGISTER

Tab – 12 I/O Address Mapping

3.4 SRAM Memory Mapping

OFFSET	FUNCTION
0000H 03BFH	CIS *1
03C0H	LCOR *1
03C2H	LCCSR *1
03C4H	-
03C6H	-
03CAH	LIOBASE0 *1
03CCH	LIOBASE1 *1
03CEH 03DFH	RESERVED
03E0H	MCOR *1
03E2H	MCCSR *1
03E4H	-
03E6H	-
03EAH	MIOBASE0 *1
03ECH	MIOBASE1 *1
03EEH 03FFH	RESERVED
0400H	NODE ID 0
0401H	NODE ID 1
0402H	NODE ID 2
0403H	NODE ID 3
0404H	NODE ID 4
0405H	NODE ID 5
0406H 07FFH	RESERVED
4000H 7FFFH	8K X 16 SRAM BUFFER

Tab – 13 Local Memory Mapping

4.0 Registers Operation

There are four register sets in AX88790:

The PCMCIA function configuration registers of LAN.
The PCMCIA function configuration registers of MODEM.
The MAC core register.
The embedded PHY registers.

4.1 PCMCIA Function Configuration Register Set of LAN

REGISTER	NAME	OFFSET
LCOR	CONFIGURATION OPTION REGISTER	3C0H
LCSR	CONFIGURATION AND STATUS REGISTER	3C2H
LIOBASE0	I/O BASED REGISTER 0	3CAH
LIOBASE1	I/O BASED REGISTER 1	3CCH

Tab – 14 PCMCIA Function Configuration Register Mapping of LAN

4.1.1 Configuration Option Register of LAN (LCOR) Offset 3C0H (Read/Write)

FIELD	R/W/C	DESCRIPTION
7	R/W	Software Reset Assert this bit will reset the LAN function of AX88790. Return a 0 to this bit will leave the LAN function of AX88790 in a post-reset state as same as that following hardware reset. The value of this bit is 0 at power-on.
6	R/W	Level IRQ This bit should be set to 1; the AX88790 always generates Level Mode Interrupt.
5:0	R/W	Function Configuration Index These six bits are used to indicate entry of the card configuration table locate in the CIS. The default value is 0 . On multifunction PC Card, Bit 5, Bit 4, Bit 3 : MODEM I/O base registers Bit 5 Bit 4 Bit 3 LAN I/O base MODEM I/O base 0 0 0 300H Decided by MIOBASE registers 0 0 1 320H 2f8H 0 1 0 340H 3e8H 0 1 1 360H 2e8H 1 0 0 380H Decided by MIOBASE registers 1 0 1 200H 2f8H 1 1 0 220H 3e8H 1 1 1 240H 2e8H Bit 2 : Enable IREQ# Routing If bit 0 of LCOR is set to 0, this bit is ignored. If bit 0 of LCOR is set to 1 and this bit is set to 1, the LAN will generate interrupt request via IREQ# signal. If this bit is set to 0, the LAN will not generate interrupt request via IREQ# line. Bit 1 : Enable Base and Limit Registers If bit 0 of LCOR is set to 0, this bit is ignored. If bit 0 of LCOR is set to 1 and this bit is set to 1,only I/O addresses that are qualified by the Base and Limit registers are passed to LAN function. If this bit is set to 0,all I/O addresses are passed to LAN function. Bit 0 : Enable Function If this bit is set to 0, the LAN function is disabled. If this bit is set to 1, the LAN function is enabled.

4.1.2 Configuration and Status Register of LAN (LCSR) Offset 3C2H (Read/Write)

FIELD	R/W/C	DESCRIPTION
7:3	-	Reserved
2	R/W	PPwrDwn : PHY power down setting While this bit set to 1, AX88790 will force embedded PHY into power down mode. As for PPWDN is active high or active low. Please refer section 2.9 Power on configuration setup signal cross-reference table. Note: The master control of Power Down mode is place on Bit 0 of CFL. If user want to enable power down mode, must set the relative bit of EEPROM that map to bit 0 of CFL register to logic 1. When this bit is set to 1, the LAN will go into power down mode. At power down mode AX88790 will disable MAC transmitting and receiving operation. But the host interface will not be affected.
1	R	Intr: Interrupt Request The LAN function will set this bit to 1 when it need interrupt service and set it to 0 when it is not request interrupt service.
0	R	IntrAck: Interrupt Acknowledge This bit will be 0. The Intr will reflect the status of interrupt requesting.

4.1.3 I/O Base Register 0/1 of LAN (LIOBASE0/1) Offset 3CAH/3CCH (Read/Write)

The I/O Base registers (LIOBASE0 and LIOBASE1) determine the base address of the I/O range used to access the LAN specific registers (MAC Core Registers).

I/O Base Register 0

FIELD	R/W/C	DESCRIPTION
7:0	R/W	Base I/O address bit 7 – 0.

I/O Base Register 1

FIELD	R/W/C	DESCRIPTION
7:0	R/W	Base I/O address bit 15 – 8.

4.2 PCMCIA Function Configuration Register Set of MODEM

REGISTER	NAME	OFFSET
MCOR	CONFIGURATION OPTION REGISTER	3E0H
MCSR	CONFIGURATION AND STATUS REGISTER	3E2H
MIOBASE0	I/O BASED REGISTER 0	3EAH
MIOBASE1	I/O BASED REGISTER 1	3ECH

Tab – 15 PCMCIA Function Configuration Register Mapping of MODEM

4.2.1 Configuration Option Register of MODEM (MCOR) Offset 3E0H (Read/Write)

FIELD	R/W/C	DESCRIPTION
7	R/W	Software Reset Assert this bit will reset the MODEM function of AX88790. Return a 0 to this bit will leave the MODEM function of AX88790 in a post-reset state as same as that following hardware reset. The value of this bit is 0 at power-on.
6	R/W	Level IRQ This bit should be set to 1; the AX88790 always generates Level Mode Interrupt.
5:0	R/W	Function Configuration Index These six bits are used to indicate entry of the card configuration table locate in the CIS. The default value is 0 . On multifunction PC Card, Bit 5, Bit4 : Reserved Bit 3 : MINT route to STSCHG# If bit 0 of MCOR is set to 0, this bit is ignored. If both bit 0 and bit 2 of MCOR are set to 1 and this bit is set to 1, the MODEM will route interrupt request to STSCHG# signal. If this bit is set to 0, the MODEM will generate interrupt request via IREQ# line. Bit 2 : MINT route to IREQ# (Enable IREQ# Routing) If bit 0 of MCOR is set to 0, this bit is ignored. If bit 0 of MCOR is set to 1 and this bit is set to 1, the MODEM will generate interrupt request via IREQ# signal. If this bit is set to 0, the MODEM will not generate interrupt request via IREQ# line. Bit 1 : Enable Base and Limit Registers If bit 0 of MCOR is set to 0, this bit is ignored. If bit 0 of MCOR is set to 1 and this bit is set to 1,only I/O addresses that are qualified by the Base and Limit registers are passed to MODEM function. If this bit is set to 0,all I/O addresses are passed to LAN function. Bit 0 : Enable Function If this bit is set to 0, the MODEM function is disabled. If this bit is set to 1, the MODEM function is enabled.

4.2.2 Configuration and Status Register of MODEM (MCSR) Offset 3E2H (Read/Write)

FIELD	R/W/C	DESCRIPTION
7:3	-	Reserved
2	R/W	MPwrDwn : Modem power down setting While this bit set to 1, MPWDN pin (pin 116) will be active to force modem chip into power down mode. As for MPWDN is active high or active low. Please refer section 2.7 Power on configuration setup signal cross-reference table.
1	R	Intr: Interrupt Request The LAN function will set this bit to 1 when it need interrupt service and set it to 0 when it is not request interrupt service.
0	R	IntrAck: Interrupt Acknowledge This bit will be 0. The Intr will reflect the status of interrupt requesting.

4.2.3 I/O Base Register 0/1 of MODEM (MIOBASE0/1) Offset 3EAH/3ECH (Read/Write)

The I/O Base registers (MIOBASE0 and MIOBASE1) determine the base address of the I/O range used to access the MODEM specific registers.

I/O Base Register 0

FIELD	R/W/C	DESCRIPTION
7:0	R/W	Base I/O address bit 7 – 0.

I/O Base Register 1

FIELD	R/W/C	DESCRIPTION
7:0	R/W	Base I/O address bit 15 – 8.

4.3 MAC Core Registers

All registers of MAC Core are 8-bit wide and mapped into pages which are selected by PS (Page Select) in the Command Register.

PAGE 0 (PS1=0,PS0=0)

OFFSET	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Page Start Register (PSTART)	Page Start Register (PSTART)
02H	Page Stop Register (PSTOP)	Page Stop Register (PSTOP)
03H	Boundary Pointer (BNRY)	Boundary Pointer (BNRY)
04H	Transmit Status Register (TSR)	Transmit Page Start Address (TPSR)
05H	Number of Collisions Register (NCR)	Transmit Byte Count Register 0 (TBCR0)
06H	Current Page Register (CPR)	Transmit Byte Count Register 1 (TBCR1)
07H	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
08H	Current Remote DMA Address 0 (CRDA0)	Remote Start Address Register 0 (RSAR0)
09H	Current Remote DMA Address 1 (CRDA1)	Remote Start Address Register 1 (RSAR1)
0AH	Reserved	Remote Byte Count 0 (RBCR0)
0BH	Reserved	Remote Byte Count 1 (RBCR1 0
0CH	Receive Status Register (RSR)	Receive Configuration Register (RCR)
0DH	Frame Alignment Errors (CNTR0)	Transmit Configuration Register (TCR)
0EH	CRC Errors (CNTR1)	Data Configuration Register (DCR)
0FH	Missed Packet Errors (CNTR2)	Interrupt Mask Register (IMR)
10H 11H	Data Port	Data Port
12H	IFGS1	IFGS1
13H	IFGS2	IFGS2
14H	MII/EEPROM Access	MII/EEPROM Access
15H	Test Register	Test Register
16H	Inter-frame Gap (IFG)	Inter-frame Gap (IFG)
17H	GPI	GPOC
18H - 1EH	Reserved	Reserved
1FH	Reset	Reserved

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PAGE 1 (PS1=0,PS0=1)

OFFSET	READ	WRITE
00H	Command Register (CR)	Command Register (CR)
01H	Physical Address Register 0 (PARA0)	Physical Address Register 0 (PAR0)
02H	Physical Address Register 1 (PARA1)	Physical Address Register 1 (PAR1)
03H	Physical Address Register 2 (PARA2)	Physical Address Register 2 (PAR2)
04H	Physical Address Register 3 (PARA3)	Physical Address Register 3 (PAR3)
05H	Physical Address Register 4 (PARA4)	Physical Address Register 4 (PAR4)
06H	Physical Address Register 5 (PARA5)	Physical Address Register 5 (PAR5)
07H	Current Page Register (CPR)	Current Page Register (CPR)
08H	Multicast Address Register 0 (MAR0)	Multicast Address Register 0 (MAR0)
09H	Multicast Address Register 1 (MAR1)	Multicast Address Register 1 (MAR1)
0AH	Multicast Address Register 2 (MAR2)	Multicast Address Register 2 (MAR2)
0BH	Multicast Address Register 3 (MAR3)	Multicast Address Register 3 (MAR3)
0CH	Multicast Address Register 4 (MAR4)	Multicast Address Register 4 (MAR4)
0DH	Multicast Address Register 5 (MAR5)	Multicast Address Register 5 (MAR5)
0EH	Multicast Address Register 6 (MAR6)	Multicast Address Register 6 (MAR6)
0FH	Multicast Address Register 7 (MAR7)	Multicast Address Register 7 (MAR7)
10H 11H	Data Port	Data Port
12H	Inter-frame Gap Segment 1 IFGS1	Inter-frame Gap Segment 1 IFGS1
13H	Inter-frame Gap Segment 2 IFGS2	Inter-frame Gap Segment 2 IFGS2
14H	MII/EEPROM Access	MII/EEPROM Access
15H	Test Register	Test Register
16H	Inter-frame Gap (IFG)	Inter-frame Gap (IFG)
17H	GPI	GPOC
18H - 1EH	Reserved	Reserved
1FH	Reset	Reserved

Tab - 17 Page 1 of MAC Core Registers Mapping

4.3.1 Command Register (CR) Offset 00H (Read/Write)

FIELD	NAME	DESCRIPTION
7:6	PS1,PS0	PS1,PS0 : Page Select The two bits selects which register page is to be accessed. PS1 PS0 0 0 page 0 0 1 page 1
5:3	RD2,RD1,RD0	RD2,RD1,RD0 : Remote DMA Command These three encoded bits control operation of the Remote DMA channel. RD2 could be set to abort any Remote DMA command in process. RD2 is reset by AX88790 when a Remote DMA has been completed. The Remote Byte Count should be cleared when a Remote DMA has been aborted. The Remote Start Address is not restored to the starting address if the Remote DMA is aborted. RD2 RD1 RD0 0 0 0 Not allowed 0 0 1 Remote Read 0 1 0 Remote Write 0 1 1 Not allowed 1 X X Abort / Complete Remote DMA
2	TXP	TXP : Transmit Packet This bit could be set to initiate transmission of a packet
1	START	START : This bit is used to active AX88790 operation.
0	STOP	STOP : Stop AX88790 This bit is used to stop the AX88790 operation.

4.3.2 Interrupt Status Register (ISR) Offset 07H (Read/Write)

FIELD	NAME	DESCRIPTION
7	RST	Reset Status : Set when AX88790 enters reset state and cleared when a start command is issued to the CR. Writing to this bit is no effect.
6	RDC	Remote DMA Complete Set when remote DMA operation has been completed
5	CNT	Counter Overflow Set when MSB of one or more of the Tally Counters has been set.
4	OVW	Over Write: Set when receive buffer ring storage resources have been exhausted.
3	TXE	Transmit Error Set when packet transmitted with one or more of the following errors ■ Excessive collisions ■ FIFO Under-run
2	RXE	Receive Error Indicates that a packet was received with one or more of the following errors CRC error Frame Alignment Error FIFO Overrun Missed Packet
1	PTX	Packet Transmitted Indicates packet transmitted with no error
0	PRX	Packet Received Indicates packet received with no error.

4.3.3 Interrupt mask register (IMR) Offset 0FH (Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	RDCE	DMA Complete Interrupt Enable. Default “low” disabled.
5	CNTE	Counter Overflow Interrupt Enable. Default “low” disabled.
4	OVWE	Overwrite Interrupt Enable. Default “low” disabled.
3	TXEE	Transmit Error Interrupt Enable. Default “low” disabled.
2	RXEE	Receive Error Interrupt Enable. Default “low” disabled.
1	PTXE	Packet Transmitted Interrupt Enable. Default “low” disabled.
0	PRXE	Packet Received Interrupt Enable. Default “low” disabled.

4.3.4 Data Configuration Register (DCR) Offset 0EH (Write)

FIELD	NAME	DESCRIPTION
7	RDCR	Remote DMA always completed
6:2	-	Reserved
1	BOS	Byte Order Select 0: MS byte placed on AD15:AD8 and LS byte on AD7-AD0 (80X86). 1: MS byte placed on AD7::AD0 and LS byte on AD15:AD0(68K)
0	WTS	Word Transfer Select 0 : Selects byte-wide DMA transfers. 1 : Selects word-wide DMA transfers.

4.3.5 Transmit Configuration Register (TCR) Offset 0DH (Write)

FIELD	NAME	DESCRIPTION
7	FDU	Full Duplex : This bit indicates the current media mode is Full Duplex or not. 0 : Half duplex 1 : Full duplex
6	PD	Pad Disable 0 : Pad will be added when packet length less than 60. 1 : Pad will not be added when packet length less than 60.
5	RLO	Retry of late collision 0 : Don’t retransmit packet when late collision happens. 1 : Retransmit packet when late collision happens.
4:3	-	Reserved
2:1	LB1,LB0	Encoded Loop-back Control These encoded configuration bits set the type of loop-back that is to be performed. LB1 LB0 Mode 0 0 0 Normal operation Mode 1 0 1 Internal NIC loop-back Mode 2 1 0 PHYcevisor loop-back
0	CRC	Inhibit CRC 0 : CRC appended by transmitter. 1 : CRC inhibited by transmitter.

4.3.6 Transmit Status Register (TSR) Offset 04H (Read)

FIELD	NAME	DESCRIPTION
7	OWC	Out of window collision
6:4	-	Reserved
3	ABT	Transmit Aborted Indicates the AX88790 aborted transmission because of excessive collision.
2	COL	Transmit Collided Indicates that the transmission collided at least once with another station on the network.
1	-	Reserved
0	PTX	Packet Transmitted Indicates transmission without error.

4.3.7 Receive Configuration (RCR) Offset 0CH (Write)

FIELD	NAME	DESCRIPTION
7	INT_RG	Interrupt Regeneration 0 : Enable interrupt regeneration function in multifunction application. (default) But must set CIS relative Enable function first, than the function will be open. 1: Disable
6	-	Reserved
5	MON	Monitor Mode 0 : Normal Operation 1 : Monitor Mode, the input packet will be checked on NODE ADDRESS and CRC but not buffered into memory.
4	PRO	PRO : Promiscuous Mode Enable the receiver to accept all packets with a physical address.
3	AM	AM : Accept Multicast Enable the receiver to accept packets with a multicast address. That multicast address must pass the hashing array.
2	AB	AB : Accept Broadcast Enable the receiver to accept broadcast packet.
1	AR	AR : Accept Runt Enable the receiver to accept runt packet.
0	SEP	SEP : Save Error Packet Enable the receiver to accept and save packets with error.

4.3.8 Receive Status Register (RSR) Offset 0CH (Read)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	DIS	Receiver Disabled
5	PHY	Multicast Address Received.
4	MPA	Missed Packet
3	FO	FIFO Overrun
2	FAE	Frame alignment error.
1	CR	CRC error.
0	PRX	Packet Received Intact

4.3.9 Inter-frame gap (IFG) Offset 16H (Read/Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6:0	IFG	Inter-frame Gap. Default value 15H.

4.3.10 Inter-frame gap Segment 1(IFGS1) Offset 12H (Read/Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6:0	IFG	Inter-frame Gap Segment 1. Default value 0cH.

4.3.11 Inter-frame gap Segment 2(IFGS2) Offset 13H (Read/Write)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6:0	IFG	Inter-frame Gap Segment 2. Default value 12H.

4.3.12 MII/EEPROM Management Register (MEMR) Offset 14H (Read/Write)

FIELD	NAME	DESCRIPTION
7	EECLK	EECLK: EEPROM Clock
6	EEO	EEO : (Read only) EEPROM Data Out value. That reflects Pin-48 EEDO value.
5	EEI	EEI EEPROM Data In. That output to Pin-49 EEDI as EEPROM data input value.
4	EECS	EECS EEPROM Chip Select
3	MDO	MDO MII Data Out
2	MDI	MDI: (Read only) MII Data In. That reflects Pin-66 MDIO value.
1	MDIR	MII STA MDIO signal Direction MII Read Control Bit, assert this bit let MDIO signal as the input signal. Deassert this bit let MDIO as output signal.
0	MDC	MDC MII Clock

4.3.13 Test Register (TR) Offset 15H (Write)

FIELD	NAME	DESCRIPTION
7:5	-	Reserved
4	TF16T	Test for Collision
3	TPE	Test pin Enable
2:0	IFG	Select Test Pins Output

4.3.14 Test Register (TR) Offset 15H (Read)

FIELD	NAME	DESCRIPTION
7:4	-	Reserved
3	RST_TXB	100BASE-TX in Reset: This signal indicates that 100BASE-TX logic of internal PHY is in reset.
2	RST_10B	10BASE-T in Reset: This signal indicates that 10BASE-T logic of internal PHY is in reset.
1	RST_B	Reset Busy: This signal indicates that internal PHY is in reset.
0	AUTOD	Autonegotiation Done: This signal goes high whenever internal PHY autonegotiation has completed. It will go low if autonegotiation has to restart.

4.3.15 General Purpose Input Register (GPI) Offset 17H (Read)

FIELD	NAME	DESCRIPTION
7	-	Reserved
6	GPI2	This register reflects GPI[2] input value. May connect to external PHY speed status.
5	GPI1	This register reflects GPI[1] input value. May connect to external PHY duplex status.
4	GPI0	This register reflects GPI[0] input value. May connect to external PHY link status.
3	-	Reserved
2	I_SPD	This register reflects internal PHY speed status value. Logic one means 100Mbps
1	I_DPX	This register reflects internal PHY duplex status value. Logic one means full duplex.
0	I_LINK	This register reflects internal PHY link status value. Logic one means link ok.

4.3.16 GPO and Control (GPOC) Offset 17H (Write)

FIELD	NAME	DESCRIPTION
7:6	-	Reserved
5	MPSET	Media Set by Program: The signal is valid only when MPSEL is set to high. When MPSET is logic 0, internal PHY is selected. When MPSET is logic 1, external MII PHY is selected.
4	MPSEL	Media Priority Select : MPSEL I_LINK GPI0 Media Selected 0 1 0 Internal PHY 0 1 1 Internal PHY 0 0 0 External MII PHY 0 0 1 Internal PHY 1 X X Depend on MPSET bit
3:0	-	Reserved

4.4 The Embedded PHY Registers

The MII management 16-bit register set implemented is as follows. And the following sub-section will describes each field of the registers. The format for the “FIELD” descriptions is as follows: the first number is the register number, the second number is the bit position in the register and the name of the instantiated pad is in capital letters. The format for the “TYPE” descriptions is as follows: R = read, W = write, LH = latch high, NA = not applicable.

ADDRESS	NAME	DESCRIPTION	DEFAULT(Hex Code)
0	MR0	Control	3000h
1	MR1	Status	7849h
2	MR2	PHY Identifier 1	0180h
3	MR3	PHY Identifier 2	BB10h
4	MR4	Autonegotiation Advertisement	01E1h
5	MR5	Autonegotiation Link Partner Ability	0000
6	MR6	Autonegotiation Expansion	0000
7	MR7	Next Page Transmit	0000
8 - 15	MR8 -15	(Reserved)	-
16	MR16	PCS Control Register	0000
17	MR17	Autonegotiation (read register A)	0000
18	MR18	Autonegotiation (read register B)	0000
19	MR19	Analog Test Register	-
20	MR20	User-defined Register	-
21	MR21	RXER Counter	0000
22 - 24	MR22 -24	Analog Test Registers	-
25 - 27	MR25 -27	Analog Test (tuner) Registers	-
28	MR28	Device Specific 1	-
29	MR29	Device Specific 2	2080
30	MR30	Device Specific 3	0000
31	MR31	Quick Status Register	-

Tab – 18 The Embedded PHY Registers

4.4.1 MR0 -- Control Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
0.15 (SW_RESET)	R/W	**Reset.** Setting this bit to a 1 will reset the PHY. All registers will be set to their default state. This bit is self-clearing. The default is 0.
0.14 (LOOPBACK)	R/W	**Loopback.** When this bit is set to 1, no data transmission will take place on the media. Any receive data will be ignored. The loopback signal path will contain all circuitry up to, but not including, the PMD. The default value is a 0.
0.13(SPEED100)	R/W	**Speed Selection.** The value of this bit reflects the current speed of operation (1 =100 Mbits/s; 0 =10 Mbits/s). This bit will only affect operating speed when the autonegotiation enable bit (register 0, bit 12) is disabled (0). This bit is ignored when autonegotiation is enabled (register 0, bit 12). This bit is ANDed with the SPEED_PIN signal.
0.12 (NWAY_ENA)	R/W	**Autonegotiation Enable.** The autonegotiation process will be enabled by set-ting this bit to a 1. The default state is a 1.
0.11 (PWRDN)	R/W	**Powerdown.** The PHY may be placed in a low-power state by setting this bit to a 1, both the 10Mbits/s transceiver and the 100Mbits/s transceiver will be powered down. While in the powerdown state, the PHY will respond to management transactions. The default state is a 0.
0.10 (ISOLATE)	R/W	**Isolate.** When this bit is set to a 1, the MII outputs will be brought to the high-impedance state. The default state is a 0.
0.9 (REDONWAY)	R/W	**Restart Autonegotiation.** Normally, the autonegotiation process is started at powerup. Setting this bit to a 1 may restart the process. The default state is a 0. The NWAYDONE bit (register 1, bit 5) is reset when this bit goes to a 1. This bit is self-cleared when autonegotiation restarts.
0.8 (FULL_DUP)	R/W	**Duplex Mode.** This bit reflects the mode of operation (1 = full duplex; 0 = half duplex). This bit is ignored when the autonegotiation enable bit (register 0, bit 12) is enabled. The default state is a 0. This bit is ORed with the F_DUP pin.
0.7 (COLTST)	R/W	**Collision Test.** When this bit is set to a 1, the PHY will assert the MCOL signal in response to MTX_EN.
0.6:0 (RESERVED)	NA	**Reserved.** All bits will read 0.

4.4.2 MR1 -- Status Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
1.15 (T4ABLE)	R	**100Base-T4 Ability.** This bit will always be a 0. 0: Not able. 1: Able.
1.14 (TXFULDUP)	R	**100Base-TX Full-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.13 (TXHAFDUP)	R	**100Base-TX Half-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.12 (ENFULDUP)	R	**10Base-T Full-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.11 (ENHAFDUP)	R	**10Base-T Half-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.10:7 (RESERVED)	R	**Reserved.** All bits will read as a 0.
1.6 (NO_PA_OK)	R	**Suppress Preamble.** When this bit is set to a 1, it indicates that the PHY accepts management frames with the preamble suppressed.
1.5 (NWAYDONE)	R	**Autonegotiation Complete.** When this bit is a 1, it indicates the autonegotiation process has been completed. The contents of registers MR4, MR5, MR6, and MR7 are now valid. The default value is a 0. This bit is reset when autonegotiation is started.
1.4 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. The default is a 0.
1.3 (NWAYABLE)	R	**Autonegotiation Ability.** When this bit is a 1, it indicates the ability to perform autonegotiation. The value of this bit is always a 1.
1.2 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching function: a link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
1.1 (JABBER)	R	**Jabber Detect.** This bit will be a 1 whenever a jabber condition is detected. It will remain set until it is read, and the jabber condition no longer exists.
1.0 (EXT_ABLE)	R	**Extended Capability.** This bit indicates that the PHY supports the extended register set (MR2 and beyond). It will always read a 1.

4.4.3 MR2, MR3 -- Identification Registers (1 and 2) Bit Descriptions

FIELD	TYPE	DESCRIPTION
2.15:0 (OUI[3:18])	R	**Organizationally Unique Identifier.** The third through the twenty-fourth bit of the OUI assigned to the PHY manufacturer by the IEEE are to be placed in bits. 2.15:0 and 3.15:10. This value is programmable.
3.15:10 (OUI[19:24])	R	**Organizationally Unique Identifier.** The remaining 6 bits of the OUI. The value for bits 24:19 is programmable.
3.9:4 (MODEL[5:0])	R	**Model Number.** 6-bit model number of the device. The model number is programmable.
3.3:0 (VERSION[3:0])	R	**Revision Number.** The value of the present revision number. The version number is programmable.

4.4.4 MR4 – Autonegotiation Advertisement Registers Bit Descriptions

FIELD	TYPE	DESCRIPTION
4.15 (NEXT_PAGE)	R/W	**Next Page.** Setting this bit to a 1 activates the next page function. This will allow the exchange of additional data. Data is carried by optional next pages of information.
4.14 (ACK)	R/W	**Acknowledge.** This bit is the acknowledge bit from the link code word.
4.13 (REM_FAULT)	R/W	**Remote Fault.** When set to 1, the PHY indicates to the link partner a remote fault condition.
4.12:10 (PAUSE)	R/W	**Pause.** When set to a 1, it indicates that the PHY wishes to exchange flow control information with its link partner.
4.9 (100BASET4)	R/W	**100Base-T4.** This bit should always be set to 0.
4.8 (100BASET_FD)	R/W	**100Base-TX Full Duplex.** If written to 1, autonegotiation will advertise that the PHY is capable of 100Base-TX full-duplex operation.
4.7 (100BASETX)	R/W	**100Base-TX.** If written to 1, autonegotiation will advertise that the PHY is capable of 100Base-TX operation.
4.6 (10BASET_FD)	R/W	**10Base-T Full Duplex.** If written to 1, autonegotiation will advertise that the PHY is capable of 10Base-T full-duplex operation.
4.5 (10BASET)	R/W	**10Base-T.** If written to 1, autonegotiation will advertise that the PHY is capable of 10Base-T operation.
4.4:0 (SELECT)	R/W	**Selector Field**. Reset with the value 00001 for IEEE 802.3.

4.4.5 MR5 – Autonegotiation Link Partner Ability (Base Page) Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
5.15 (LP_NEXT_PAGE)	R	**Link Partner Next Page.** When this bit is set to 1, it indicates that the link partner wishes to engage in next page exchange.
5.14 (LP_ACK)	R	**Link Partner Acknowledge.** When this bit is set to 1, it indicates that the link partner has successfully received at least three consecutive and consistent FLP bursts.
5.13 (LP_REM_FAULT)	R	**Remote Fault.** When this bit is set to 1, it indicates that the link partner has a fault.
5.12:5 (LP_TECH_ABILITY)	R	**Technology Ability Field.** This field contains the technology ability of the link partner. These bits are similar to the bits defined for the MR4 register (see Table 16).
5.4:0 (LP_SELECT)	R	**Selector Field.** This field contains the type of message sent by the link partner. For IEEE 802.3 compliant link partners, this field should read 00001.

4.4.6 MR5 –Autonegotiation Link Partner (LP) Ability Register (Next Page) Bit Descriptions

FIELD	TYPE	DESCRIPTION
5.15 (LP_NEXT_PAGE)	R	**Next Page**. When this bit is set to logic 0, it indicates that this is the last page to be transmitted. Logic 1 indicates that additional pages will follow.
5.14 (LP_ACK)	R	**Acknowledge.** When this bit is set to a logic 1, it indicates that the link partner has successfully received its partner's link code word.
5.13 (LP__MES_PAGE)	R	**Message Page.** This bit is used by the NEXT _PAGE function to differentiate a message page (logic 1) from an unformatted page (logic 0).
5.12 (LP_ACK2)	R	**Acknowledge 2.** This bit is used by the NEXT_PAGE function to indicate that a device has the ability to comply with the message (logic 1) or not (logic 0).
5.11 (LP_TOGGLE)	R	**Toggle**. This bit is used by the arbitration function to ensure synchroniza-tion with the link partner during next page exchange. Logic 0 indicates that the previous value of the transmitted link code word was logic 1. Logic 1 indicates that the previous value of the transmitted link code word was logic 0.
5.10:0 (MCF)	R	**Message/Unformatted Code Field**. With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the IEEE 802.3u standard.

4.4.7 MR6 – Autonegotiation Expansion Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
6.15:5 (RESERVED)	R	**Reserved**.
6.4 (PAR_DET_FAULT)	R/LH	**Parallel Detection Fault.** When this bit is set to 1, it indicates that a fault has been detected in the parallel detection function. This fault is due to more than one technology detecting concurrent link conditions. This bit can only be cleared by reading this register.
6.3 (LP_NEXT_PAGE_ABLE)	R	**Link Partner Next Page Able.** When this bit is set to 1, it indicates that the link partner supports the next page function.
6.2 (NEXT_PAGE_ABLE)	R	**Next Page Able.** This bit is set to 1, indicating that this device supports the NEXT_PAGE function.
6.1 (PAGE_REC)	R/LH	**Page Received**. When this bit is set to 1, it indicates that a NEXT_PAGE has been received.
6.0 (LP_NWAY_ABLE)	R	**Link Partner Autonegotiation Capable.** When this bit is set to 1, it indicates that the link partner is autonegotiation capable.

4.4.8 MR7 –Next Page Transmit Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
7.15 (NEXT_PAGE)	R/W	**Next Page.** This bit indicates whether or not this is the last next page to be transmitted. When this bit is 0, it indicates that this is the last page. When this bit is 1, it indicates there is an additional next page.
7.14 (ACK)	R	**Acknowledge.** This bit is the acknowledge bit from the link code word.
7.13 (MESSAGE)	R/W	**Message Page.** This bit is used to differentiate a message page from an unformatted page. When this bit is 0, it indicates an unformatted page. When this bit is 1, it indicates a formatted page.
7.12 (ACK2)	R/W	**Acknowledge 2.** This bit is used by the next page function to indicate that a device has the ability to comply with the message. It is set as follows: When this bit is 0, it indicates the device cannot comply with the message. When this bit is 1, it indicates the device will comply with the message.
7.11 (TOGGLE)	R	**Toggle.** This bit is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit will always take the opposite value of the toggle bit in the previously exchanged link code word: If the bit is a logic 0, the previous value of the transmitted link code word was a logic 1. If the bit is a 1, the previous value of the transmitted link code word was a 0. The initial value of the toggle bit in the first next page transmitted is the inverse of the value of bit 11 in the base link code word, and may assume a value of 1 or 0.
7.10:0 (MCF)	R/W	**Message/Unformatted Code Field.** With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the IEEE 802.3u standard.

4.4.9 MR16 – PCS Control Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
16.15 (LOCKED)	R	**Locked.** Locked pin from descrambler block.
16.14-12 (UNUSED)	R	**Unused.** Will always be read back as 0.
16.11-4 (TESTBITS)	R/W	**Generic Test Bits.** These bits have no effect on the PCS block. They are for external use only. A 0 should be written to these bits.
16.3 (LOOPBACK)	R/W	**Loopback Configure.** When this bit is high, the entire loopback is performed in the PCS macro. When this bit is low, only the collision pin is disabled in loopback.
16.2 (SCAN)	R/W	**Scan Test Mode**.
16.1 (FORCE LOOPBACK)	R/W	**Force Loopback.** Force a loopback without forcing idle on the transmit side or disabling the collision pin.
16.0 (SPEEDUP COUNTERS)	R/W	**Speedup Counters.** Reduce link monitor counter to 10 us from 620 us. (Same as FASTTEST = 1.)

4.4.10 MR17 –Autonegotiation Register A Bit Descriptions

FIELD	TYPE	DESCRIPTION
17.15-13	R	**Reserved. Always 0.**
17.12	R	**Next Page Wait.**
17.11	R	**Wait Link_Fail_Inhibit_Wait_Timer (Link Status Check).**
17.10	R	**Wait Autoneg_Wait_Timer (Link Status Check).**
17.9	R	**Wait Break_Link_Timer (Transmit Disable).**
17.8	R	**Parallel Detection Fault.**
17.7	R	**Autonegotiation Enable.**
17.6	R	**FLP Link Good Check.**
17.5	R	**Complete Acknowledge.**
17.4	R	**Acknowledge Detect.**
17.3	R	**FLP Link Good.**
17.2	R	**Link Status Check.**
17.1	R	**Ability Detect.**
17.0	R	**Transmit Disable.**

4.4.11 MR18 –Autonegotiation Register B Bit Descriptions

FIELD	TYPE	DESCRIPTION
18.15	R	**Receiving FLPs**. Any of FLP Capture, Clock, Data_0, or Data_1 (FLP Rcv).
18.14	R	**FLP Pass** (FLP Rcv).
18.13	R	**Link Pulse Count** (FLP Rcv).
18.12	R	**Link Pulse Detect** (FLP Rcv).
18.11	R	**Test Pass** (NLP Rcv).
18.10	R	**Test Fail Count** (NLP Rcv).
18.9	R	**Test Fail Extend** (NLP Rcv).
18.8	R	**Wait Max Timer Ack** (NLP Rcv).
18.7	R	**Detect Freeze** (NLP Rcv).
18.6	R	**Test Fail** (NLP Rcv).
18.5	R	**Transmit Count Ack** (FLP Xmit).
18.4	R	**Transmit Data Bit** (FLP Xmit).
18.3	R	**Transmit Clock Bit** (FLP Xmit).
18.2	R	**Transmit ability** (FLP Xmit).
18.1	R	**Transmit Remaining Acknowledge** (FLP Xmit).
18.0	R	**Idle** (FLP Xmit).

4.4.12 MR20 –User Defined Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
20.[15:0]	R/W	The data written into this user-defined register appears on the REG20_OUT[15:0] bus.

4.4.13 MR21 –RXER Counter Register Bit Descriptions

FIELD	TYPE	DESCRIPTION
21.0	W	This bit, when 0 puts this register in 16-bit counter mode. When 1, it puts this register in 8-bit counter mode. This bit is reset to a 0 and cannot be read.
21.15:0	R	When in 16-bit counter mode, these maintain a count of RXERs. It is reset on a read operation.
21.7:0	R	When in 8-bit counter mode, these maintain a count of RXERs. It is reset on a read operation
21.11:8	R	When in 8-bit mode, these contain a count of false carrier events (802.3 section 27.3.1.5.1). It is reset on a read operaton.
21.15:12	R	When in 8-bit mode, these contain a count of disconnect events (Link Unstable 6, 802.3 section 27.3.1.5.1). It is reset on a read operation.

4.4.14 MR28 –Device-Specific Register 1 (Status Register) Bit Descriptions

FIELD	TYPE	DESCRIPTION
28.15:9 (UNUSED)	R	**Unused.** Read as 0.
28.8 (BAD_FRM)	R/LH	**Bad Frame.** If this bit is a 1, it indicates a packet has been received without an SFD. This bit is only valid in 10Mbits/s mode. This bit is latching high and will only clear after it has been read or the device has been reset.
28.7 (CODE)	R/LH	**Code Violation.** When this bit is a 1, it indicates a Manchester code violation has occurred. The error code will be output on the MRXD lines. Refer to Table 1 for a detailed description of the MRXD pin error codes. This bit is only valid in 10Mbits/s mode. This bit is latching high and will only clear after it has been read or the device has been reset.
28.6 (APS)	R	**Autopolarity Status.** When register 30, bit 3 is set and this bit is a 1, it indicates the PHY has detected and corrected a polarity reversal on the twisted pair. If the APF_EN bit (register 30, bit 3) is set, the reversal will be corrected inside the PHY. This bit is not valid in 100Mbits/s operation.
28.5 (DISCON)	R/LH	**Disconnect.** If this bit is a 1, it indicates a disconnect. This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.4 (UNLOCKED)	R/LH	**Unlocked.** Indicates that the TX scrambler lost lock. This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.3 (RXERR_ST)	R/LH	**RX Error Status.** Indicates a false carrier. This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.2 (FRC_JAM)	R/LH	**Force Jam.** This bit will latch high until read. This bit is only valid in 100Mbits/s mode.
28.1 (LNK100UP)	R	**Link Up 100.** This bit, when set to a 1, indicates a 100Mbits/s transceiver is up and operational.
28.0 (LNK10UP)	R	**Link Up 10.** This bit, when set to a 1, indicates a 10Mbits/s transceiver is up and operational.

4.4.15 MR29 –Device-Specific Register 2 (100Mbps Control) Bit Descriptions

FIELD	TYPE	DESCRIPTION
29.15 (LOCALRST)	R/W	**Management Reset.** This is the local management reset bit. Writing logic 1 to this bit will cause the lower 16 registers and registers 28 and 29 to be reset to their default values. This bit is self-clearing.
29.14 (RST1)	R/W	**Generic Reset 1.** This register is used for manufacture test only.
29.13 (RST2)	R/W	**Generic Reset 2.** This register is used for manufacture test only.
29.12 (100_OFF)	R/W	**100Mbits/s Transmitter Off.** When this bit is set to 0, it forces TPI low and TPIN- high. This bit defaults to 1.
29.11 (LED_BLINK)	R/W	**LED Blinking.** This register, when 1, enables LED blinking. This is ORed with LED_BLINK_EN. Default is 0.
29.10 (CRS_SEL)	R/W	**Carrier Sense Select.** MCRS will be asserted on receive only when this bit is set to a 1. If this bit is set to logic 0, MCRS will by asserted on receive or transmit. This bit is ORed with the CRS_SEL pin.
29.9 (LINK_ERR)	R/W	**Link Error Indication.** When this bit is a 1, a link error code will be reported on MRXD[3:0] of the PHY when MRX_ER is asserted on the MII. The specific error codes are listed in the MRXD pin description. If it is 0, it will disable this function.
29.8 (PKT_ERR)	R/W	**Packet Error Indication Enable.** When this bit is a 1, a packet error code, which indicates that the scrambler is not locked, will be reported on MRXD[3:0] of the PHY when MRX_ER is asserted on the MII. When this bit is 0, it will disable this function.
29.7 (PULSE_STR)	R/W	**Pulse Stretching.** When this bit is set to 1, the CS, XS, and RS output signals will be stretched between approximately 42 ms- 84 ms. If this bit is 0, it will disable this feature. Default state is 0.
29.6 (EDB)	R/W	**Encoder/Decoder Bypass.** When this bit is set to 1, the 4B/5B-encoder and 5B/4B-decoder function will be disabled. This bit is ORed with the EDBT pin.
29.5 (SAB)	R/W	**Symbol Aligner Bypass.** When this bit is set to 1, the aligner function will be disabled.
29.4 (SDB)	R/W	**Scrambler/Descrambler Bypass.** When this bit is set to 1, the scrambling/ descrambling functions will be disabled. This bit is ORed with the SDBT pin.
29.3 (CARIN_EN)	R/W	**Carrier Integrity Enable.** When this bit is set to a 1, carrier integrity is enabled. This bit is ORed with the CARIN_EN pin.
29.2 (JAM_COL)	R/W	**Jam Enable.** When this bit is a 1, it enables JAM associated with carrier integrity to be ORed with MCOLMCRS.
29.1 (FEF-EN)	R/W	**Far-End Fault Enable**. This bit is used to enable the far-end fault detection and transmission capability. This capability may only be used if autonegotiation is disabled. This capability is to be used only with media, which does not support autonegotiation. Setting this bit to 1 enables far-end fault detection and logic 0 will disable the function. Default state is 0.
29.0 (FX)	R/W	**Fiber-Optic Mode.** When this bit is a 1, the PHY is in fiber-optic mode. This bit is ORed with FX_MODE.

4.4.16 MR30 –Device-Specific Register 3 (10Mbps Control) Bit Descriptions

FIELD	TYPE	DESCRIPTION
30.15 (Test10TX)	R/W	When high and 10Base-T is powered up, a continuous 10 MHz signal (1111) will be transmitted. This is only meant for testing. Default 0.
30.14 (RxPLLEn)	R/W	When high, all 10Base-T logic will be powered up when the link is up. Otherwise, portions of the logic will be powered down when no data is being received to conserve power. Default is 0.
30.13 (JAB_DIS)	R/W	**Jabber Disable.** When this bit is 1, disables the jabber function of the 10Base-T receive. Default is 0.
30.12:7 (UNUSED)	R/W	**Unused.** Read as 0.
30.6 (LITF_ENH)	R/W	**Enhanced Link Integrity Test Function.** When high, function is enabled. This is ORed with the LITF_ENH input. Default is 0.
30.5 (HBT_EN)	R/W	**Heartbeat Enable.** When this bit is a 1, the heartbeat function will be enabled. Valid in 10Mbits/s mode only.
30.4 (ELL_EN)	R/W	**Extended Line Length Enable.** When this bit is a 1, the receive squelch levels are reduced from a nominal 435 mV to 350 mV, allowing reception of signals with a lower amplitude. Valid in 10Mbits/s mode only.
30.3 (APF_EN)	R/W	**Autopolarity Function Disable.** When this bit is a 0 and the PHY is in 10Mbits/s mode, the autopolarity function will determine if the TP link is wired with a polarity reversal. If there is a polarity reversal, the PHY will assert the APS bit (register 28, bit 6) and correct the polarity reversal. If this bit is a 1 and the device is in 10Mbits/s mode, the reversal will not be corrected.
30.2 (RESERVED)	R/W	**Reserved**.
30.1 (SERIAL _SEL)	R/W	**Serial Select.** When this bit is set to a 1, 10Mbits/s serial mode will be Selected. When the PHY is in 100Mbits/s mode, this bit will be ignored.
30.0 (ENA_NO_LP)	R/W	**No Link Pulse Mode.** Setting this bit to a 1 will allow 10Mbits/s operation with link pulses disabled. If the PHY is configured for 100Mbits/s operation, setting this bit will not affect operation.

4.4.17 MR31 –Device-Specific Register 4 (Quick Status) Bit Descriptions

FIELD	TYPE	DESCRIPTION
31.15 (ERROR)	R	**Receiver Error.** When this bit is a 1, it indicates that a receive error has been detected. This bit is valid in 100Mbits/s only. This bit will remain set until cleared by reading the register. Default is a 0.
31.14 (RXERR_ST)/(LINK_STAT_CHANGE)	R	**False Carrier.** When bit [31.7] is set to 0 and this bit is a 1, it indicates that the carrier detect state machine has found a false carrier. This bit is valid in 100Mbits/s only. This bit will remain set until cleared by reading the register. Default is 0. **Link Status Change.** When bit [31.7] is set to a 1, this bit is redefined to become the LINK_STAT_CHANGE bit and goes high whenever there is a change in link status (bit [31.11] changes state)
31.13 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. Default is a 0.
31.12 (UNLOCKED)/(JABBER)	R	**Unlocked/Jabber.** If this bit is set when operating in 100Mbits/s mode, it indicates that the TX descrambler has lost lock. If this bit is set when operating in 10Mbits/s mode, it indicates a jabber condition has been detected. This bit will remain set until cleared by reading the register.
31.11 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching low function: a link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
31.10 (PAUSE)	R	**Link Partner Pause.** When this bit is set to a 1, it indicates that the LU3X54FTL wishes to exchange flow control information.
31.9 (SPEED100)	R	**Link Speed.** When this bit is set to a 1, it indicates that the link has negotiated to 100Mbits/s. When this bit is a 0, it indicates that the link is operating at 10Mbits/s.
31.8 (FULL_DUP)	R	**Duplex Mode.** When this bit is set to a 1, it indicates that the link has negotiated to full-duplex mode. When this bit is a 0, it indicates that the link has negotiated to half-duplex mode.
31.7 (INT_CONF)	R/W	**Interrupt Configuration.** When this bit is set to a 0, it defines bit [31.14] to be the RXERR_ST bit and the interrupt pin (MASK_STAT_INT) goes high whenever any of bits [31.15:12] go high, or bit [31.11] goes low. When this bit is set high, it redefines bit [31.14] to become the LINK_STAT_CHANGE bit, and the interrupt pin (MASK_STAT_INT) goes high only when the link status changes (bit [31.14] goes high). This bit defaults to 0.
31.6 (INT_MASK)	R/W	**Interrupt Mask.** When set high, no interrupt is generated by this channel under any condition. When set low, interrupts are generated according to bit [31.7].
31.5:3 (LOW_AUTO__STATE)	R	**Lowest Autonegotiation State.** These 3 bits report the state of the lowest autonegotiation state reached since the last register read, in the priority order defined below: 000: Autonegotiation enable. 001: Transmit disable or ability detect. 010: Link status check. 011: Acknowledge detect. 100: Complete acknowledge. 101: FLP link good check. 110: Next page wait. 111: FLP link good.
31.2:0 (HI_AUTO_STATE)	R	**Highest Autonegotiation State.** These 3 bits report the state of the highest autonegotiation state reached since the last register read, as defined above for bit [31.5:3].

5.0 Device Access Functions

5.1 PCMCIA interface access functions.

5.1.1 Attribute Memory access function functions.

Attribute Memory Read function

Function Mode	REG#	CE2#	CE1#	SA0	OE#	WE#	SD[15:8]	SD[7:0]
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8 bits)	L	H	L	L	L	H	High-Z	Even-Byte
	L	H	L	H	L	H	High-Z	Not Valid
Word Access (16 bits)	L	L	L	X	L	H	Not Valid	Even-Byte
Odd Byte Only Access	L	L	H	X	L	H	Not Valid	High-Z

Attribute Memory Write function

Function Mode	REG#	CE2#	CE1#	SA0	OE#	WE#	SD[15:8]	SD[7:0]
Standby Mode	X	H	H	X	X	X	X	X
Byte Access (8 bits)	L	H	L	L	H	L	X	Even-Byte
	L	H	L	H	H	L	X	X
Word Access (16 bits)	L	L	L	X	H	L	X	Even-Byte
Odd Byte Only Access	L	L	H	X	H	L	X	X

5.1.1 I/O access function functions.

I/O Read function

Function Mode	REG#	CE2#	CE1#	SA0	OE#	WE#	SD[15:8]	SD[7:0]
Standby Mode	X	H	H	X	X	X	High-Z	High-Z
Byte Access (8 bits)	L	H	L	L	L	H	High-Z	Even-Byte
	L	H	L	H	L	H	High-Z	Odd-Byte
Word Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
I/O Inhibit	H	X	X	X	L	H	High-Z	High-Z
Odd Byte Only Access	L	L	H	X	L	H	Odd-Byte	High-Z

I/O Write function

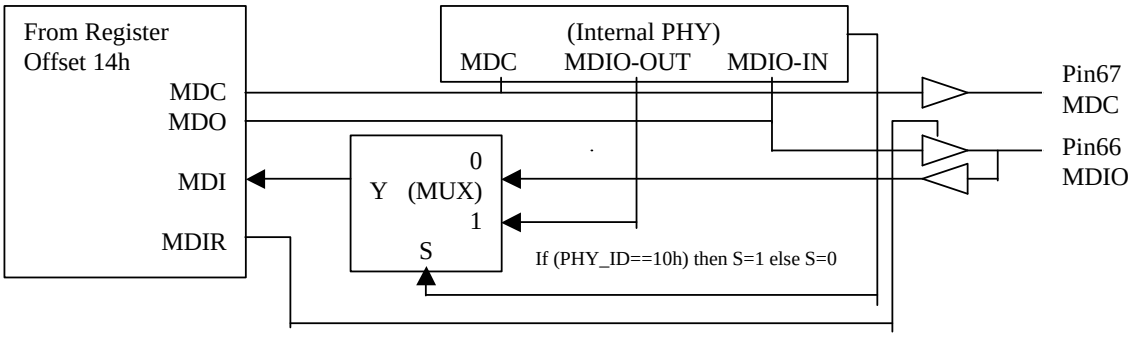
Function Mode	REG#	CE2#	CE1#	SA0	IORD#	IOWR#	SD[15:8]	SD[7:0]
Standby Mode	X	H	H	X	X	X	X	X
Byte Access (8 bits)	L	H	L	L	H	L	X	Even-Byte
	L	H	L	H	H	L	X	Odd-Byte
Word Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Inhibit	H	X	X	X	H	L	X	X
Odd Byte Only Access	L	L	H	X	H	L	Odd-Byte	X

5.2 MII Station Management functions.

Basic Operation

The primary function of station management is to transfer control and status information about the PHY to a management entity. This function is accomplished by the MDC clock input from MAC entity, which has a maximum frequency of 12.5 MHz (for internal PHY only, as to external PHY please refer to the relevant specification), along with the MDIO signal.

The **Internal PHY address is fixed to 10h** and the equivalent circuit is shown as below:



A specific set of registers and their contents (described in Tab-19) defines the nature of the information transferred across the MDIO interface. Frames transmitted on the MII management interface will have the frame structure shown in Tab-18. The order of bit transmission is from left to right. Note that reading and writing the management register must be completed without interruption.

Read/Write (R/W)	Pre	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
R	1. . .1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
W	1. . .1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Tab - 19 MII Management Frame Format

Field	Descriptions
Pre	**Preamble**. The PHY will accept frames with no preamble. This is indicated by a 1 in register 1, bit 6.
ST	**Start of Frame.** The start of frame is indicated by a 01 pattern.
OP	**Operation Code**. The operation code for a read transaction is 10. The operation code for a write transaction is a 01.
PHYADD	**PHY Address**. The PHY address is 5 bits, allowing for 32 unique addresses. The first PHY address bit transmitted and received is the MSB of the address. A station management entity that is attached to multiple PHY entities must have prior knowledge of the appropriate PHY address for each entity.
REGAD	**Register Address.** The register address is 5 bits, allowing for 32 unique registers within each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	**Turnaround**. The turnaround time is a 2-bit time spacing between the register address field, and the data field of a frame, to avoid drive contention on MDIO during a read transaction. During a write to the PHY, these bits are driven to 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the PHY during the second bit time.
DATA	**Data**. The data field is 16 bits. The first bit transmitted and received will be bit 15 of the register being addressed.
IDLE	**Idle Condition.** The IDLE condition on MDIO is a high-impedance state. All three state drivers will be disabled and the PHY's pull-up resistor will pull the MDIO line to logic 1.

Tab - 20 MII Management Frames- field Description

6.0 Electrical Specification and Timings

6.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+85	°C
Storage Temperature	Ts	-55	+150	°C
Supply Voltage	Vdd	-0.3	+4.6	V
Input Voltage	Vin	-0.3	5.5*	V
Output Voltage	Vout	-0.3	Vdd+0.5	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+220	°C

Note: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability.
Note: * All digital input signals can sustain 5 Volts input voltage except pin-79 LCLK/XTALIN

6.2 General Operation Conditions

Description	SYM	Min	Tpy	Max	Units
Operating Temperature	Ta	0	25	+75	°C
Supply Voltage	Vdd	+3.14	+3.30	+3.46	V

6.3 DC Characteristics

(Vdd=3.3V, Vss=0V, Ta=0°C to 75°C)

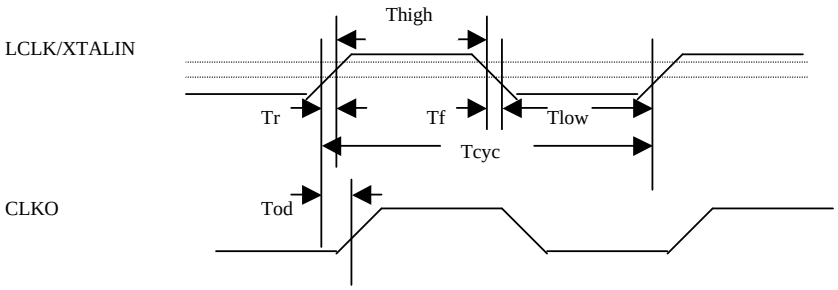
Description	SYM	Min	Tpy	Max	Units
Low Input Voltage	Vil	-		0.8	V
High Input Voltage	Vih	1.9		-	V
Low Output Voltage	Vol	-		0.4	V
High Output Voltage	Voh	Vdd-0.4		-	V
Input Leakage Current	Iil	-1		+1	uA
Output Leakage Current	Iol	-1		+1	uA

Description	SYM	Min	Tpy	Max	Units
Power Consumption (3.3V)	SPt3v		87	120	mA

Note: Please reference "Appendix B: Power Consumption Reference Data"

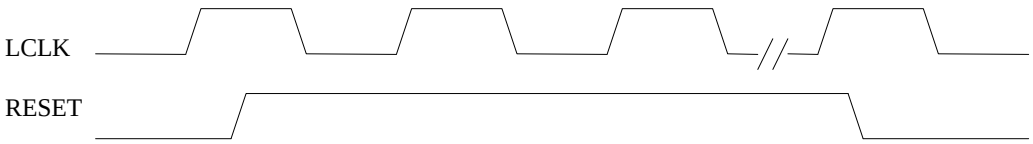
6.4 A.C. Timing Characteristics

6.4.1 XTAL / CLOCK



Symbol	Description	Min	Typ.	Max	Units
Tcyc	CYCLE TIME		40		ns
Thigh	CLK HIGH TIME	16	20	24	ns
Tlow	CLK LOW TIME	16	20	24	ns
Tr/Tf	CLK SLEW RATE	1	-	4	ns
Tod	LCLK/XTALIN TO CLKO OUT DELAY		10		

6.4.2 Reset Timing



Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	100	-	-	LClk

Note: Some chips may need long power down for successful PHY auto negotiation

Root of cause:

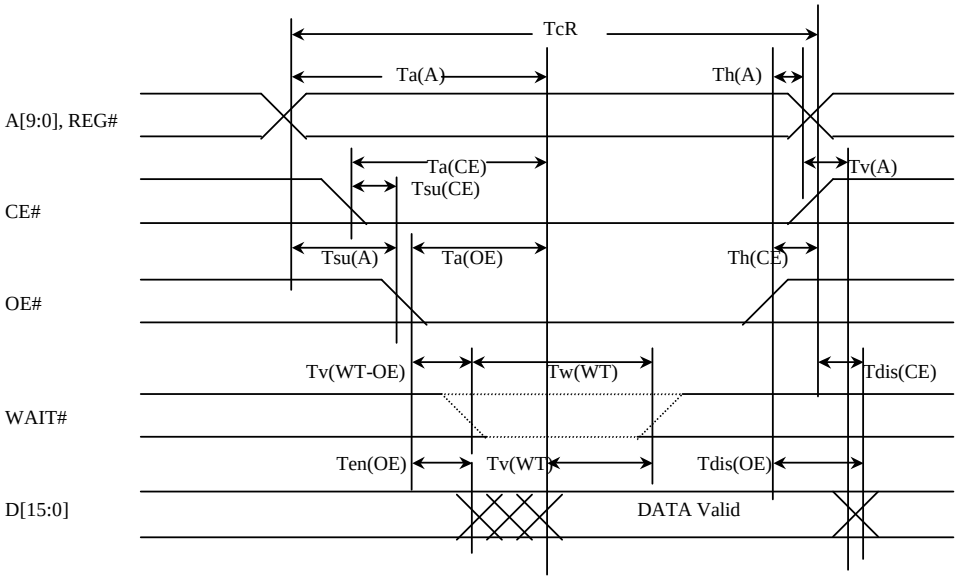
The PHY inside of AX88790 has a special request due to the semiconductor's process. Namely, it needs a very long power down for successful Auto Negotiation for some chips. We made a test in lab and found it would be no problem if the PHY's initial time kept for 2 sec for all chips**.** If the power down is less then this number, some of the PHY's Auto Negotiation will not be complete and there will be potential to cause the link fail. If the auto negotiation time is not long enough, uncertain numbers of chip may not work properly.

Countermeasure:
Following actions on chip initialization will fix the problem of long auto negotiation.

1. Set the PHY register MR0 with 0x800h (1000,0000,0000) -- bit 11 of MR0 to '1' (Power down Mode).
2. Wait for 2.5 sec

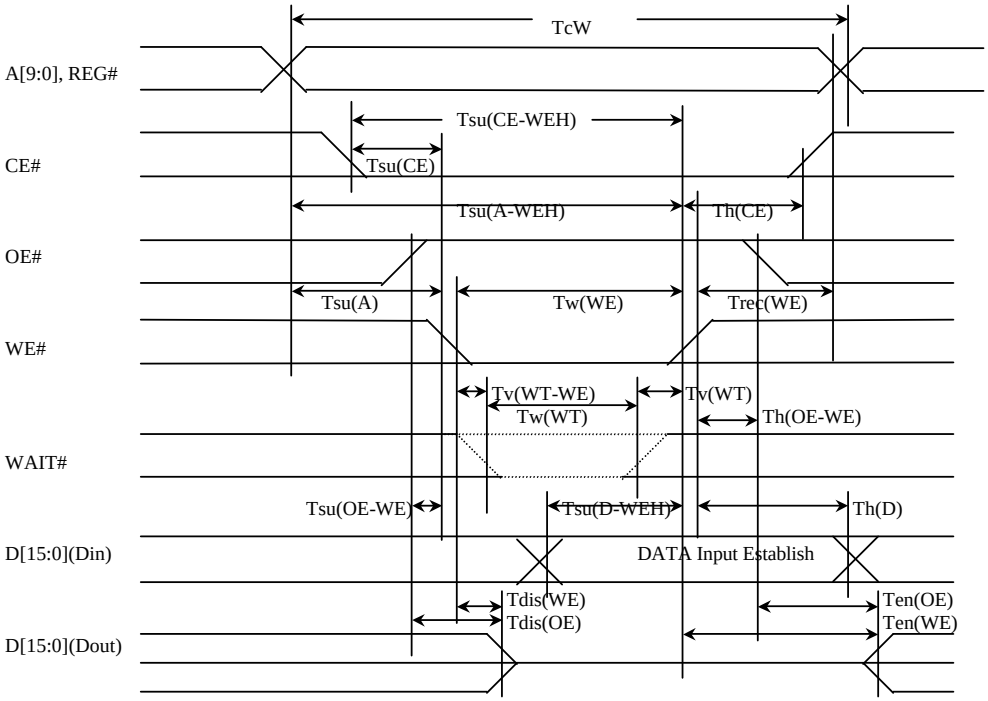
3. Set the PHY register MR0 with 0x1200h(0001,0010,0000,0000) -- bit 12,9 of MR0 to '1' (auto negotiation enable and restart auto negotiation)

6.4.3 Attribute Memory Read Timing



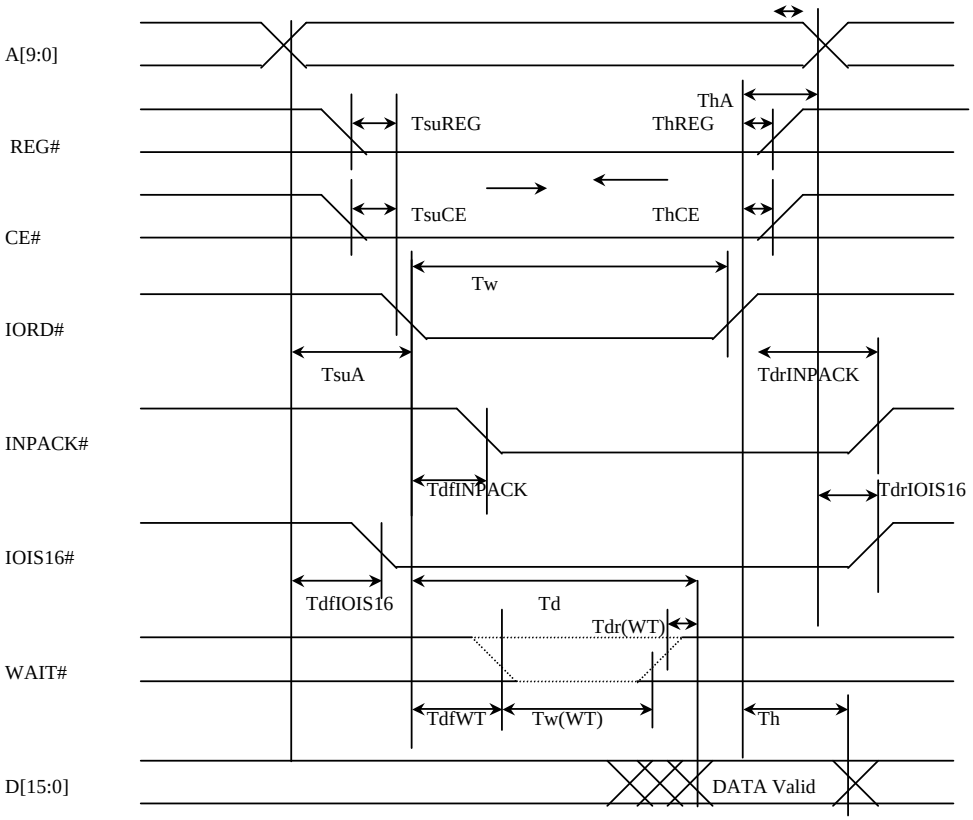
Symbol	Description	Min	Typ.	Max	Units
TcR	READ CYCLE TIME	300	-	-	ns
Ta(A)	ADDRESS ACCESS TIME	-	-	120	ns
Ta(CE)	CARD ENABLE ACCESS TIME	-	-	100	ns
Ta(OE)	OUTPUT ENABLE ACCESS TIME	-	-	100	ns
Tdis(OE)	OUTPUT DISABLE TIME FROM OE#	0.5	-	-	ns
Ten(OE)	OUTPUT ENABLE TIME FROM OE#	-	-	100	ns
Tv(A)	DATA VALID FROM ADDRESS CHANGE	0	-	-	ns
Tsu(A)	ADDRESS SETUP TIME	30	-	-	ns
Th(A)	ADDRESS HOLD TIME	20	-	-	ns
Tsu(CE)	CARD ENABLE SETUP TIME	0	-	-	ns
Th(CE)	CARD ENABLE HOLD TIME	20	-	-	ns
Tv(WT-OE)	WAIT# VALID FROM OE#	-	-	10	ns
Tw(WT)	WAIT# PULSE WIDTH	-	-	200	ns
Tv(WT)	DATA SETUP FOR WAIT# RELEASED	100	-	-	ns

6.4.4 Attribute Memory Write Timing



Symbol	Description	Min	Typ.	Max	Units
TcW	WRITE CYCLE TIME	250	-	-	ns
Tw(WE)	WRITE PULSE WIDTH	150	-	-	ns
Tsu(A)	ADDRESS SETUP TIME	30	-	-	ns
Tsu(A-WEH)	ADDRESS SETUP TIME FOR WE#	180	-	-	ns
Tsu(CE-WEH)	CARD ENABLE SETUP TIME FOR WE#	180	-	-	ns
Tsu(D-WEH)	DATA SETUP TIME FOR WE#	80	-	-	ns
Th(D)	DATA HOLD TIME	30	-	-	ns
Trec(WE)	WRITE RECOVER TIME	30	-	-	ns
Tdis(WE)	OUTPUT DISABLE TIME FROM WE#	-	-	5	ns
Tdis(OE)	OUTPUT DISABLE TIME FROM OE#	-	-	5	ns
Ten(WE)	OUTPUT ENABLE TIME FROM WE#	5	-	-	ns
Ten(OE)	OUTPUT ENABLE TIME FROM OE#	5	-	-	ns
Tsu(OE-WE)	OUTPUT ENABLE SETUP TIME FROM OE#	10	-	-	ns
Th(OE-WE)	OUTPUT ENABLE HOLD TIME FROM OE#	10	-	-	ns
Tsu(CE)	CARD ENABLE SETUP TIME	0	-	-	ns
Th(CE)	CARD ENABLE HOLD TIME	20	-	-	ns
Tv(WT-WE)	WAIT# VALID FROM WE#	-	-	15	ns
Tw(WT)	WAIT# PULSE WIDTH	-	-	200	ns
Tv(WT)	WE# HIGH FROM WAIT# RELEASED	0	-	-	ns

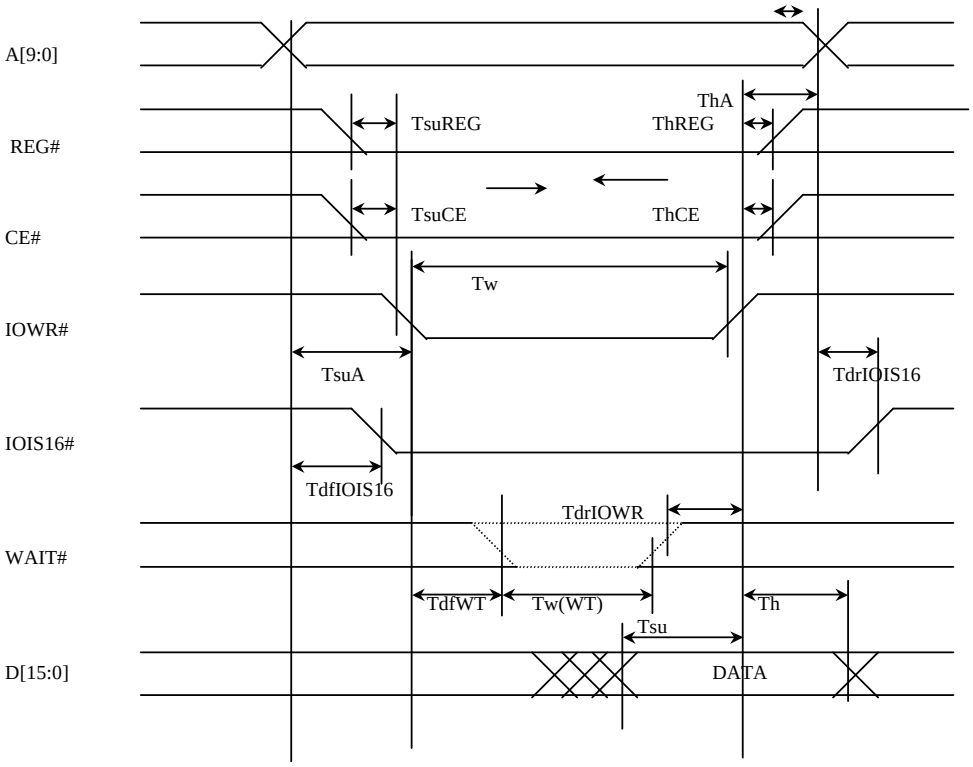
6.4.5 I/O Read Timing



Symbol	Description	Min	Typ.	Max	Units
Td	DATA DELAY AFTER IORD#	-	-	50	ns
Th	DATA HOLD FOLLOWING IORD#	0.5	-	-	ns
Tw	IORD# WIDTH TIME	165	-	-	ns
TsuA	ADDRESS SETUP BEFORE IORD#	70	-	-	ns
ThA	ADDRESS HOLD BEFORE IORD#	20	-	-	ns
TsuCE	CE# SETUP BEFORE IORD#	5	-	-	ns
ThCE	CE# HOLD BEFORE IORD#	20	-	-	ns
TsuREG	REG# SETUP BEFORE IORD#	5	-	-	ns
ThREG	REG# HOLD BEFORE IORD#	0	-	-	ns
TdfINPACK	INPACK# DELAY FALLING FROM IORD#	0	-	10	ns
TdrINPACK	INPACK# DELAY RISING FROM IORD#	-	-	10	ns
TdfIOIS16	IOIS16# DELAY FALLING FROM ADDRESS*	-	-	10	ns
TdrIOIS16	IOIS16# DELAY RISING FROM ADDRESS*	-	-	0	ns
TdfWT	WAIT# DELAY FALLING FROM IORD#	-	-	5	ns
Tdr(WT)	DATA DELAY FROM WAIT# RISING	-	-	0	us
Tw(WT)	WAIT# WIDTH TIME	-	-	100	ns

* Note : The address includes REG# and CE1# signal

6.4.6 I/O Write Timing

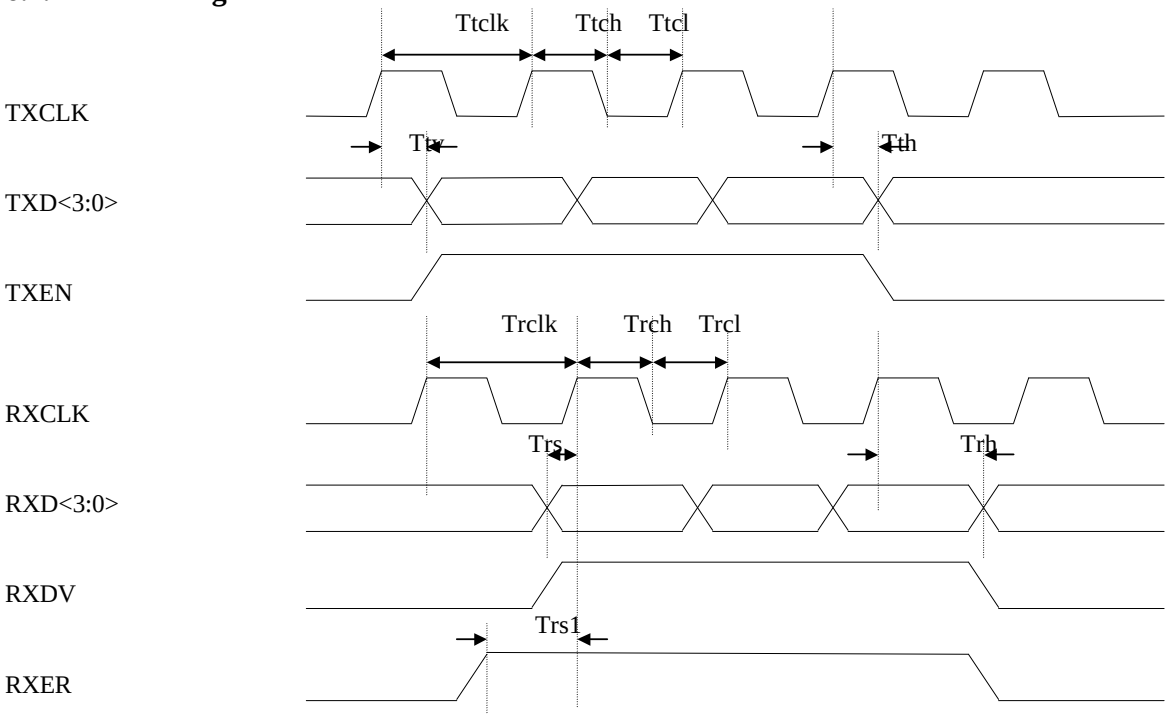


Symbol	Description	Min	Typ.	Max	Units
Tsu	DATA SETUP BEFORE IOWR#	60	-	-	ns
Th	DATA HOLD FOLLOWING IOWR#	30	-	-	ns
Tw	IOWR# WIDTH TIME	165	-	-	ns
TsuA	ADDRESS SETUP BEFORE IOWR#	70	-	-	ns
ThA	ADDRESS HOLD BEFORE IOWR#	20	-	-	ns
TsuCE	CE# SETUP BEFORE IOWR#	5	-	-	ns
ThCE	CE# HOLD BEFORE IOWR#	20	-	-	ns
TsuREG	REG# SETUP BEFORE IOWR#	5	-	-	ns
ThREG	REG# HOLD BEFORE IOWR#	0	-	-	ns
TdfIOIS16	IOIS16# DELAY FALLING FROM ADDRESS*	-	-	10	ns
TdrIOIS16	IOIS16# DELAY RISING FROM ADDRESS*	-	-	0	ns
TdfWT	WAIT# DELAY FALLING FROM IOWR#	-	-	**	ns
Tw(WT)	WAIT# WIDTH TIME	-	-	**	ns
TdrIOWR	IOWR# HIGH FROM WAIT# HIGH	0	-	-	us

*Note : The address includes REG# and CE1# signal

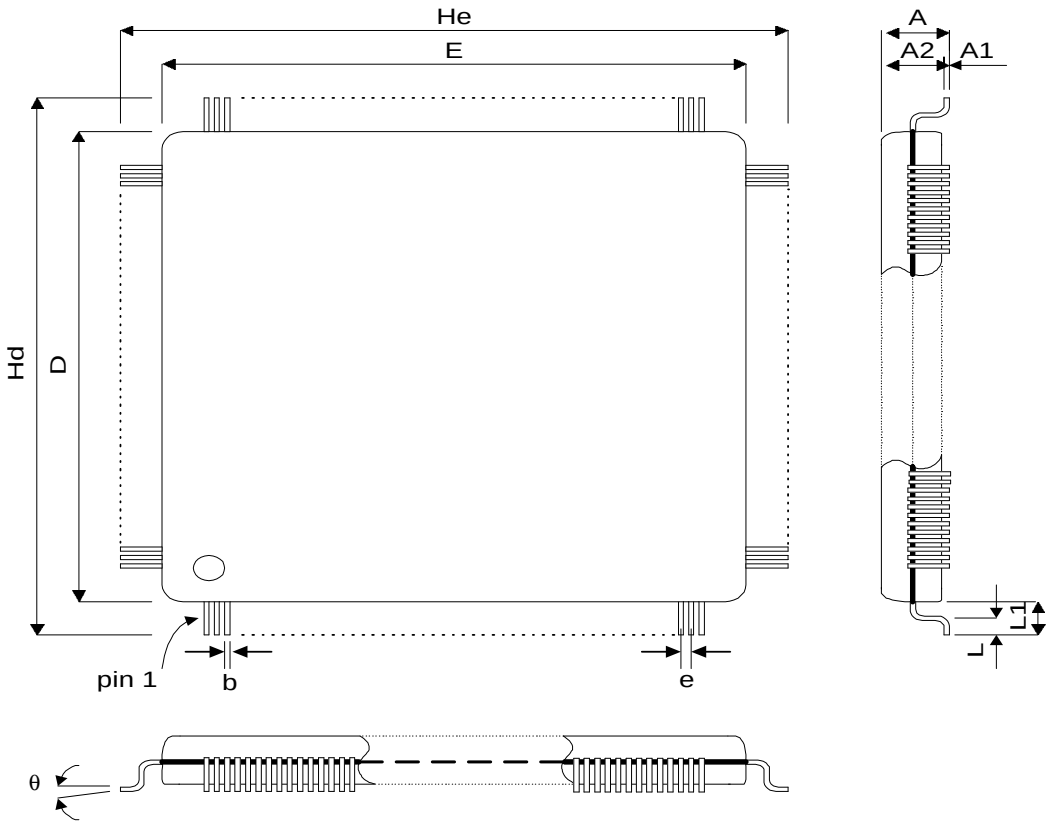
** Note : There is no wait state while I/O Write operation

6.4.7 MII Timing



Symbol	Description	Min	Typ.	Max	Units
Ttclk	Cycle time(100Mbps)	-	40	-	ns
Ttclk	Cycle time(10Mbps)	-	400	-	ns
Ttch	high time(100Mbps)	14	-	26	ns
Ttch	high time(10Mbps)	140	-	260	ns
Trch	low time(100Mbps)	14	-	26	ns
Trch	low time(10Mbps)	140	-	260	ns
Ttv	Clock to data valid	-	-	20	ns
Tth	Data output hold time	5	-	-	ns
Trclk	Cycle time(100Mbps)	-	40	-	ns
Trclk	Cycle time(10Mbps)	-	400	-	ns
Trch	high time(100Mbps)	14	-	26	ns
Trch	high time(10Mbps)	140	-	260	ns
Trcl	low time(100Mbps)	14	-	26	ns
Trcl	low time(10Mbps)	140	-	260	ns
Trs	data setup time	6	-	-	ns
Trh	data hold time	10	-	-	ns
Trs1	RXER data setup time	10	-	-	ns

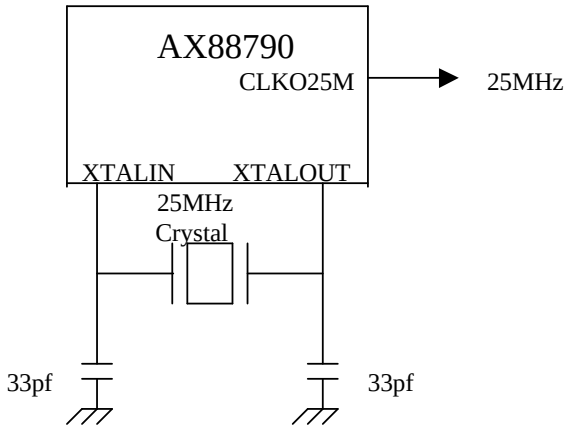
7.0 Package Information



SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.1	0.15
A2	1.35	1.40	1.45
A			1.6
b	0.17	0.22	0.27
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e		0.5	
Hd	15.60	16.00	16.40
He	21.00	22.00	23.00
L	0.45	0.60	0.75
L1		1.00	
θ	0°		7°

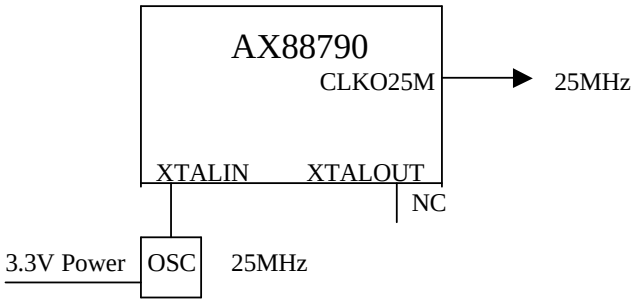
Appendix A: Application Note 1

A.1 Using Crystal 25MHz



Note: The capacitors (33pf) may be various depend on the specification of crystal. While designing, please refer to the suggest circuit provided by crystal supplier.

A.2 Using Oscillator 25MHz



Appendix B: Power Consumption Reference Data

The following reference data of power consumption are measured base on prime application, that is AX88790 + EEPROM + 74LV04, at 3.3V/25 °C room temperature.
Note: 74LV04 is used for LEDs buffer or driver. Designer may omit the part and drive LED directly by AX88790.

Item	Test Conditions	Typical Value	Units
1	Power save mode (Power Down register bit set to “1” asserted)	3	mA
2	Idel without Link	16	mA
3	Idel with 10M Link	22	mA
4	Idel with 100M Link	80	mA
5	Full traffic with 10Mbps at half-duplex mode	37 – 69	mA
6	Full traffic with 10Mbps at full-duplex mode	31 – 57	mA
7	Full traffic with 100Mbps at half-duplex mode	83	mA
8	Full traffic with 100Mbps at full-duplex mode	87	mA
9	Power save mode (Power Down register bit set to “1” asserted) no LED drive	0	mA
10	Idel without Link, no LED drive	12	mA
11	Idel with 10M Link, no LED drive	15	mA
12	Idel with 100M Link, no LED drive	74	mA
13	Full traffic with 10Mbps at half-duplex mode, no LED drive	40 – 68	mA
14	Full traffic with 10Mbps at full-duplex mode, no LED drive	35 – 60	mA
15	Full traffic with 100Mbps at half-duplex mode, no LED drive	76	mA
16	Full traffic with 100Mbps at full-duplex mode, no LED drive	76	mA

Errata of AX88790

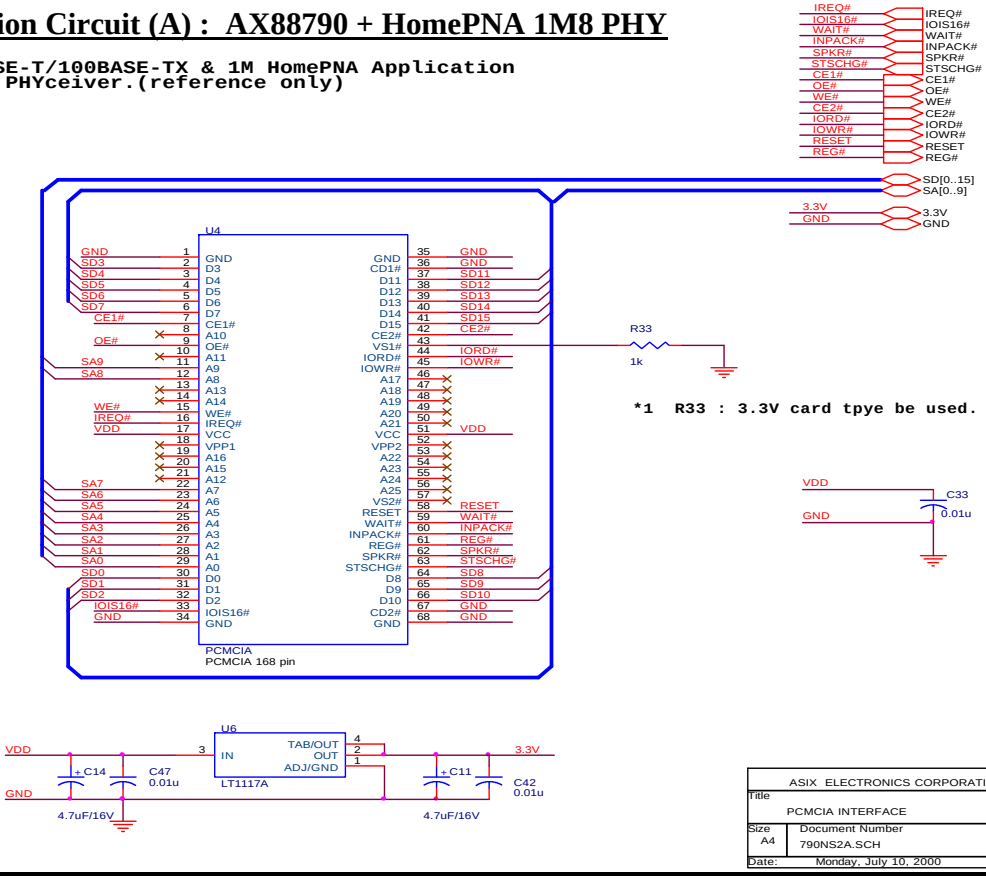
1. MII Station Management functions have some differences from previous target specification.

Description: The target specification is using station management can access both internal PHY registers and external PHY registers when the PHY address is matched as describe in section 5.2. Anyway, this version can only access the current selected PHY's registers. How do you know which is the selected media or PHY? Please refer to section 4.3.16 GPO and Control (GPOC) register.

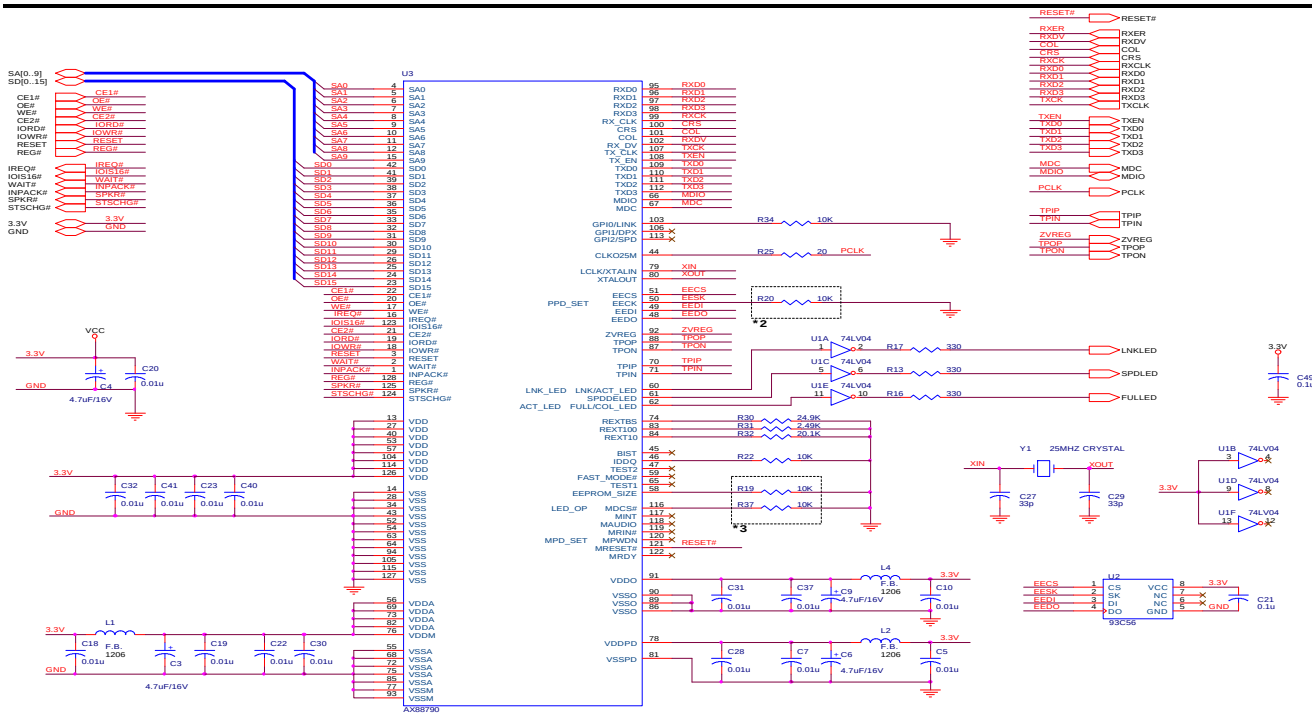
Solution: The defect will not affect single media application that is using embedded PHY. When using MII interface connects to external media (for example HomePNA) to come out with combo solution. Care must be taken, be sure which media is the current selected when you access PHY registers.

Demonstration Circuit (A) : AX88790 + HomePNA 1M8 PHY

AX88790 10BASE-T/100BASE-TX & 1M HomePNA Application with NS83851 PHYceiver.(reference only)



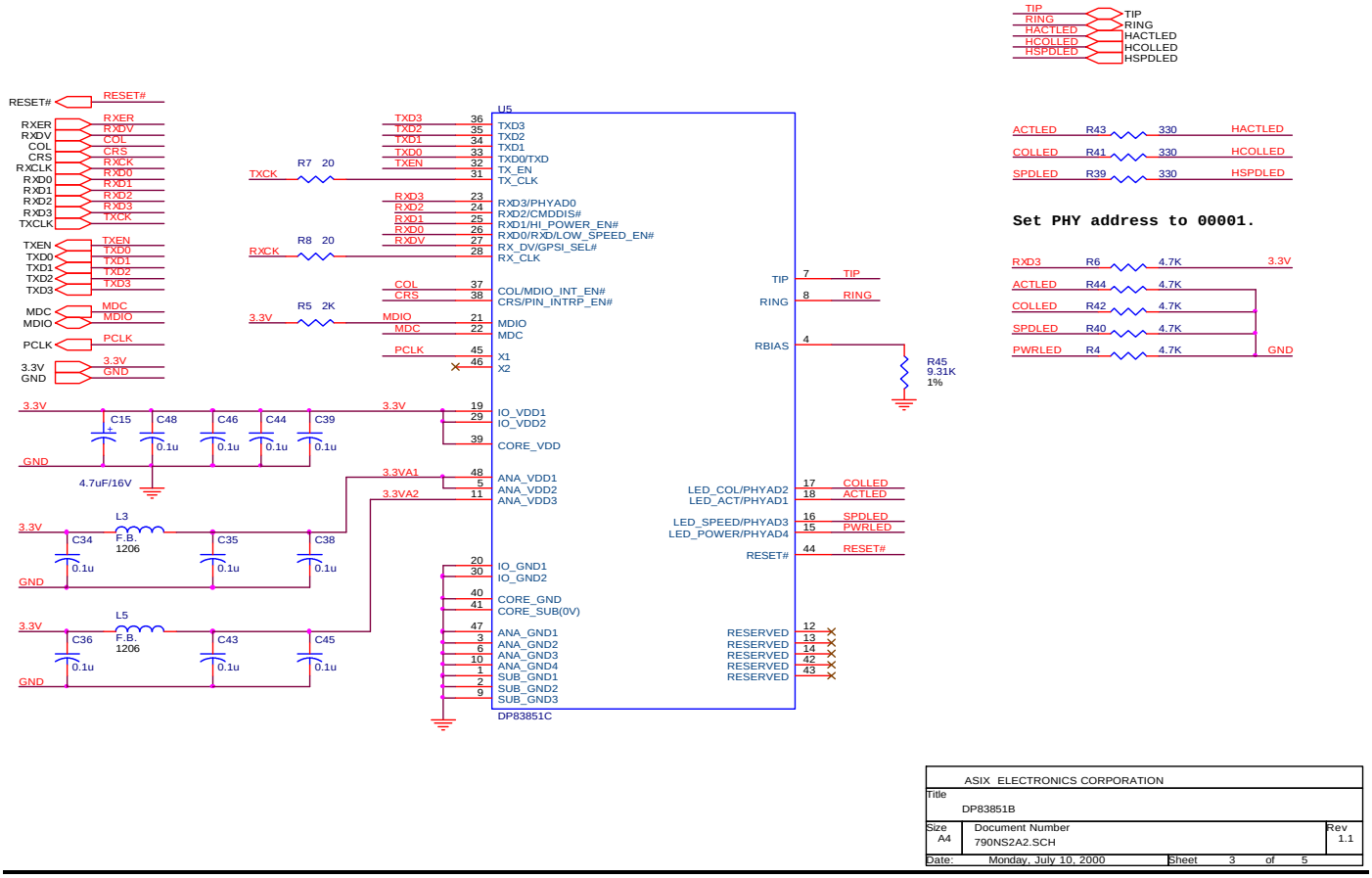
ASIX ELECTRONICS CORPORATION		
Title: PCMCIA INTERFACE		
Size: A4	Document Number: 790NS2A.SCH	Rev: 1.1
Date: Monday, July 10, 2000	Sheet 1 of 5	

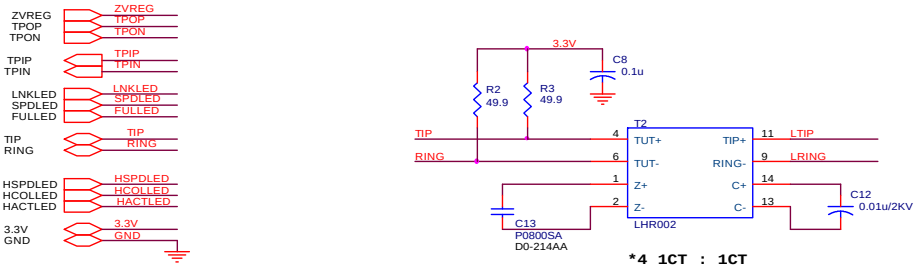


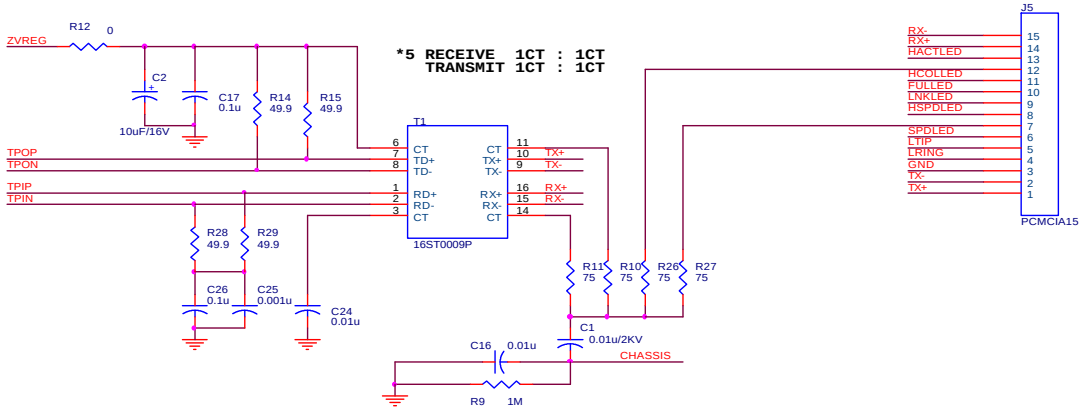
*2 Pin 50 PPD_SET = 0 : Internal PHY in normal mode.(default)
Pin 50 PPD_SET = 1 : Internal PHY in power down mode.(match up CIS)

*3 Pin 58 EEPROM SIZE = 0 : 93C46 type 256 byte EEPROM is used.
Pin 58 EEPROM SIZE = 1 : 93C56 type 512 byte EEPROM is used. (default)
Pin 116 I_OP = 0 : LNK/ACT & FULL/COL LED Display be used.
Pin 116 I_OP = 1 : LNK & ACT LED Display be used.

ASIX ELECTRONICS CORPORATION		
Title: AX88790		
Size: A3	Document Number: 790NS2A1.SCH	Rev: 1.1
Date: Monday, July 10, 2000	Sheet 2 of 5	







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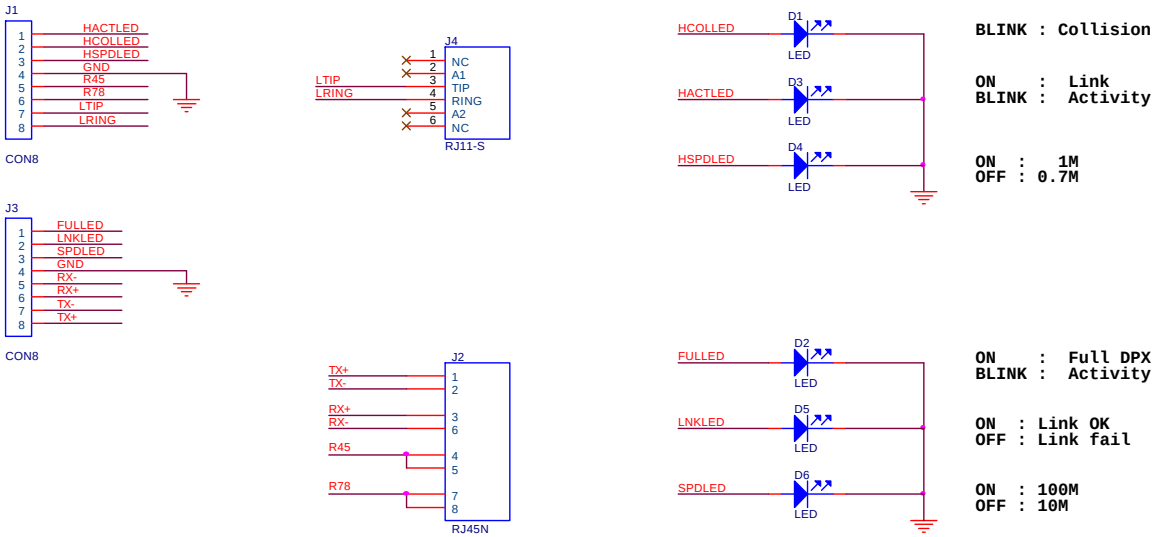
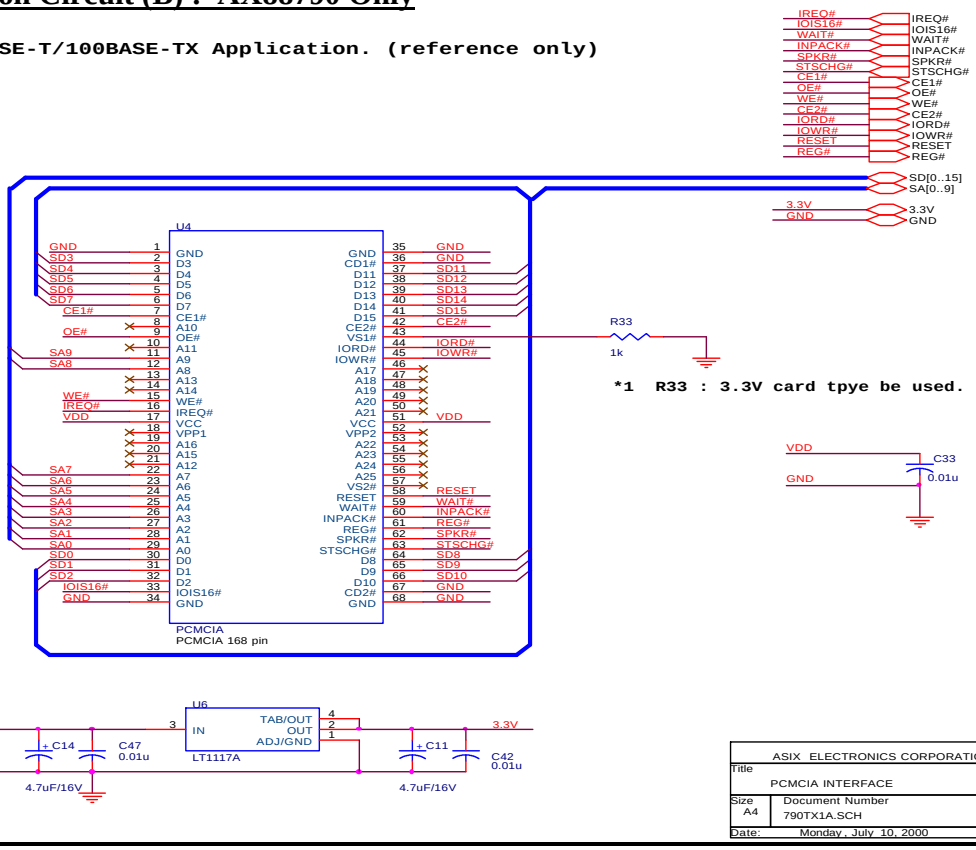
Date: Monday, July 10, 2000	Sheet 4 of 5	



ASIX ELECTRONICS CORPORATION		
Title: RJ45 / RJ11 CONNECT & LED		
Size: A4	Document Number: 790NS2A4.SCH	Rev: 1.1
Date: Monday, July 10, 2000	Sheet 5 of 5	

Demonstration Circuit (B) : AX88790 Only

AX88790 10BASE-T/100BASE-TX Application. (reference only)



ASIX ELECTRONICS CORPORATION		
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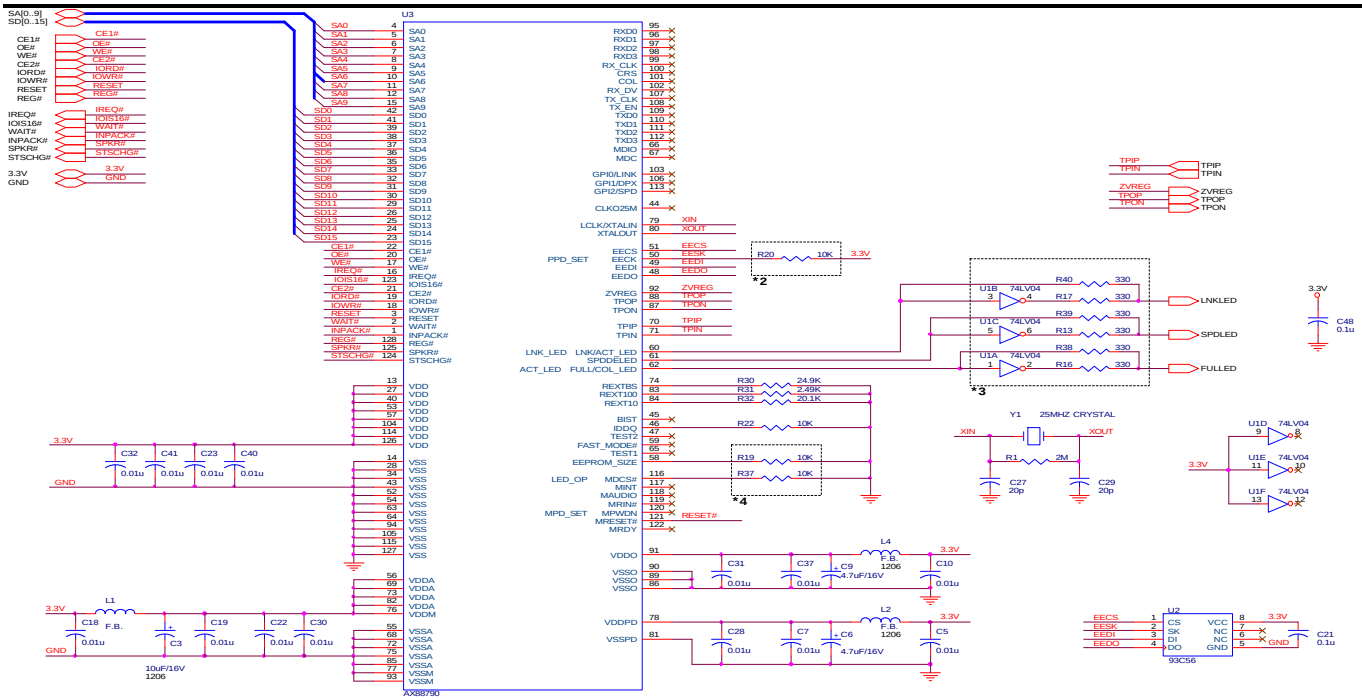
Size: A4	Document Number: 790TX1A.SCH	Rev: 1.1
Date: Monday, July 10, 2000	Sheet 1 of 4	

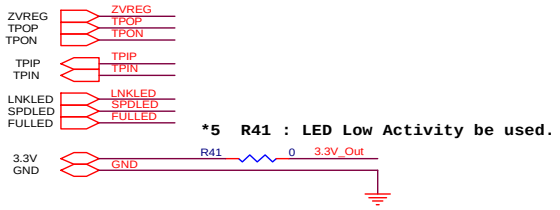


*2 Pin 50 PPD_SET = 0 : Internal PHY in normal mode.(default)
Pin 50 PPD_SET = 1 : Internal PHY in power down mode.(match up CIS)

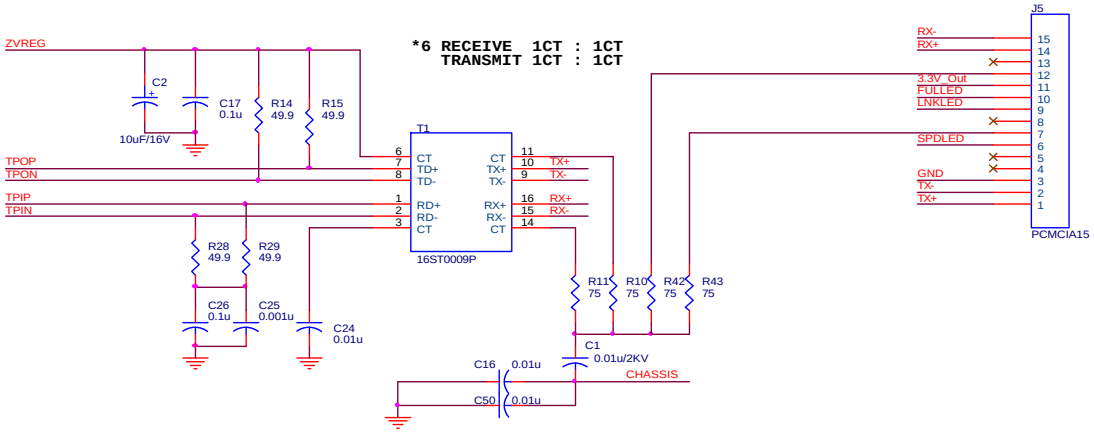
*3 LED Low Activity : R40,R39,R38 be used.
LED High Activity : R17,R13,R16,U1 be used.

*4 Pin 58 EEPROM SIZE = 0 : 93C46 type 256 byte EEPROM is used.
Pin 58 EEPROM SIZE = 1 : 93C56 type 512 byte EEPROM is used. (default)
Pin 116 I_OP = 0 : LNK/ACT & FULL/COL LED Display be used.
Pin 116 I_OP = 1 : LNK & ACT LED Display be used.

ASIX ELECTRONICS CORPORATION			
Title: AX88790			
Size: A3	Document Number: 790TX1A1.SCH		Rev: 1.2
Date: Thursday, August 31, 2000	Sheet 2 of 4		



***5 R41 : LED Low Activity be used.**



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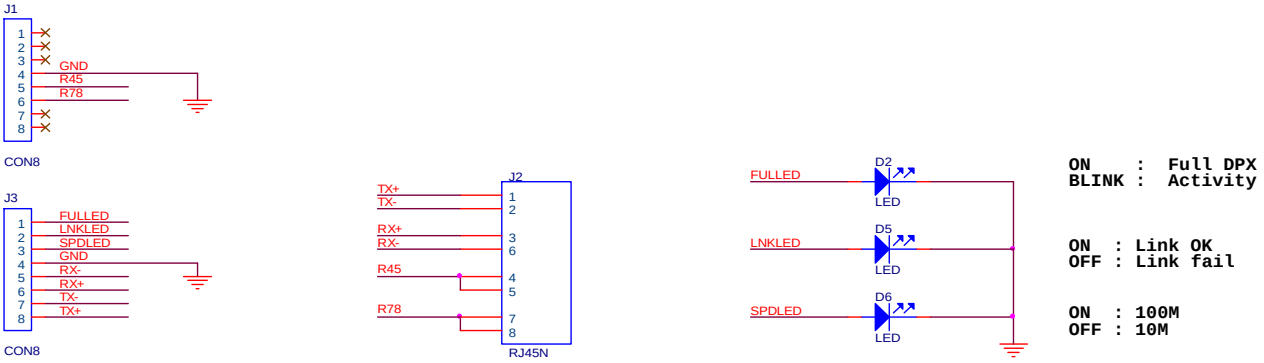
Date: Monday, July 10, 2000	Sheet 3 of 4	



ASIX ELECTRONICS CORPORATION			
Title: RJ45 CONNECT & LED			
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