Silicon Image

PanelLink®
Technology

SiI 1162
PanelLink Transmitter

Data Sheet

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Silicon Image, Inc.

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Application Information

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Revision History

Revision	Date	ECN	Comment
A	2/4/03	ECN-DS-0081-A	First Release.
B	3/15/2004	200400290	SiI1162CSU Universal part added; Fig 13,14,16 fixed; JEDEC Pkg code updated; Part marking spec updated; Pin 24 (CTL3/A1) fix; I²C Slave Addressing fix. PD# clarification for I²C mode. I²C register descriptions defaults clarified.

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General Description

The SiI 1162 transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions in a single link interface. The SiI 1162 transmitter uses a 12-bit interface, taking in one half-pixel per clock edge.

Designed to accommodate ultra high speed parallel interfaces such as the Intel DVO port, the SiI 1162 transmitter reduces pin count to a bare minimum and at the same time improves signal timing. The SiI 1162's innovative design eases board design requirements as well.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Scaleable Bandwidth: 25 - 165 megapixels per second
- Flexible Input Clocking: Single Clock Dual edge or Differential Clock input mode
- I^2C Slave Programming Interface
- Low Voltage Interface: 3.0V to 3.6V range and 1.0 to 1.9V range
- Monitor Detection supported through Hot Plug and Receiver Detection
- De-skewing Option: varies clock to data input timing
- Low Power: 3.3V core operation and power down mode
- Cable Distance Support: over 5 meter DVI cable
- DVI 1.0 Compliant with significantly greater margin than competitive solutions
- Low pin count and smaller 48-pin TSSOP package
- BIOS and driver compatible with SiI 164 transmitter
- Pb-Free Universal packaging (see page 1)

SiI 1162 Pin Diagram

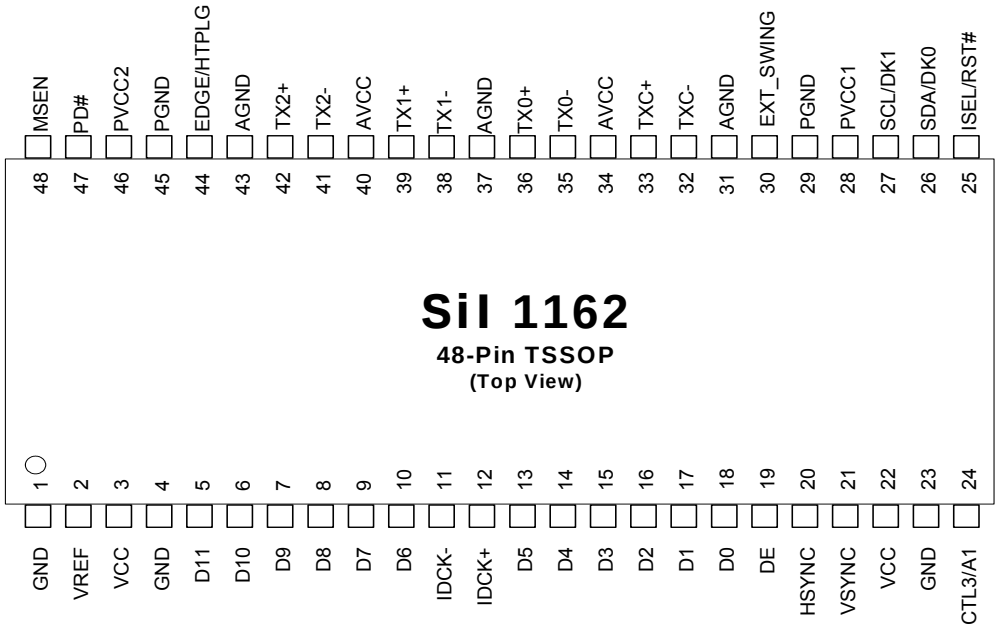


Figure 1. SiI 1162 Pin Diagram

Functional Block Diagram

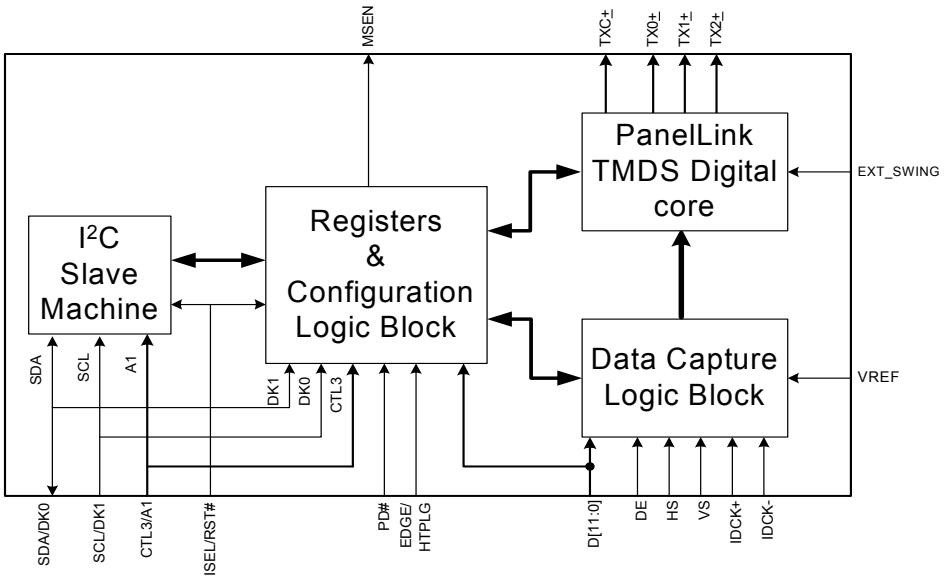


Figure 2. Functional Block Diagram

PanelLink TMDS Digital Core

The PanelLink TMDS core encodes video information onto three TMDS differential data lines and the differential clock. The video data is input by the Data Capture Logic Block, as a 12-bit bus, using differential clock with dual edge or single clock with dual edge. A resistor tied to the EXT_SWING pin is used to control the TMDS swing amplitude.

I²C Interface, Registers and Configuration Logic

The SiI 1162 can support either I²C mode or non-I²C mode. In I²C mode, the SiI 1162 uses a slave I²C interface, capable of running at 400kHz, for communication with the host. This interface is not 5V tolerant. If the switching levels from the host are not 3.3V, then a voltage level shifter must be used. See Figure 15 or Figure 16 for a system diagram.

The device may be powered down using the PD# pin or with an internal register. The SiI 1162 is reset using the ISEL/RST# pin.

A connected display may be detected using the DVI Hot Plug signal, attached to the HTPLG pin or with the Receiver Sense logic internal to the SiI 1162. The state of the detection, or an interrupt signal indicating a change of state, may be read from the MSEN bit. For systems with multiple I²C devices, pin A1 can be used to change the I²C address of the SiI 1162.

In non-I²C mode, de-skew pins DK0 and DK1 can be set to adjust the setup and hold times to the SiI 1162 by pull-up or pull-down resistors. The CTL3 pin can also be used for backward compatibility with older Silicon Image devices. The PD# pin can be used in non-I²C mode to put the device in power down. Similarly, the PD# bit in the registers can be used in I²C mode to put the device in power down. The EDGE pin can be used to control the polarity of the clock or the edge responsible to latch the first pixel of incoming data.

Data Capture Logic

Data is input to the SiI 1162 by way of a 12-bit bus. Logic operations such as inversion and edge swapping can be set by programmable registers described in I2C Register Definitions section or by setting control pins in non-I²C mode before transmitting over the TMDS lines. Voltage level input on VREF sets the SiI 1162 in High Swing or Low Swing Mode. In High Swing Mode, only single clock (IDCK+) dual edge is processed. IDCK- is ignored in High Swing Mode. In Low Swing Mode DVO mode, IDCK± differential clock dual edge is processed.

Electrical Specifications

Absolute Maximum Conditions

Absolute Maximum Conditions are defined as the worst-case condition the part will tolerate without sustaining damage. Permanent device damage may occur if absolute maximum conditions are exceeded. Proper operation under these conditions is not guaranteed. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_J	Junction Temperature (with power applied)			125	°C
T_{STG}	Storage Temperature	-65		150	°C

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)[1]	0	25	70	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)[2]			36	°C/W
	Thermal Resistance (Junction to Ambient)[3]			60	°C/W
	Thermal Resistance (Junction to Ambient)[4]			85	°C/W

Notes:
1. Airflow at 0m/s.
2. Includes soldered connection of E-pad to PCB. See page 1.
3. E-pad not soldered to multilayer PCB. See page 1.
4. E-pad not soldered to dual layer PCB. See page 1.

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Swing High-level Input Voltage	$V_{REF} = V_{CC}$	2.0		V_{CC} + 0.3	V
V_{IL}	High Swing Low-level Input Voltage	$V_{REF} = V_{CC}$	–0.3		0.8	V
V_{DDQ}[2]	Low Swing Voltage		1.0		3.0	V
V_{SH}	Low Swing High-level Input Voltage	$V_{REF} = V_{DDQ}/2$	$V_{DDQ}/2$ + 100mV			V
V_{SL}	Low Swing Low-level Input Voltage	$V_{REF} = V_{DDQ}/2$			$V_{DDQ}/2$ – 100mV	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			VCC + 0.8	V
I_{IL}	Input Leakage Current		-10		10	µA

Notes:
1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
2. VDDQ defines the maximum voltage level of Low Swing input. It is not an actual input voltage. Chip characterization for Low Swing operation is performed at 1.5V only. Voltage level of Low Swing input should never exceed absolute maximum rating.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50Ω R_{EXT_SWING} = 380Ω		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]				AVCC		V
V_{REF}	Input Reference Voltage	Low Swing		0.50	V_{DDQ}/2	0.95	V
		High Swing		3.0	3.3	3.6	V
I_{DOS}	Differential Output Short Circuit Current[1]	V_{OUT} = 0V				5	µA
I_{PDQ}	Quiet Power-down Current[2]	25°C Ambient, V_{cc} = 3.3V				2	mA
I_{PD}	Power-down Current[3]	IDCK = 165MHz, ½ pixel/clock edge, R_{EXT_SWING} = 380Ω, Worst Case Pattern[5] 0°C Ambient V_{cc} = 3.6V	Low Swing mode			2	mA
			High Swing mode			2	mA
I_{CCTL}	Transmitter Supply Current, Low-Swing	IDCK = 165MHz, ½ pixel/clock edge, R_{EXT_SWING} = 380Ω, Low Swing mode	Typical Pattern[4,6] 25°C Ambient V_{cc} = 3.3V		120		mA
			Worst Case Pattern[5,6] 0°C Ambient V_{cc} = 3.6V			150	mA
I_{CCTH}	Transmitter Supply Current, High-Swing	IDCK = 165MHz, ½ pixel/clock edge, R_{EXT_SWING} = 380Ω, High Swing mode	Typical Pattern[4,6] 25°C Ambient V_{cc} = 3.3V		115		mA
			Worst Case Pattern[5,6] 0°C Ambient V_{cc} = 3.6V			150	mA

Notes:

1. Guaranteed by Characterization.
2. Quiet Power-down current measured with no transmitter input pins toggling, but include source termination as described on page 1.
3. Power-down current measured with input data bus and control signals toggling.
4. Typical pattern contains a gray scale area, a checkerboard area and a text area.
5. Worst Case pattern contains black and white checkerboard pattern, each checker is one pixel wide.
6. Transmitter fitted with source termination and R_{EXT_SWING} at 380Ω.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{CIP}	IDCK Period	one pixel per clock	6		40	ns	Figure 3	4
F_{CIP}	IDCK Frequency	one pixel per clock	25		165	MHz	Figure 3	4
T_{CIH}	IDCK High Time	IDCK = 165MHz	2.6			ns	Figure 3	4
T_{CIL}	IDCK Low Time	IDCK = 165MHz	2.9			ns	Figure 3	4
S_{LHT}	Differential Swing Low-to-High Transition Time	R_{LOAD} = 50Ω, R_{EXT_SWING} = 380Ω	170	200	230	ps	Figure 4	6
S_{HLT}	Differential Swing High-to-Low Transition Time	R_{LOAD} = 50Ω, R_{EXT_SWING} = 380Ω	170	200	230	ps	Figure 4	6
T_{IJIT}	Worst Case IDCK Jitter				1	ns		2
T_{SHS}	Data, DE, VSYNC, HSYNC Setup Time to IDCK+ falling/rising edge	V_{REF} = VCC (High Swing Input)	0.5			ns	Figure 8	1,5,7
T_{HHS}	Data, DE, VSYNC, HSYNC Hold Time from IDCK + falling/rising edge	V_{REF} = VCC (High Swing Input)	0.6			ns	Figure 8	1,5,7
T_{SLS}	Data, DE, VSYNC, HSYNC Setup Time to IDCK+ falling/rising edge	V_{REF} = V_{DDQ}/2 (Low Swing Input)	See note 8			ns	Figure 7	1,5
T_{HLS}	Data, DE, VSYNC, HSYNC Hold Time from IDCK+ falling/rising edge	V_{REF} = V_{DDQ}/2 (Low Swing Input)	See note 8			ns	Figure 7	1,5
T_{HDE}	DE high time				8191	T_{CIP}	Figure 6	1
T_{LDE}	DE low time		128			T_{CIP}	Figure 6	1,5
T_{DDF}	VSYNC and HSYNC Delay from DE falling edge			1		T_{CIP}	Figure 5	
T_{DDR}	VSYNC and HSYNC Delay to DE rising edge			1		T_{CIP}	Figure 5	
T_{I2CDVD}	SDA Data Valid Delay from SCL high to low transition	C_L = 400pf			1000	ns	Figure 9	3
T_{RESET}	ISEL/RST# Signal Low Time required for valid reset		50			µs	Figure 10	
T_{STEP}	De-skew step size increment	See page 1 for range				ps	Figure 12	

Notes:

1. Guaranteed by design.
2. Actual jitter tolerance may be higher depending on the frequency of the jitter.
3. All Standard mode I^2C (100kHz and 400kHz) timing requirements are guaranteed by design.
4. Minimum frequency (maximum IDCK period) defined per DVI 1.0 Specification, section 2.3.1.
5. DE Low time defined as per DVI 1.0 Specification, Section 3.4 Link Timing Requirements.
6. TMDS rise and fall times per DVI 1.0 Specification, Table 4-4, as 0.4*T_{BIT} maximum, where T_{BIT} = 1/10th of T_{CIP}.
7. Typical VCC is defined at 3.3V.
8. The SiI 1162 Low Swing timing mode is designed to meet all Intel DVO operational requirements. The DVO interface is proprietary to Intel Corp. and therefore these timings cannot be disclosed here. Refer to the Intel DVO 2.0 specification for details.

Input Timing Diagrams

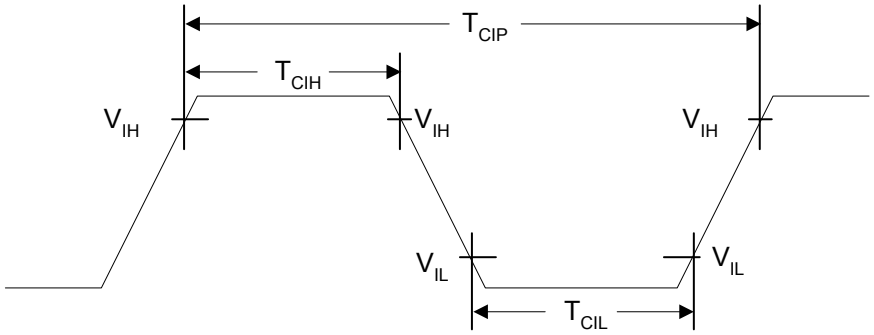


Figure 3. Clock Cycle/High/Low Times in High Swing Mode

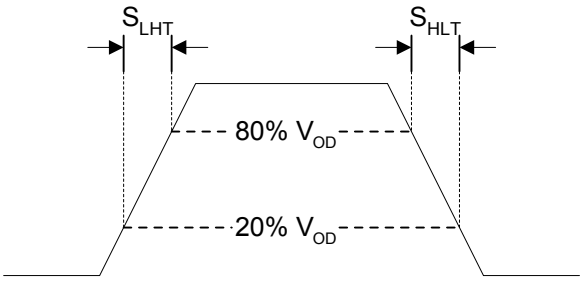


Figure 4. Differential Transition Times

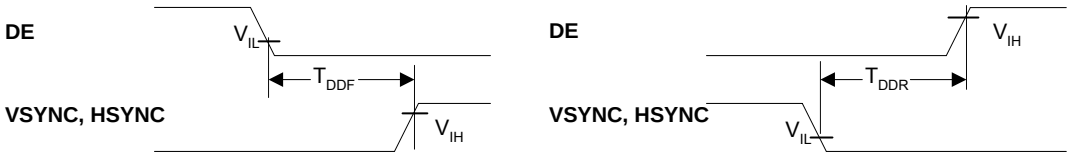


Figure 5. VSYNC, HSYNC Delay Times to DE

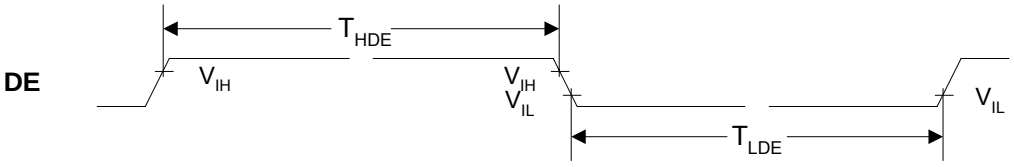


Figure 6. DE High/Low Times

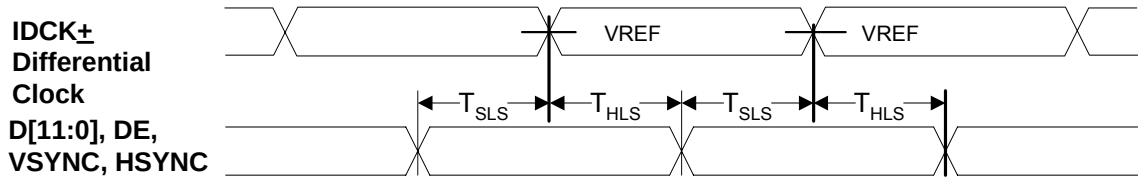


Figure 7. Low Swing Control and Data Setup/Hold Times to IDCK+ Differential Clock

Note that VREF is set to $V_{DDQ}/2$ in Low Swing Mode.

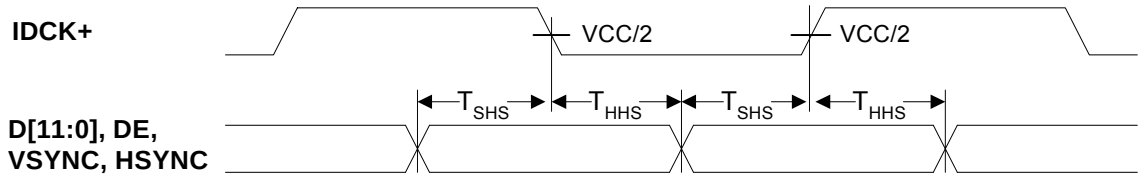


Figure 8. High Swing Control and Data Setup/Hold Times to IDCK+

Note that typical VCC is 3.3V.

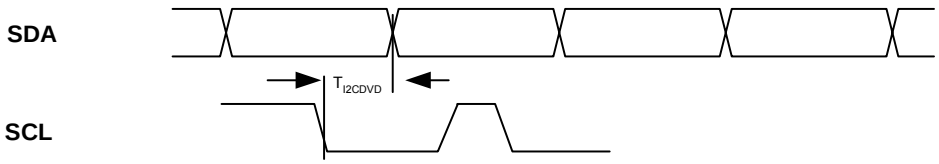


Figure 9. I²C Data Valid Delay (driving Read Cycle data)

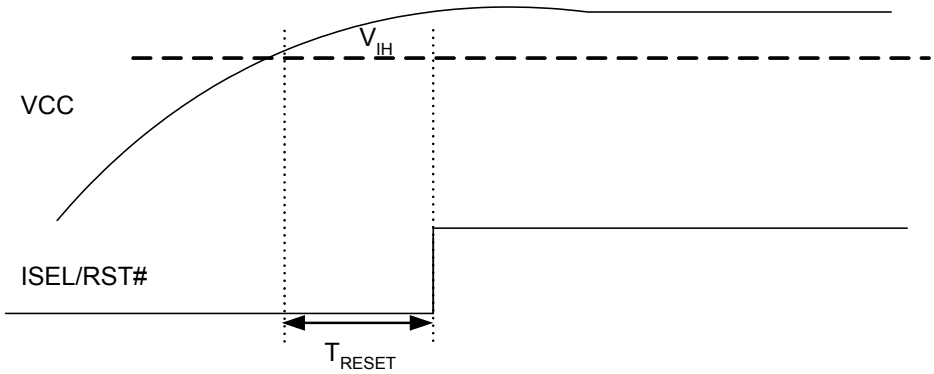


Figure 10. ISEL/RST# Minimum Timing

Note that VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before ISEL/RST# is high. ISEL/RST# must also be pulled LOW for T_{RESET} before accessing registers.

Data Mapping

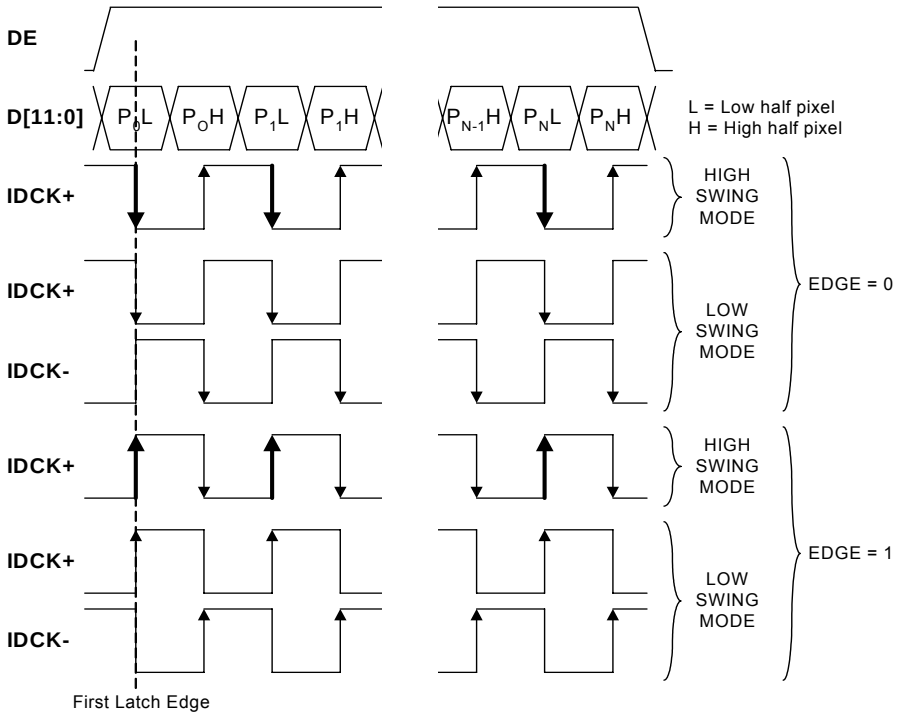


Figure 11. Logical Interface Options for 12-bit Mode

Table 1. 12-bit Mode Data Mapping

	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
Pin Name	Low	High	Low	High	Low	High
D11	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

Notes

1. In Figure 11, clock edges represented by arrows signify the latching edge. The dark arrows indicate the primary latch edge. The lower half of the pixel (L) is latched by the primary clock edge.
2. Color Pixel Components: R = RED, G = GREEN, B = BLUE
3. Bit significance within a color: [7:0] = [MSB:LSB]
4. In Low Swing Mode, IDCK+ represents the differential clock.

Data De-skew

Input clock to data setup/hold time can be adjusted through the use of the de-skew feature. It should be noted that it is the clock that is being adjusted internally. The configuration pins DK[1:0] or applicable I^2C registers can be used to vary the input setup/hold time by T_{CD}.

If ISEL/RST# pin is set LOW and the SiI 1162 is not in I^2C mode, the DK[1:0] pins can be used to control the T_{CD} value. The DK[1:0] pins contain internal pull-down resistors and if left unconnected, they will be set to 00. If ISEL/RST# pin is set HIGH and the SiI 1162 is in I^2C mode, the DK[1:0] bits can be used to control the T_{CD} value Table 2 lists the De-skew time increment range and the effect on Setup and Hold.

Table 2. DK[1:0] Increments and Effect on Setup and Hold times

DK[1:0]	De-Skew Time (T_{CD})	Setup and Hold Time Effect
01	-100ps to -400ps	Better Setup time, higher Hold time.
00	0 ps	No effect. Default and recommended setting.
10	+100ps to +400ps	Better Hold time, higher Setup time.
11	0 ps	No effect but not recommended.

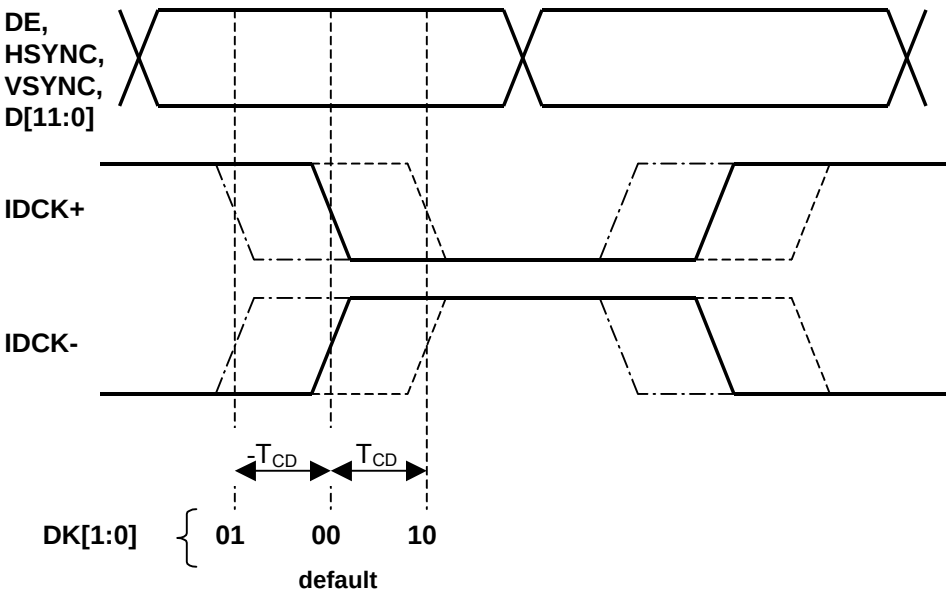


Figure 12. SiI 1162 De-skewing Feature Timing

Pin Descriptions

Input Pins

Pin Name	Pin #	Type	Description
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11	18 17 16 15 14 13 10 9 8 7 6 5	In	12-bit pixel bus input. This bus inputs one-half pixel (12-bits) at every latch both falling and rising edge of the clock.
IDCK+	12	In	Input Data Clock +. This pin must be used in High Swing Mode for dual edge data latching. In Low Swing Mode Input clock is sensed differentially (IDCK+ minus IDCK-).
IDCK-	11	In	Input Data Clock –. This clock is only used in low swing mode (VREF = V_{DDQ}/2). In Low Swing Mode Input clock is sensed differentially (IDCK+ minus IDCK-). In case only IDCK+ is supplied in low swing mode, tie this pin to the same voltage level (V_{DDQ}/2) with VREF pin. Dual clock single edge clocking (using either rising or falling edge of both clock inputs) is not supported.
DE	19	In	Data enable. This signal is high when input pixel data is valid to the transmitter and low otherwise. It is critical that this signal have the same setup/hold timing as the data bus.
HSYNC	20	In	Horizontal Sync input control signal.
VSYNC	21	In	Vertical Sync input control signal.
CTL3/A1	24	In	The use of this multi-function input depends on the setting of ISEL/RST#. This input is regular high-swing 3.3V CMOS level input, not affected by V_{REF}. It has a weak pull-down resistor so that if left unconnected, it will be LOW. **ISEL/RST# = LOW** General Purpose Input CTL3 is active, for backward compatibility. **ISEL/RST# = HIGH** A1 is active, this bit is used to set the second bit of the I^2C device address.

Status Pin

Pin Name	Pin #	Type	Description
MSEN	48	Out	Monitor Sense. This pin is an open collector output. The behavior of this output depends on whether I^2C interface is enabled or disabled. **I^2C bus is disabled (ISEL/RST# = LOW)** A HIGH level indicates a powered on receiver is detected at the differential outputs. A LOW level indicates a powered on receiver is not detected. This function can only be used in DC-coupling systems. **I^2C bus is enabled (ISEL/RST# = HIGH)** The output is programmable through the I^2C interface (see register definitions, page 14). An external 5K pull-up resistor is required on this pin for systems without internal pull-up resistor.

Configuration/Programming Pins

Pin Name	Pin #	Type	Description
ISEL/RST#	25	In	I^2C Interface Select: If HIGH, then the I^2C interface is active. If LOW, the I^2C is inactive and the chip configuration is read from the configuration strapping pins. This pin also acts as an asynchronous reset to the I^2C interface controller. The reset is active when this input is held LOW. If ISEL/RST# = LOW, then the DK[1:0] pins should be used to configure the De-skew option.
SCL/DK1	27	In	I^2C Clock: If ISEL/RST# = HIGH, then this pin is the I^2C clock input. This pin is an open collector input. Data Deskew 1: If ISEL/RST# = LOW, then this pin selects the data deskew DK1. DK1 has a weak internal pull down resistor. Please refer to Data De-skew section or Table 2 for illustration.

SDA/DK0	26	In	I^2C Data:
			If (ISEL/RST# = HIGH), then this pin is the I^2C data line.
			This pin is an open collector input.
			Data Deskew 1:
			If (ISEL/RST# = LOW), then this pin selects data deskew DK0.
			DK0 has a weak internal pull down resistor.
			Please refer to Data De-skew section on page 1 or Table 2 for illustration.

EDGE/HTPLG	44	In	Hot Plug input: If the I^2C bus is enabled (ISEL/RST# = HIGH), then this pin is used to monitor the "Hot Plug" detect signal. (Refer to the DVI Specification.) **NOTE:** This Input is ONLY 3.3V tolerant and has no internal de-bouncer circuit. Edge mode: If the I^2C bus is disabled (ISEL/RST# = LOW), then this pin decides the polarity of the input clock. Low selects falling edge latched first in dual edge mode High selects rising edge latched first in dual edge mode

Input Voltage Reference Pin

Pin Name	Pin #	Type	Description
VREF	2	Analog In	Input Reference Voltage: Selects the swing range of the digital parallel data inputs (D[11:0], DE, VSYNC, HSYNC and IDCK+). To enable High Swing Mode, VREF should be set to 3.3V. When VREF is below 2.0V, the digital parallel data inputs are Low Swing inputs. In Low Swing mode, VREF must be set to V_{DDQ}/2. For DVO mode, VREF should be set to 0.75V. CTL3 is always set to High Swing Mode.

Power Management Pin

Pin Name	Pin #	Type	Description
PD#	47	In	Power Down (active LOW) In non-I^2C mode (ISEL/RST# = LOW), a HIGH level on PD# indicates normal operation and a LOW level indicates power down mode. During power down mode, digital input, output buffers and the PanelLink Digital core are powered down however MSEN and I^2C interface are NOT disabled. In I^2C mode (ISEL/RST# = HIGH), the PD# pin is ignored. Power down is controlled via the PD# bit in the I^2C registers (bit 0, reg 0x8). Note that when ISEL/RST# = HIGH, this pin should be tied LOW to ensure the chip is powered off when RESET is asserted.

Differential Signal Data Pins

Pin Name	Pin #	Type	Description
TX0+	36	Analog	TMDS Low Voltage Differential Signal output data pairs.
TX0-	35	Analog	
TX1+	39	Analog	
TX1-	38	Analog	
TX2+	42	Analog	
TX2-	41	Analog	
TXC+	33	Analog	TMDS Low Voltage Differential Signal output clock pairs.
TXC-	32	Analog	
EXT_SWING	30	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. This resistor sets the amplitude of the voltage swing. A smaller resistor value sets a larger voltage swing and vice versa. For remote display applications with source termination, a 380Ω resistor is recommended (see page 1). In lieu of a 380Ω resistor, the more commonly available 390Ω resistor can also be used to achieve satisfactory results. Without the source termination (for short cables), use a 510Ω resistor.

Power and Ground Pins

Pin Name	Pin #	Type	Description
VCC	3,22	Power	Digital VCC, must be set to 3.3V nominal.
GND	1,4,23	Ground	Digital GND.
AVCC	34,40	Power	Analog VCC, must be set to 3.3V nominal.
AGND	31,37,43	Ground	Analog GND.
PVCC1	28	Power	PLL Driver Analog VCC, must be set to 3.3V nominal.
PVCC2	46	Power	Filter PLL Analog VCC, must be set to 3.3V nominal.
PGND	29,45	Ground	PLL Analog GND.

I²C Registers

I²C Register Mapping

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Notes
0x0	VND_IDL (RO)								0x01	
0x1	VND_IDH (RO)								0x00	
0x2	DEV_IDL (RO)								0x06	
0x3	DEV_IDH (RO)								0x00	
0x4	DEV_REV (RO)								0x00	
0x5	RSVD									
0x6	FRQ_LOW (RO)								0x20	
0x7	FRQ_HIGH (RO)								0x64	
0x8	RSVD		VEN (R/W)	HEN (R/W)	RSVD		EDGE (RW)	PD# (RW)	0x34	
0x9	VLOW (RO)	MSEL[2:0] (RW)			TSEL (RW)	RSEN (RO)	HTPLG (RO)	MDI (RW)	0x06	3
0xA	RSVD	DK[1:0] (RW)		RSVD	CTL[3:0] (RW)				0x90	
0xB	RSVD									
0xC	VDJK[7:0]								0x89	5
0xD	RSVD									
0xE	RSVD									
0xF	RSVD									

Notes:

1. All values are Bit 7(msb) and Bit 0(lsb).
2. Registers that can be written and read from are listed as (RW) while registers that can be read only are listed as (RO).
3. After the RESET signal is de-asserted in I²C mode, only MDI retains the programmed value set before the reset. All other R/W registers do not retain their value after a reset, but are set back to the default values shown in the table.
4. Registers and bits listed as RSVD are reserved and for Silicon Image, Inc. use only.
5. Default setting for the VDJK register 0x0C is 0x89, which is optimum for most applications.

I²C Register Definitions

Register Name	Access	Description
VND_IDL	RO	Vendor ID Low byte (0x01)
VND_IDH	RO	Vendor ID High byte (0x00)
DEV_IDL	RO	Device ID Low byte (0x06)
DEV_IDH	RO	Device ID High byte (0x00)
DEV_REV	RO	Device Revision (0x00)
FRQ_LOW	RO	Low frequency limit in Megahertz. (0x20). IDCK frequency limit.
FRQ_HIGH	RO	High frequency limit minus 65MHz in Megahertz. (0x64). IDCK frequency limit.
HEN	RW	Horizontal Sync Enable: 0 – HSYNC input is transmitted as fixed LOW 1 – HSYNC input is transmitted as is (Default after RESET)
VEN	RW	Vertical Sync Enable: 0 – VSYNC input is transmitted as fixed LOW 1 – VSYNC input is transmitted as is (Default after RESET)
EDGE	RW	Edge Select (same function as EDGE pin) 0 –Falling edge latched first in dual edge mode (Default after RESET) 1 –Rising edge latched first in dual edge mode
PD#	RW	Power Down mode (same function as PD# pin) 0 – Power Down (Default after RESET) 1 – Normal operation
VLOW	RO	Voltage Swing Mode 0 – VREF signal indicates low swing inputs 1 – VREF indicates high swing inputs
MSEL[2:0]	RW	Select source of the MSEN output pin 000 – Force MSEN outputs high (disabled) (Default after RESET) 001 – Outputs the MDI bit (interrupt) 010 – Outputs the RSEN bit (receiver detect) 011 – Outputs the HTPLG bit (hot plug detect) 1XX – Reserved
TSEL	RW	Interrupt Generation Method 0 – Interrupt bit (MDI) is generated by monitoring RSEN (Default after RESET) 1 – Interrupt bit (MDI) is generated by monitoring HTPLG
RSEN	RO	This bit is HIGH if a powered on receiver is connected to the transmitter outputs, LOW otherwise. This function is only available for use in DC-coupled systems.
HTPLG	RO	Hot Plug Detect input, the state of HTPLG pin can be read from this bit.
MDI	RW	Monitor Detect Interrupt: 0 – Detection signal has changed logic level (write one to this bit to clear) 1 – Detection signal has not changed state
DK[1:0]	RW	De-Skewing Setting (Always enabled in I²C mode): 00 – Default Setting (Default after RESET with ISEL/RST#=HIGH) 01 – Maximum Hold time 10 – Maximum Setup time 11 – No Effect
CTL[3:0]	RW	General Purpose bits. (Default after RESET = 0x0)
VDJK	RW	VDJK register should be programmed to 0x89.

Note that the **VND_ID**, **DEV_ID** and **DEV_REV** fields are identical to the values in the SiI 164 transmitter. This provides backward compatibility with earlier BIOS and driver support. No changes are needed for the SiI 1162.

I²C Slave Interface

The SiI 1162 slave state machine does not require an internal clock and supports only byte read and write. Page mode is not supported. The 7-bit binary address of the I²C machine is "0111 00A_1R" where R =1 sets a read operation while R=0 sets a write operation. Pin A1 by default has a weak internal pull down resistor, making the default I²C address 0x70. To set the value of A1 to a bit 1 or to set the I²C address for the SiI 1162 to 0x72, a pull up resistor should be added. Please see Figure 13 for a byte read operation and Figure 14 for a byte write operation. For more detailed information on I²C protocols please refer to I²C Bus Specification version 2.1 available from Philips Semiconductors Inc.

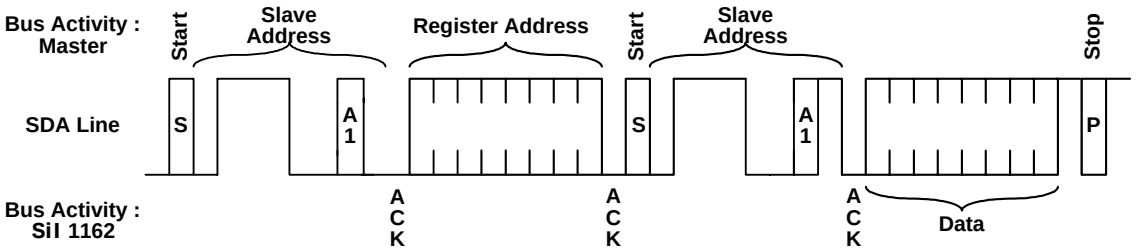


Figure 13. I²C Byte Read

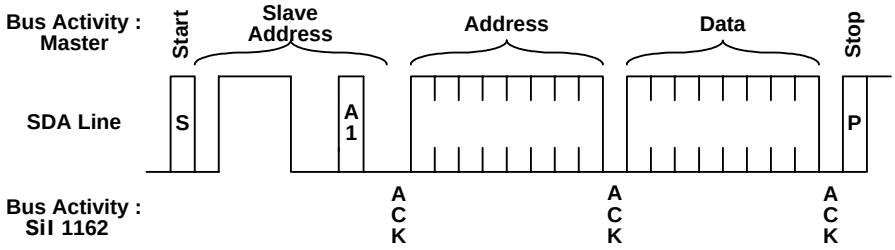


Figure 14. I²C Byte Write

I²C Programming Sequence Example

To program the SiI 1162 under the following conditions, use the sample programming sequence in Table 3:

- Data latched in 12-bit mode,
- Dual Edge Clock with Primary Edge as the falling edge,
- De-skew enabled at nominal setting, and
- No Hotplug detection through MSEN pin.

Table 3. Sample Programming Sequence for SiI 1162

Register	Value	Description
0x08	0x30	Enable HEN, VEN, 1st data latched on falling edge with PD# low until all registers are programmed.
0x09	0x00	MSEN disabled.
0x08	0x31	Set PD# to High after the registers above have been programmed.

Enabling Hot Plug Detection Mode

As documented in the VESA Digital Flat Panel Standard, all monitors are required to support Hot Plug Detection but support is optional for the host. The SiI 1162 supports the Hot Plug Detect feature. In I^2C mode, use the HTPLG input. It should be noted that the HTPLG pin on the SiI 1162 is only 3.3V tolerant therefore HTPLG voltage level from the DVI connector should be level shifted or clamped at 3.3V.

When the voltage level at the HTPLG pin is 3.3V, the HTPLG bit will be set to 1. To output the HTPLG bit via the MSEN pin, register bits MSEL [2:0] should be programmed to 0b011.

The SiI 1162 can also be programmed to enable the Hot Plug Detection Mode via the Receiver Sense function. In this mode, HTPLG pin is not required. By programming MSEL [2:0] to 0b010, SiI 1162 will output the RSEN bit state though the MSEN pin when the SiI 1162 is connected to a powered receiver.

RESET Description

The input pin ISEL/RST# serves as an asynchronous RESET (active LOW) for the I^2C slave controller in I^2C mode. The programming registers that are accessible over the I^2C bus do not retain their previous values during and after the RESET. Register bits PD# and MSEL[2:0] are both disabled after RESET. The minimum low time for proper RESET is T_{RESET}. The state of these bits is set during the RESET period according to the following rules:

- **After a RESET, the SiI 1162 will be turned OFF.** When RESET is asserted, the SiI 1162 power down control bit, PD#, is forced to 0. When the SiI 1162 comes out of RESET (ISEL/RST# is set HIGH), the SiI 1162 will be turned OFF. To turn the SiI 1162 back ON, the PD# bit must be set to 1 over the I^2C bus.

- **After a RESET, MSEN output is disabled.** When RESET is asserted, MSEN [2:0] is forced to '000'. This causes the MSEN output to be tri-stated.

Design Recommendations

1.5V to 3.3V I²C Bus Level-Shifting

To program the SiI 1162 via I²C mode, SDA and SCL swing level must be 3.3V. DVO sources have I²C swing of 1.5V. To ensure proper initialization of the SiI 1162 a bi-directional voltage level-shifting circuit between the SiI 1162 I²C bus and the VGA or driving source should be implemented. To achieve this, use either a dual N-channel transistor like Fairchild Semiconductor's NDC7002N or the Philips GTL2010 High Speed Bus Switch. Refer to Figure 15 for a schematic example using a dual N-channel transistor for translating an I²C 1.5V signal to 3.3V I²C signal and vice versa.

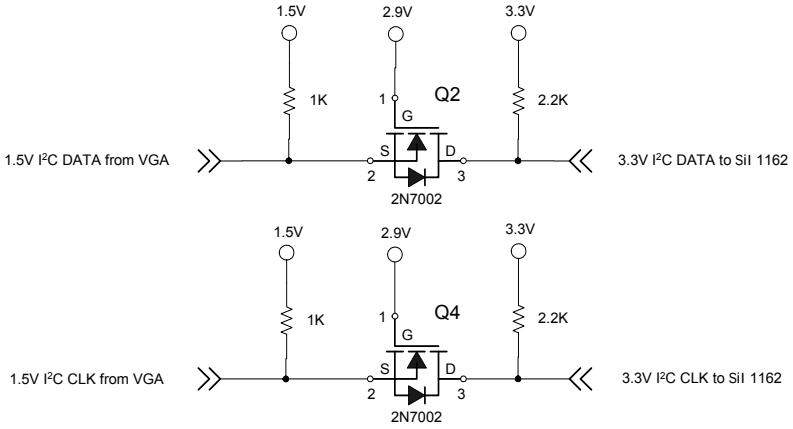


Figure 15. I²C Bus Voltage Level-Shifting using Fairchild NDC7002N

Figure 16 illustrates a schematic example using the Philips GTL 2010 to achieve a 1.5V to 3.3V and 5V bi-directional level-shift.

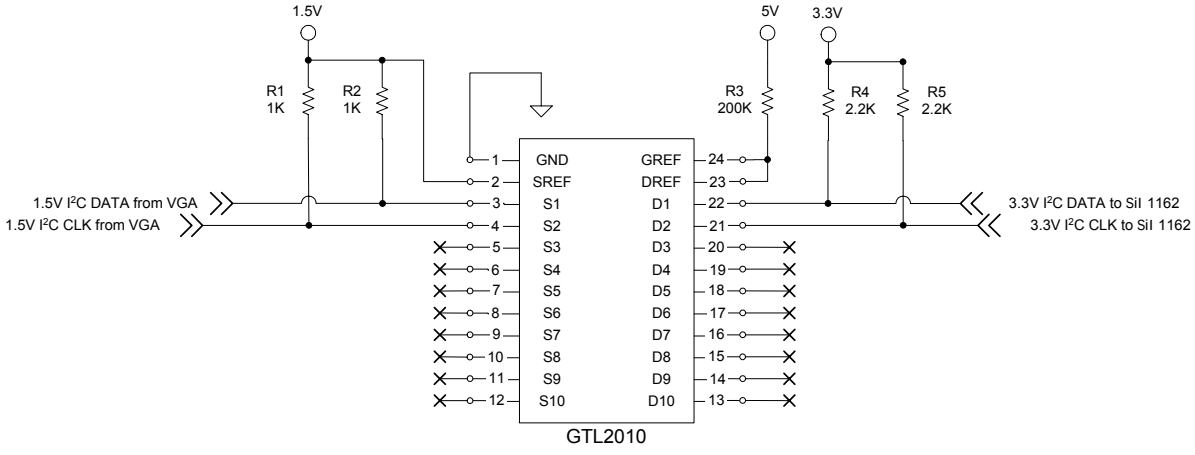


Figure 16. I²C Bus Voltage Level Shifting using Philips GTL 2010

Voltage Ripple Regulation

The power supply to VCC pins is very important to the proper operation of the transmitter. Two examples of regulators are shown in Figure 17 and Figure 18.

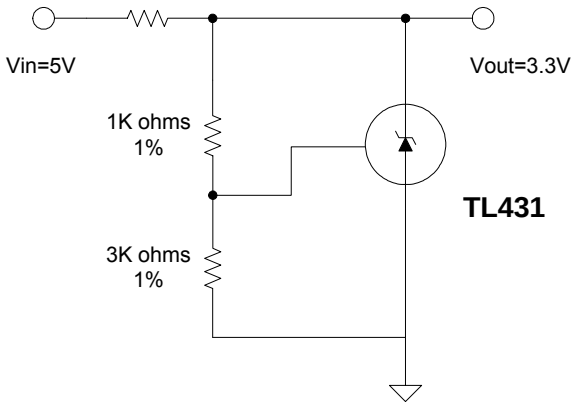


Figure 17. Voltage Regulation using TL431

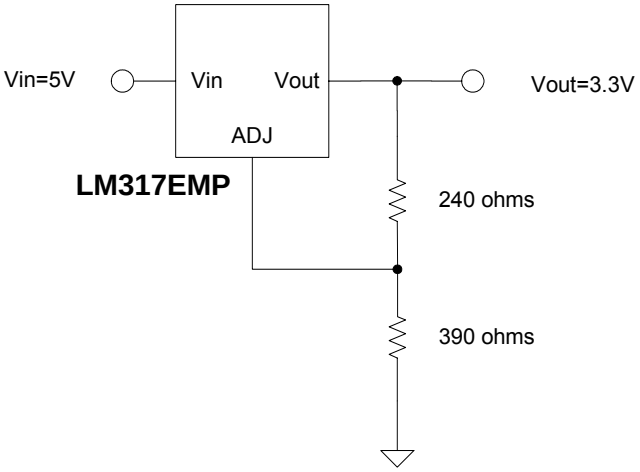


Figure 18. Voltage Regulation using LM317

Decoupling and bypass capacitors are also involved with power supply connections, as described in detail in Figure 19 and Figure 20.

PCB Ground Planes

All ground pins on the device should be connected to the same, contiguous ground plane in the PCB. This helps to avoid ground loops and inductances from one ground plane segment to another. Such low-inductance ground paths are critical for return currents, which affect EMI performance. The entire ground plane surrounding the PanelLink transmitter should be one piece, and include the ground vias for the DVI connector.

Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 20. Place these components as closely as possible to the PanelLink device pins, and avoid routing through vias if possible, as shown in Figure 19, which is representative of the various types of power pins on the transmitter.

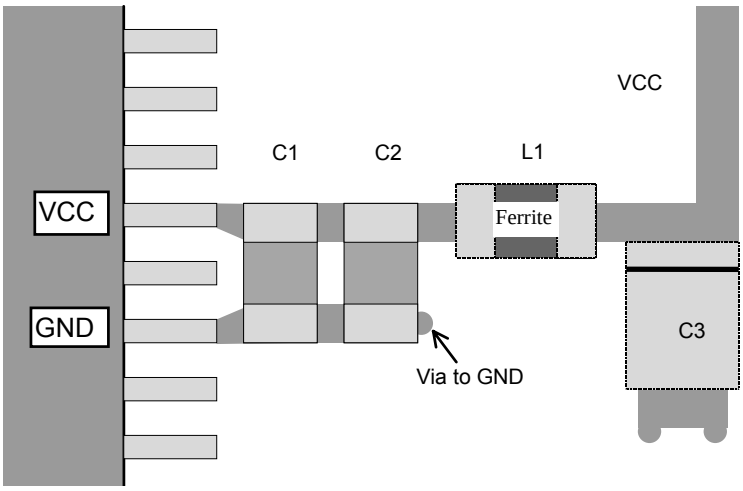


Figure 19. Decoupling and Bypass Capacitor Placement

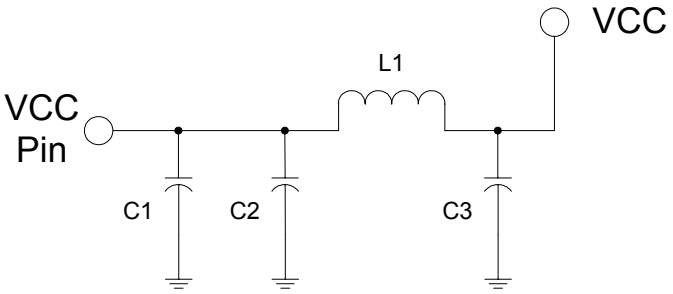


Figure 20. Decoupling and Bypass Schematic

The values shown in Table 4 are recommendations that should be adjusted according to the noise characteristics of the specific board-level design. Pins in one group (such as VCC) may share C2, the ferrite and C3. Each Power pin should have a separate C1 placed as close as possible to the pin.

Table 4. Recommended Components

C1	C2	C3	L1
100 – 300 pF	2.2 – 10 µF	10 µF	+200Ω

Series Damping Resistors on Parallel Inputs

Series resistors (22Ω to 33Ω) are effective in lowering the data-related emissions and reducing reflections. Series resistors should be placed as close as possible to the D[11:0], HSYNC, VSYNC, DE and IDCK+ output pins of the chip driving the transmitter. See Figure 21 for an illustration.

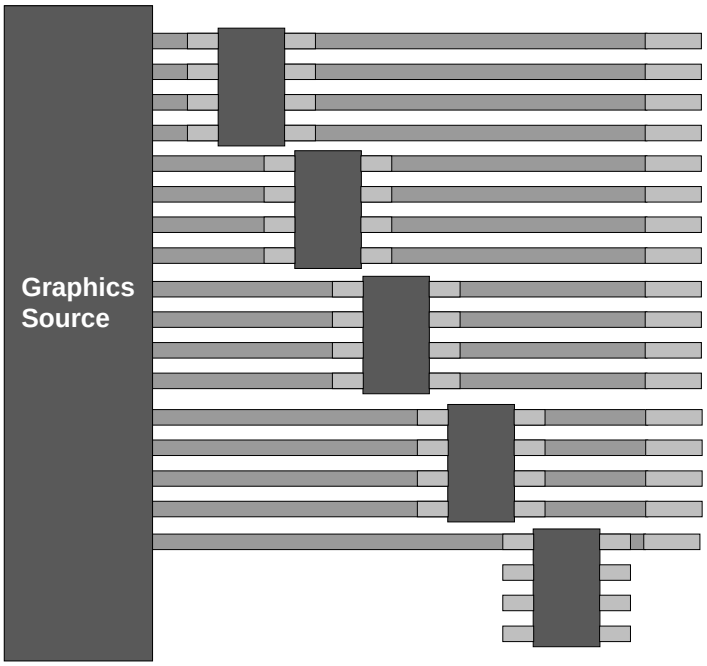


Figure 21. Transmitter Input Series Damping Resistors

Source Termination Resistors on Differential Outputs

Source termination, consisting of a 300Ω resistor and a 0.1µF capacitor, may be used on the differential outputs of the SiI 1162 to improve signal swings. See Figure 22 for an illustration. Repeat the circuit for each of the four differential output pairs: TX0+, TX1+, TX2+, TXC+.

Note that the specific value for the source termination resistor and capacitor will depend on the PCB layout and construction. Different values may be needed to create optimum DVI-compliant output waveforms from the transmitter.

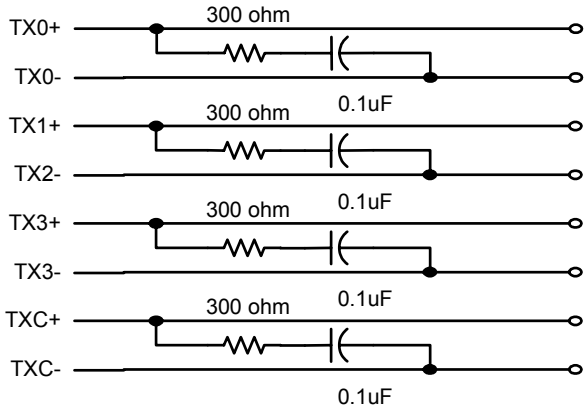
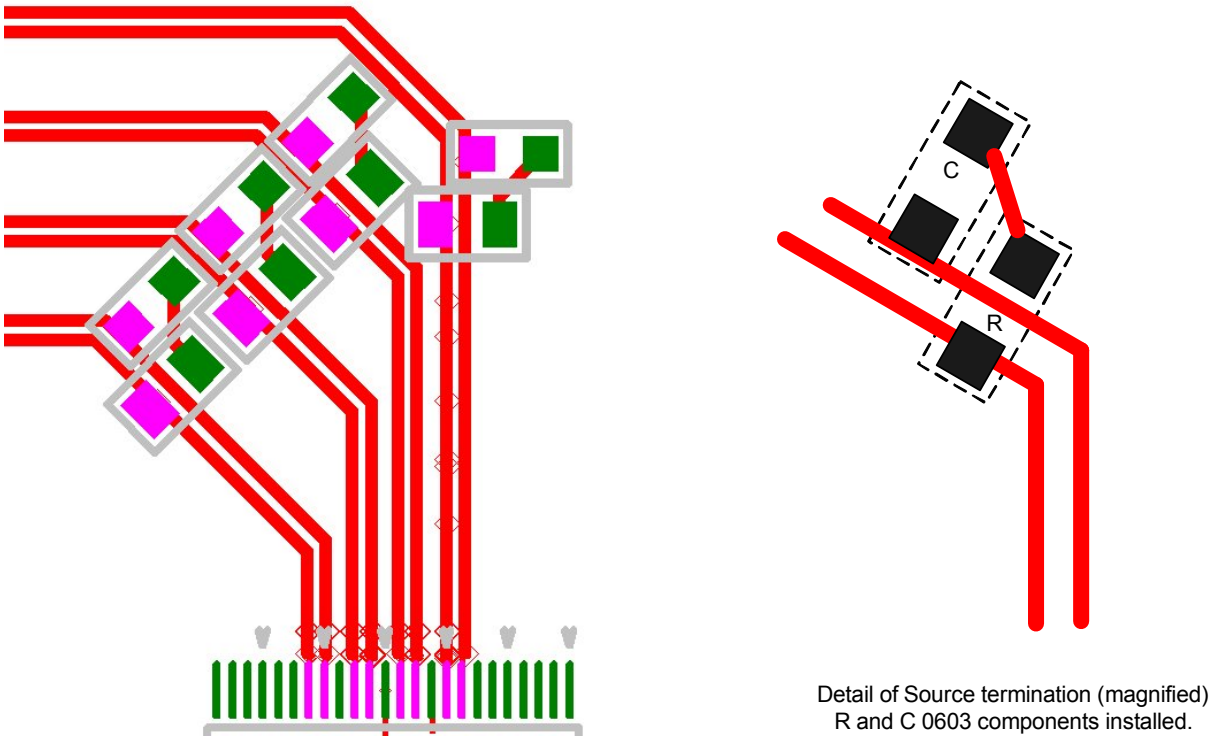


Figure 22. Differential Output Source Terminations

Source termination suppresses signal reflection to prevent non-DVI compliant receivers from erroneously sampling the TMDS signals at high frequencies(beyond 135MHz). The impact on DVI compliant receivers is minimal. Therefore Silicon Image recommends source termination for most applications. Note that the capacitor is required to meet DVI idle mode DC offset requirements and must not be omitted. Note also that the signal suppression requires the R_{EXT_SWING} value to be changed. Refer to recommendations on page 1. Power consumption will be slightly higher when using source termination.



Detail of Source termination (magnified)
R and C 0603 components installed.

Figure 23. Source Termination Layout Illustration

The layout in Figure 23 has been developed to minimize trace stubs on the differential TMDS lines, while providing pads for the source termination components(left-hand magnified view). Source termination components should be placed close to the transmitter pins. The resistor and capacitor are shown installed on the pads provided (right-hand magnified view).

Transmitter Layout

The routing for the SiI 1162 chip is relatively simple since no spiral skew compensation is needed. However, a few small precautions are required to achieve the full performance and reliability of DVI.

The Transmitter can be placed fairly far from the output connector, but care should be taken to route each differential signal pair together and achieve impedance of 100Ω between the differential signal pair. However, note that the longer the differential traces are between the transmitter and the output connector, the higher the chance that external signal noise will couple onto the low-voltage signals and affect image quality.

Do not split or have asymmetric trace routing between the differential signal pair. Vias are very inductive and can cause phase delay if applied unevenly within a differential pair. Vias should be minimized or avoided if possible by placing all differential traces on the top layer of the PCB.

Figure 24 illustrates an incorrect routing of the differential signal from the SiI 1162 to the DVI connector. Figure 25 illustrates the correct method to route the differential signal from the SiI 1162 to the DVI connector. Figure 26 illustrates recommended routing for differential traces at the DVI connector.

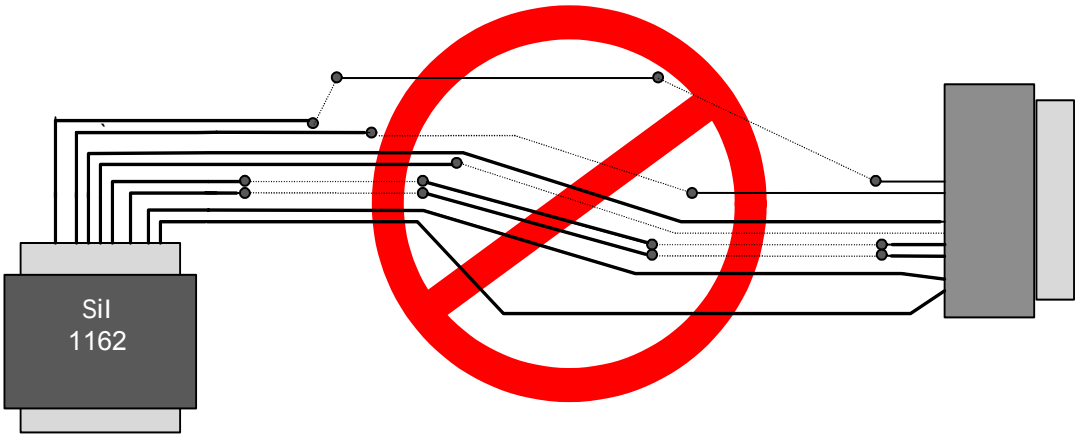


Figure 24. Example of Incorrect Differential Signal Routing

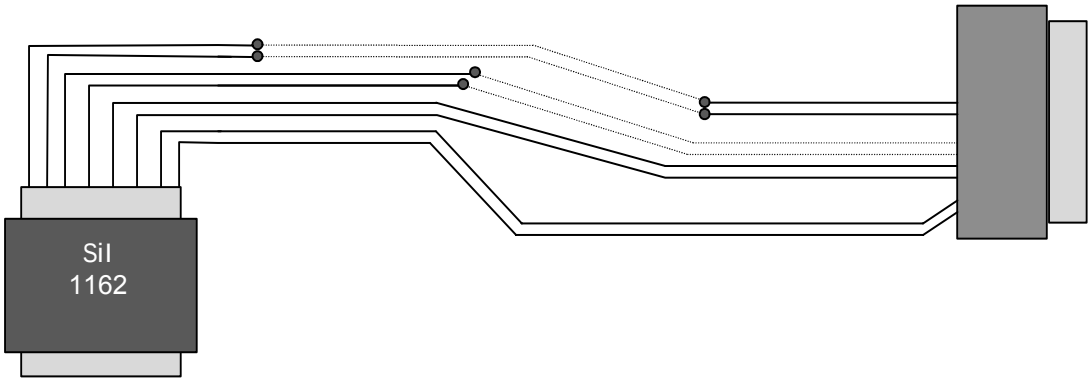


Figure 25. Example of Correct Differential Signal Routing

In addition to following the trace routing recommendations, length differences between intra-pair traces listed in column 2 of Table 5 and inter-pair traces listed in column 3 of Table 5, should be controlled to minimize DVI skew. Spacing between inter-pair DVI traces should be observed to reduce trace-to-trace couplings. For example, having wider gaps between inter-pair DVI traces will minimize noise coupling. It is also strongly advised that ground not be placed adjacent to the DVI traces on the same layer. Table 5 lists the recommended limits for the parameters listed above.

Table 5. Routing Guidelines for DVI Traces

Parameter	Intra-pair or Differential pair length	Inter-pair or Differential pair to Differential pair length	Recommended Inter–pair Trace Separation Based on 2 Layer Board	Recommended Inter–pair Trace Separation Based on 4 Layer Board
Max	±0.75”	±3”		
Min			2x trace width	2x trace width

The layout in Figure 26 illustrates an optimized AGP ADD Card with source termination, input termination resistors and DVI connector mapping which follows the guidelines listed above. The trace length from the SiI 1162 to the DVI connector can be long; however, it is strongly recommended that the intra-pair and inter-pair trace lengths follow the guidelines listed in Table 5.

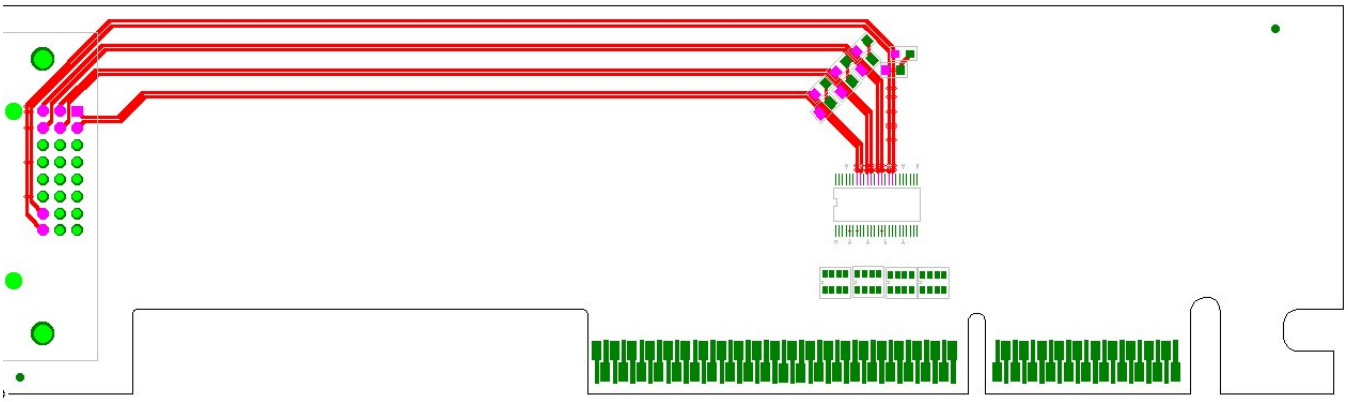


Figure 26. Source Termination to DVI Connector Illustration

Recommended Circuits

Note that the Hot Plug pin on the DVI connector will output a voltage up to 5V. A level-shifting circuit as illustrated in Figure 27 is needed to connect to the HTPLG pin on the SiI 1162, as the device's input pin is not 5V tolerant.

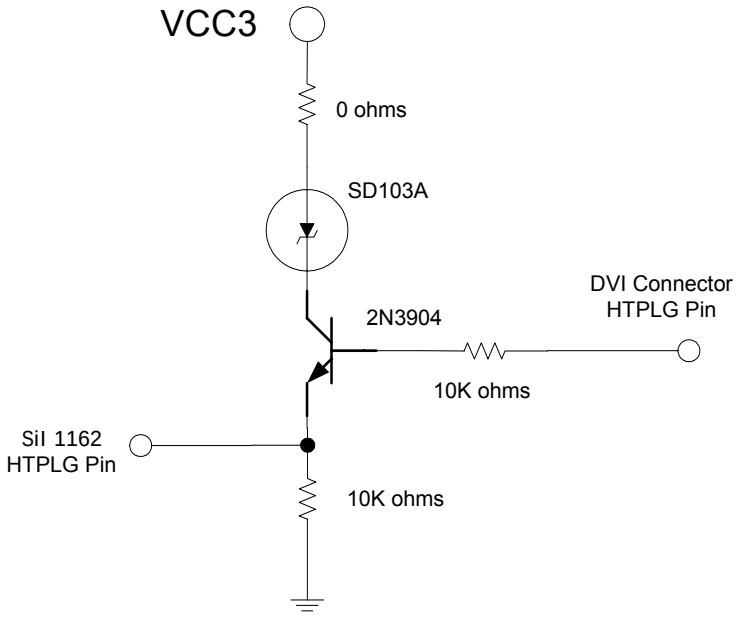
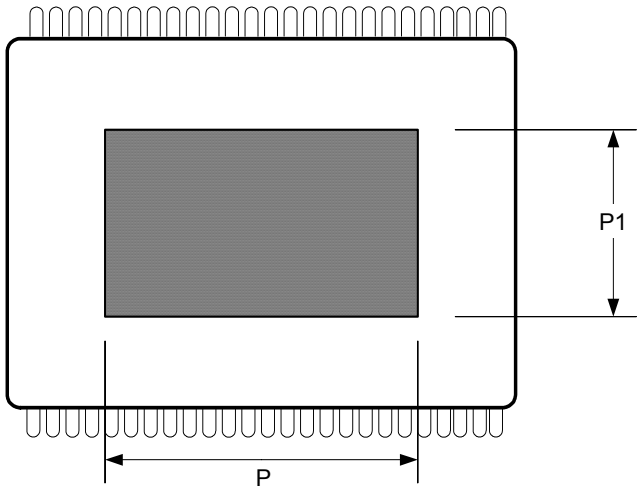


Figure 27. Recommended Hot Plug Connection

Packaging

E-pad Enhancement

The SiI 1162 is packaged in a 48-pin TSSOP package with E-pad. The E-pad dimensions are shown in Figure 28.



E-pad Dimensions

		typ	max
P1	E-pad Height		2.3
P	E-pad Width		5.5

All dimensions are in millimeters.

E-pad is centered on the package center lines.

Figure 28. E-pad Diagram

The E-pad is designed to allow better heat dissipation, and can be soldered down to further improve heat dissipation in extreme operating environments (ambient temperatures above 70°C) or for high operating frequencies (well in excess of 165MHz). For all other applications the E-pad does not need to be soldered down.

Determining Heat Dissipation Requirements

Generally, the thermal performance of a package can be represented by the following parameter (JEDEC standard JESD 51-2, 51-6):

θ_{JA} , Thermal resistance from junction to ambient

$$\theta_{JA} = (T_J - T_A) / P_H$$

Where: T_J is the junction temperature
T_A is the ambient temperature
P_H is the power dissipation

θ_{JA} represents the resistance to the heat flow from the chip to ambient air. It is an index of heat dissipation capability. Lower θ_{JA} means better thermal performance.

Implementation of the thermal landing area, combined with complete soldering of the package to the landing area, results in a θ_{JA} of 36°C/W for a multi-layer PCB (4 or more layers). If the SiI 1162 package is assembled to a two-layer PCB without the thermal landing area, the θ_{JA} increases to 85°C/W; if instead it is assembled to a multi-layer PCB without the thermal landing area, θ_{JA} is only 60°C/W due to the improved ability of the multi-layer PCB to carry away heat.

In order to determine the usefulness of soldering the SiI 1162 to the PCB thermal landing area, the following discussion may be helpful.

- In the case of no thermal landing pad on a two-layer PCB (θ_{JA} = 85°C/W), assuming a worst-case scenario with operation at the maximum ambient temperature (70°C), maximum voltage (3.6V), and with peak current draw (150mA), the junction temperature would be about 46°C above ambient, or 116°C. This is still well below the maximum allowable junction temperature of 125°C.
- In the same case but on a multi-layer PCB (θ_{JA} = 60°C/W), the junction temperature would only be about 103°C.
- If in this same application airflow became restricted and the ambient temperature peaked at 90°C, the chip would be operating out of spec. But by soldering the chip in the described application to a thermal landing area on the PCB (θ_{JA} = 36°C/W), the junction temperature could be limited to 110°C.

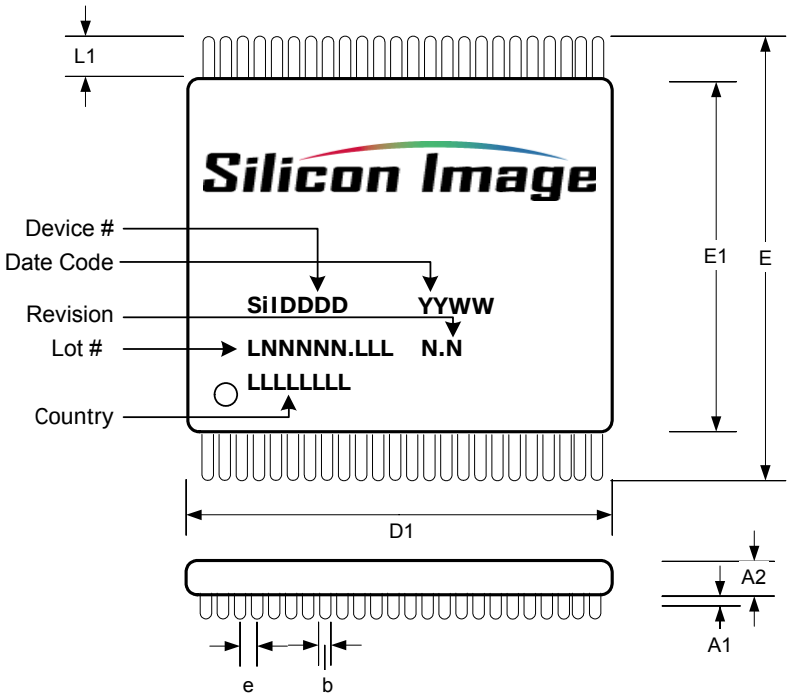
Based on this discussion, it is clear that designing a thermal landing area on the PCB for use with the SiI 1162 part is rarely necessary, but could be considered for applications where unanticipated extremes might be encountered. Operating outside of chip specifications is not recommended; contact your Silicon Image representative for analysis of non-standard operational requirements.

Designing with E-pad Landing Area

If designing the PCB to solder down the E-pad, keep the following in mind.

- The ground connections from die to lead-frame are down-bonded to the E-pad to minimize ground inductance. Therefore, the E-pad must **not** be electrically connected to any other voltage level except ground (GND).
- When providing a thermal landing area for soldering the E-pad, design the PCB with a clearance of at least 0.25mm between the edge of the E-pad and the inner edges of the lead pads to avoid any electrical shorts.
- The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias can double as ground connections, attaching internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package.
- For optimum thermal performance, it is recommended that the via diameter be 12 to 13 mils (0.30 to 0.33mm) and the via barrel be plated with 1 ounce copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be ‘tented’ with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1mm) larger than the via diameter.
- Package stand-off is also a consideration. For a nominal stand-off of 0.1mm (see Figure 29, dimension ‘A1’), the stencil thickness of 5 to 8 mils should provide a good solder joint between the E-pad and the thermal land. The aperture opening should be subdivided into an array of smaller openings.

Dimensions and Marking



JEDEC Package Code MO-153-CD

		typ	max
A	Thickness		1.10
A1	Stand-off		0.15
A2	Body Thickness		0.95
D1	Body Size	9.70	
E1	Body Size	4.40	4.50
E	Footprint		6.40
L1	Lead Length		0.95
b	Lead Width		0.23
c	Lead Thickness		0.20
e	Lead Pitch	0.40	

Dimensions in millimeters.

Overall thickness A=A1+A2.

Lead length L1 = (E-E1)/2.

Device	**Device Number**
Standard	SiI1162
Pb-Free	SiI1162U

Legend	**Description**
LNNNNN.LLL	Lot Number
YY	Year of Mfr
WW	Week of Mfr
N.N	Revision Number
LLLLLLL	Country of Packaging

Figure 29. 48-pin TSSOP Package Dimensions and Marking Specification

Ordering Information

Standard Part Number: SiI1162CS48

Pb-Free Part Number: SiI1162CSU ('U' designates universal lead-free package)

Note: All Silicon Image Pb-Free (Universal) packages are also rated for the standard Sn/Pb reflow process. Please refer to the document (SiI-CM-0058) "Reflow Temperature Profile of Standard Leaded and Lead-free or Green Packages", for more details.

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