SH66L06A

1K 4-bit Micro-controller with LCD Driver

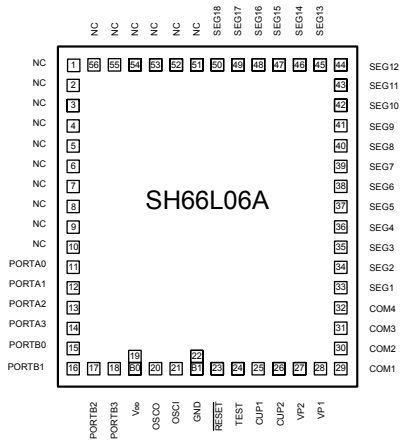
Features

- SH6610C-based single-chip 4-bit micro-controller with LCD driver
- ROM: 1024 X 16 bits
- RAM: 288 X 4 bits
  - 32 System Control Register
  - 256 Data memory
  - 18 LCD RAM
- Operation Voltage: 1.2V - 1.7V
- 8 CMOS Bi-directional I/O pads
- 4-Level Stack (Including Interrupts)
- Two 8-bit Auto Re-Loaded Timers/Counters
- Warm-Up Timer
- Powerful Interrupt Sources:
  - External interrupt (Low active)
  - Timer0 interrupt
  - Timer1 interrupt
  - PORTB interrupt (Low active)
- Oscillator (Code Option)
  - Crystal Oscillator: 32.768kHz
  - RC Oscillator: 131kHz
- Instruction Cycle Time (4/f**osc**)
- LCD Driver:
  - 18SEG X 4COM (1/4 Duty, 1/3 Bias)
  - 18SEG X 3COM (1/3 Duty, 1/2 Bias)
- Two Low Power Operation Modes: HALT And STOP
- Built-in Watchdog Timer (Code Option)
- Built-in Voltage Doubler And Tripler Charge Pump Circuit
- Built-in Alarm Generator
- Low power consumption
- Bonding option for multi-code software
- Available in CHIP FORM

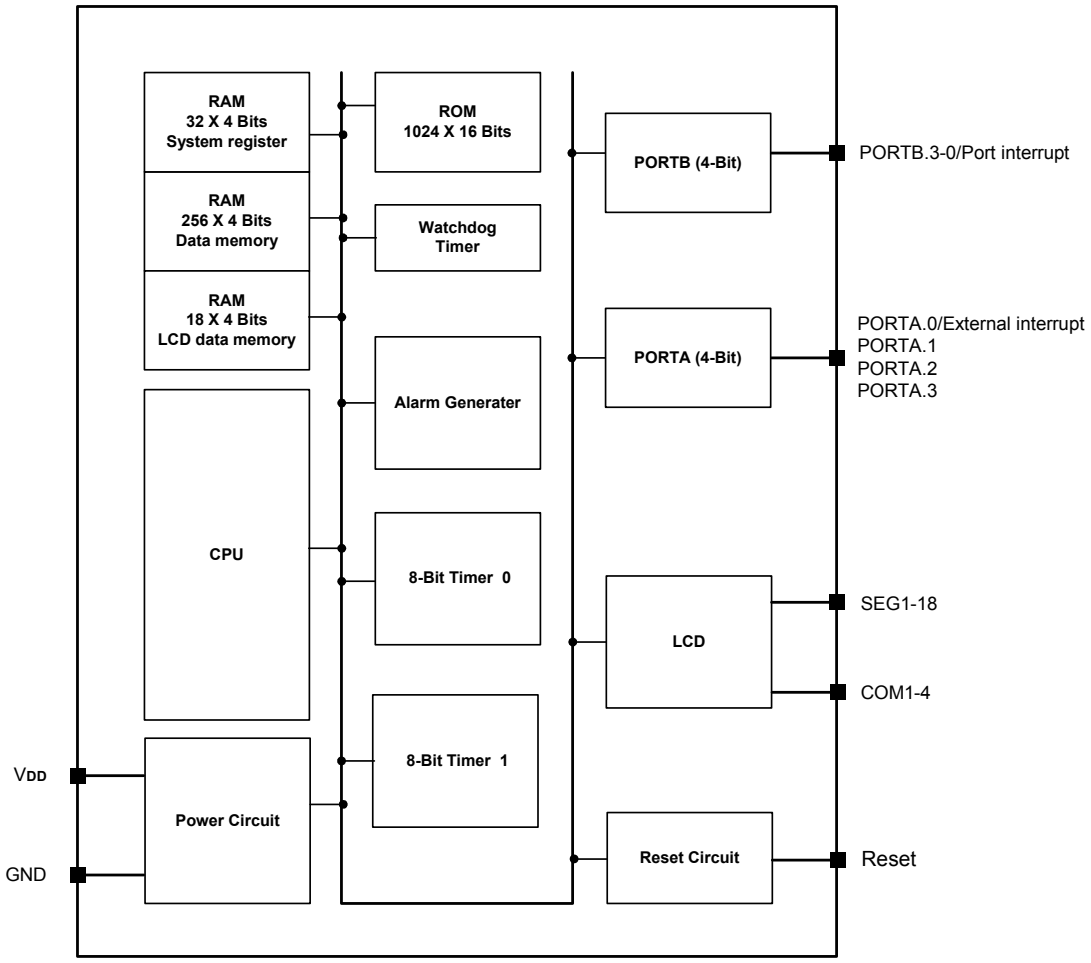
General Description

SH66L06A is a single-chip 4-bit micro-controller. This device integrates a SH6610C CPU core, SRAM, timer, alarm generator, LCD driver, I/O port, voltage pump and program ROM. The SH66L06A is suitable for calculator application.

Pad Configuration



Block Diagram



Pad Description (Total 58 pads for mask type)

Pad No.	Designation	I/O	Description
33 - 50	SEG1 - 18	O	Segment signal output for LCD display
29 - 32	COM1 - 4	O	Common signal output for LCD display
28, 27	VP1, VP2	P	Power supply pad for LCD driver
25, 26	CUP1 - 2	P	Connection for voltage doubler capacitor
24	TEST	I	Test pad internally pull-down. (No connect for user)
23	$\overline{\text{RESET}}$	I	Pad reset input
19	V_{DD}	P	Power supply pad
	B0	I	Bonding option (Internally pull-low)
	B1	I	Bonding option (Internally pull-high)
22	GND	P	Ground pad
20	OSCO	O	OSC output pad. No output in RC mode.
21	OSCI	I	OSC input pad, connected to a crystal or external resistor.
11 - 14	PORTA.0 - 3	I/O	Bit programmable I/O, PORTA.0 could be external interrupt input ($\overline{\text{INT}}$) PORTA.1, PORTA.2 could be buzzer output PORTA.1 (BD), PORTA.2 ($\overline{\text{BD}}$)
15 - 18	PORTB.0 - 3	I/O	Bit programmable I/O, vector interrupt (Active low level)
51 - 56, 1 - 10	NC	-	Not used

Which, I: input; O: output; P: Power; Z: High impedance

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code Bit7 - Bit4 is placed into TBR and Bit3-Bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H-3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address Bit9 - Bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC by the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register and I/O: $000 - $01F
Data memory $020 - $11F:
LCD RAM space: $300 - $311: (18 X 4 bits)

RAM bank table:

Bank0 B = 0	**Bank1** B = 1	**Bank2** B = 2	**Bank6** B = 6
$020 - $07F	$080 - $0FF	$100 - $17F	$300 - $3FF

Where, B: RAM bank bit use in instructions

2.2. Configuration of System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags register
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit2-0: Timer0 Mode register
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit2-0: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble register
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble register
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register low nibble register
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter register high nibble register
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A - $0C	-	-	-	-	-	Reserved
$0D	-	-	B1	B0	R	Bit1-0: Bonding option
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	-	LCDOFF	HLM	PAM	R/W	Bit0: PORTA.1, PORTA.2 as Alarm O/P control register Bit1: Heavy load Mode control register Bit2: LCD display OFF control register
$14	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control register
$15	PPULL	1	1	-	R/W	Bit2-1: must keep it to “1”. In the User’s program. Bit3: Port pull-up control register
$16 - $19	-	-	-	-	-	Reserved
$1A	WDT	-	-	-	R/W	Watchdog timer overflow flag register
$1B	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1D - $1F	-	-	-	-	-	Reserved

For SH66L06A, after the chip reset, please first write *11*B to $15. Otherwise, the halt current and stop current will be abnormal

3. ROM

The ROM can address 1024 X 16 bits of program area from $000 to $3FF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Jump to External interrupt service routine
$002	JMP*	Jump to TIMER0 service routine
$003	JMP*	Jump to TIMER1 service routine
$004	JMP*	Jump to PB service routine (PORTB)

* JMP instruction can be replaced by any instruction.

4. Initial State

4.1. System Register State

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset	Pad Reset	WDT Reset
$00	IEX	IET0	IET1	IEP	0000	0000	0000
$01	IRQX	IRQT0	IRQT1	IRQP	0000	0000	0000
$02	-	T0M.2	T0M.1	T0M.0	-000	-000	-000
$03	-	T1M.2	T1M.1	T1M.0	-000	-000	-000
$04	T0L.3	T0L.2	T0L.1	T0L.0	0000	0000	0000
$05	T0H.3	T0H.2	T0H.1	T0H.0	0000	0000	0000
$06	T1L.3	T1L.2	T1L.1	T1L.0	0000	0000	0000
$07	T1H.3	T1H.2	T1H.1	T1H.0	0000	0000	0000
$08	PA.3	PA.2	PA.1	PA.0	0000	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000	0000
$0A - $0C	-	-	-	-	----	----	----
$0D	-	-	B1	B0	--uu	--uu	--uu
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-xxx	-uuu
$13	-	LCDOFF	HLM	PAM	-100	-P00	-100
$14	AEC3	AEC2	AEC1	AEC0	0000	0000	0000
$15	PPULL	1	1	-	000-	000-	000-
$16 - $19	-	-	-	-	----	----	----
$1A	WDT	-	-	-	1---	1---	0---
$1B	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000	0000
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000	0000
$1D - $1F	-	-	-	-	----	----	----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.
P = 1 (Single solar supply application option disable) P = unchanged (Single solar supply application option enable).

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

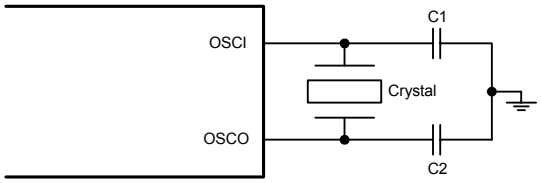
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock $f_{SYS} = f_{OSC}/4$

5.1. Instruction Cycle Time:

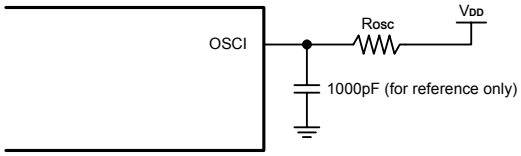
(1) 4/32.768kHz (≈ 122μs) for 32.768kHz oscillator.
(2) 4/131 kHz (≈ 30.53μs) for 131kHz oscillator.

5.2. Oscillator Type:

(1) Crystal oscillator: 32.768kHz



(2) RC oscillator: 131kHz



5.3. Capacitor Selection for Oscillator

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3x8)	KDS
			φ 3x8 - 32.768KHz	Vectron International

Notes:

1. **Capacitor values are used for design guidance only!**
2. These capacitors were tested with the crystals listed above for basic start-up and operation. **They are not optimized.**
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal, the user should consult the crystal manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures.

6. I/O Port

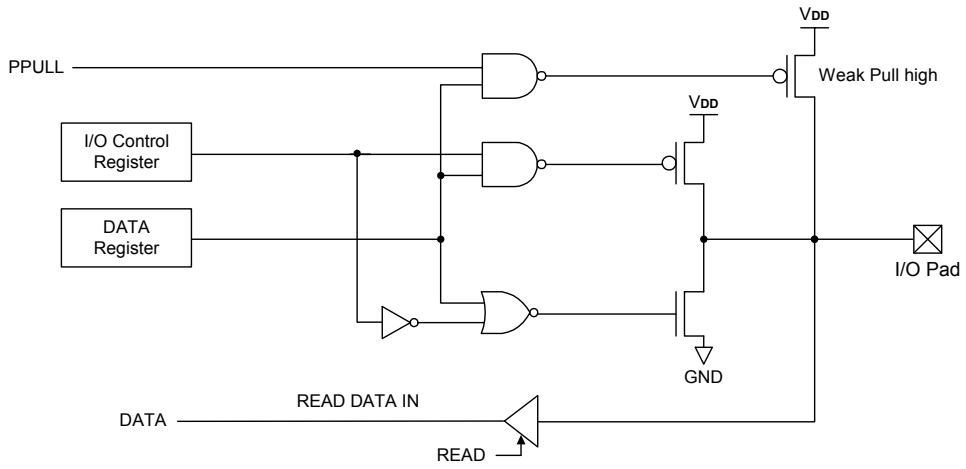
The MCU provides 8 bi-directional I/O ports. The PORT data is put in register $08 - $09. The PORT control register ($1B - $1C) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PPULL of $15 and the data of the PORT, when the PORT is used as input.

Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$1B	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$1C	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register

PA (/B) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pad



When PAM = 1 (System register $13 Bit0), PORTA.1 - 2 are used as Alarm output.

Controlling the Pull-up MOS

System Register $15:

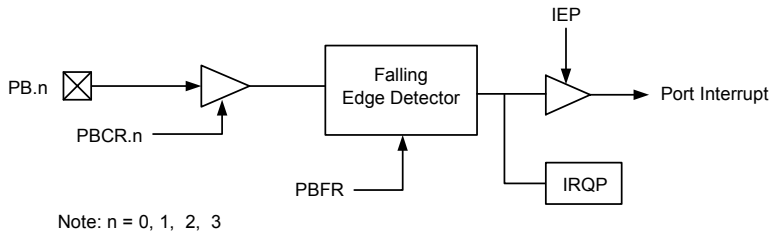
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	PPULL	1	1	-	R/W	Bit3: Port pull-up control register
	1	X	X	X		Port Pull-high enable
	0	X	X	X		Port Pull-high disable

These ports contain pull-up MOS controlled by program. System register $15 Bit3 (PPULL) simultaneously controls ON/OFF of all pull-up MOS. Pull -up MOS is also controlled by the port data registers (PA and PB) of each port. (Write 0 could turn off the pull-up MOS.) Thus the pull-up MOS can be turned ON/OFF individually.

If the “Single solar supply application” code option is enabled, the pull-up MOS is also controlled by the port I/O control registers (PACR and PBCR) of each port. Only when the port is used as input, the PPULL (System register $15 Bit3) is available. That means when the port is used as output, the relevant pull-up MOS will be turned off even if the PPULL system register $15 Bit3 is set to 1 as well as the port data register.

PORTB Interrupt

The PORTB is used as the port interrupt source. Following is the port interrupt function block-diagram.



Note: n = 0, 1, 2, 3

Port Interrupt (PB INT) Programming Notes:

■ If user wants to generate an interrupt when a low level emerges on the port, the following must be executed.

If “Single solar supply application” is enabled:

1. Set the port as input port, fill port data register with “1” and avoid port floating.
2. Pull-high the port (Use external pull-high resistance or set PULL to “1”).

In order to correctly return from the port interrupt-processing subroutine, the low level applying on the port must be released before the relative IRQ flag clearing and IE resetting. Otherwise, it is possible to reenter the active interrupt.

External Interrupt

PORTA.0 is shared with external interrupt (Low active).

If the “Single solar supply application” code option is disabled, an external interrupt will occur when a low level emerges on the PORTA.0.

If the “Single solar supply application” code option is enabled, the external interrupt is available only when

1. Set the port as input port, fill port data register with “1” and avoid port floating.
2. Pull-high the port (Use external pull-high resistance or set PPULL to “1”).

In order to correctly return from the external (PORTA.0) interrupt-processing subroutine, the low level applying on the PORTA.0 must be released before the relative IRQ flag clearing and IE resetting. Otherwise, it is possible to reenter the active interrupt.

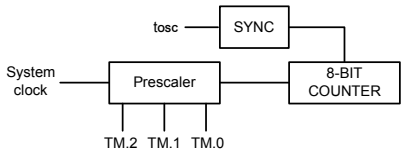
7. Timer

SH66L06A has two 8-bit timers.

The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

7.1. Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has both low-order digits and high-order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer/counter is automatically loaded with the contents of the load register when the high-order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: The register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

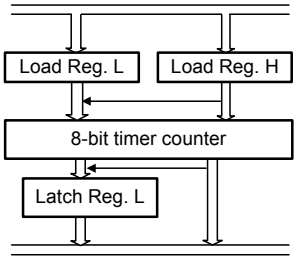
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.2. Timer0 and Timer1 Mode Register

The timer can be programmed in several different prescalers by setting Timer Mode register (T0M, T1M).

The clock source pre-scale by the 8-level counter first, then generate the output plus to timer counter. The Timer Mode registers (T0M, T1M) are 3-bit registers used for the timer control as shown in Table 1 and Table 2.

Table 1: Timer0 Mode Register ($02)

T0M.2	T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

Table 2: Timer1 Mode Register ($03)

T1M.2	T1M.1	T1M.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

8. Interrupt

Four interrupt sources are available on SH66L06A:
- External interrupt (Low active)
- Timer0 interrupt
- Timer1 interrupt
- PORTB interrupt (Low active)

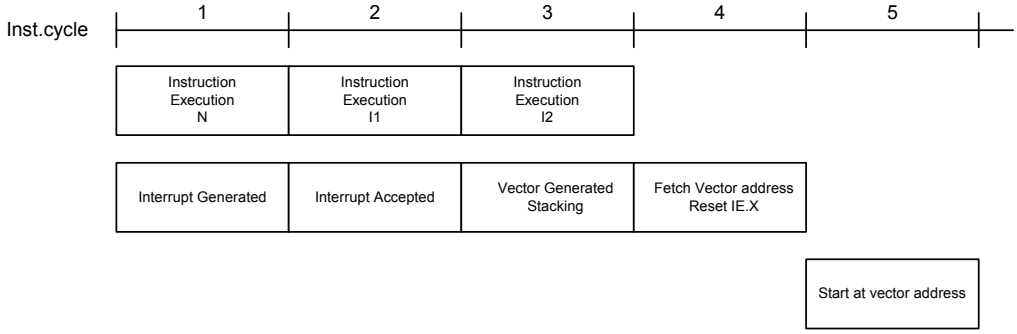
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are clear to "0" at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags register
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags register

When IEx is set to "1" and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are cleared to "0" automatically, so when IRQx is 1 and IEx is set to "1" again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

External Interrupt

When Bit3 of system register $00 (IEX) is set to "1", the external interrupt will be enabled, and a low level applying on the external interrupt I/O port will generate an external interrupt. External Interrupt can be used to wake the CPU from HALT or STOP mode.

Timer Interrupt

The input clocks of Timer0 and Timer1 are based on system clock source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1 = 1), If the interrupt enable flag is enabled (IET0 or IET1 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port Low Active Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.

Any one of the I/O input port applying with a low level would generate an interrupt request (IRQP = 1). In order to avoid multi-responses, it is strongly recommended that the relative input port cannot be connected with a low level all the time. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

9. LCD Driver

The LCD driver contains a controller, a voltage generator, 4 common driver pads and 18 segment driver pads. There are two different driving modes: 1/4 duty and 1/3 bias, 1/3 duty and 1/2 bias (COM4 same as COM1). The driving mode is controlled by code option. The controller consists of display data RAM and a duty generator. The LCD data RAM is a dual port RAM that transfers data to segment pads automatically without program control. LCD RAM can be used as data memory if needed.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When LCD off, both common and segment output low.

System Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	-	LCDOFF	HLM	PAM	R/W	Bit0: PORTA.1, PORTA.2 as Alarm O/P control register Bit1: Heavy load Mode control register Bit2: LCD power control register
	X	X	X	0		PORTA.1, PORTA.2 as I/O port
	X	X	X	1		PORTA.1, PORTA.2 as ALARM output
	X	X	0	X		No heavy load
	X	X	1	X		Heavy Load mode
	X	0	X	X		LCD display on, pump on
	X	1	X	X		LCD display off, pump off *

*: Please refer to the "Program Notes" described as below for details.

Heavy Load Mode (HLM): This mode is designed for the 32kHz crystal oscillator, so that the oscillation can be maintained in a noisy power environment. The power might drop suddenly when the ALARM is driving a speaker. The HLM is designed to control this power variation. The consumption of power will increase during the use of the HLM mode, but it will not affect the RC oscillator.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	PPULL	1	1	-	R/W	Bit2-1: must keep it to "1". In the User's program. Bit3: Port pull-up control register

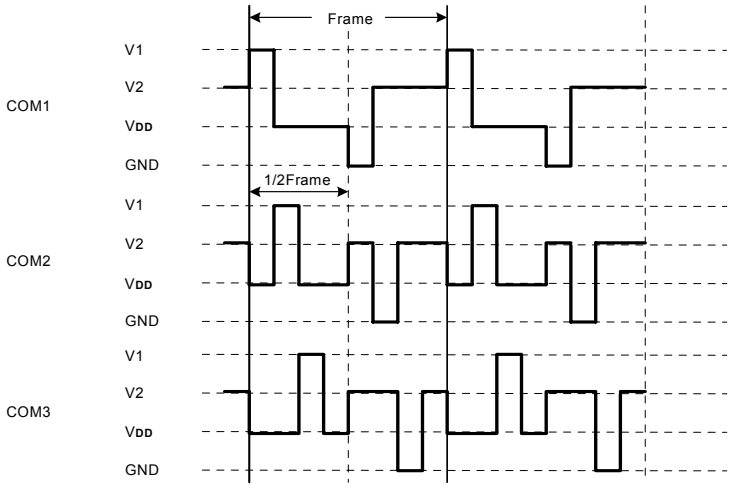
For SH66L06A, after the chip reset, please first write *11*B to $15. Otherwise, the halt current and stop current will be abnormal.

LCD Frame Frequency

The LCD Frame Frequency has two modes when the chip is used in RC application. The mode is controlled by the "Clock source" code option.

The code option and LCD Frame Frequency are shown as below:

Code Option	LCD frame frequency	
	1/3 duty, 1/2 bias	1/4 duty, 1/3 bias
32.768kHz Crystal	About 43Hz	About 32Hz
131kHz RC with normal LCD frame frequency	About 43Hz	About 32Hz
131kHz RC with 1/2 LCD frame frequency	About 21Hz	About 16Hz



Program Notes:

The LCD pump circuit and the LCD display will be turned off automatically after the CPU has received a “STOP” instruction. The user should turn on the LCD pump (Set LCDOFF = 0) after the next wake up.

If the “Single solar supply application” code option is disabled

1. The LCDOFF (System register $13 Bit2) will be set to 1 when the pad reset has been issued or the power on reset has been released. At this time, the LCD display will be disabled.
2. The LCD pump circuit is off after power on reset. When the LCDOFF (System register $13 Bit2) is cleared to 0, the LCD pump circuit will turn on. It will turn off only after receiving a “STOP” instruction.
3. Set LCDOFF = 1 disables LCD display output only, and won’t turn off the LCD pump circuit.

If the “Single solar supply application” code option is enabled

1. The LCDOFF (System register $13 Bit2) will be set to 1 after the power on reset has been released. At this time, the LCD pump circuit and the LCD display will be turned off.
2. When the LCDOFF (System register $13 Bit2) is cleared to 0 by the programming writing, the LCD pump circuit will be turned on, then the LCD display will be turned on, too.
3. The user should turn on the LCD pump (Set LCDOFF = 0) after the next wake up.
4. In addition, the LCD pump circuit and the LCD display will also be turned off if the LCDOFF (System register $13 Bit2) is set to 1 by the programming writing.
5. The LCDOFF (System register $13 Bit2) will be unchanged when the pad reset has been issued.

“Single solar supply application” code option is disabled

	LCDOFF	PUMP CIRCUIT	Display
PWR	1	OFF	OFF
WDT	1	OFF	OFF
STOP	1	OFF	OFF
Pad RESET	1	U	OFF

“Single solar supply application” code option is enabled

	LCDOFF	PUMP CIRCUIT	Display
PWR	1	OFF	OFF
WDT	1	OFF	OFF
STOP	1	OFF	OFF
Pad RESET	U	U	U

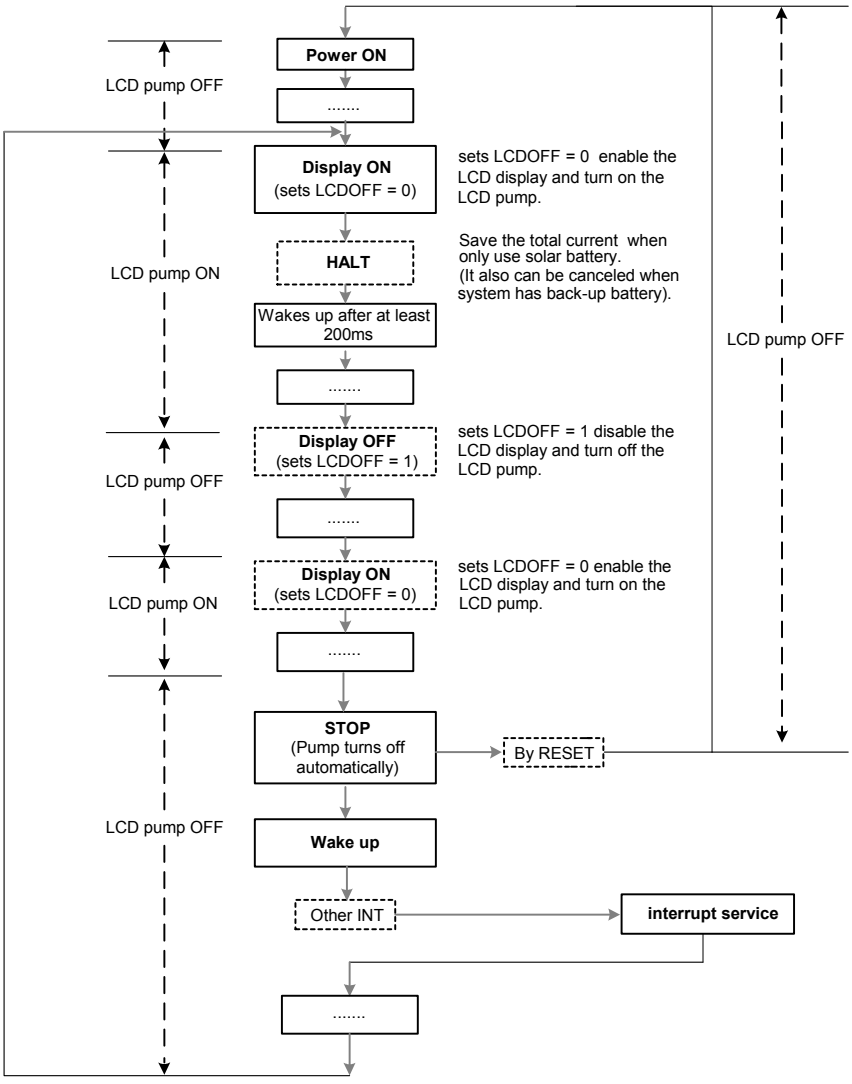
LCDOFF Program Setting

Code Option	LCDOFF	PUMP CIRCUIT	Display
"Single solar supply application" code option is disabled	0	ON	ON
	1	U	OFF
"Single solar supply application" code option is enabled	0	ON	ON
	1	OFF	OFF

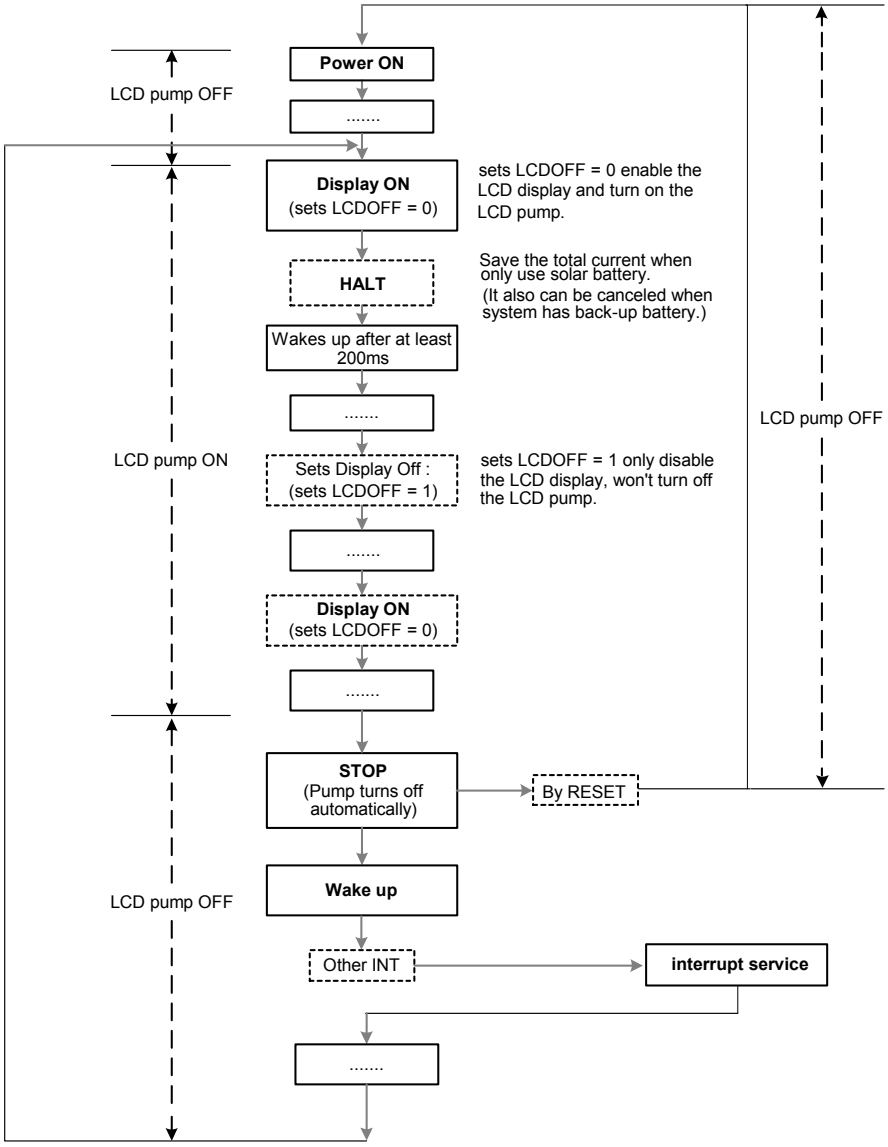
Legend: U = unchanged

Example:

Single Solar Supply Application Enable



Single Solar Supply Application Disable



Configuration of LCD RAM Area: (SEG 1 - 18, 1/4 duty)

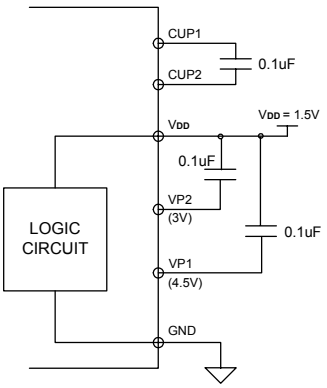
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1	309H	SEG10	SEG10	SEG10	SEG10
301H	SEG2	SEG2	SEG2	SEG2	30AH	SEG11	SEG11	SEG11	SEG11
302H	SEG3	SEG3	SEG3	SEG3	30BH	SEG12	SEG12	SEG12	SEG12
303H	SEG4	SEG4	SEG4	SEG4	30CH	SEG13	SEG13	SEG13	SEG13
304H	SEG5	SEG5	SEG5	SEG5	30DH	SEG14	SEG14	SEG14	SEG14
305H	SEG6	SEG6	SEG6	SEG6	30EH	SEG15	SEG15	SEG15	SEG15
306H	SEG7	SEG7	SEG7	SEG7	30FH	SEG16	SEG16	SEG16	SEG16
307H	SEG8	SEG8	SEG8	SEG8	310H	SEG17	SEG17	SEG17	SEG17
308H	SEG9	SEG9	SEG9	SEG9	311H	SEG18	SEG18	SEG18	SEG18

Configuration of LCD RAM Area: (SEG1 - 18, 1/3 duty)

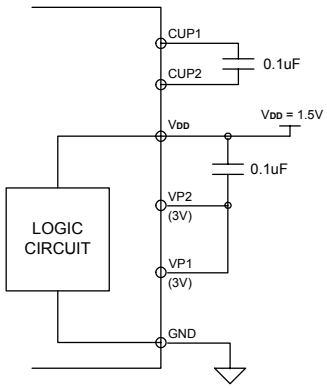
Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
300H	-	SEG1	SEG1	SEG1	309H	-	SEG10	SEG10	SEG10
301H	-	SEG2	SEG2	SEG2	30AH	-	SEG11	SEG11	SEG11
302H	-	SEG3	SEG3	SEG3	30BH	-	SEG12	SEG12	SEG12
303H	-	SEG4	SEG4	SEG4	30CH	-	SEG13	SEG13	SEG13
304H	-	SEG5	SEG5	SEG5	30DH	-	SEG14	SEG14	SEG14
305H	-	SEG6	SEG6	SEG6	30EH	-	SEG15	SEG15	SEG15
306H	-	SEG7	SEG7	SEG7	30FH	-	SEG16	SEG16	SEG16
307H	-	SEG8	SEG8	SEG8	310H	-	SEG17	SEG17	SEG17
308H	-	SEG9	SEG9	SEG9	311H	-	SEG18	SEG18	SEG18

Connection Diagram

1. V_{DD} = 1.5V, 4.5V LCD, 1/4 duty, 1/3bias



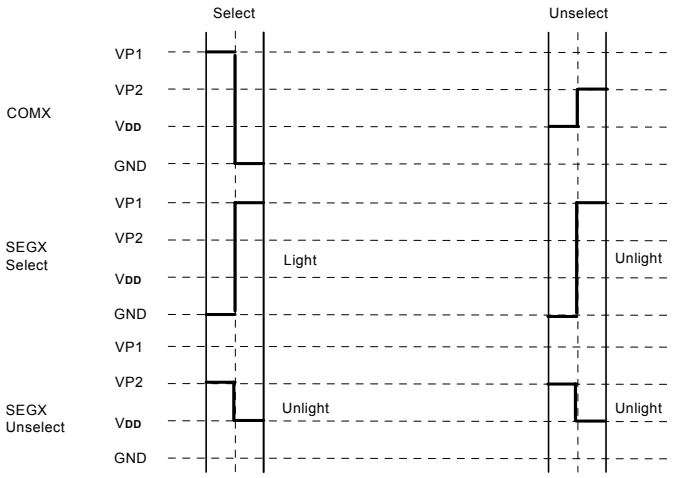
2. V_{DD} = 1.5V, 3V LCD, 1/3 duty, 1/2bias

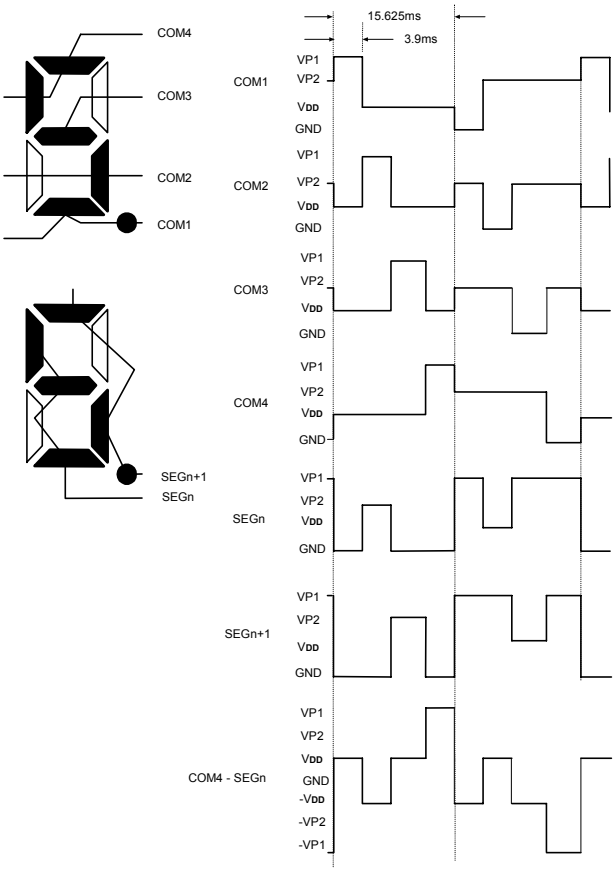


Program Notes:

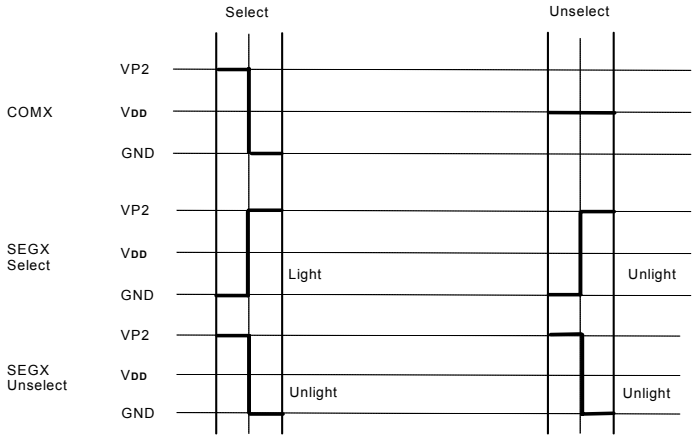
The pump circuit frequency can be 4kHz, or 2kHz (Selected by code option). When using the small LCD panel, the user can select 2kHz pump frequency to save power. When using the large LCD panel, the user can select 4kHz pump frequency to have more power supply ability for LCD use. LCD duty and bias are selected by code option.

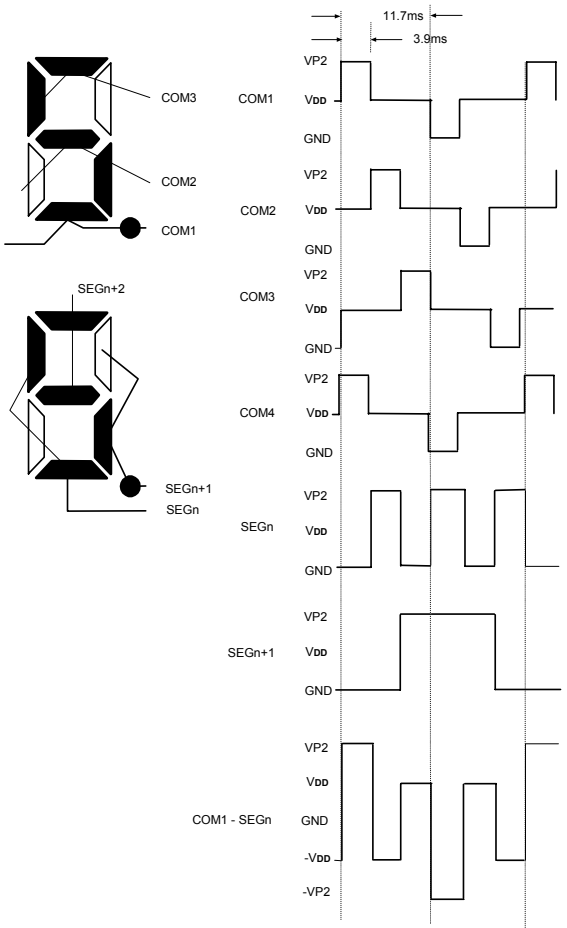
1/4 duty, 1/3 bias LCD Waveform (V_{DD} = 1.5V, V_{P1} = 4.5V, V_{P2} = 3V)





1/3 duty, 1/2 bias LCD Waveform (V_{DD} = 1.5V, V_{P1} = V_{P2} = 3V)





10. Alarm Output

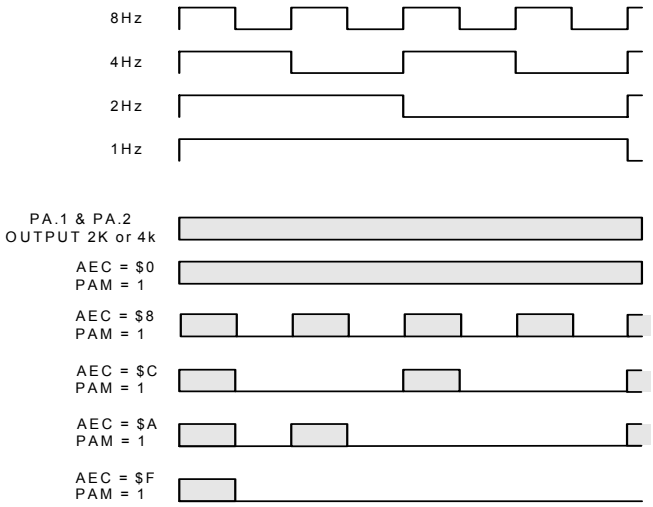
System Register $14:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	AEC3	AEC2	AEC1	AEC0	R/W	ALARM envelope control register
	0	0	0	0	R/W	DC envelope (Default)
	X	X	X	1	R/W	1Hz envelope AND other envelope choice logically
	X	X	1	X	R/W	2Hz envelope AND other envelope choice logically
	X	1	X	X	R/W	4Hz envelope AND other envelope choice logically
	1	X	X	X	R/W	8Hz envelope AND other envelope choice logically

Default carrier frequency is 4kHz, can be selected to 2kHz by code option.
WRITE mode: controls the envelope selection.
READ mode can read out current envelope waveforms.

To activate the ALARM function, first switch the PAM to ALARM OUTPUT mode. After setting PAM to 1, then set the proper envelope. When the data writes to AEC, the envelope counter will be synchronized. The programmer can read back the envelope from AEC register and make any pattern changes needed by programmer. The Read operation will not affect the alarm output waveform.

The programming alarm waveform is shown below:



Alarm output waveform

11. Watchdog Timer

The watchdog timer is a down-count counter, and its clock source is fetched from the system clock, so it will not run in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option. To prevent it timing out and generating a device reset condition, users should write watchdog timer reset bit ($1A Bit3) as “1” before timing-out.

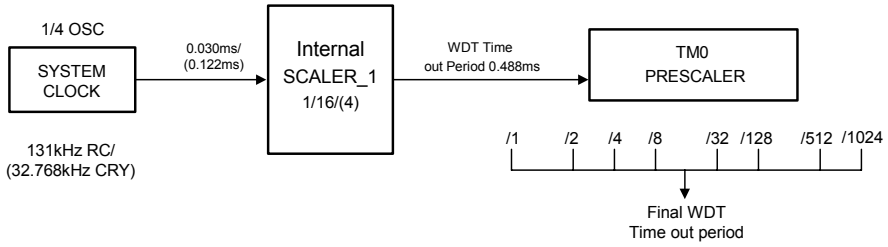
System Register $1A

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$1A	WDT				R/W	Bit3: Watchdog timer reset/flag register (Write 1 to reset WDT)

The WDT has a time-out period of more than 0.5ms (V_{DD} = 1.5V 131kHz RC or 32.768kHz Crystal). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:1024 can be assigned to the watchdog timer under software control by writing to the T0M register ($02 Bit2 - Bit0).

Prescaler Divide Ratio:

T0M.2	T0M.1	T0M.0	Prescaler divide ratio	Timer-out period
1	1	1	1:1	0.5ms
1	1	0	1:2	1.0ms
1	0	1	1:4	2.0ms
1	0	0	1:8	4.0ms
0	1	1	1:32	16.0ms
0	1	0	1:128	64.0ms
0	0	1	1:512	256.0ms
0	0	0	1:1024 (Power on initial)	512.0ms



Notes:

If enabled by the code option, the Watchdog Timer will be cleared when the WDT bit is set in Power-On initial. The WDT bit will be cleared only if the Watchdog Timer time-out occurs both in normal operation mode and in the HALT mode. The Watchdog Timer is cleared when the device wakes up from the STOP mode, regardless of the source of wake-up.

Status and Condition

WDT	Condition
1	Power-On reset
0	WDT cause reset during normal operation
0	WDT cause reset in HALT mode
1	Pad reset during normal operation or in HALT mode
1	Pad reset or interrupt wake-up in STOP mode

Program Notes:

1. If the system clock is changed by the code option, the time-out period of the Watchdog Timer will also fix at approx. 0.5ms.
2. The WDT can use a prescaler with a division ratio of up to 1:2048 to prolong the time-out periods by writing to the T0M register. Since the T0M register is shared with Timer0, the WDT has the same prescaler value as Timer0. If T0M register is changed for some proper use, the WDT’s time-out period will also be changed.

12. HALT and STOP Mode

After the execution of HALT instruction, SH66L06A will enter the HALT mode. In the HALT mode, the CPU will stop operating. But peripheral (Timer, LCD) circuit will keep status.

After the execution of STOP instruction, SH66L06A will enter the STOP mode. The whole chip (Including oscillator) will stop operating.

In the HALT mode, SH66L06A can be waked up if any interrupt occurs.

In the STOP mode, SH66L06A can be waked up if port or external interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

13. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

A. Power-on Reset for OSC

(1) In 131kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{12}$ (4096).
(2) In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

B. Pad Reset for OSC

(1) In 131kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{8}$ (256).
(2) In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{10}$ (1024).

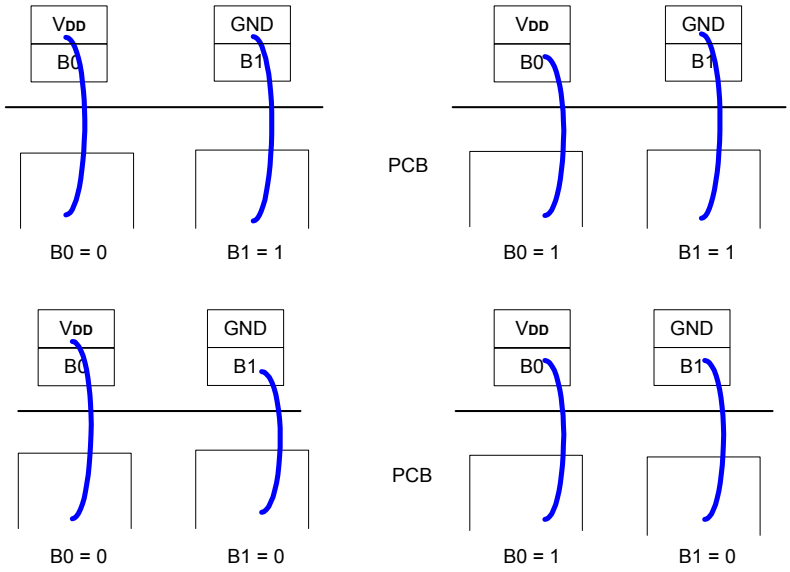
C. Wake up from STOP mode

(1) In 131kHz RC oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{8}$ (256).
(2) In 32.768kHz Crystal oscillator mode, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

14. Bonding Option

System Register $0D:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	-	-	B1	B0	R	B1, B0: Bonding option register
	X	X	1	0	R	Default bonding option
	X	X	0	0	R	B1 bond to GND
	X	X	1	1	R	B0 bond to VDD
	X	X	0	1	R	B1 bond to GND & B0 bond to VDD



SH66L06A Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that varies depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

Program Notes:

To correctly fetch the contents of bonding options in variety applications, it is necessary to insert a dummy read instruction before the genuine reading from the $0D system register.

15. Code Option

Addresses: $800
Body data: 0110 1011 1010 0110 (6BA6)

Addresses: $801
Data: CHAP F1DW S0R0 0000

CH (Clock source):
- 00 = 32.768kHz Crystal (Default)
- 10 = 131kHz RC with normal LCD frame frequency
- 11 = 131kHz RC with 1/2 LCD frame frequency

A (Alarm carrier frequency)
- 0 = 4kHz (Default)
- 1 = 2kHz

PF (LCD Pump circuit frequency)
- 01 = 2kHz(Default)
- 10 = 4kHz

D (Duty and bias option)
- 0 = 1/3 duty, 1/2 bias (Default)
- 1 = 1/4 duty, 1/3 bias

W (Watch Dog Timer)
- 0 = Disable (Default)
- 1 = Enable

S (Single solar supply application)
- 0 = Disable (Default)
- 1 = Enable

R (Reset type select)
- 0 = Level trigger (Low active) (Default)
- 1 = Edge trigger (Falling edge active)

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page	B	RAM bank
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +3.0V

Input Voltage . . . . . .-0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . .0°C to +70°C

Storage Temperature . . . . . .-55°C to +125°C

***Comments**

Stresses exceed those listed under **"Absolute Maximum Ratings"** may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions exceed those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	1.2	1.5	1.7	V	32.768kHz ≤ fosc ≤ 131kHz
Operating Current	I_{OP}	-	3	6	μA	fosc = 32.768kHz Crystal, All output pads unload execute NOP instruction, (excluding LCD bias current, WDT off, Alarm disable.)
		-	10	15	μA	fosc = 131kHz RC, All output pads unload execute NOP instruction, (excluding LCD bias current, WDT off, Alarm disable.)
Standby Current	I_{SB}	-	2	4	μA	fosc = 32.768kHz Crystal, All output pads unload (HALT mode), excluding LCD current. (Not in heavy load mode)
		-	5	9	μA	fosc = 131kHz RC , All output pads unload (HALT mode), excluding LCD current. (Not in heavy load mode)
		-	-	0.5	μA	All output pads unload (STOP mode), LCD off
Input High Voltage	V_{IH}	0.8 X V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB OSCI (Driven by external clock)
		0.85 X V_{DD}	-	V_{DD} + 0.3	V	$\overline{INT0}$, $\overline{RESET}$, TEST (Schmitt trigger input)
Input Low Voltage	V_{IL}	GND - 0.3	-	0.2 X V_{DD}	V	PORTA, PORTB OSCI (Driven by external clock)
		GND - 0.3	-	0.15 X V_{DD}	V	$\overline{INT0}$, $\overline{RESET}$, TEST (Schmitt trigger input)
Output High Voltage	V_{OH}	0.8 X V_{DD}	-	-	V	PORTB, PORTA.0, 3 (I_{OH} = -8μA)
		0.8 X V_{DD}	-	-	V	BD/$\overline{BD}$ (PORTA.1, PORTA.2), I_{OH} = -0.3mA
		V_{P1} - 0.2	-	-	V	SEGx, (I_{OH} = -3μA)
		V_{P1} - 0.2	-	-	V	COMx, (I_{OH} = -8μA)
Output Low Voltage	V_{OL}	-	-	0.2 X V_{DD}	V	PORTB, PORTA.0, 3 (I_{OL}= 0.3mA)
		-	-	0.2 X V_{DD}	V	BD/$\overline{BD}$ (PORTA.1, PORTA.2), (I_{OL} = 0.3mA)
		-	-	0.2	V	SEGx, (I_{OL} = 3μA)
		-	-	0.2	V	COMx, (I_{OL} = 8μA)
Pull-up Resistor	R_P	-	150	-	KΩ	PULL-UP resistor (V_{OH} = 0, I_{OH} = -10μA)
RESET Pull-high Resistor	R_{RP}	-	200	-	KΩ	Pull high resistor for RESET pad input "1" (Only in edge trigger type)
		-	1000	-	KΩ	Pull high resistor for RESET pad input "0" (Only in edge trigger type)
LCD Lighting	I_{LCD}	-	-	1	μA	No panel loaded. LCD pump frequency = 4k

DC Electrical Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reset Current	I_{REST}	-	-	20	μA	Reset current

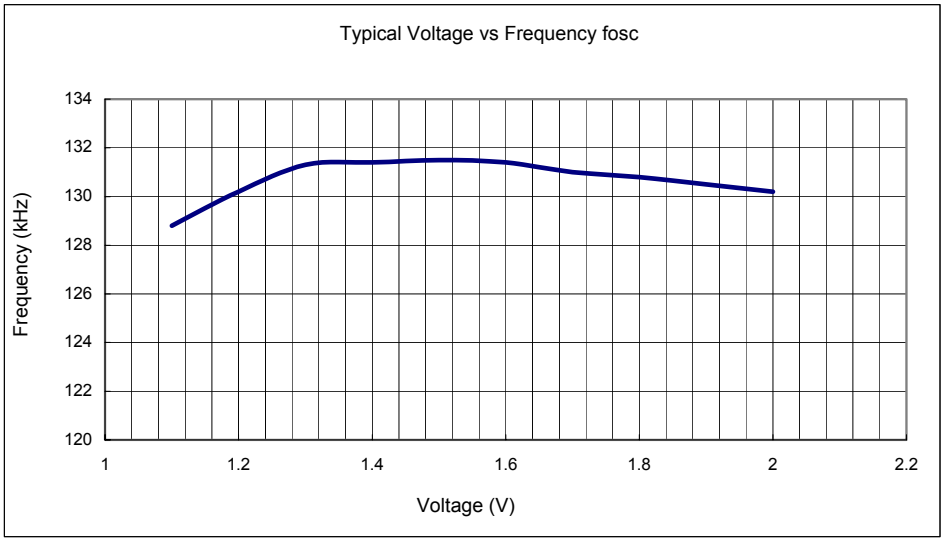
AC Characteristics (V_{DD} = 1.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time (Crystal)	T_{STT}	-	1	2	S	f_{OSC} = 32.768kHz
Frequency Variation (RC)	Δ F/F	-	-	±30	%	Include supply voltage and chip to chip variation OSC = 131kHz RC

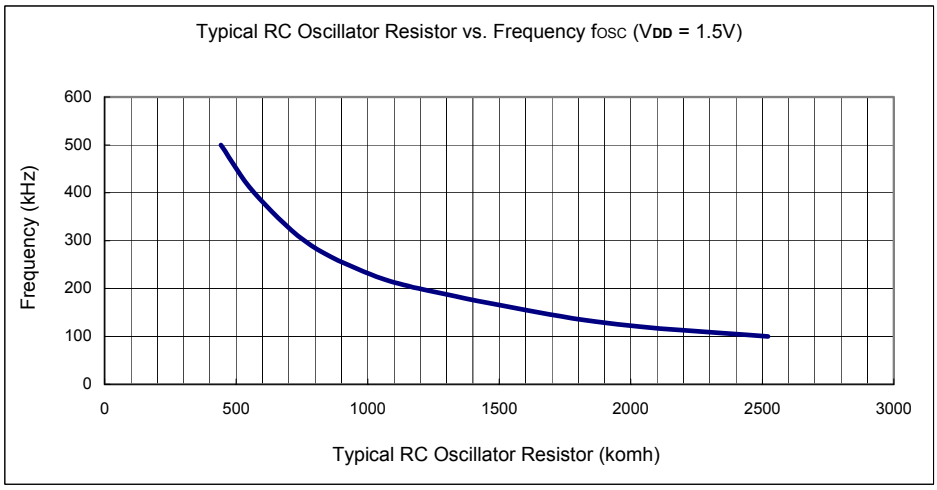
RC Oscillator Characteristics Graphs

RC Oscillator Characteristics Graphs (For reference only)

(a) Typical Voltage vs Frequency fosc



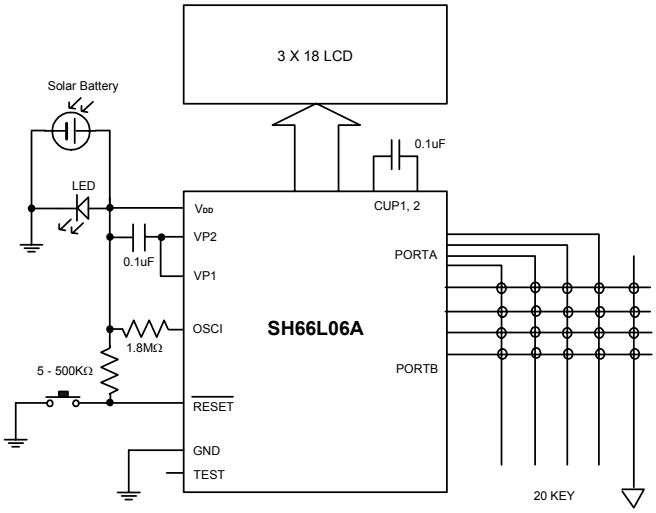
(b) Typical RC Oscillator Resistor vs. Frequency fosc (V_{DD} = 1.5V)



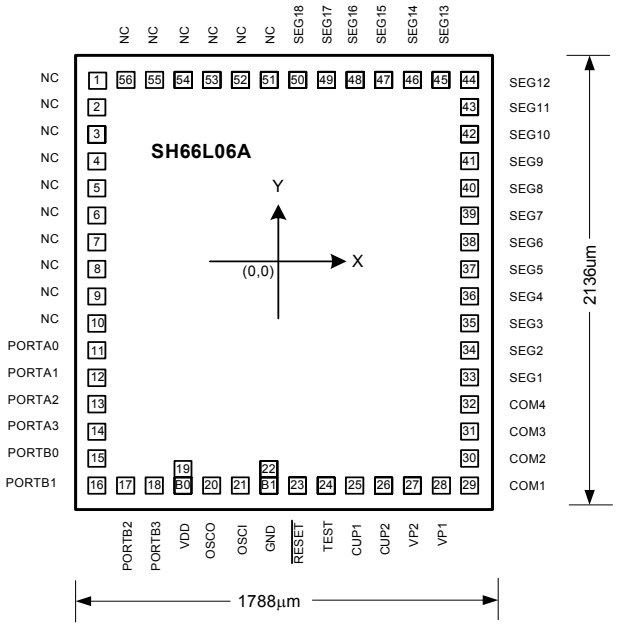
Application Circuits (For reference only)

SH66L06A chip substrate connects to system ground.

AP1: (1) Operating voltage: 1.5V
(2) Oscillator: RC: 131kHz (Code Option)
(3) LCD: 3V, 1/3 duty, 1/2 bias,
(4) PORTA - B: I/O



Bonding Diagram



*** Substratum connects to ground.**

Pad Location Unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	NC	-760	935	17	PORTB2	-637.5	-935
2	NC	-760	792.5	18	PORTB3	-517.5	-935
3	NC	-760	662.5	19	VCC	-402.5	-841
4	NC	-760	496.3		B0	-402.5	-935
5	NC	-760	381.3	20	OSCO	-287.5	-935
6	NC	-760	264.1	21	OSCI	-172.5	-935
7	NC	-760	149.1	22	GND	-57.5	-841
8	NC	-760	31.9		B1	-57.5	-935
9	NC	-760	-83.1	23	$\overline{\text{RESET}}$	57.5	-935
10	NC	-760	-200.3	24	TEST	172.5	-935
11	PORTA0	-760	-315.3	25	CUP1	287.5	-935
12	PORTA1	-760	-432.5	26	CUP2	402.5	-935
13	PORTA2	-760	-547.5	27	VP2	517.5	-935
14	PORTA3	-760	-672.5	28	VP1	637.5	-935
15	PORTB0	-760	-802.5	29	COM1	760	-935
16	PORTB1	-760	-935	30	COM2	760	-802.5

Pad Location (Continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
31	COM3	760	-672.5	44	SEG12	760	935
32	COM4	760	-547.5	45	SEG13	637.5	935
33	SEG1	760	-432.5	46	SEG14	517.5	935
34	SEG2	760	-315.3	47	SEG15	402.5	935
35	SEG3	760	-200.3	48	SEG16	287.5	935
36	SEG4	760	-83.1	49	SEG17	172.5	935
37	SEG5	760	31.9	50	SEG18	57.5	935
38	SEG6	760	149.1	51	NC	-57.5	935
39	SEG7	760	264.1	52	NC	-172.5	935
40	SEG8	760	381.3	53	NC	-287.5	935
41	SEG9	760	496.3	54	NC	-402.5	935
42	SEG10	760	662.5	55	NC	-517.5	935
43	SEG11	760	792.5	56	NC	-637.5	935

Ordering Information

Part No.	Package
SH66L06AH	CHIP FORM

Data Sheet Revision History

Version	Content	Date
2.0	Revised the description about the PORTB & PORTC and External interrupts.	Mar. 2007
1.0	Original	Jan. 2007