SH66P51

OTP 2K 4-bit Micro-controller with LCD Driver

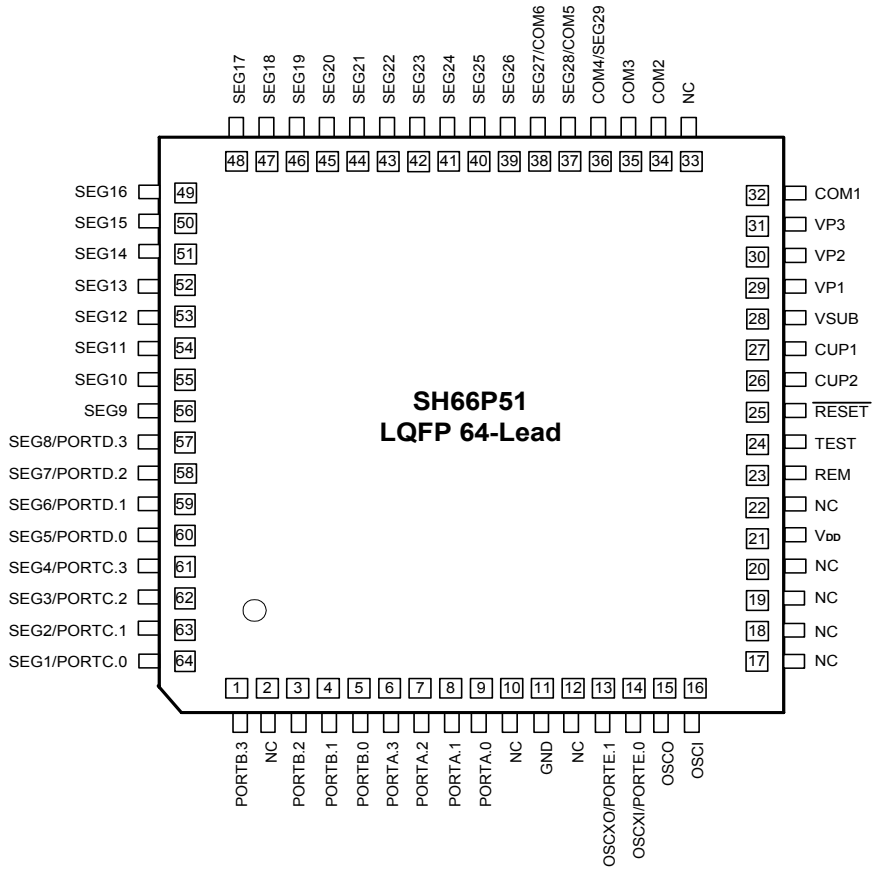
Features

- SH6610C-based single-chip 4-bit micro-controller
- OTP ROM: 2K X 16 bits
- RAM: 128 X 4 bits (Data RAM)
- Operation voltage: 1.8V - 3.6V (Typically 3.0V)
- 18 CMOS bi-directional I/O pins
  PORTA - PORTE;
  PORTC shared with LCD SEG1 - 4
  PORTD shared with LCD SEG5 - 8
  PORTE shared with OSCXI, OSCXO
- 4-level subroutine nesting (including interrupts)
- One 8-bit auto re-load timer/counter
- One 8-bit base timer
- Warm-up timer for power-on reset
- Powerful interrupt sources:
  - Internal interrupt (Timer0).
  - Internal interrupt (Base Timer)
  - External interrupts: PORTB & PORTC (falling edge).
- Built-in remote control programmable carrier synthesizer
- Built-in in LCD voltage regulator
- Pull-high resistor for reset pin (select by Code Option)
- Built-in Low Power Detect (2.3 ± 0.1V)
- LCD driver:
  3 X 29 dots (1/3 duty 1/3 bias)
  4 X 28 dots (1/4 duty 1/3 bias)
  5 X 27 dots (1/5 duty 1/3 bias)
  6 X 26 dots (1/6 duty 1/3 bias)
- Dual Clock Source
  OSC (select by Code Option):
  - Crystal oscillator: 32.768kHz
  - RC oscillator: 131kHz
  OSCX:
  - Ceramic/Crystal oscillator: 400k - 4MHz
  - Built-in RC: (4MHz ± 2%)
- Instruction Cycle Time (4/**fosc**)
- Two low power operation modes: HALT and STOP
- Built-in watchdog timer
- Built-in Low Voltage Reset Circuit (1.7 ± 0.1V)

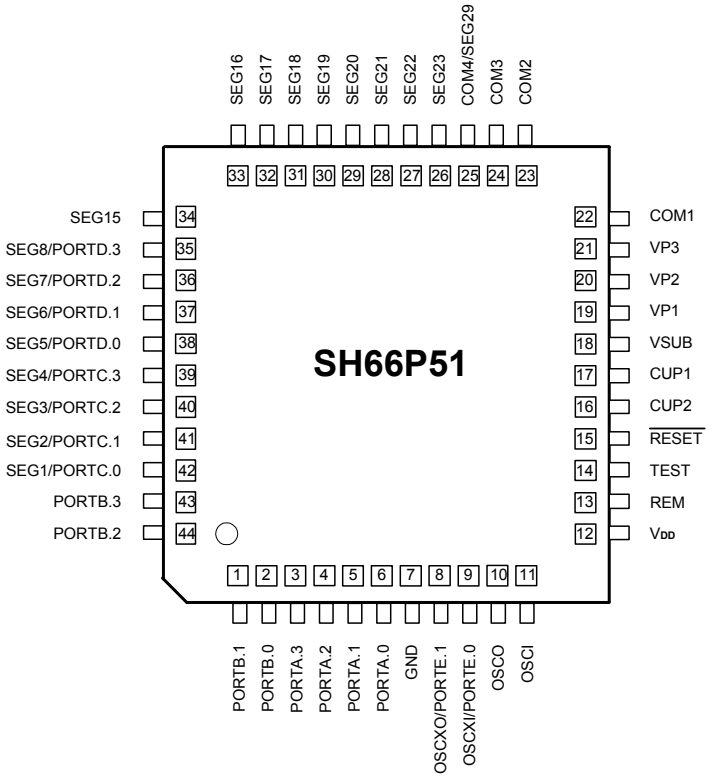
General Description

SH66P51 is dedicated to infrared remote control transmitter with LCD applications. This chip integrates the SH6610C 4-bit CPU core with SRAM, OTP ROM, one 8-bit timer, one base timer, LCD driver, programmable input/output driving buffers, carrier synthesizer, and voltage regulator. This chip integrates a dual-oscillator to enhance the total chip performance.

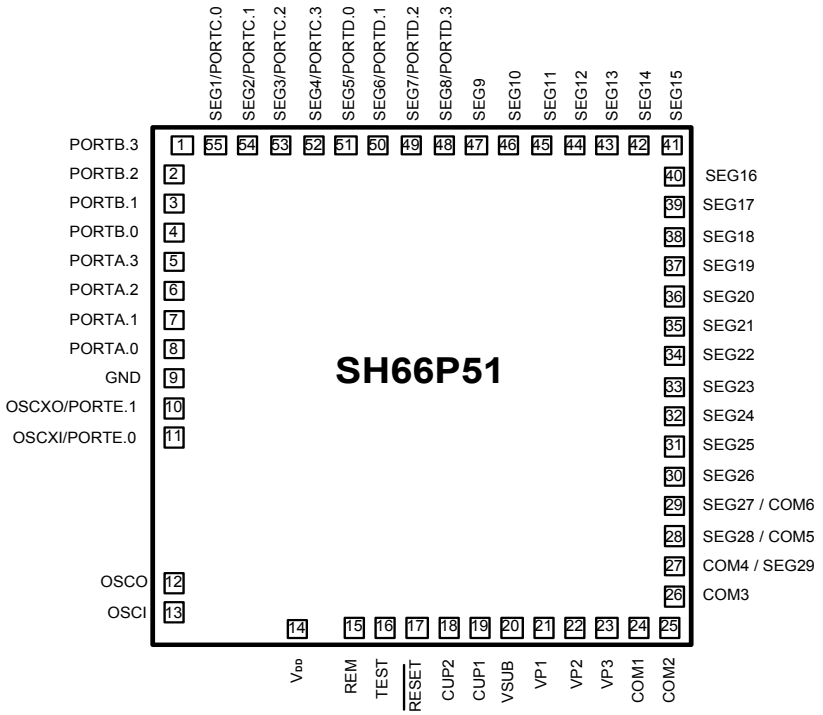
Pin Configuration (64 LQFP Package)



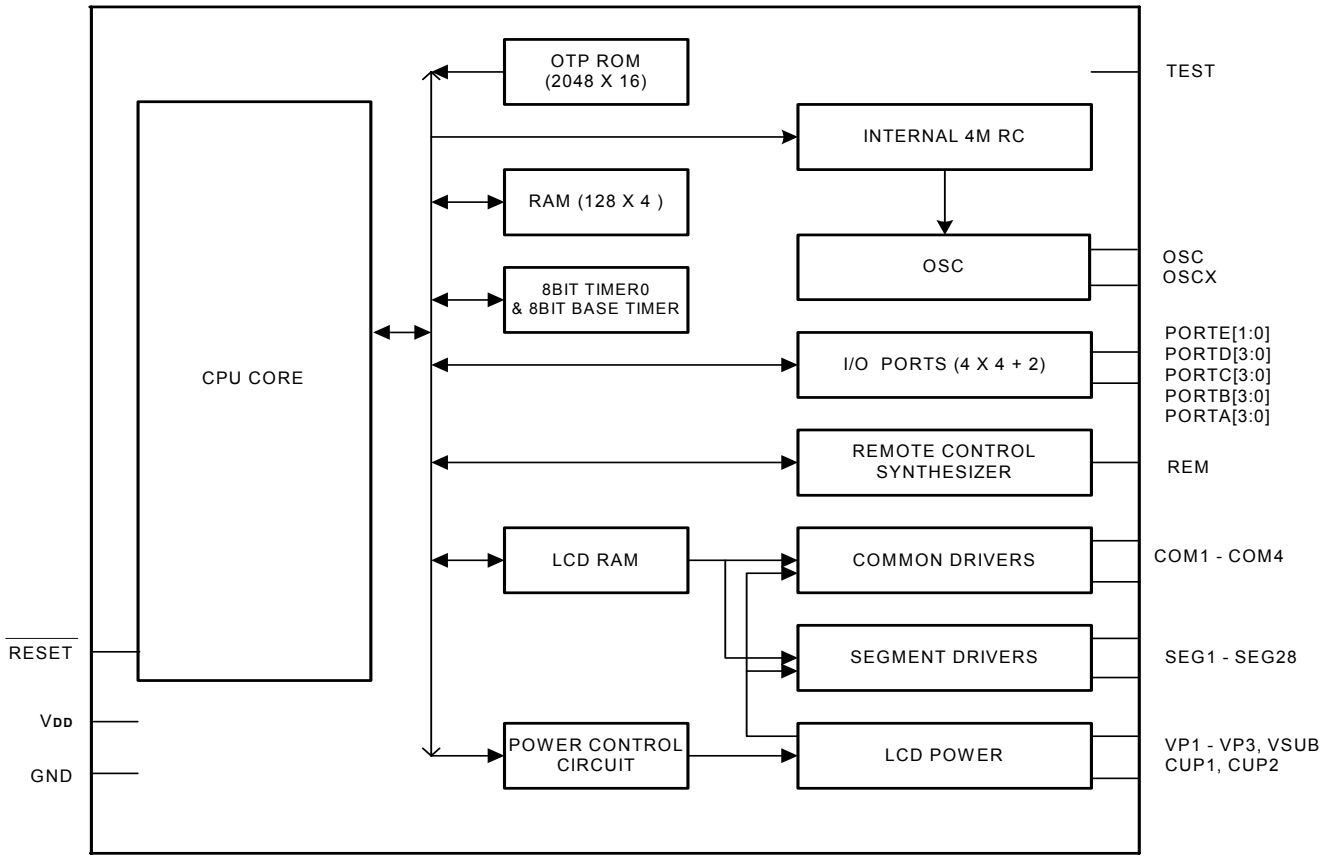
Pin Configuration (44 OFP Package)



Pad Configuration



Block Diagram



Pin Descriptions

Pin No.	Designation	I/O	Descriptions
29 - 31	VP1 - VP3	P	Power supply pin for LCD
27 - 26	CUP1 - 2	P	Connection for LCD bias capacitor
28	VSUB	P	Power supply pin, connected to external capacitor
25	$\overline{\text{RESET}}$	I	Reset input (Optional internal pull-high)
24	TEST	I	Test pin (Internal pull-low)
23	REM	O	Carrier synthesizer for infrared or RF output pin
21	V_{DD}	P	Power supply
16	OSCI	I	Oscillator input pin
15	OSCO	O	Oscillator output pin
14	OSCXI/PORTE.0	I/O	Oscillator X input pin connected to ceramic oscillator Shared with bit programmable I/O pin
13	OSCXO/PORTE.1	I/O	Oscillator X output pin connected to ceramic oscillator Shared with bit programmable I/O pin
11	GND	P	Ground pin
9 - 6	PORTA [0:3]	I/O	Bit programmable I/O
5, 4, 3, 1	PORTB [0:3]	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge)
64 - 61	SEG1 - SEG4/ PORTC [0:3]	I/O	LCD segment 1 - 4 Shared with bit programmable I/O pins, Vector Interrupt (Active falling edge)
60 - 57	SEG5 - SEG8/ PORTD [0:3]	I/O	LCD segment 5 - 8. Shared with bit programmable I/O pins
56 - 39	SEG9 - SEG26	O	LCD Segment 9 - 26
38 - 36	SEG27 - SEG29 /COM6 - COM4	O	LCD Segment 27, 28, 29. Shared with LCD Common 6, 5, 4
32, 34, 35	COM1 - COM3	O	LCD Common 1 - 3

OTP Programming Pin Description (OTP Program Mode)

Pin No.	Symbol	I/O	Shared by	Descriptions
21	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
24	V_{PP}	P	TEST	Programming high voltage Power supply (+11V)
11	GND	P	GND	Ground
16	SCK	I	OSCI	Programming Clock input pin
9	SDA	I/O	PORTA.0	Programming Data pin

Pad Descriptions (Total 55 Pad)

Pad No.	Designation	I/O	Descriptions
21 - 23	VP1 - VP3	P	Power supply pin for LCD
19 - 18	CUP1 - 2	P	Connection for LCD bias capacitor
20	VSUB	P	Power supply pin, connected to external capacitor
17	$\overline{\text{RESET}}$	I	Reset input (Optional internal pull-high)
16	TEST	I	Test pin (Internal pull-low)
15	REM	O	Carrier synthesizer for infrared or RF output pin
14	V_{DD}	P	Power supply
13	OSCI	I	Oscillator input pin
12	OSCO	O	Oscillator output pin
11	OSCXI/PORTE.0	I/O	Oscillator X input pin connected to ceramic oscillator Shared with bit programmable I/O pin
10	OSCXO/PORTE.1	I/O	Oscillator X output pin connected to ceramic oscillator Shared with bit programmable I/O pin
9	GND	P	Ground pin
8 - 5	PORTA [0:3]	I/O	Bit programmable I/O
4 - 1	PORTB [0:3]	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge)
55 - 52	SEG1 - SEG4 / PORTC [0:3]	I/O	LCD Segment 1 - 4 Shared with bit programmable I/O pins, Vector Interrupt (Active falling edge)
51 - 48	SEG5 - SEG8 / PORTD [0:3]	I/O	LCD Segment 5 - 8 Shared with bit programmable I/O pins
47 - 30	SEG9 - SEG26	O	LCD Segment 9 - 26
29 - 27	SEG27-SEG29 / COM6 - COM4	O	LCD Segment 27, 28, 29. Shared with LCD Common 6, 5, and 4
24 - 26	COM1 - COM3	O	LCD Common 1 - 3

OTP Programming Pad Description (OTP Program Mode)

Pad No.	Symbol	I/O	Shared by	Descriptions
14	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
16	V_{PP}	P	TEST	Programming high voltage Power supply (+11V)
9	GND	P	GND	Ground
13	SCK	I	OSCI	Programming Clock input pad
8	SDA	I/O	PORTA.0	Programming Data pad

Functional Descriptions

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K. The program counter cans only 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (28) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:
System register and I/O: $000 - $027
Data memory: $028 - $0A7
LCD RAM space: $300 - $33A

2.2. Configuration of System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	IEBT	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base Timer Mode register
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low digit
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high digit
$06	-	-	-	LPD	R	Bit0: 2.3V LPD flag
$07	-	LCDON	-	-	R/W	Bit2: Set LCD display ON
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE
$0D	-	-	-	REMO REM	W R	Bit0: REMO output data Bit0: REM pin output status
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PULLEN	CPS2	CPS1	CPS0	R/W	Bit2 - 0: Carrier counter source pre-divider Bit3: Port pull-high enable control
$14	OXS	-	OXM	OXON	R/W	Bit0: Turn on OSCX oscillator Bit1: CPU clocks select (1: OSCX/0: OSC) Bit3: OSCX type selection
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit0, 1: Select LCD DUTY (1/3 or 1/4 or 1/5 or 1/6) Bit2: Set PORTC as LCD Segment1 - 4 Bit3: Set PORTD as LCD Segment5 - 8
$16	PAIN	PBIN	PCIN	PDIN	R/W	Control PORTA - PORTD input and output access enable or disable. Used in key matrix's application
$17	-	-	-	PEIN	R/W	Control PORTE input and output access enable or disable. Used in key matrix's application
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control

Configuration of System Register (continued):

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C			PECR.1	PECR.0	R/W	PORTE input/output control
$1D	-	-	-	-	-	Reserved
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit0 - 2: Watchdog timer control Bit3: Watchdog timer overflow flag
$1F	-	-	-	-	-	Reserved
$20	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register
$21	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register
$22	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register
$23	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register
$24 - 27	-	-	-	-	-	Reserved

3. ROM

The ROM can address 2048 X 16 bits of program area from $000 to $7FF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	JMP*	Reserved
$002	JMP*	Jump to TIMER0 interrupt service routine
$003	JMP*	Jump to Base timer interrupt service routine
$004	JMP*	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

4. Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power On Reset /Pin Reset /Low Voltage Reset	WDT Reset
$00	-	IET0	IEBT	IEP	-000	-000
$01	-	IRQT0	IRQBT	IRQP	-000	-000
$02	-	TM0.2	TM0.1	TM0.0	-000	-uuu
$03	BTM.3	BTM.2	BTM.1	BTM.0	0000	uuuu
$04	TL0.3	TL0.2	TL0.1	TL0.0	xxxx	xxxx
$05	TH0.3	TH0.2	TH0.1	TH0.0	xxxx	xxxx
$06	-	-	-	LPD	---0	---0
$07	-	LCDON	-	-	-0--	-u--
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	-	-	PE.1	PE.0	--00	--00
$0D	-	-	-	REM	---0	---0
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	PULLEN	CPS2	CPS1	CPS0	0000	0uuu
$14	OXS	-	OXM	OXON	0-00	u-0u
$15	O/S1	O/S0	DUTY1	DUTY0	1100	uuuu
$16	PAIN	PBIN	PCIN	PDIN	0000	uuuu
$17	-	-	-	PEIN	---0	---u
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C			PECR.1	PECR.0	--00	--00
$1D	-	-	-	-	-	-
$1E	WDT	WDT.2	WDT.1	WDT.0	0000	1000
$1F	-	-	-	-	-	-
$20	CFL3	CFL2	CFL1	CFL0	0000	uuuu
$21	CFL7	CFL6	CFL5	CFL4	0000	uuuu
$22	CFH3	CFH2	CFH1	CFH0	0000	uuuu
$23	CFH7	CFH6	CFH5	CFH4	0000	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented.

4.2. Others Initial States:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.

System clock = fosc/4

5.1. Instruction Cycle Time:

(1) 4/32.768kHz (≈122.07μs) for 32.768kHz oscillator
(2) 4/131kHz (≈30.52μs) for 131kHz oscillator
(3) 4/455kHz (≈ 8.79μs) for 455kHz oscillator
(4) 4/4MHz (= 1μs) for 4MHz oscillator

5.2. Circuit Configuration

SH66P51 has two on-chip oscillation circuits OSC and OSCX.

OSC is a low frequency crystal (Typ. 32.768kHz) or RC (Typ. 131kHz) determined by the Code Option. This is designed for low frequency operation. OSCX also has two types: ceramic/crystal (Typ. 4MHz) or internal RC (4MHz ± 2%) determined by system register. It is designed for high frequency operation.

It is possible to select the high speed CPU processing by a high frequency clock and select low power operation by low operation clock. At starting of reset initialization, OSC starts oscillation and OSCX is turned off. Immediately after reset initialization, the OSC clock is automatically selected as the system clock input source.

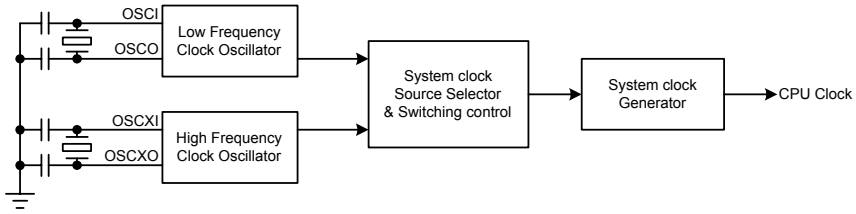
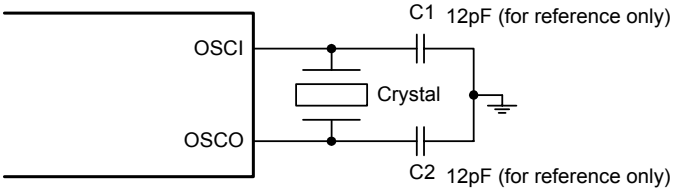


Figure 1. Oscillator Block Diagram

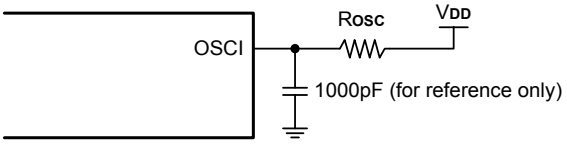
5.3. OSC Oscillation

The OSC generates the basic clock pulses that provide the CPU and peripherals (Base timer, LCD) with an operating clock.

(1) OSC Crystal Oscillator



(2) OSC RC Oscillator

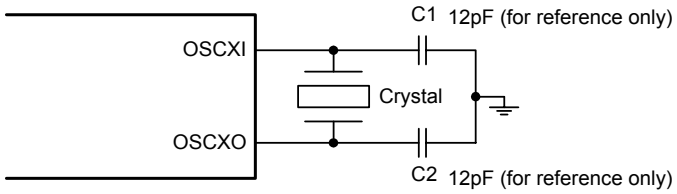


External ROSC RC

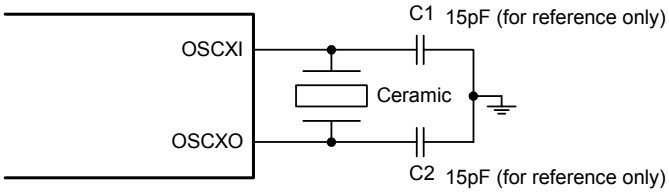
5.4. OSCX Oscillation

The OSCX is an internal 4MHz RC or external ceramic/crystal oscillator. The software options select the ceramic or internal RC as the CPU's clock.

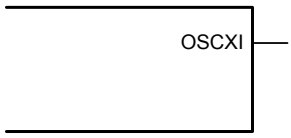
(1) OSCX Crystal Oscillator



(2) OSCX Ceramic Resonator



(3) OSCX internal RC Oscillator



Internal 4MHz RC

When the internal 4MHz RC is selected, the OSCXI pin and OSCXO pin is also set as PORTE.0, PORTE.1.

5.5. Control of Oscillator

The oscillator control register configuration is shown as blow.

Address	Bit3	Bit2	Bit1	Bit0	R/W
$14	OXS	-	OXM	OXON	R/W

OXON: OSCX oscillation on/off.
0: Turn-off OSCX oscillation 1: Turn-on OSCX oscillation
OXM: switching system clock.
0: select OSC as system clock 1: select OSCX as system clock
OXS: OSCX oscillator type selection
0: OSCX set as ceramic oscillator 1: OSCX set as RC oscillator, and set OSCXI/OSCXO as PORTE

5.6. Programming Notes

It takes at least 5 ms for the OSCX oscillation circuit to turn on until the oscillation stabilizes. When switching the CPU system clock from OSC to OSCX, the user must wait a minimum of 5ms since the OSCX oscillation is running. However, the start time varies with respect to oscillator characteristics and the condition of use. Thus the wait time depends on the application. When switching from OSCX to OSC, the user should switch clock first then turn off OSCX. If switching from OSCX to OSC and turning off OSCX in one instruction, the OSCX turn off control will be delayed for one instruction cycle automatically to prevent CPU operation error. Following is the timing of system clock switching.

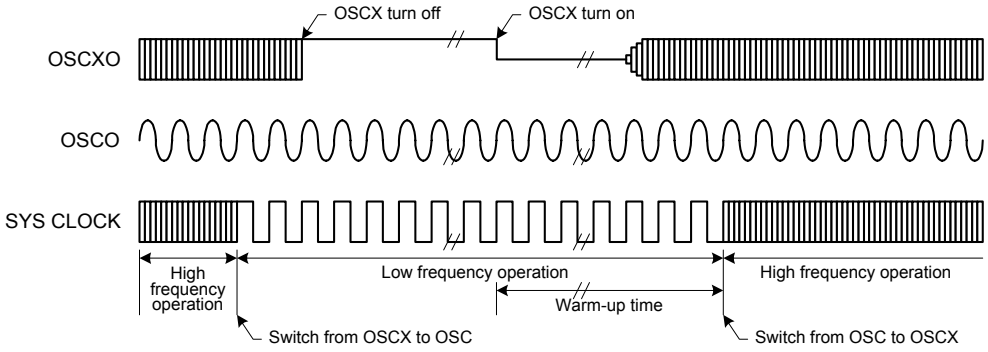


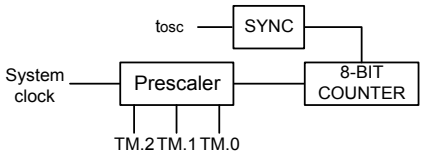
Figure 2. Timing of System Clock Switching

6. Timer0

The timer/counter has the following features:

- 8-bit up-counting timer/counter
- Automatic re-load counter
- 8-level prescaler
- Interrupt on overflow from $FF to $00

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

6.1. Timer0 Configuration and Operation

The Timer0 consist of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

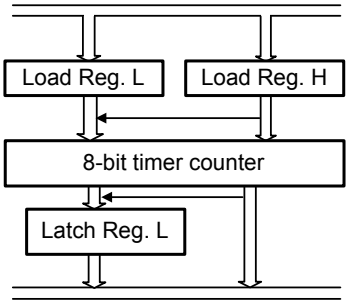
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



6.2. Timer0 Mode Register

The timer can be programmed in several different prescalers by setting Timer0 Mode register (TM0).

The 8-bit counter prescaler overflow output pulses. The Timer0 Mode registers (TM0) are 3-bit registers used for the timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

7. Base Timer

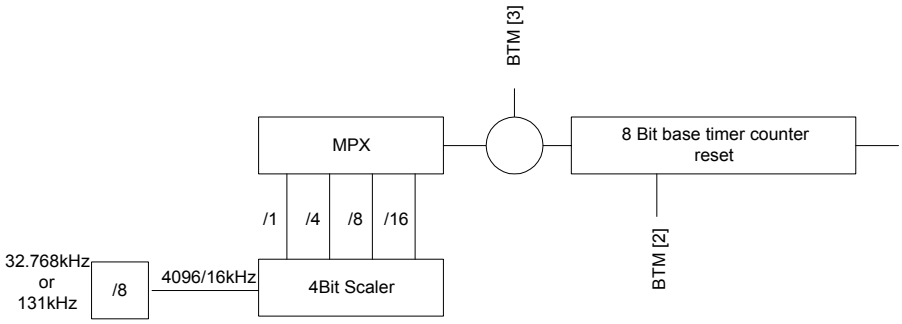
The MCU has a base timer that is shared with the warm-up timer and the clock source is base timer pre-scaler output pulse (scaled from OSC clock, Crystal 32.768kHz or RC 131kHz). After MCU is reset, it counts at every clock-input signal. When it counts to $FF, right after next clock input, counter counts to $00 and generates an overflow. This causes the interrupt flag of base timer to be set to “1”. Therefore, the base timer can function as an interval timer periodically, generating overflow output as every 256th clock signal input.

The timer accepts 4096Hz or 16KHz clock, and base timer generates an accurate timing interrupt. The program for accurate timing can reset this base time pre-scaler.

This clock-input source is selected by BTM register.

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$03	BTM.3	BTM.2	BTM.1	BTM.0	R/W	Base timer mode register
	1	0	X	X	R/W	Enable the base timer
	Else states		X	X	R/W	Disable the base timer, clear base timer counters and keep them as $00

BTM.1	BTM.0	Prescaler Ratio	Clock Source
0	0	/1	fosc/8
0	1	/4	fosc/32
1	0	/8	fosc/64
1	1	/16	fosc/128



8. I/O PORT

The SH66P51 provides 18 I/O pins. Each I/O pin contains pull-high MOS controllable by the program. Sections below show the circuit configuration of I/O ports.

PORTA, PORTB, PORTC, PORTD, PORTE

Each of these ports contains 4 bits or 2bits I/O pins (PORTC, PORTD are shared with LCD SEG1 - 8, PORTE are shared with OSCXI/OSCXO). The port control register can control ON/OFF of the output buffer for port. Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control
$1C	-	-	PECR.1	PECR.0	R/W	PORTE input/output control

PA (/B/C/D) CR.n, (n = 0, 1, 2, 3), PECR.n (n = 0, 1)

1: Set I/O as an output buffer.

0: Set I/O as an input buffer (power-on initial).

The following sections show the circuit configuration of the I/O ports.

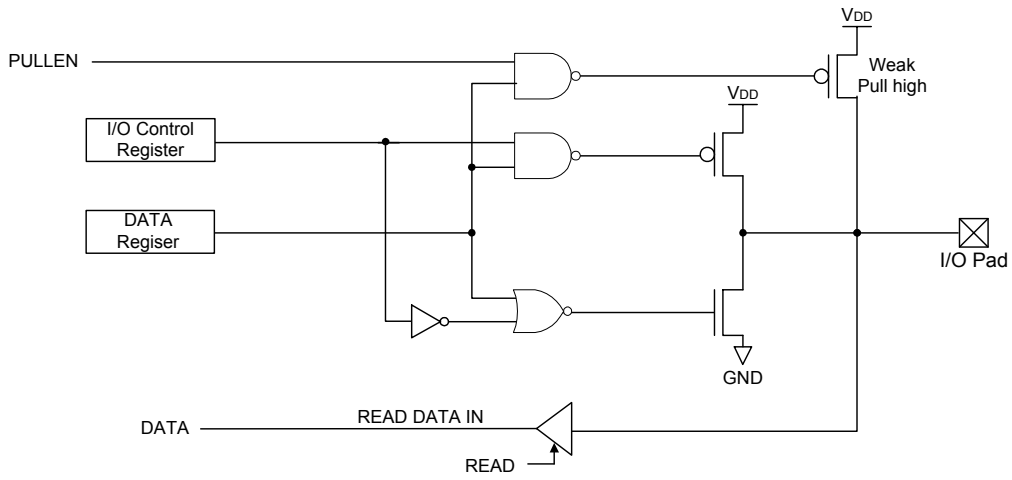


Figure 3. Port Configuration Function Block Diagram

I/O Share Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	OXS	-	OXM	OXON	R/W	Bit0: Turn on OSCX oscillator Bit1: CPU clocks select (1: OSCX/0: OSC) Bit3: OSCX type selection
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit0, 1: Select LCD DUTY (1/3 or 1/4 or 1/5 or 1/6) Bit2: Set PORTC as LCD Segment1 - 4 Bit3: Set PORTD as LCD Segment5 - 8

OXS: 0: OSCX set as ceramic oscillator (Default)
1: OSCX set as RC oscillator, and set OSCXI/OSCXO as PORTE

O/S0: 0: select PORTC as I/O ports
1: select PORTC as LCD Segment 1 - 4 (Default)

O/S1: 0: select PORTD as I/O ports
1: select PORTD as LCD Segment 5 - 8 (Default)

The default value of O/S0, O/S1 is “1”, after Power on/Pad/LVR reset. It means that the PORTC, PORTD is shared to Segment 1 - 8 and output GND after Power on/Pad/LVR reset. So, the PORTC, PORTD shouldn’t be pulled high by external signal source to avoid the additional leakage current when reset.

Controlling the Pull-high MOS

These ports contain pull-high MOS controlled by the program. PULLEN register controls On/Off of all pull-high MOS simultaneously. Pull-high MOS is controlled by the port data registers (PA, PB, PC, PD, PE) of each port also. Thus, the pull-high MOS can be turned on and off individually.

To turn on the pull-high resistor, PULLEN must be set to “1”, and write “1” to the port data register.

Port Function Control is below:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PULLEN	CPS2	CPS1	CPS0	R/W	Bit2 - 0: Carrier counter source pre-divider Bit3: Port pull high enable control

PULLEN Port Pull-low enables control
1 = Enable PORT pull-high
0 = Disable PORT pull-high(power-on initialization)

Ports as Key Matrix

SH66P51’s I/O can make up of key matrix and PORTC - PORTD can use as LCD segment output as same time. In this application, user should control that scanning key matrix share the timing of LCD display. Only when user scan key matrix, all of Ports are used as I/O; otherwise PORTC, PORTD use as LCD segment output to drive LCD panel. The Ports used as I/O or segment is controlled by software.

In scan key application, when user doesn’t execute operation of scan key, Ports which don’t share as LCD segment output should be set as I/O, disabled it’s pull high resistor and input/output access by write system register ($16 - $1C) ’s corresponding bit. Execute above operation can prevent LCD voltage input to the general I/O Ports and Port’s pull high or output affect the LCD segment’s waveform.

When user wants to scan key, all ports, which make up of the key matrix should be used as general I/O, the ports’ pull high resistor and input access should be enabled by clear the system register ($16, $17) ’s corresponding bit.

Key Matrix's IO Ports Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$16	PAIN	PBIN	PCIN	PDIN	R/W	Control PORTA - PORTD input and output access enable or disable. Used in key matrix's application
$17	-	-	-	PEIN	R/W	Control PORTE input and output access enable or disable. Used in key matrix's application

PAIN…PEIN: In the key matrix's application, control PORTA - PORTE input and output access.
0: Enable PORTA - PORTE pull-high resistor and I/O access, Ports in normal state
1: Disable PORTA - PORTE pull-high resistor and its I/O access

Port Interrupt

The PORTB and PORTC are used as port interrupt sources. Since PORT I/O is bit programmable I/O, so only the input port can generate an external interrupt. Any one of the PORTB and PORTC input pin transitions from V_{DD} to GND would generate an interrupt request. Further falling edge transition would not be able to make an interrupt request until all of the input pins have returned to V_{DD}. The following is the port interrupts function block-diagram.

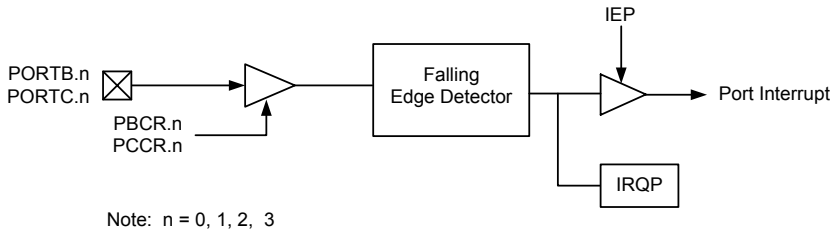


Figure 4. PORT Interrupt Block Diagram

8. Remote Control Carrier Synthesizer

The device has a built-in carrier synthesizer for infrared or RF remote control circuits.

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	PULLEN	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier counter source pre-divider Bit3: Port pull high enable control
$0D	-	-	-	REMO REM	W R	Bit0: REMO output data Bit0: REM pin output status

The carrier synthesizer can be programmed in several different pre-scaler ratios by setting CPS2 - 0.

CPS2	CPS1	CPS0	Pre-scaler Divide Ratio	Ratio N
0	0	0	System clock/2^{11}	2048
0	0	1	System clock/2^{9}	512
0	1	0	System clock/2^{7}	128
0	1	1	System clock/2^{5}	32
1	0	0	System clock/2^{3}	8
1	0	1	System clock/2^{2}	4
1	1	0	System clock/2^{1}	2
1	1	1	System clock/2^{0}	1

The carrier-generating counter is an 8-bit count-up counter and two 8-bit data load registers (High level data register and Low level data register). Writing data into the data load registers can initialize the counter.

After system reset, the counter is automatically loaded with the contents of high level data register and output high level at the same time. Following when counter counts overflow from $FF to $00,the counter is automatically loaded with the contents of low level data register and output low level at the same time. When counter counts overflow again from $FF to $00 again, the counter will be loaded with the contents of high level data register again. The above sequences make up a complete loop. So the carrier synthesizer can output continuous carrier wave of certain duties and certain period.

If REMO is set to “1” from “0”, the carrier counter will be initialized to load high level data register and output high level whatever states the counter is.

Load register programming: User can modify low level data register to change the width of the low level or modify high level data register to change the width of high level. In the way the carrier synthesizer can output carrier wave of different duties and different period.

REM will remain outputting carrier wave in HALT mode, but will output GND in STOP mode.

Carrier Load Data Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$20	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register
$21	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register
$22	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register
$23	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register

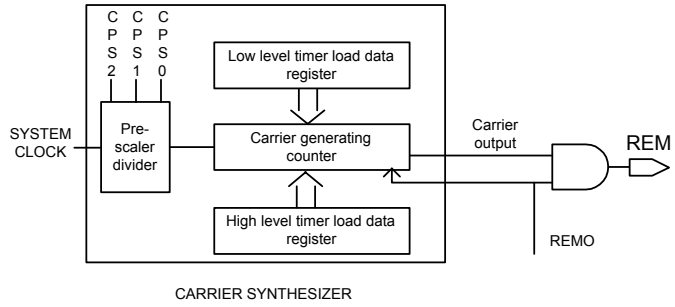


Figure 5. Remote Control Functional Block Diagram

For Example:

System clock	CPS2, CPS1, CPS0	CFL	CFH	Carrier Duty	Carrier Frequency
4M/4	1, 1, 1	$EF	$F8	8/25 ≈ 1/3	40.00kHz
4M/4	1, 1, 1	$EF	$F7	9/26 ≈ 1/3	38.46kHz
4M/4	1, 1, 1	$F2	$F3	13/27 ≈ 1/2	37.04kHz
4M/4	1, 1, 1	$EB	$F9	7/28 = 1/4	35.71kHz
480k/4	1, 1, 1	$FE	$FF	1/3 = 1/3	40.00kHz
455k/4	1, 1, 1	$FE	$FF	1/3 = 1/3	37.92kHz
432k/4	1, 1, 1	$FE	$FF	1/3 = 1/3	36.00kHz

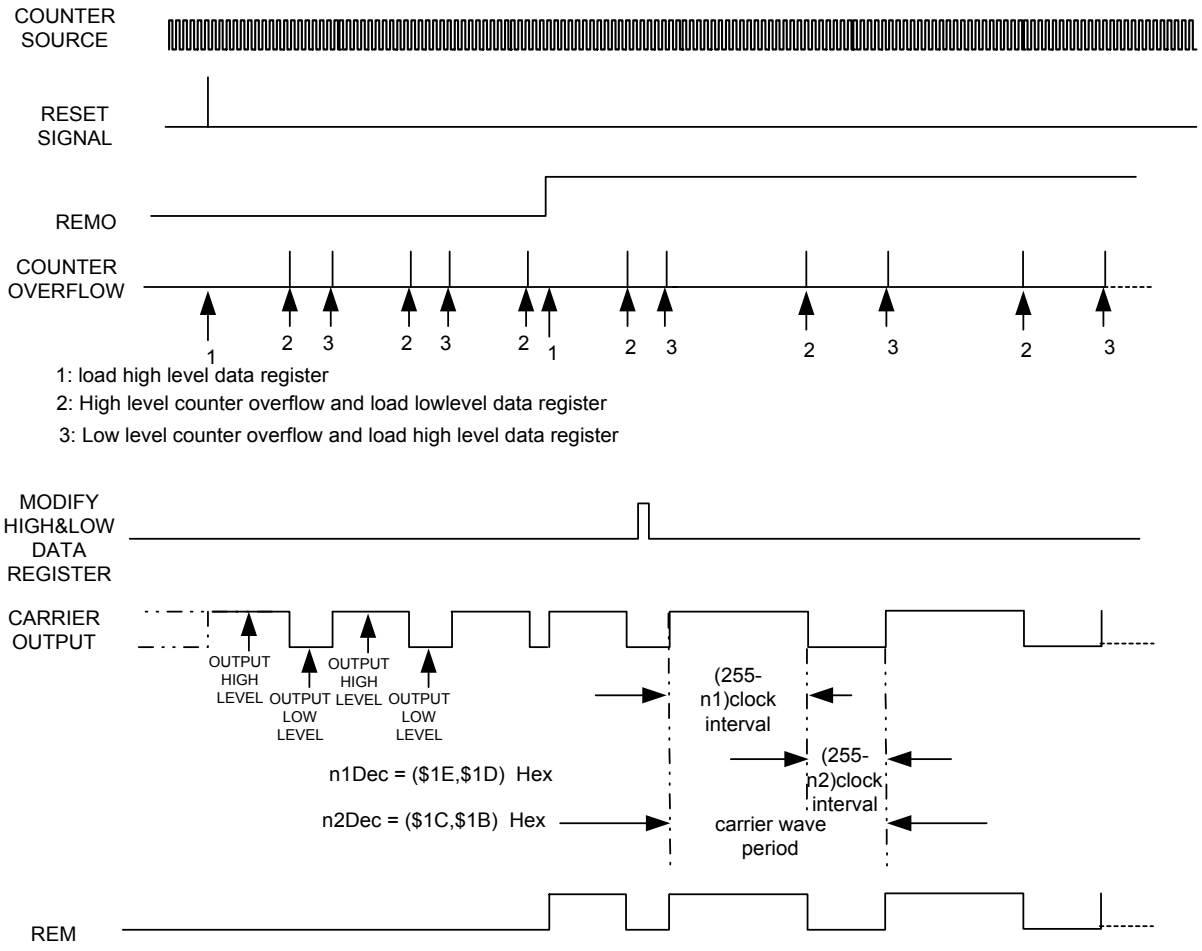


Figure 6. Carrier Synthesize Wave

9. LCD Driver

The LCD driver contains a controller, a voltage regulator generator, 6 common driver pins and 26 segment driver pins. There are four different driving programmable modes: 1/3 duty and 1/3 bias, 1/4 duty and 1/3 bias, 1/5 duty and 1/3 bias and 1/6 duty and 1/3 bias. The driving mode is controlled by the system register $15 and the power on initialization status is 1/4 duty, 1/3 bias.

When 1/5 duty and 1/3 bias mode are used, COM6 are used as SEG27.
When 1/4 duty and 1/3 bias mode are used, COM5 - 6 are used as SEG28 - 27.
When 1/3 duty and 1/3 bias mode are used, COM4 - 6 are used as SEG29 - 27.

The controller consists of display data RAM and a duty generator.

The LCD SEG1 - 4 can also be used as I/O port (PORTC), which is selected by bit2 of the system register $15 and the LCD SEG5 - 8 can also be used as I/O port (PORTD), which is selected by bit3 of the system register $15. LCD RAM could be used as data memory if needed.

When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When LCD off, both common and segment output low.

9.1. LCD Control Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$07	-	LCDON	-	-	R/W	Bit2: Set LCD display ON
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit0, 1: Select LCD DUTY (1/3 or 1/4 or 1/5 or 1/6) Bit2: Set PORTC as LCD Segment1 - 4 Bit3: Set PORTD as LCD Segment5 - 8

LCD Segment:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit2: Select PORTC or LCD segment Bit3: Select PORTD or LCD segment
	X	0	X	X		PORTC as I/O ports
	X	1	X	X		PORTC as LCD SEG 1 - 4
	0	X	X	X		PORTD as I/O ports
	1	X	X	X		PORTD as LCD SEG 5 - 8

LCD Duty:
DUTY1, DUTY0: LCD duty control

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$15	O/S1	O/S0	DUTY1	DUTY0	R/W	Bit0, 1: LCD duty control
	X	X	0	0		LCD driver = 1/4 duty, 1/3 bias
	X	X	0	1		LCD driver = 1/3 duty, 1/3 bias
	X	X	1	0		LCD driver = 1/5 duty, 1/3 bias
	X	X	1	1		LCD driver = 1/6 duty, 1/3 bias

LCD Clock:
LCD clock is divided from OSC, so LCD frame frequency will change in proportion to the variation of OSC frequency in spite of OSC type.

FRAME Frequency (When fosc = 32.768kHz/131kHz)	
IN 1/6 DUTY MODE	42.7Hz
IN 1/5 DUTY MODE	34.1Hz
IN 1/4 DUTY MODE	32Hz
IN 1/3 DUTY MODE	42.7Hz

9.2. Configuration of LCD RAM

LCD 1/4 duty 1/3 bias (4 X 28)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
$300	SEG1	SEG1	SEG1	SEG1	$30E	SEG15	SEG15	SEG15	SEG15
$301	SEG2	SEG2	SEG2	SEG2	$30F	SEG16	SEG16	SEG16	SEG16
$302	SEG3	SEG3	SEG3	SEG3	$310	SEG17	SEG17	SEG17	SEG17
$303	SEG4	SEG4	SEG4	SEG4	$311	SEG18	SEG18	SEG18	SEG18
$304	SEG5	SEG5	SEG5	SEG5	$312	SEG19	SEG19	SEG19	SEG19
$305	SEG6	SEG6	SEG6	SEG6	$313	SEG20	SEG20	SEG20	SEG20
$306	SEG7	SEG7	SEG7	SEG7	$314	SEG21	SEG21	SEG21	SEG21
$307	SEG8	SEG8	SEG8	SEG8	$315	SEG22	SEG22	SEG22	SEG22
$308	SEG9	SEG9	SEG9	SEG9	$316	SEG23	SEG23	SEG23	SEG23
$309	SEG10	SEG10	SEG10	SEG10	$317	SEG24	SEG24	SEG24	SEG24
$30A	SEG11	SEG11	SEG11	SEG11	$318	SEG25	SEG25	SEG25	SEG25
$30B	SEG12	SEG12	SEG12	SEG12	$319	SEG26	SEG26	SEG26	SEG26
$30C	SEG13	SEG13	SEG13	SEG13	$31A	SEG27	SEG27	SEG27	SEG27
$30D	SEG14	SEG14	SEG14	SEG14	$31B	SEG28	SEG28	SEG28	SEG28

LCD 1/3 duty 1/3 bias (3 X 29)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	-	COM3	COM2	COM1		-	COM3	COM2	COM1
$300	-	SEG1	SEG1	SEG1	$30F	-	SEG16	SEG16	SEG16
$301	-	SEG2	SEG2	SEG2	$310	-	SEG17	SEG17	SEG17
$302	-	SEG3	SEG3	SEG3	$311	-	SEG18	SEG18	SEG18
$303	-	SEG4	SEG4	SEG4	$312	-	SEG19	SEG19	SEG19
$304	-	SEG5	SEG5	SEG5	$313	-	SEG20	SEG20	SEG20
$305	-	SEG6	SEG6	SEG6	$314	-	SEG21	SEG21	SEG21
$306	-	SEG7	SEG7	SEG7	$315	-	SEG22	SEG22	SEG22
$307	-	SEG8	SEG8	SEG8	$316	-	SEG23	SEG23	SEG23
$308	-	SEG9	SEG9	SEG9	$317	-	SEG24	SEG24	SEG24
$309	-	SEG10	SEG10	SEG10	$318	-	SEG25	SEG25	SEG25
$30A	-	SEG11	SEG11	SEG11	$319	-	SEG26	SEG26	SEG26
$30B	-	SEG12	SEG12	SEG12	$31A	-	SEG27	SEG27	SEG27
$30C	-	SEG13	SEG13	SEG13	$31B	-	SEG28	SEG28	SEG28
$30D	-	SEG14	SEG14	SEG14	$31C	-	SEG29	SEG29	SEG29
$30E	-	SEG15	SEG15	SEG15	-	-	-	-	-

LCD 1/5 duty 1/3 bias (5 X 27)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	-	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	-	-	-	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	-	-	-	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	-	-	-	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	-	-	-	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	-	-	-	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	-	-	-	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	-	-	-	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	-	-	-	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$328	-	-	-	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$329	-	-	-	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$32A	-	-	-	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$32B	-	-	-	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$32C	-	-	-	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$32D	-	-	-	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$32E	-	-	-	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$32F	-	-	-	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$330	-	-	-	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$331	-	-	-	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$332	-	-	-	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$333	-	-	-	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$334	-	-	-	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$335	-	-	-	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$336	-	-	-	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$337	-	-	-	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$338	-	-	-	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$339	-	-	-	SEG26
$31A	SEG27	SEG27	SEG27	SEG27	$33A	-	-	-	SEG27

LCD 1/6 duty 1/3 bias (6 X 26)

Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		-	-	COM6	COM5
$300	SEG1	SEG1	SEG1	SEG1	$320	-	-	SEG1	SEG1
$301	SEG2	SEG2	SEG2	SEG2	$321	-	-	SEG2	SEG2
$302	SEG3	SEG3	SEG3	SEG3	$322	-	-	SEG3	SEG3
$303	SEG4	SEG4	SEG4	SEG4	$323	-	-	SEG4	SEG4
$304	SEG5	SEG5	SEG5	SEG5	$324	-	-	SEG5	SEG5
$305	SEG6	SEG6	SEG6	SEG6	$325	-	-	SEG6	SEG6
$306	SEG7	SEG7	SEG7	SEG7	$326	-	-	SEG7	SEG7
$307	SEG8	SEG8	SEG8	SEG8	$327	-	-	SEG8	SEG8
$308	SEG9	SEG9	SEG9	SEG9	$328	-	-	SEG9	SEG9
$309	SEG10	SEG10	SEG10	SEG10	$329	-	-	SEG10	SEG10
$30A	SEG11	SEG11	SEG11	SEG11	$32A	-	-	SEG11	SEG11
$30B	SEG12	SEG12	SEG12	SEG12	$32B	-	-	SEG12	SEG12
$30C	SEG13	SEG13	SEG13	SEG13	$32C	-	-	SEG13	SEG13
$30D	SEG14	SEG14	SEG14	SEG14	$32D	-	-	SEG14	SEG14
$30E	SEG15	SEG15	SEG15	SEG15	$32E	-	-	SEG15	SEG15
$30F	SEG16	SEG16	SEG16	SEG16	$32F	-	-	SEG16	SEG16
$310	SEG17	SEG17	SEG17	SEG17	$330	-	-	SEG17	SEG17
$311	SEG18	SEG18	SEG18	SEG18	$331	-	-	SEG18	SEG18
$312	SEG19	SEG19	SEG19	SEG19	$332	-	-	SEG19	SEG19
$313	SEG20	SEG20	SEG20	SEG20	$333	-	-	SEG20	SEG20
$314	SEG21	SEG21	SEG21	SEG21	$334	-	-	SEG21	SEG21
$315	SEG22	SEG22	SEG22	SEG22	$335	-	-	SEG22	SEG22
$316	SEG23	SEG23	SEG23	SEG23	$336	-	-	SEG23	SEG23
$317	SEG24	SEG24	SEG24	SEG24	$337	-	-	SEG24	SEG24
$318	SEG25	SEG25	SEG25	SEG25	$338	-	-	SEG25	SEG25
$319	SEG26	SEG26	SEG26	SEG26	$339	-	-	SEG26	SEG26

LCD Power

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$07	-	LCDON	-	-	R/W	Bit2: Set LCD display ON
	X	0	X	X		LCD OFF
	X	1	X	X		LCD ON

* When LCD is off, COM & SEG output GND in LCD application.
SH66P51 builds in a voltage regulator and it can generate a stable voltage for LCD when V_{DD} between 2.0V and 3.6V.
* The following diagram is the application diagram for LCD power circuit

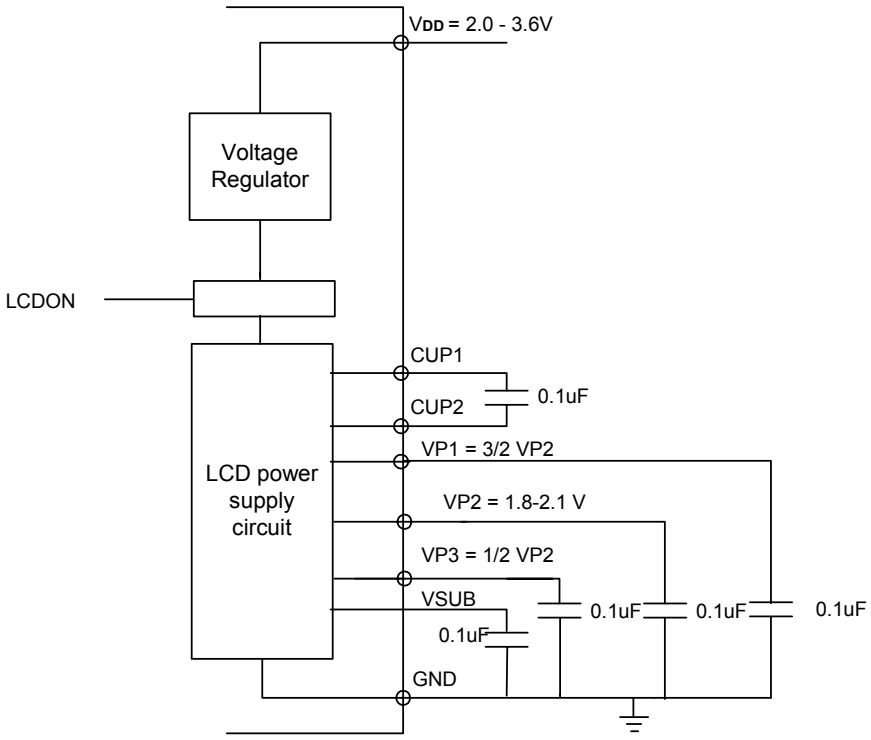


Figure 7. LCD Power Circuit Diagram

10. Interrupt

Three interrupt sources are available on SH66P51:

- Timer0 overflow interrupt
- Base timer overflow interrupt
- Port's falling edge detection interrupt (PBC)

Interrupt Control Bits and Interrupt Service

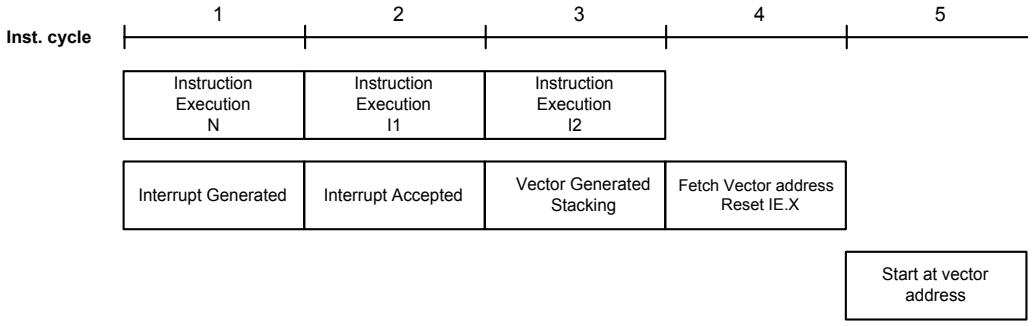
The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to "0" at initialization by the chip reset.

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	IEBT	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags

When IEx is set to "1" and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to "0" automatically, thus, when IRQx is 1 and IEx is set to "1" again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

Interrupt Servicing Sequence Diagram:



Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

Timer Interrupt

The input clock of Timer0 is based on system clock and the input clock of Base timer is based on OSC clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQBT = 1), If the interrupt enable flag is enabled (IET0 or IEBT = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port Falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input can not generate an interrupt request.

Any one of the I/O input pin transitions from VDD to GND would generate an interrupt request (IRQP = 1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to V_{DD}. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

11. HALT and STOP Mode

After the execution of HALT instruction, SH66P51 will enter the HALT mode. In the HALT mode, CPU will STOP operating. But peripheral circuit (Timer0, Base timer) will keep status.

After the execution of STOP instruction, SH66P51 will enter the STOP mode. The whole chip (including oscillator) will STOP operating.

In the HALT mode, SH66P51 can be waked up if any interrupt occurs.

In the STOP mode, SH66P51 can be waked up if port interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to halt /stop is executed.

12. Low Power Detect (LPD)

The LPD function monitors the supply voltage of the battery

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$06	-	-	-	LPD	R	Bit0: 2.3V LPD flag

Functions of LPD Circuit:
The LPD circuit has the following functions:
LPD bit = 1 when $V_{DD} \leq V_{LPD}$ (= 2.3 ± 0.1V)
LPD bit = 0 when $V_{DD} > V_{LPD}$ (= 2.3 ± 0.1V)

13. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR circuit has the following functions:
- Generates a system reset when $V_{DD} \leq V_{LVR}$ (= 1.7 ± 0.1V).
- Cancels the system reset when $V_{DD} > V_{LVR}$ (= 1.7 ± 0.1V).

14. Watchdog Timer

Watchdog timer is a down-count counter, and its clock source is OSC clock (32.768kHz Crystal or 131kHZ RC) and will not run in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the Code Option.

The watchdog timer control bits ($1E bit2 - bit0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E bit3) will be automatically set to “1” by hardware when the watchdog timer overflows. And the flag ($1E bit3) will be clear to “0” when read $1E. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power ON
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit0 - 2: Watchdog timer control Bit3: Watchdog timer overflow flag. (Read only)	0000
	X	0	0	0		Watchdog timer-out period = 2^{17}/fosc	Yes
	X	0	0	1		Watchdog timer-out period = 2^{15}/fosc	
	X	0	1	0		Watchdog timer-out period = 2^{13}/fosc	
	X	0	1	1		Watchdog timer-out period = 2^{11}/fosc	
	X	1	0	0		Watchdog timer-out period = 2^{10}/fosc	
	X	1	0	1		Watchdog timer-out period = 2^{9}/fosc	
	X	1	1	0		Watchdog timer-out period = 2^{8}/fosc	
	X	1	1	1		Watchdog timer-out period = 2^{7}/fosc	
	0	X	X	X		No watchdog timer overflow reset	Yes
	1	X	X	X		Watchdog timer overflow	

Note:
Watchdog timer overflow period is valid for V_{DD} = 3V.

15. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

- Power-on Reset/Low voltage Reset/Pin Reset warm-up time interval:
- Wake-up from stop mode
- Watchdog Reset

(1) In RC oscillator mode, the warm-up counter prescaler divide ratio is /2^{10} (1024).
(2) In internal 4M RC oscillator mode, the warm-up counter prescaler divide ratio is /2^{15} (32768).
(3) In Crystal oscillator or Ceramic resonator mode, the warm-up counter prescaler divide ratio is /2^{13} (8192).

16. Code Option

OSC: (Code Option)
- 0: Crystal oscillator 32.768kHz Crystal
- 1: RC oscillator: 131kHz RC

WDT: (Code Option)
- 0: Enable the watchdog timer
- 1: Disable the watchdog timer

Reset internal pull-high resistor: (Code Option)
- 0: Enable
- 1: Disable

Instruction Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC <- Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx <- Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC <- Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx <- Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC <- Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx <- Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC <- Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx <- Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC <- Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx <- Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC <- Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx <- Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC <- Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx <- Mx & AC	
SHR	11110 0000 000 0000	0 -> AC[3], AC[0] -> CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC <- Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx <- Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC <- Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx <- Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx <- Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx <- Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx <- Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx <- Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx <- Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC <- Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx <- AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx <- I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC <- X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC <- X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC <- X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC <- X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC <- X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC <- X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC <- X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC <- X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST <- CY, PC +1 PC <- X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC <- ST; TBR <- hhhh, AC <- lll	
RTNI	11010 1000 000 0000	CY, PC <- ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC <- X (Include p)	
TJMP	11110 1111 111 1111	PC <- (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Rating*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -10℃ to +70℃

Storage Temperature . . . . . -55℃ to +125℃

*Comments

Stresses exceed those listed under **"Absolute Maximum Ratings"** may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions exceed those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.8	3.0	3.6	V	30kHz ≤ f_{OSC} ≤ 4MHz
Low Voltage Reset voltage	V_{LVR}	1.6	1.7	1.8	V	30kHz ≤ f_{OSC} ≤ 4MHz
Low Power Detect voltage	V_{LPD}	2.2	2.3	2.4	V	30kHz ≤ f_{OSC} ≤ 4MHz
Operating Current	I_{OP}	-	0.3	0.5	mA	f_{OSCX} = 4MHz, (OSCX as system clock) All output pins unloaded, Execute NOP instruction. V_{DD} = 3.0V
Stand by Current 1 (HALT)	I_{SB1}	-	4	6	μA	f_{OSC} = 32.768kHz crystal, OSCX off All output pins unloaded (HALT mode), LCD on, without LCD panel, WDT on. V_{DD} = 3.0V
Stand by Current 2 (STOP)	I_{SB2}	-	-	1	μA	All output pins unloaded (STOP mode), LCD off, WDT off. V_{DD} = 3.0V
Input Low Voltage	V_{IL1}	GND - 0.3	-	V_{DD} X 0.3	V	I/O ports, pins tri-state
Input Low Voltage	V_{IL2}	GND - 0.3	-	V_{DD} X 0.15	V	$\overline{RESET}$, TEST, OSCI (Schmitt trigger input)
Input High Voltage	V_{IH1}	V_{DD} X 0.7	-	V_{DD} + 0.3	V	I/O ports, pins tri-state
Input High Voltage	V_{IH2}	V_{DD} X 0.85	-	V_{DD} + 0.3	V	$\overline{RESET}$, TEST, OSCI (Schmitt trigger input)
Input Leakage Current	I_{IL}	-1	-	1	μA	I/O ports, GND < V_{IN}< V_{DD}
REM sink current	I_{REM1}	0.3	-	-	mA	V_{REM1} = 0.3V (V_{DD} = 3.0V)
REM driving current	I_{REM2}	-5	-9	-	mA	V_{REM2} = 1V (V_{DD} = 3.0V)
Pull-high Resistor	RP	-	150	-	kΩ	Pull-high resistor (V_{DD} = 3.0V)
Output High Voltage	V_{OH1}	V_{DD} - 0.7	-	-	V	PORTB-PORTE, I_{OH1} = -0.5mA (V_{DD} = 3.0V)
Output High Voltage	V_{OH2}	V_{DD} - 0.7	-	-	V	PORTA, I_{OH2} = -5mA (V_{DD} = 3.0V)
Output Low Voltage	V_{OL1}	-	-	GND + 0.6	V	PORTB-PORTE, I_{OL1} = 1mA (V_{DD} = 3.0V)
Output Low Voltage	V_{OL2}	-	-	GND + 0.6	V	PORTA, I_{OL2} = 10mA (V_{DD} = 3.0V)
LCD ON driving resistor	R_{ON}	-	5	-	kΩ	LCD SEG1-29, COM1-6 the voltage variation of V1, V2, V3 is less than 0.2V

LCD Voltage Regulator Circuitry (GND = 0V, V_{DD} = 2.0 - 3.6V, T_A = 5 - 45℃ unless otherwise specified)

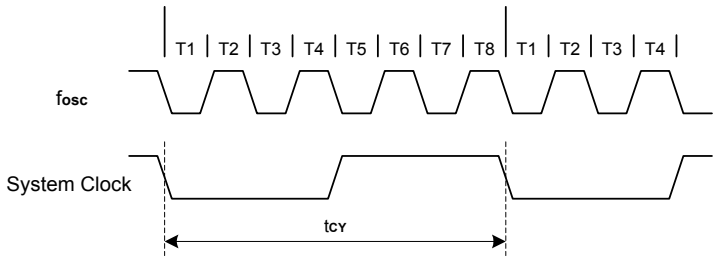
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Regulator output voltage (VP2 output voltage)	V2	1.8	2.0	2.1	V	Connecting a 200k resistor between VP2 and GND. Without LCD panel load.

AC Electrical Characteristics (V_{DD} = 3.0V GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillator Start time	t_{OST}	-	1	2	s	Oscillator = 32.768kHz
Internal RC Frequency Variation	f_{OSCX}	3.92	4	4.08	MHz	V_{DD} = 2.0 - 3.6V, T_A = +5℃ to +45℃

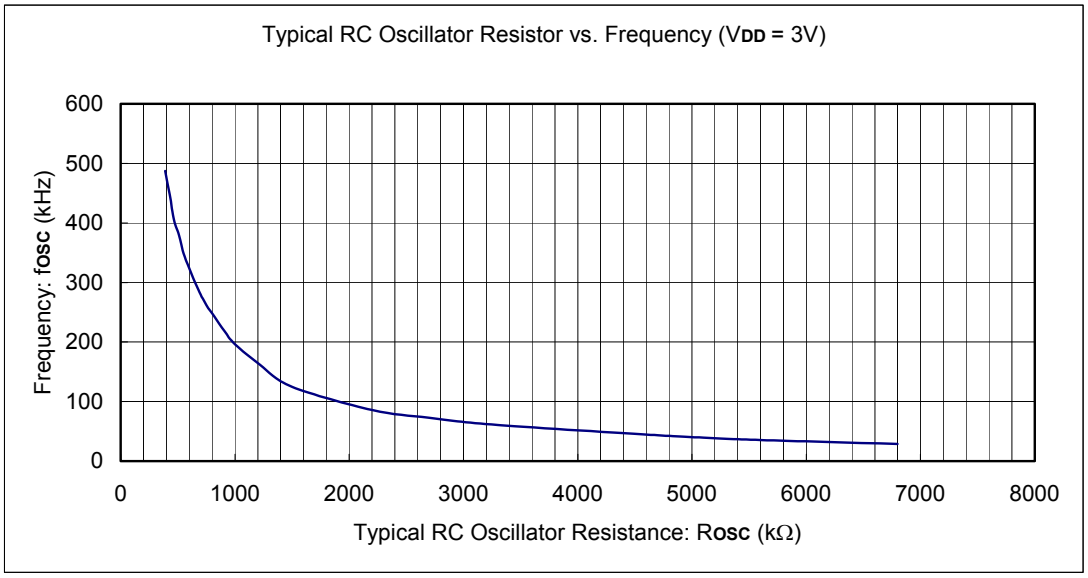
Timing Waveform

System Clock Timing Waveform:

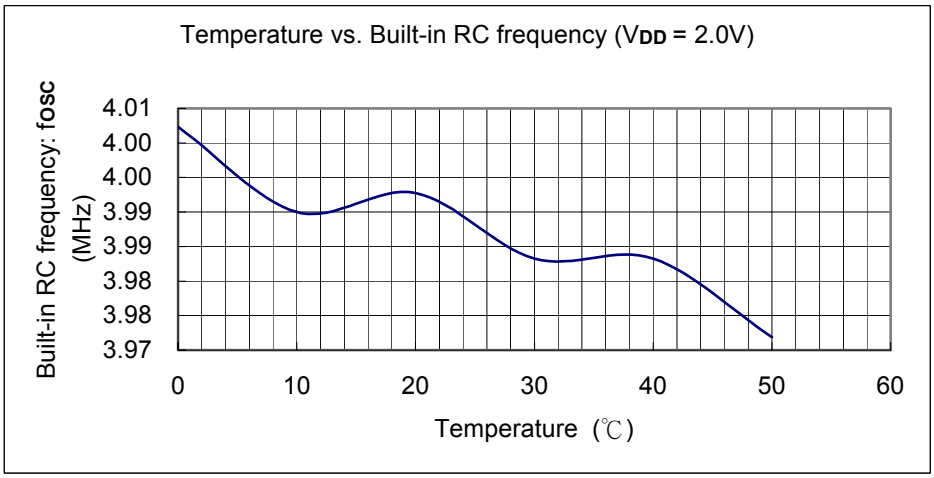


RC Oscillator Characteristics Graphs (for reference only)

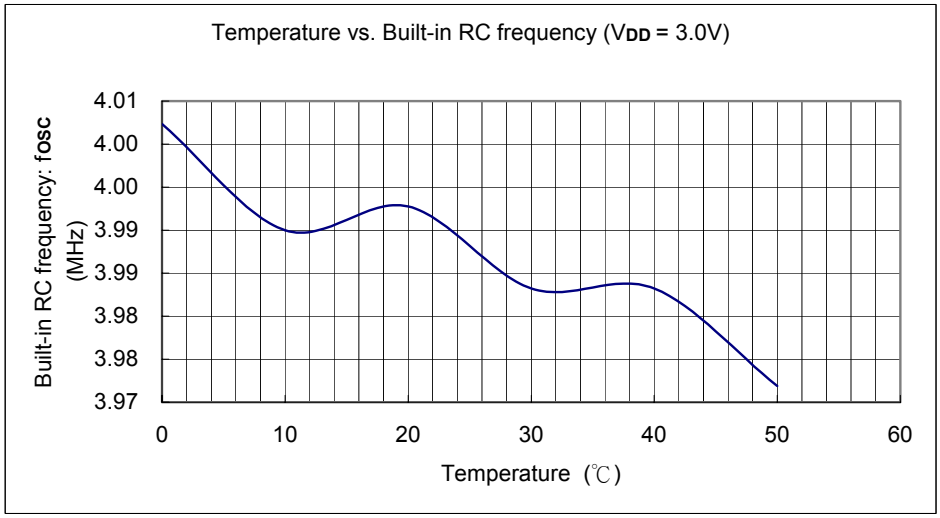
(1) Typical RC Oscillator Resistor vs. Frequency: (for reference only)



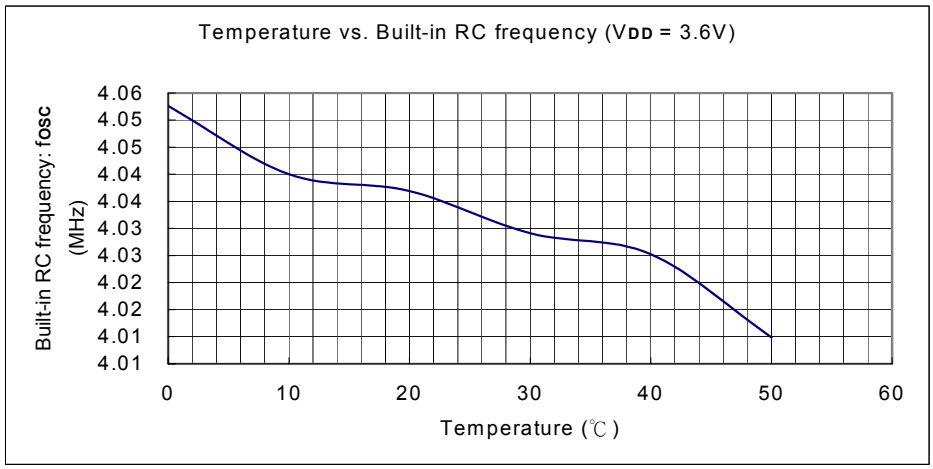
(2) Build-in RC Oscillator Frequency vs. Operating Ambient Temperature: (for reference only)



Temperature vs. Built-in RC fosc (VDD = 2.0V)



Temperature vs. Built-in RC fosc (VDD = 3.0V)



Temperature vs. Built-in RC fosc (VDD = 3.6V)

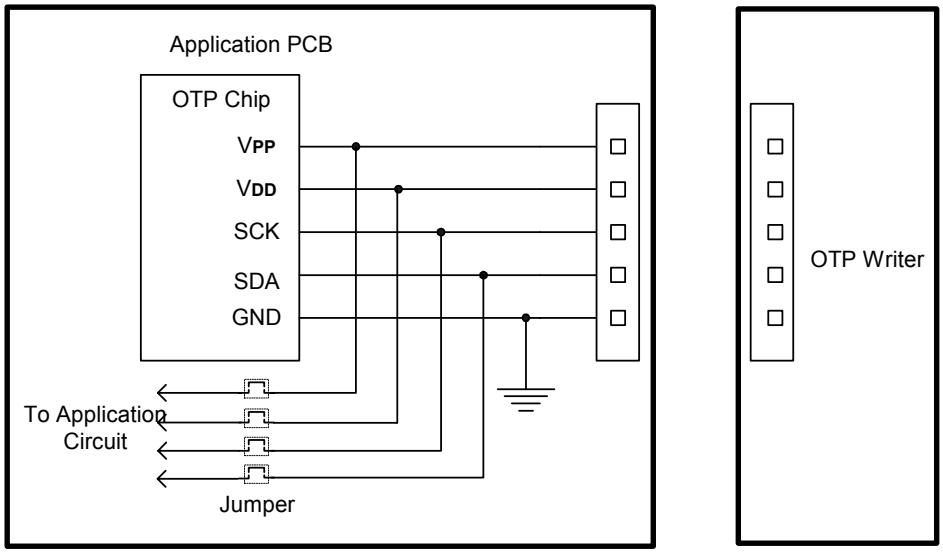
In System Programming Notice for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.

[For few OTP chip with more V_{DD} pads, the V_{DD} pads should be connected together.]



The recommended steps are the followings:

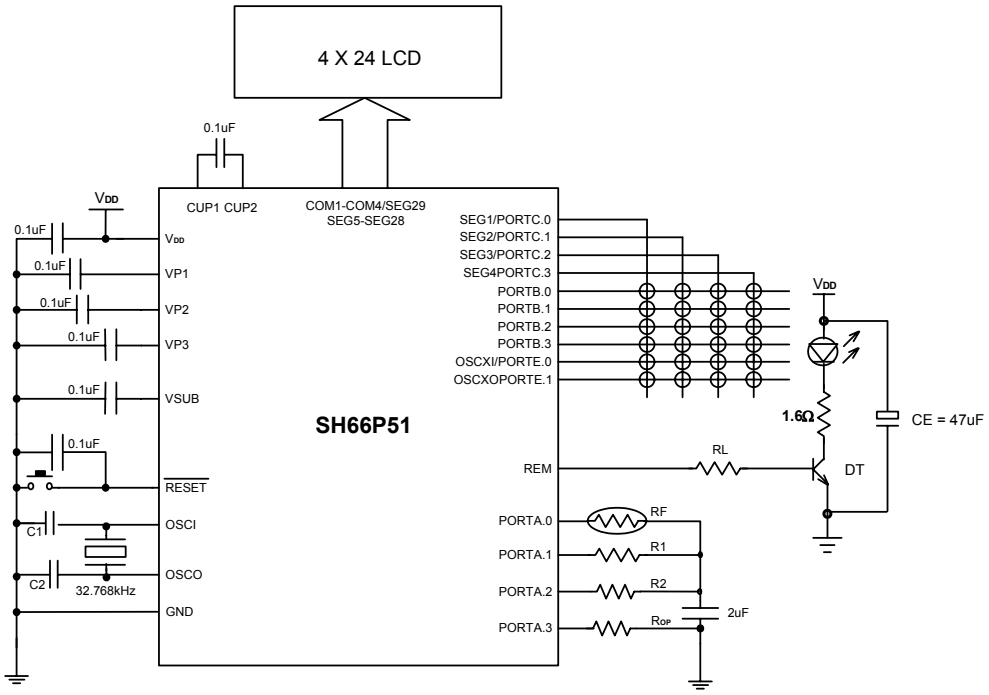
(1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.
(2) Connect the programming interface with OTP writer and begin programming.
(3) Disconnect OTP writer and shorten these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Application Circuit (for reference only)

AP1 (Remote Control)

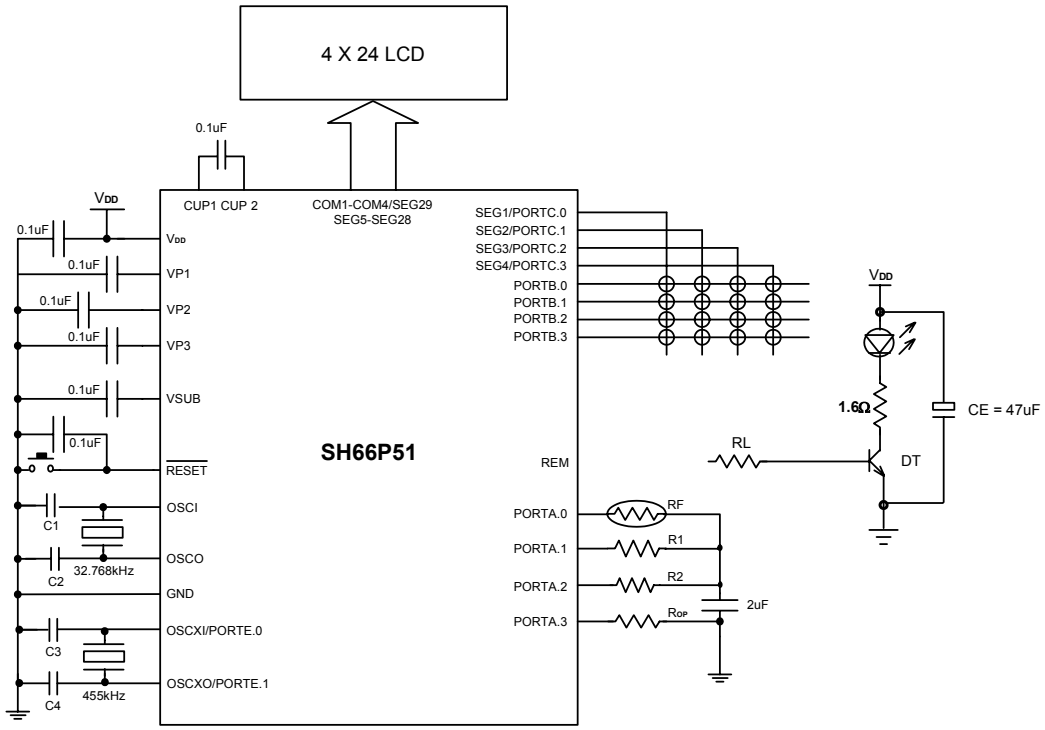
(1) Operating voltage: 3.0V
(2) Oscillator: Crystal 32.768kHz and Internal RC
(3) PORTA.0 - PORTA.2, PORTB, PORTC, PORTE: I/O Buffers
(4) PORTA.3: Input Buffers
(5) RL = 0 is possible, but the REM specification is revised to reduce power consumption



RF: Temperature Sensor
R1, 2: Reference Resistor
ROP: Option Resistor
C1, C2: 12pF (for reference only)

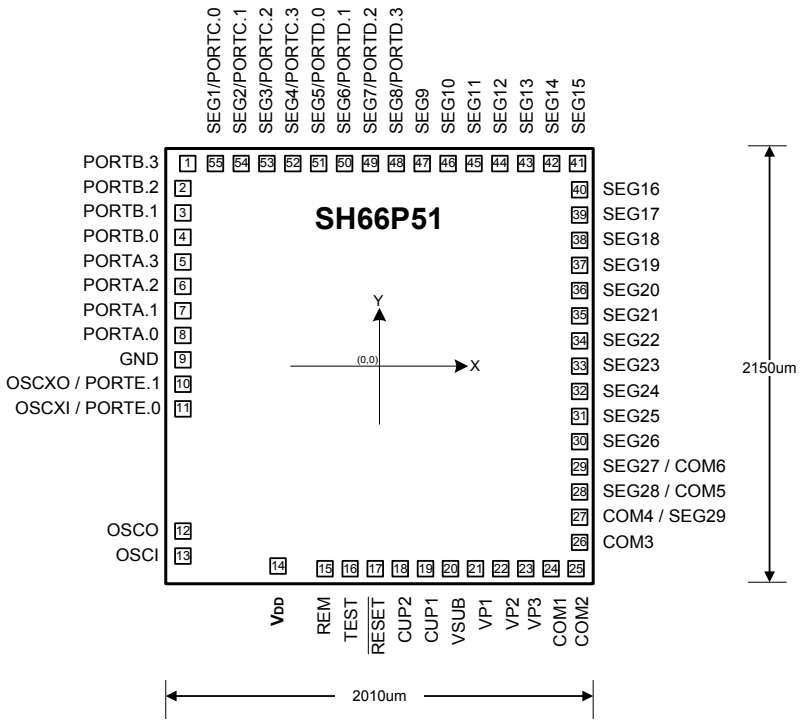
AP2 (Remote Control)

(1) Operating voltage: 3.0V
(2) Oscillator: Crystal 32.768kHz and Crystal 455kHz
(3) PORTA.0 - PORTA.2, PORTB, PORTC: I/O Buffers
(4) PORTA.3: Input Buffers
(5) RL = 0 is possible, but the REM specification is revised to reduce power consumption



RF: Temperature Sensor
R1, 2: Reference Resistor
ROP: Option Resistor
C1, C2: 12pF(for reference only)
C3, C4: 30pF(for reference only)

Bonding Diagram



* Substratum connects to GND.

Pad Location unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTB.3	-867.5	947.5	19	CUP1	172.5	-947.4
2	PORTB.2	-878.5	810.05	20	VSUB	287.5	-947.4
3	PORTB.1	-878.5	690.05	21	VP1	402.5	-947.4
4	PORTB.0	-878.5	570.05	22	VP2	517.5	-947.4
5	PORTA.3	-878.5	455.05	23	VP3	632.6	-947.4
6	PORTA.2	-878.5	340.05	24	COM1	747.5	-947.4
7	PORTA.1	-878.5	225.05	25	COM2	867.5	-947.4
8	PORTA.0	-878.5	110.05	26	COM3	878.5	-809.95
9	GND	-878.5	-4.95	27	COM4/SEG29	878.5	-689.95
10	OSCXO/PORTE.1	-878.5	-119.95	28	SEG28/COM5	878.5	-574.95
11	OSCXI/PORTE.0	-878.5	-234.95	29	SEG27/COM6	878.5	-459.95
12	OSCO	-878.5	-796.3	30	SEG26	878.5	-344.95
13	OSCI	-878.5	-911.3	31	SEG25	878.5	-229.95
14	V_{DD}	-494.8	-933.4	32	SEG24	878.5	-114.95
15	REM	-291.1	-947.4	33	SEG23	878.5	0.05
16	TEST	-174.3	-947.4	34	SEG22	878.5	115.05
17	$\overline{\text{RESET}}$	-57.5	-947.4	35	SEG21	878.5	230.05
18	CUP2	57.5	-947.4	36	SEG20	878.5	345.05

Pad Location (continued)

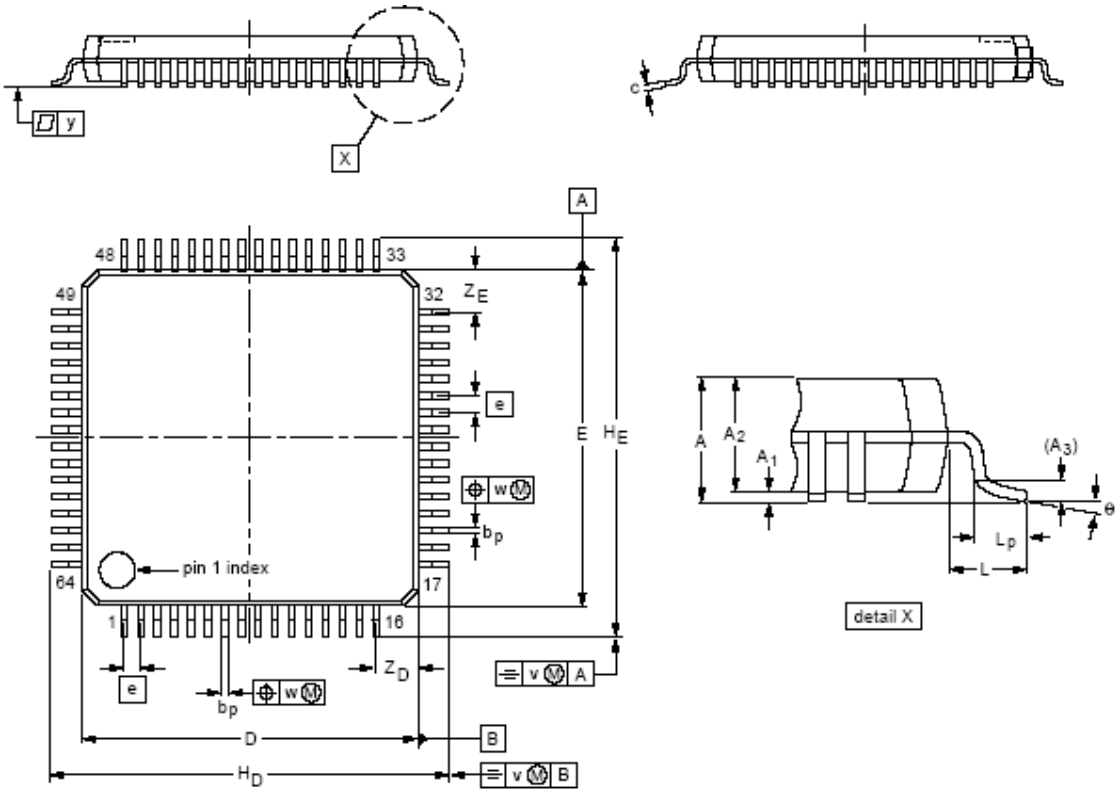
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
37	SEG19	878.5	460.05	47	SEG9	172.5	947.5
38	SEG18	878.5	575.05	48	SEG8/PORTD.3	57.5	947.5
39	SEG17	878.5	690.05	49	SEG7/PORTD.2	-57.5	947.5
40	SEG16	878.5	810.05	50	SEG6/PORTD.1	-172.5	947.5
41	SEG15	872.5	947.5	51	SEG5/PORTD.0	-287.5	947.5
42	SEG14	747.5	947.5	52	SEG4/PORTC.3	-402.5	947.5
43	SEG13	632.5	947.5	53	SEG3/PORTC.2	-517.5	947.5
44	SEG12	517.5	947.5	54	SEG2/PORTC.1	-632.5	947.5
45	SEG11	402.5	947.5	55	SEG1/PORTC.0	-747.5	947.5
46	SEG10	287.5	947.5	-	-	-	-

Ordering Information

Part No.	Package
SH66P51H	Chip Form
SH66P51P	LQFP 64-Lead
SH66P51F/044FR	QFP 44

Package Information

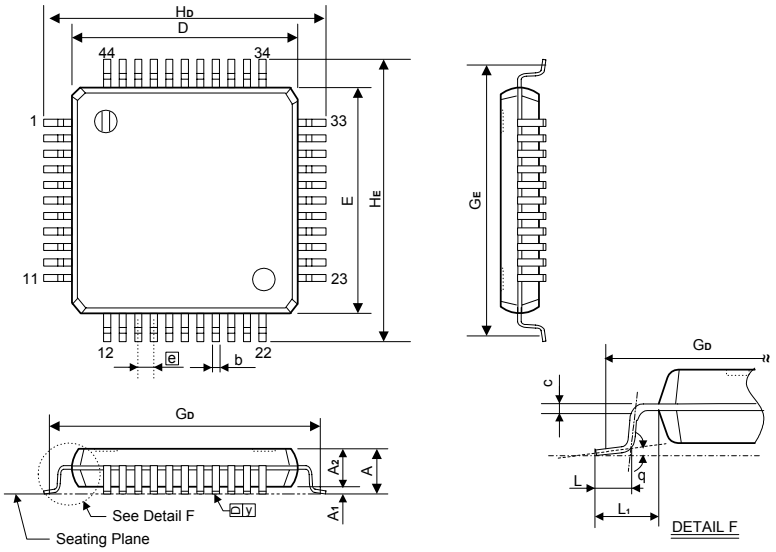
LQFP 64-Lead Package unit: inch/mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

QFP 44 Outline Dimensions unit: inch/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.70 Max.
A1	0.01 Min. 0.02Max.	0.25 Min. 0.50Max.
A2	0.079+0.008 -0.004	2.00+0.2 -0.1
b	0.012 Typ.	0.30 Typ.
c	0.006 ± 0.002	0.15 ± 0.05
D	0.394 ± 0.004	10.00 ± 0.10
E	0.394 ± 0.004	10.00 ± 0.10
e	0.031 Typ.	0.80 Typ.
GD	0.488 NOM.	12.40 NOM.
GE	0.488 NOM.	12.40 NOM.
HD	0.519 ± 0.008	13.20 ± 0.20
HE	0.519 ± 0.008	13.20 ± 0.20
L	0.035+0.002 -0.006	0.88+0.05 -0.15
L1	0.063 Typ.	1.60 Typ.
y	0.004 Max.	0.10 Max.
θ	0° ~ 7°	0° ~ 7°

Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions GD & GE are for PC Board surface mount pad pitch design reference only.

Data Sheet Revision History

Version	Content	Date
2.3	Add QFP 44 Package	Nov. 2006
2.2	Modify Warm-up Counter	Jun. 2006
2.1	Modify LCD Voltage	Nov. 2005
2.0	Delete QFP 64 Package	Jul. 2005
1.0	Original	Mar. 2005