SH66P31B

OTP 1K 4-bit Micro-controller

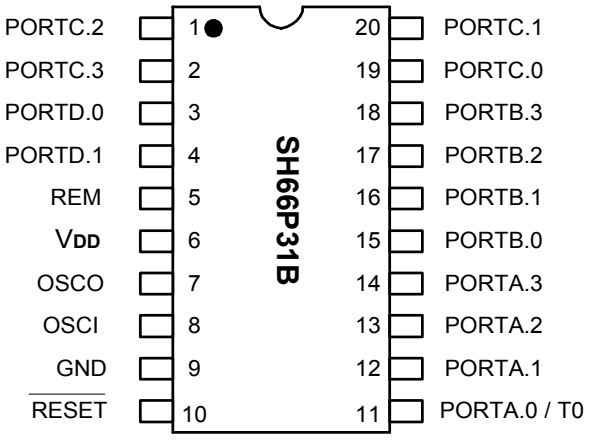
Features

- SH6610C-Based Single-Chip 4-bit Micro-Controller
- OTP ROM: 1024 X 16 bits
- RAM:
  - 32 X 4 Bits System Register
  - 48 X 4 bits Data Memory
- Operation Voltage:
  - V_{DD} = 1.8V - 3.6V
  - V_{DD} = V_{LPD} - 3.6V (LPD enable)
- 14 CMOS Bi-directional I/O pins
- 4-level Stack (Including Interrupts)
- One 8-bit Auto Re-loaded Timer/Counter
- Warm-Up Timer
- Powerful Interrupt Sources:
  - Timer0 Interrupt
  - External Interrupts: PORTA/B/C (Falling edge)
- Oscillator (code option)
  - Ceramic Resonator: 400kHz - 4MHz
  - External Input Clock: 400kHz - 4MHz
- Instruction Cycle Time:
  - 4/**fosc**
  - 16/**fosc**
- Two Low Power Operation Modes: HALT and STOP
- Reset
  - Built-in Power-on Reset (POR)
- Built-in remote control carrier synthesizer by software option
- Port interrupt source select (code option)
- 20-pin DIP/SOP/TSSOP package

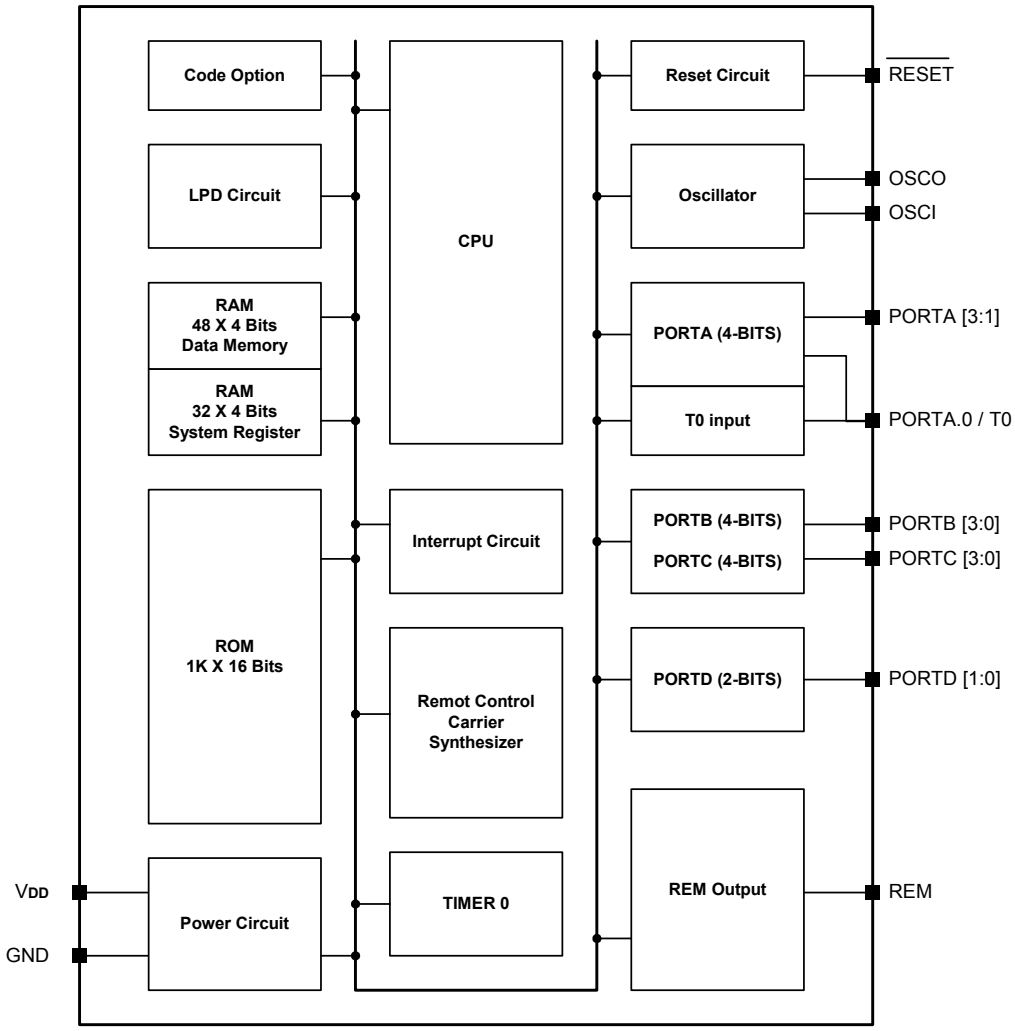
General Description

SH66P31B is a single-chip 4-bit micro-controller. This device integrates an SH6610C CPU core, RAM, 1K words of OTP ROM, timer, and programmable input/output driving buffers and carrier synthesizer. The standby function, which can be used to stop/start the ceramic resonator oscillation, facilitates the low power dissipation of the system. The SH66P31B is suitable for infrared remote control transmitter application.

Pin Configuration



Block Diagram



Pin Descriptions

Pin No.	Designation	I/O	Description
2, 1, 20, 19	PORTC.3 - 0	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge).
4, 3	PORTD.1 - 0	I/O	Bit programmable I/O pins.
5	REM	O	Carrier synthesizer for infrared or RF output pin.
6	V_{DD}	P	Power supply. In the OTP program mode, Shared with OTP V_{DD} power supply (+5.5V).
7	OSCO	O	Oscillator output pin connected to ceramic oscillator.
8	OSCI	I	Oscillator input pin connected to ceramic oscillator. In the OTP program mode, shared with clock input.
9	GND	P	Ground pin.
10	$\overline{\text{RESET}}$	I	Reset input (active low), has no internal Pull High Resistor. In the OTP program mode, Shared with OTP V_{PP} power supply (+11.0V).
11	PORTA.0/T0	I/O	Bit programmable I/O pin shared with external event counter input T0. In the OTP program mode, Shared with data I/O.
14 - 12	PORTA.3 - 1	I/O	Bit programmable I/O pins.
18 - 15	PORTB.3 - 0	I/O	Bit programmable I/O pins, Vector Interrupt (Active falling edge).

OTP Programming Pin Description (OTP Program Mode)

Pad No.	Designation	I/O	Shared by	Description
6	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V).
10	V_{PP}	P	$\overline{\text{RESET}}$	Programming high voltage Power supply (+11.0V).
9	GND	P	GND	Ground.
8	SCK	I	OSCI	Programming Clock input pin.
11	SDA	I/O	PORTA.0	Programming Data pin.

Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter cans only 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (28) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7 - bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register and I/O: $000 - $01F
Data memory: $020 - $04F

2.2. Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low nibble
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high nibble
$06	-	-	-	-	-	Reserved
$07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	-	-	PD.1	PD.0	R/W	PORTD
$0C	-	-	-	-	-	Reserved
$0D	-	-	-	REMO	R/W	REM Data Output
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PULLEN	CPS	CF1	CF0	W	Bit1-0: Carrier Frequency Control Bit2: Carrier OSC pre-divider Bit3: Port Pull-high MOS Control
$14	-	-	-	-	-	Reserved
$15	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 - 0): 0101: LPD Enable (Power-on initial) 1010: LPD Disable
$16	PACR.3	PACR.2	PACR.1	PACR.0	W	Set PORTA to be output control
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	W	Set PORTB to be output control
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	W	Set PORTC to be output control
$19	-	-	PDCR.1	PDCR.0	W	Set PORTD to be output control
$1A	-	-	-	-	-	Reserved
$1B	-	-	-	-	-	Reserved
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge Bit1: T0 signal source
$1D	-	-	-	-	-	Reserved
$1E	-	-	-	-	-	Reserved
$1F	-	-	-	-	-	Reserved

* Please refer to SH6610C user's manual for more detailed information on System Register.

3. ROM

The ROM can address 1024 X 16 bits of program area from $000 to $3FF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	NOP	Reserved
$002	JMP*	Jump to TIMER0 service routine
$003	NOP	Reserved
$004	JMP *	Jump to Port interrupt service routine

* JMP instruction can be replaced by any instruction.

4. Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on reset
$00	-	IET0	-	IEP	-x-x
$01	-	IRQT0	-	IRQP	-x-x
$02	-	TM0.2	TM0.1	TM0.0	-xxx
$03	-	-	-	-	
$04	TL0.3	TL0.2	TL0.1	TL0.0	0000
$05	TH0.3	TH0.2	TH0.1	TH0.0	0000
$06	-	-	-	-	
$07	-	-	-	-	
$08	PA.3	PA.2	PA.1	PA.0	xxxx
$09	PB.3	PB.2	PB.1	PB.0	xxxx
$0A	PC.3	PC.2	PC.1	PC.0	xxxx
$0B	-	-	PD.1	PD.0	xxxx
$0C	-	-	-	-	
$0D	-	-	-	REMO	---0
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx
$0F	INX.3	INX.2	INX.1	INX.0	xxxx
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx
$11	-	DPM.2	DPM.1	DPM.0	xxxx
$12	-	DPH.2	DPH.1	DPH.0	xxxx
$13	PULLEN	CPS	CF1	CF0	0000
$14	-	-	-	-	
$15	LPD3	LPD2	LPD1	LPD0	0101
$16	PACR.3	PACR.2	PACR.1	PACR.0	0000
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000
$19	-	-	PDCR.1	PDCR.0	0000
$1A	-	-	-	-	
$1B	-	-	-	-	
$1C	-	-	T0S	T0E	--00
$1D	-	-	-	-	
$1E	-	-	-	-	
$1F	-	-	-	-	

Legend: x = unknown, u = unchanged, - = unimplemented read as “0”.

4.2. Others Initial State:

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

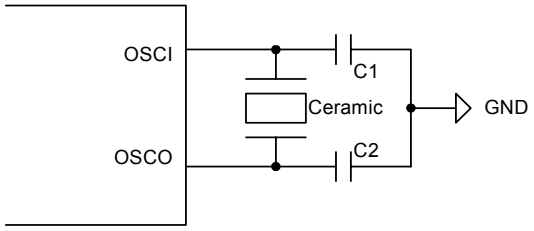
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = fosc/4 or fosc/16 (Code option)
fosc/4 function is used for oscillator frequency lower than 500kHz.

5.1. Instruction Cycle Time:

(1) 4/455kHz (≈ 8.79μs) for 455kHz oscillator.
(2) 16/455kHz (≈ 35.16μs) for 455kHz oscillator.
(3) 16/4MHz (= 4μs) for 4MHz oscillator.

5.2. Oscillator Type

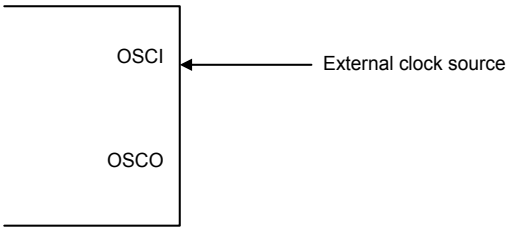
(1) Ceramic Resonator: 400kHz - 4MHz



Note:

Recommended oscillator manufacturer and part number
ZT3.58M3
- fosc = 3.58MHz, Built-in 30pF capacitance, Operating Temperature range from -20℃ to +80℃
- From China Shanghai JINGBO Electronics CO., LTD
More manufacturer and type of ceramic resonator will be added in.

(2) External input clock: 400kHz - 4MHz



Capacitor Selection for Oscillator

Ceramic Resonators			Recommend Type	Manufacturer
Frequency	C1	C2		
455kHz	47 - 100pF	47 - 100pF	ZT 455E	JingBo Electronic Shanghai
3.58MHz	-	-	ZT 3.58M*	JingBo Electronic Shanghai
4MHz	-	-	ZT 4M*	JingBo Electronic Shanghai

*- The specified ceramic resonator has internal built-in load capacity

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (φ 3 X 8)	KDS
4MHz	8 - 15pF	8 - 15pF	49S-4.000M-F16E	JingBo Electronic Shanghai
8MHz	8 - 15pF	8 - 15pF	49S-8.000M-F16E	JingBo Electronic Shanghai

Notes:

1. Capacitor values are used for design guidance only!
2. These capacitors were tested with the crystals listed above for basic start-up and operation. They are not optimized.
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufacturers.

6. I/O Ports

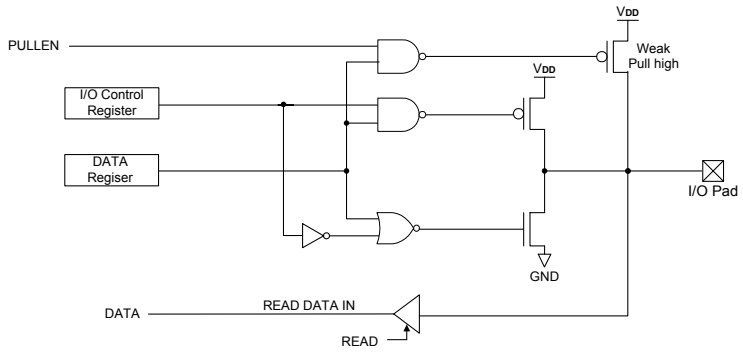
The MCU provides 14 bi-directional I/O ports. The PORT data put in register $08 - $0B. The PORT control register ($16 - $19) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PULLEN of $13 and the data of the port, when the PORT is used as input.

System Register ($08 - $0B, $16 - $19)

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	-	-	PD.1	PD.0	R/W	PORTD
$16	PACR.3	PACR.2	PACR.1	PACR.0	W	PORTA input/output control
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	W	PORTB input/output control
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	W	PORTC input/output control
$19	-	-	PDCR.1	PDCR.0	W	PORTD input/output control

PA (/B/C/D) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin



System Register $13

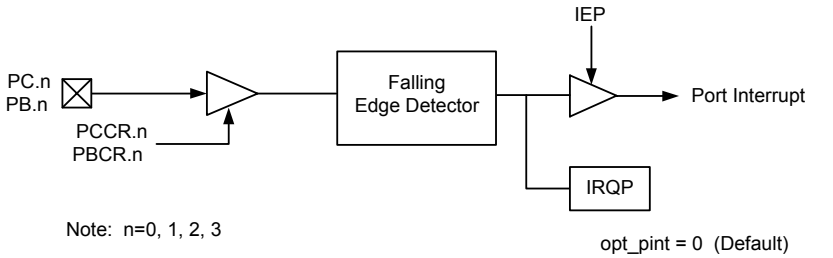
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PULLEN	CPS	CF1	CF0	W	Bit3: Port Pull-high resistor Control

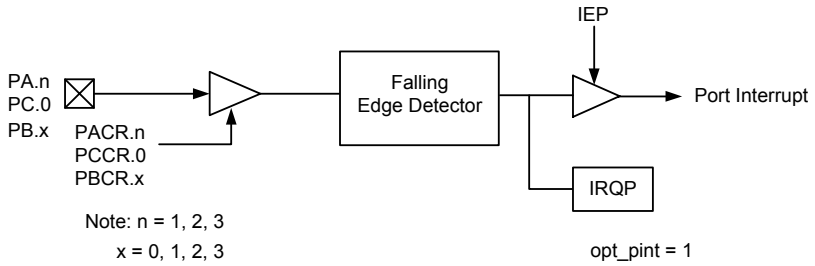
PULLEN Port Pull-high resistor enables control
0 = Disable PORT pull-high resistor (power-on initial)
1 = Enable PORT pull-high resistor

Port Interrupt

When opt_pint is “0” (Default), PORTB.0 - 3, PORTC.0 - 3 are used as port interrupt sources. When opt_pint is “1”, PORTA.1 - 3,PORTB.0 - 3 and PORTC.0 are used as port interrupt sources. Since PORT I/O is a bit programmable I/O, only the transitions from V_{DD} to GND will generate an interrupt request. Thus, further falling edge transitions can not be able to make interrupt request until all of the pins return to V_{DD}.

PORT Interrupt Block Diagram





Port Interrupt PROGRAMMING NOTES：

■ If user wants to generate an interrupt when a falling edge from V_{DD} to GND emerges on the port, the following must be executed.

1. Set the port as input port, fill port data register with “1”.
2. Pull-high the port (Use external pull-high resistance or set PULLEN to “1”).
   And further falling edge transition would not be able to make interrupt request until all of the pins return to V_{DD}.
3. Set corresponding IEP to “1” and clear IRQP to “0”.

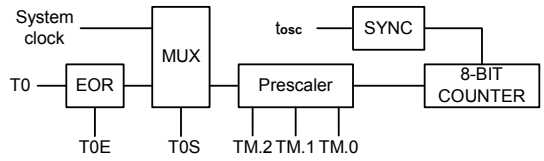
7. Timer

The device has one 8-bit auto re-load timer/counter.

The timer/counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

7.1. Timer0 Configuration and Operation

The Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

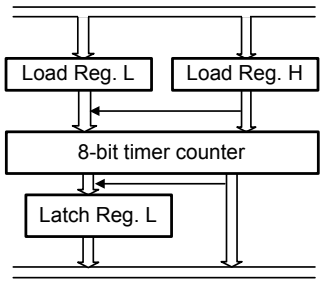
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.2. Timer Mode Register

The timer can be programmed in several different prescalers by setting Timer Mode register (TM0).

The 8-bit counter prescaler overflow output pulses. The Timer Mode registers (TM0) are 3-bit registers used for the timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$ (initial)	System clock/T0
0	0	1	$/2^{9}$	System clock/T0
0	1	0	$/2^{7}$	System clock/T0
0	1	1	$/2^{5}$	System clock/T0
1	0	0	$/2^{3}$	System clock/T0
1	0	1	$/2^{2}$	System clock/T0
1	1	0	$/2^{1}$	System clock/T0
1	1	1	$/2^{0}$	System clock/T0

7.3. External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer0 source, it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t**osc**) and low (at least 2 t**osc**). When the prescaler ratio selects/2^0, it is the same as the system clock input.

The requirement is as follows

T0H (T0 high time) $\geq$ 2 * **tosc** + ΔT

T0L (T0 low time) $\geq$ 2 * **tosc** + ΔT; ΔT = 20ns

When another prescaler ratio is selected, the TM0 is scaled by the asynchronous ripple counter, so that the prescaler output is symmetrical. Then:

$$\text{T0 high time} = \text{T0 low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period
N = prescaler value

The requirement is:

$$\frac{N * T0}{2} \geq 2 * tosc + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$\text{T0} = \text{Timer0 period} \geq \frac{4 * tosc + 2 * \Delta T}{N}$$

Systems Register $1C:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1C	-	-	T0S	T0E	W	Bit0: T0 signal edge Bit1: T0 signal source
	-	-	X	0	W	Increment on low-to-high transition T0 pin (Power-on initial)
	-	-	X	1	W	Increment on high-to-low transition T0 pin
	-	-	0	X	W	System clock (Power-on initial)
	-	-	1	X	W	Transition on T0 pin

T0E: T0 signal edge
0: Increment on low-to-high transition T0 pin (Power on initial)
1: Increment on high-to-low transition T0 pin

T0S: T0 signal source
0: System clock (Power on initial)
1: Transition on T0 pin

8. Interrupt

Two interrupt sources are available on SH66P31B:
- Timer0 interrupt
- PORTA, B, C interrupts (Falling edge)

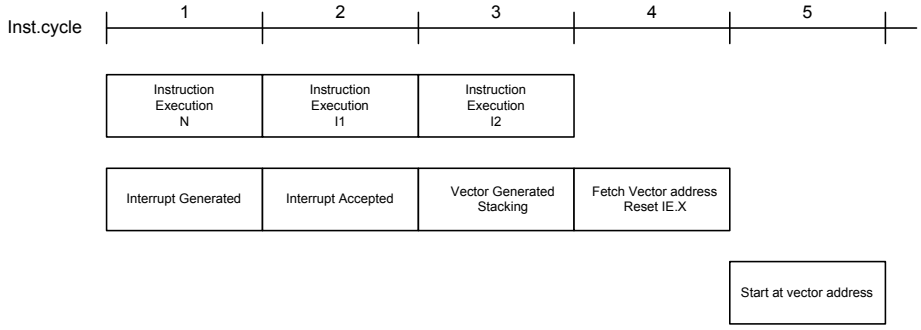
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are clear to “0” at initialization by the chip reset.

System Register:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	-	IET0	-	IEP	W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	W	Interrupt request flags

When IEx is set to “1” and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are clear to “0” automatically, so when IRQx is 1 and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the CPU interrupt service, user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions.

However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

Timer Interrupt

The input clocks of Timer0 are based on system clock or external clock/event T0 input as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 = 1), If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port Falling Edge Interrupt

Only the digital input port can generate a port interrupt. The analog input cannot generate an interrupt request.

Any one of the I/O input pin transitions from V_{DD} to GND would generate an interrupt request (IRQP = 1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to V_{DD}. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

9. Remote Control Synthesizer

The device has a built-in carrier synthesizer for infrared or RF remote control circuits.

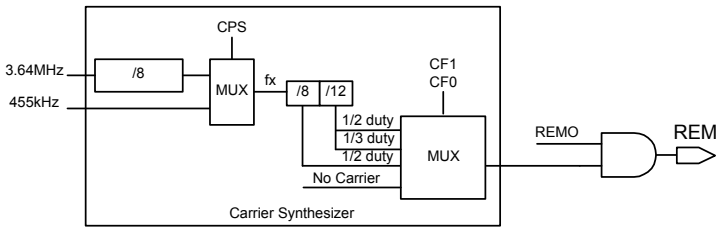
System Register ($0D):

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0D	-	-	-	REMO	R/W	Bit0: REM output data.
	-	-	-	0	R/W	REM output data disable
	-	-	-	1	R/W	REM output data enable

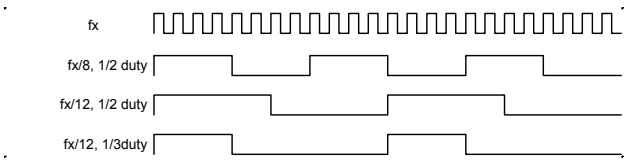
System Register ($13):

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$13	PULLEN	CPS	CF1	CF0	W	Bit1-0: Carrier Frequency Control Bit2: Carrier OSC prescaler Bit3: Port Pull-high resistor Control
	X	0	X	X	W	fx = fosc (default)
	X	1	X	X	W	fx = fosc/8
	X	X	0	0	W	No carrier (default)
	X	X	0	1	W	fx/8, 1/2 duty
	X	X	1	0	W	fx/12, 1/3 duty
	X	X	1	1	W	fx/12, 1/2 duty

The functional block diagram is show as below:



Remote Control Functional Block Diagram



Remote Carrier Duty

10. Low Power Detection (LPD)

The LPD function monitors the supply voltage and applies an internal reset in the micro-controller at battery replacement. If the applied circuit satisfies the following conditions, the LPD can be incorporated by the software control.

The software enable flag controls LPD circuit on/off.

LPD circuit Operating ambient temperature is T_A = -20℃ to + 70℃

Functions of LPD Circuit:

The LPD circuit has the following functions:

Generates an internal reset signal when $V_{DD} \leq V_{LPD}$.

Cancels the internal reset signal when $V_{DD} > V_{LPD}$.

Stops the oscillator operation and force the CPU to enter STOP mode when $V_{DD} \leq V_{LPD}$.

As $V_{DD} \leq V_{LPD}$, the LPD reset will delay about 1.2ms before being triggered. If V_{DD} goes back to $V_{DD} > V_{LPD}$, without any delay then cancel the LPD reset.

LPD Control Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	LPD3	LPD2	LPD1	LPD0	W	LPD Enable Control (LPD3 - 0): When LPD function enable code option = 0 0101: LPD Enable (Power-on initial) 1010: LPD Disable When LPD function enable code option = 1 xxxx: LPD Enable

11. HALT and STOP Mode

After the execution of HALT instruction, SH66P31B will enter HALT mode. In HALT mode, the CPU will stop operating; but the peripheral circuit (timer) will keep operating.

After the execution of STOP instruction, SH66P31B will enter STOP mode.

In STOP mode, the entire chip (including oscillator) will stop operating.

In HALT mode, SH66P31B can be waked up if any interrupt occurs.

In STOP mode, SH66P31B can be waked up if port interrupt occurs.

12. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions

Power-on Reset

Wake up from Stop Mode

Warm-up time interval:

(1) In Crystal oscillator or Ceramic resonator mode, f_{OSC} = 455kHz, the warm-up time interval is 9 ms.

(2) In Crystal oscillator or Ceramic resonator mode, f_{OSC} = 4MHz, the warm-up time interval is 1.02 ms

13. Code Option

Port Interrupt Source Select:

0: Int. source: PB, PC (Default)

1: Int. source: PA.1 - 3, PB.0 - 3, PC.0

Instruction Cycle Time:

0: Instruction cycle time = 4/f_{OSC} (Default) - (only use for less than 500kHz oscillator)

1: Instruction cycle time = 16/f_{OSC}

LPD Function Enable Select:

0: Use LPD register ($15) control (Default = 0)

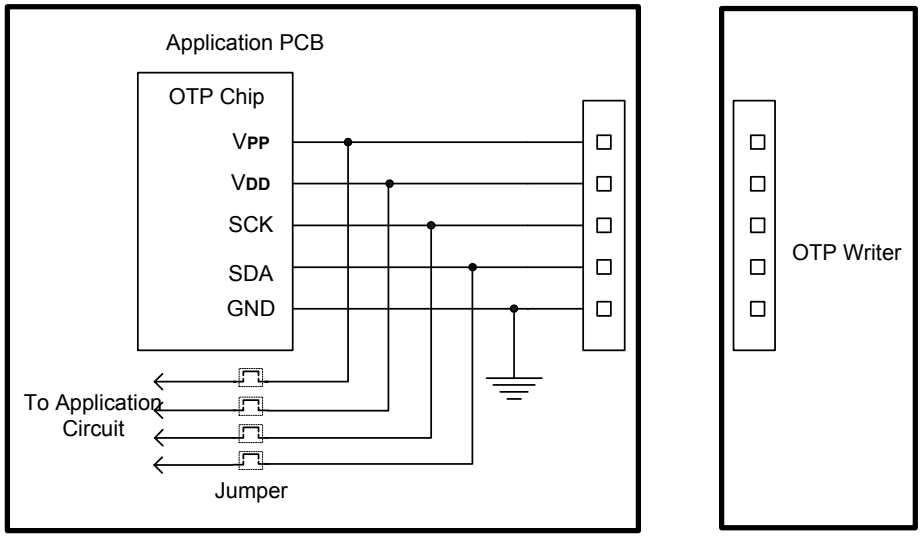
1: LPD always enable, LPD register ($15) inactive.

In System Programming Notice for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended steps are the followings:

(1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.
(2) Connect the programming interface with OTP writer and begin programming.
(3) Disconnect OTP writer and short these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.

1. Arithmetic and Logical Instructions

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC <- Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx <- Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC <- Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx <- Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC <- Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx <- Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC <- Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx <- Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC <- Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx <- Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC <- Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx <- Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC <- Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx <- Mx & AC	
SHR	11110 0000 000 0000	0 -> AC [3], AC [0] -> CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC <- Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx <- Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC <- Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx <- Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx <- Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx <- Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx <- Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx <- Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx <- Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC <- Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx <- AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx <- I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC <- X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC <- X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC <- X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC <- X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC <- X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC <- X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC <- X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC <- X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST <- CY, PC + 1 PC <- X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC <- ST; TBR <- hhhh, AC <- ll	
RTNI	11010 1000 000 0000	CY, PC <- ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC <- X (Include p)	
TJMP	11110 1111 111 1111	PC <- (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
P	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Rating*

DC Supply Voltage . . . . . .-0.3V to +7.0V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . -20℃ to +70℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses exceed those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.8 - 3.0V, GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.8	3.0	3.6	V	LPD function disable
	V_{LPD}	3.0	3.6	V		LPD function enable
Operating Current	I_{OP}	-	0.3	1	mA	All output pins unload (Execute NOP instruction), V_{DD} = 3.0V
Stand by Current 1 (HALT)	I_{SB1}	-	40	-	μA	f_{OSC} = 455kHz; CPU stop ALL output pins unload, LPD off ,V_{DD} = 3.0V
		-	200	-	μA	f_{OSC} = 4M; CPU stop ALL output pins unload, LPD off, V_{DD} = 3.0V
Stand by Current 2 (STOP)	I_{SB2}	-	-	1	μA	OSC STOP ALL output pins unload, LPD off, V_{DD} = 3.0V
REM sink current	I_{REM1}	0.25	-	-	mA	V_{REM1} = 0.3V, V_{DD} = 3.0V
REM driving current	I_{REM2}	-5	-9	-	mA	V_{REM2} = 1V, V_{DD} = 3.0V
Input Low Voltage 1	V_{IL1}	GND	-	V_{DD} X 0.2	V	I/O ports, pins tri-state
Input Low Voltage 2	V_{IL2}	GND	-	V_{DD} X 0.15	V	$\overline{\text{RESET}}$
Input Low Voltage 3	V_{IL3}	GND	-	V_{DD} X 0.3	V	OSCI (Driven with external clock, for reference)
Input High Voltage 1	V_{IH1}	V_{DD} X 0.7	-	V_{DD}	V	I/O Ports, pins tri-state
Input High Voltage 2	V_{IH2}	V_{DD} X 0.8	-	V_{DD}	V	$\overline{\text{RESET}}$
Input High Voltage 3	V_{IH3}	V_{DD} X 0.7	-	V_{DD}	V	OSCI (Driven with external clock, for reference)
High-level Input Current 1	I_{IH1}	-	-	0.2	μA	I/O ports; $V_{I/O}$ = 3.0V, V_{DD} = 3.0V
High-level Input Current 2	I_{IH2}	-	1	5	μA	$V_{\overline{\text{RESET}}}$ = V_{DD}, V_{DD} = 3.0V
Low-level Input Current 1	I_{IL1}	-35	-	-10	μA	I/O ports with pull-high; $V_{I/O}$ = GND, V_{DD} = 3.0V
Low-level Input Current 2	I_{IL2}	-	-	-1	μA	I/O ports with no pull-high; $V_{I/O}$ = GND, V_{DD} = 3.0V
Low-level Input Current 3	I_{IL3}	-3	1	3	μA	For OSCI, V_{DD} = 3.0V
Low-level Input Current 4	I_{IL4}	-5	-	-	μA	$V_{\overline{\text{RESET}}}$ = GND, V_{DD} = 3.0V
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = -1.0mA, V_{DD} = 3.0V
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O ports, I_{OL} = 5mA, V_{DD} = 3.0V
Oscillator Start time	t_{OSC1}	-	-	20	ms	Ceramic Oscillator = 455kHz, V_{DD} = 3.0V

LPD Circuitry Electrical Characteristics

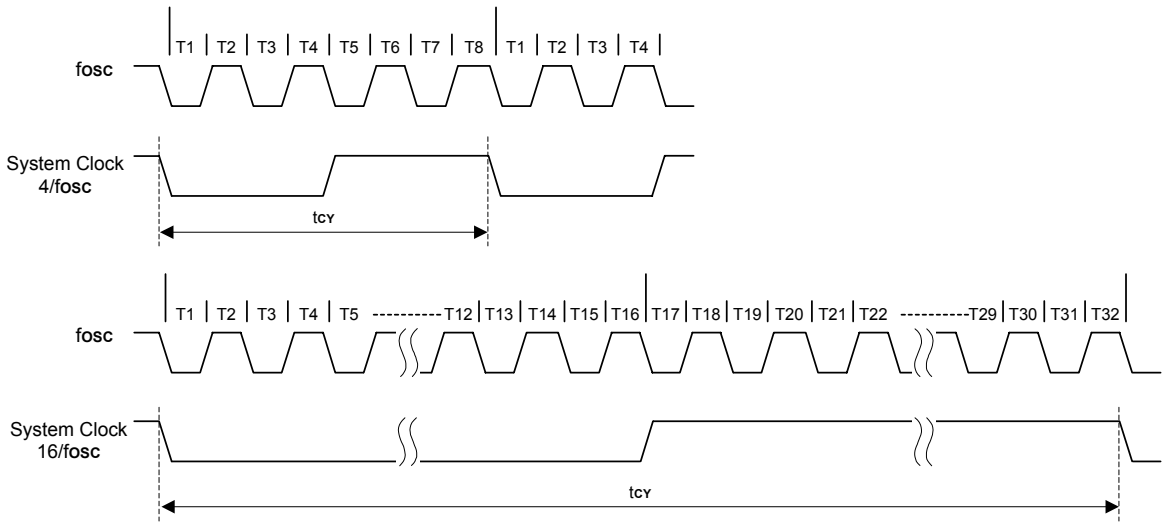
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LPD-detected Voltage	V_{LPD}	1.6	-	2.1	V	T_A = -20℃ to +70℃
	V_{LPD25}	1.7	-	2.0	V	T_A = 25℃
LPD circuit current	I_{LPD}	-	2.0	3.5	μA	T_A = -20℃ to +70℃

AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, unless otherwise specified)

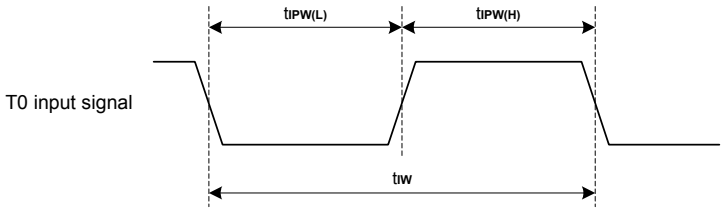
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Instruction Cycle Time	t_{CY}	1	-	10	μs	
T0 Input Width	t_{IW}	(t_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
High Pulse Width	t_{IWH}	1/2t_{IW}	-	-	ns	
Low Pulse Width	t_{IWL}	1/2t_{IW}	-	-	ns	

Timing Waveform

(a) System Clock Timing Waveform:



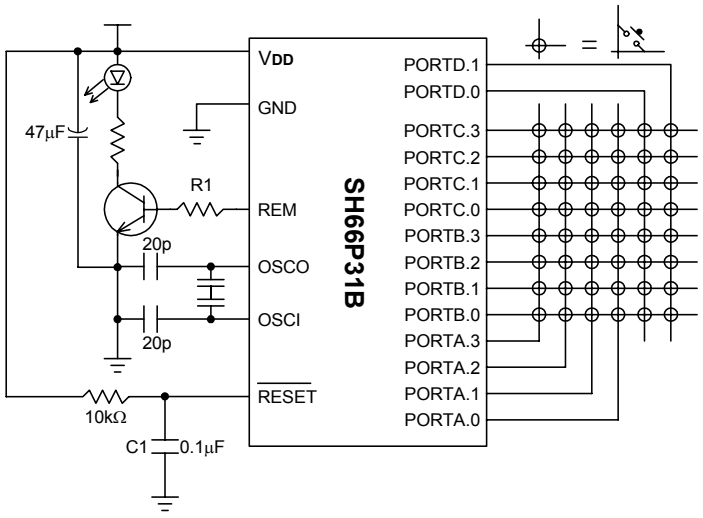
(b) T0 Input Waveform:



Application Circuits (For Reference Only)

AP1: Remote Control (48 Keys)

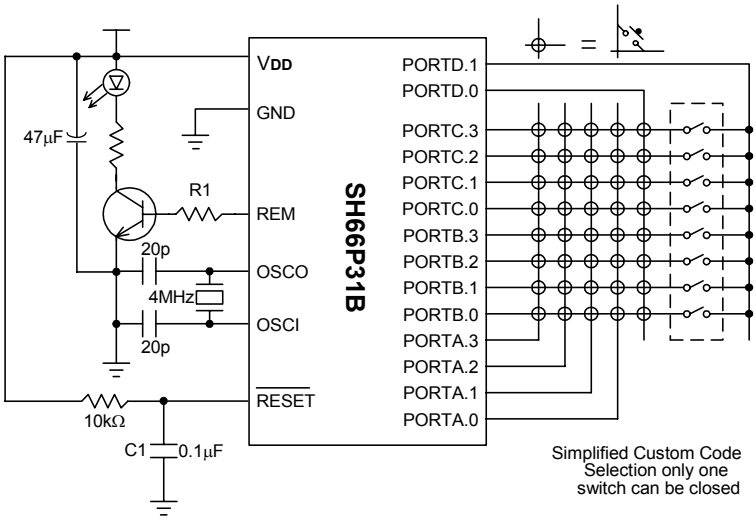
(1) Operating Voltage: V_{DD} = 3.0V
(2) Oscillator: Ceramic 400kHz - 4MHz
(3) PORTA, D: I/O Buffers
(4) PORTB and C: Input Buffers
(5) R1 = 0 is possible, but the REM specification is revised to reduce power consumption



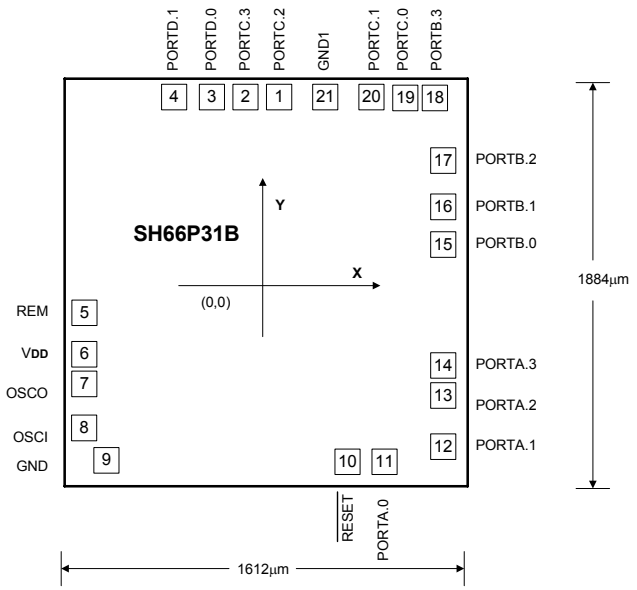
AP2: Remote Control (40 Keys)

Operating Voltage: V_{DD} = 3.0V.

The simplified code option would not sink any power consumption since PORTD.1 short with other I/O ports. Because PORTD.1 can be programmed as input only with pull-high, so that PORTB or PORTC can be scanned out to detect PORTD.1 option. After detection, PORTD.1 pull-high resistor can be turned off by software, if there is an option selected. If there is no option selected, then the pull-high resistor cannot be turned off, so that PORTD.1 would not be floating.



Bonding Diagram



*** Substrate connects to GND.**

Pad Location Unit: μm

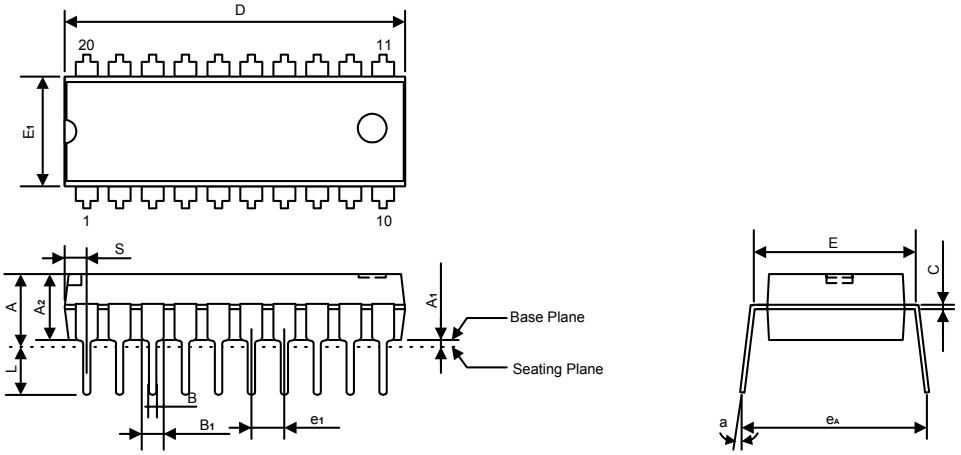
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	PORTC.2	237.9	736	12	PORTA.1	871.95	-707
2	PORTC.3	17.9	736	13	PORTA.2	871.95	-487
3	PORTD.0	-107.1	736	14	PORTA.3	871.95	-377
4	PORTD.1	-327.1	736	15	PORTB.0	871.95	145.8
5	REM	-851.95	-56.8	16	PORTB.1	871.95	255.8
6	VDD	-851.95	-242.85	17	PORTB.2	871.95	475.8
7	OSCO	-851.95	-381.15	18	PORTB.3	787.9	736
8	OSCI	-851.95	-601.15	19	PORTC.0	677.9	736
9	GND	-798.85	-719	20	PORTC.1	457.9	736
10	$\overline{\text{RESET}}$	430.75	-719.3	21	GND.1	347.9	736
11	PORTA.0	621.65	-724				

Ordering Information

Part No.	Package
SH66P31B	20L DIP
SH66P31BM	20L SOP
SH66P31BX	20L TSSOP

Package Information

P-DIP 20L Outline Dimensions unit: inches/mm

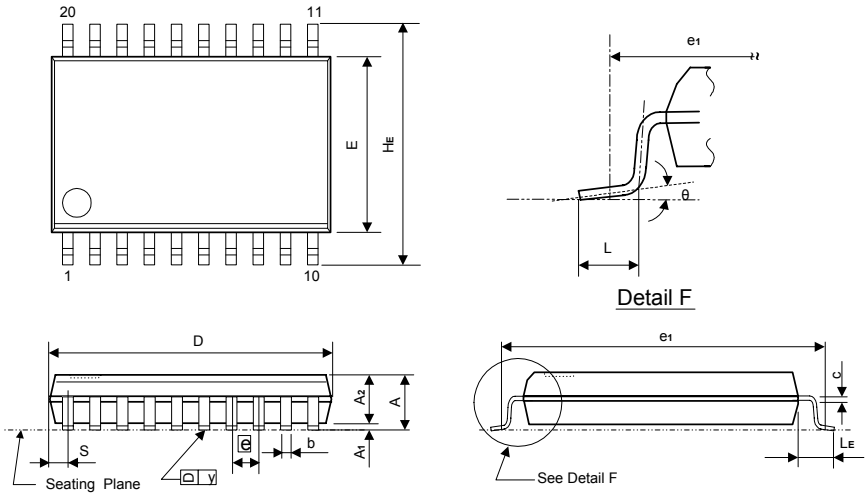


Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.057± 0.008	1.45± 0.2
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.026 Typ. (1.046 Max.)	26.06 Typ. (26.57 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.078 Max.	1.98 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash

SOP 20L (W.B.) Outline Dimensions unit: inches/mm

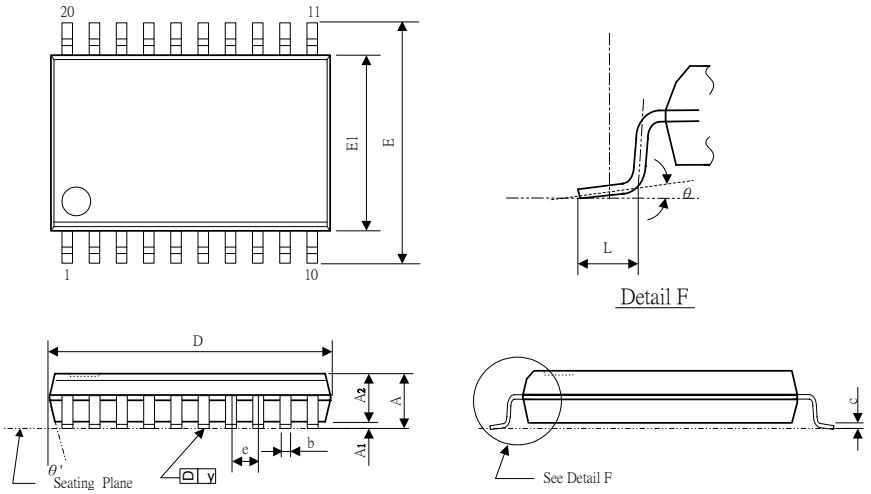


Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.69 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016+0.004 -0.002	0.41+0.10 -0.05
C	0.010+0.004 -0.002	0.25+0.10 -0.05
D	0.500 ± 0.02	12.80 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.032 ± 0.008	0.81 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.042 Max.	1.07 Max.
y	0.004 Max.	0.10 Max.
θ	0° - 10°	0° - 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

TSSOP 20L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.048	---	---	1.20
A_1	0.002	---	0.006	0.05	---	0.15
A_2	0.031	0.039	0.041	0.80	1.00	1.05
b	0.007	---	0.012	0.19	---	0.30
C	0.004	---	0.008	0.09	---	0.20
D	0.252	0.256	0.260	6.40	6.50	6.60
E	---	0.252	---	---	6.40	---
E1	0.169	0.173	0.177	4.30	4.40	4.50
e		0.026	---	---	0.65	---
L	0.018	0.024	0.030	0.45	0.60	0.75
y	---	---	0.004	---	---	0.10
θ	0°	---	8°	0°	---	8°
θ'	---	12°	---	---	12°	---

Notes:
1. Package body sizes exclude mold flash protrusions or gate burrs.
2. Tolerance±0.1mm unless otherwise specified.
3. Coplanarity:0.1mm.
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

Data Sheet Revision History

Version	Content	Date
2.1	Add Pad GND1 in Bonding diagram	Jan. 2008
2.0	Package information update	Apr. 2007
1.0	Original	Sep. 2005