SH66K33A

MASK 1K 4-bit Micro-controller

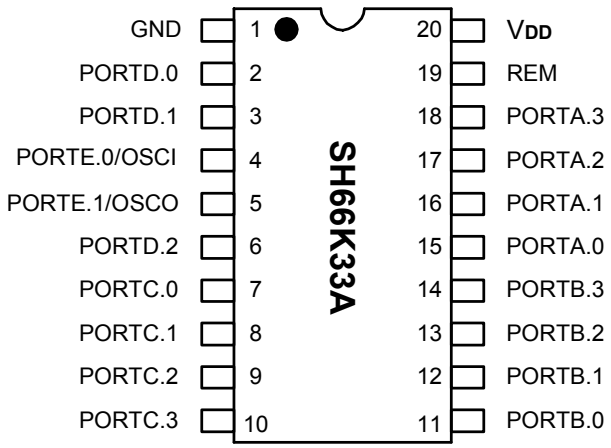
Features

- SH6610C-Based Single-Chip 4-bit Micro-Controller
- ROM: 1K X 16 bits
- RAM: 80 X 4 bits
  - 32 System Control Register
  - 48 Data memory
- Operation Voltage: 1.8V - 3.6V (Typically 3.0V)
- 16 CMOS Bi-directional I/O pins and 1 COMS input pin
- 4-Level Stack (Including interrupts)
- One 8-bit Auto Re-Loaded Timer/Counter
- Warm-up Timer
- Powerful Interrupt Sources:
  - Timer0 Interrupt
  - External Interrupts: PORTB & PORTC & PORTD (Rising edge)
- Oscillator (Code Option)
  - Crystal Oscillator: 400kHz - 4MHz
  - Ceramic Resonator: 400kHz - 4MHz
  - Internal RC Oscillator: 4MHz ± 4% (different from SH67P33A)
- Instruction Cycle Time (4/fosc or 16/fosc)
- Two Low Power Operation Modes: HALT And STOP
- Reset
  - Built-in Watchdog Timer
  - Built-in Power-on Reset (POR)
- Available In CHIP FORM
- 20-pin DIP/TSSOP/SOP package
- Mask type
- Low Voltage Reset function
- Remote Control Programmable Carrier Synthesizer

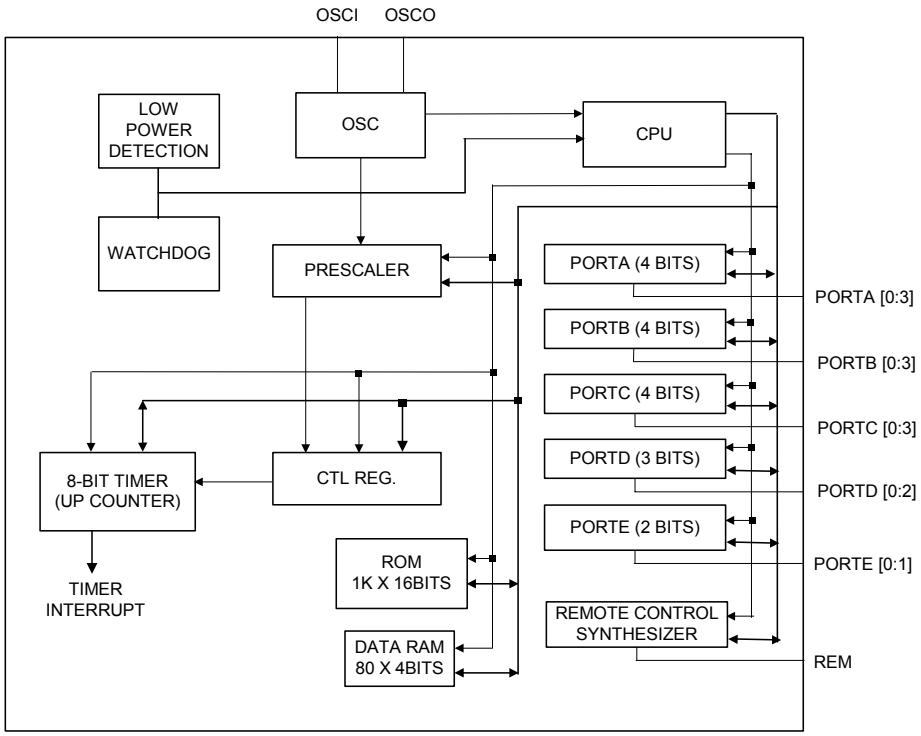
General Description

SH66K33A is a single-chip 4-bit micro-controller. This device integrates a SH6610C CPU core, RAM, ROM, timer, programmable input/output pins and carrier synthesizer. When in standby status, system will stop oscillator and remain low power consumption. The SH66K33A is suitable for infrared remote control transmitter application.

Pin Configuration (20-Lead DIP/SOP/TSSOP Package)



Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
10 - 7	PORTC.3 - 0	I/O	Bit programmable I/O pins, Vector Interrupt (Active rising edge).
2	PORTD.0	I	Input pin.
6,3	PORTD.2 - 1	I/O	Bit programmable I/O pins.
19	REM	O	Carrier synthesizer for infrared or RF output pin.
20	V_{DD}	P	Power supply.
4	PORTE.0/OSCI	I/O	Bit programmable I/O pin, shared with oscillator input pin connected to ceramic/crystal oscillator.
5	PORTE.1/OSCO	I/O	Bit programmable I/O pin, shared with oscillator output pin connected to ceramic/crystal oscillator.
1	GND	P	Ground pin.
18 - 15	PORTA.3 - 0	I/O	Bit programmable I/O pins.
14 - 11	PORTB.3 - 0	I/O	Bit programmable I/O pins, Vector Interrupt (Active rising edge).

Function Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bit:

Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter cans only 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)
Decimal adjustments for addition/subtraction (DAA, DAS)
Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)
Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)
Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or CALL instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The TBR and AC are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 which comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 4 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 4 levels. If the number of calls and interrupt requests exceeds 4, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register and I/O: $000 - $01F
Data memory: $020 - $04F

2.2. Configuration of System Register

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags
$02	-	TM0.2	TM0.1	TM0.0	R/W	Timer0 Mode register (Prescaler)
$03	-	-	-	-	-	Reserved
$04	TL0.3	TL0.2	TL0.1	TL0.0	R/W	Timer0 load/counter register low nibble
$05	TH0.3	TH0.2	TH0.1	TH0.0	R/W	Timer0 load/counter register high nibble

Configuration of System Register (continue):

Address	Bit3	Bit2	Bit1	Bit0	R/W	Description
$06 - $07	-	-	-	-	-	Reserved
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	-	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	PE.1	PE.0	R/W	PORTE
$0D	-	-	-	REMO REM	W R	Bit0: REMO output data. Bit0: REM pin output status.
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	PPULL	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier count source prescaler control Bit3: Port Pull-low enable Control
$14	$\overline{WDT}$	-	-	-	R/W	Bit3: Watchdog timer reset/flag (write 1 to reset WDT timer)
$15	LVR3	LVR2	LVR1	LVR0	R/W	LVR Enable Control (LVR3 - 0): 1010: LVR Disable Else: LVR Enable (Power-on initial 0000)
$16	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$19	-	PDCR.2	PDCR.1	-	R/W	PORTD input/output control
$1A	-	-	PECR.1	PECR.0	R/W	PORTE input/output control
$1B	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register (low nibble)
$1C	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register (high nibble)
$1D	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register (low nibble)
$1E	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register (high nibble)
$1F	-	-	-	-	-	Reserved

3. ROM

The ROM can address 1024 X 16 bits of program area from $000 to $3FF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
$000	JMP*	Jump to RESET service routine
$001	NOP	Reserved
$002	JMP*	Jump to TIMER0 interrupt service routine
$003	NOP	Reserved
$004	JMP*	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

4. Initial State

4.1. System Register State:

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset	LVR Reset	WDT Reset
$00	-	IET0	-	IEP	-0-0	-0-0	-0-0
$01	-	IRQT0	-	IRQP	-0-0	-0-0	-0-0
$02	-	TM0.2	TM0.1	TM0.0	0000	0000	uuuu
$03	-	-	-	-	-	-	-
$04	TL0.3	TL0.2	TL0.1	TL0.0	xxxx	uuuu	uuuu
$05	TH0.3	TH0.2	TH0.1	TH0.0	xxxx	uuuu	uuuu
$06 - $07	-	-	-	-	-	-	-
$08	PA.3	PA.2	PA.1	PA.0	0000	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000	0000
$0B	-	PD.2	PD.1	PD.0	-000	-000	-000
$0C	-	-	PE.1	PE.0	--00	--00	--00
$0D	-	-	-	REMO REM	---0	---0	---0
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-xxx	-uuu
$13	PPULL	CPS2	CPS1	CPS0	0000	0000	0uuu
$14	$\overline{\text{WDT}}$	-	-	-	1---	1---	0---
$15	LVR3	LVR2	LVR1	LVR0	0000	0000	uuuu
$16	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000	0000
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000	0000
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000	0000
$19	-	PDCR.2	PDCR.1	-	-00-	-00-	-00-
$1A	-	-	PECR.1	PECR.0	--00	--00	--00
$1B	CFL3	CFL2	CFL1	CFL0	0000	0000	uuuu
$1C	CFL7	CFL6	CFL5	CFL4	0000	0000	uuuu
$1D	CFH3	CFH2	CFH1	CFH0	0000	0000	uuuu
$1E	CFH7	CFH6	CFH5	CFH4	0000	0000	uuuu
$1F	-	-	-	-	-	-	-

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'.

4.2. Others Initial States:

Others	Power-on Reset	LVR Reset	WDT Reset
Program Counter (PC)	$000	$000	$000
CY	Undefined	Unchanged	Unchanged
Accumulator (AC)	Undefined	Unchanged	Unchanged
Data Memory	Undefined	Unchanged	Unchanged

5. System Clock and Oscillator

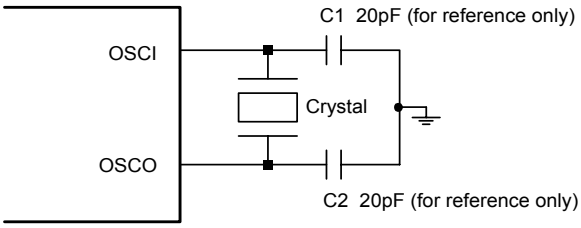
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = fosc/4 or fosc/16 (Code Option)

5.1. Instruction Cycle Time:

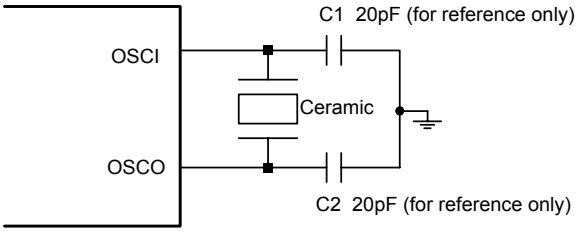
(1) 4/455kHz (≈ 8.79μs) for 455kHz oscillator.
(2) 16/455kHz (≈ 35.16μs) for 455kHz oscillator.
(3) 4/4MHz (= 1μs) for 4MHz oscillator.
(4) 16/4MHz (= 4μs) for 4MHz oscillator.

5.2. Oscillator Type

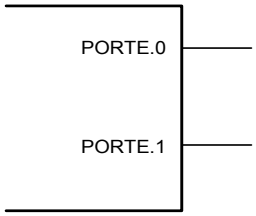
(1) Crystal Oscillator: 400kHz - 4MHz



(2) Ceramic Resonator: 400kHz - 4MHz



(3) RC Oscillator: 4MHz



Internal Rosc RC

When use Internal RC oscillator, OSCI is used as PORTE.0 and OSCO is used as PORTE.1.

6. I/O Ports

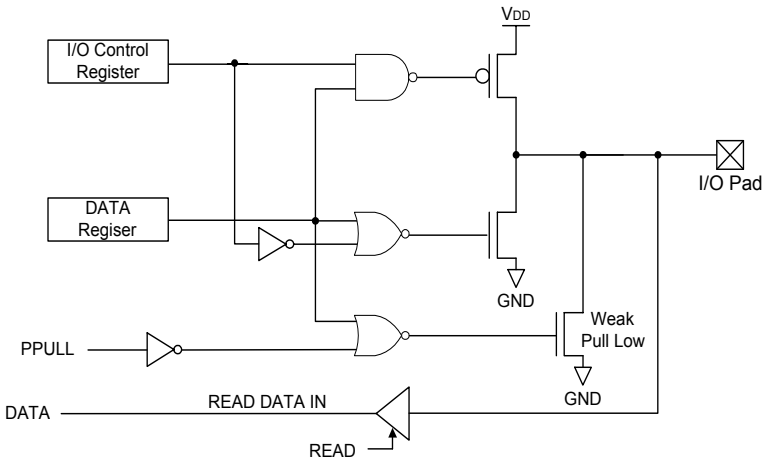
The MCU provides 16 Bi-directional I/O pins and 1 input pin. The PORT data put in register $08 - $0C. The PORT control register ($16 - $1A) controls the PORT as input or output. Each I/O pin has an internal pull-low resistor, which is controlled by PPULL of $13 and the data of port, when the PORT is used as input.

Port I/O mapping address is shown as follows:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data
$0B	-	PD.2	PD.1	PD.0	R/W	PORTD data
$0C	-	-	PE.1	PE.0	R/W	PORTE data
$16	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control
$17	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control
$18	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control
$19	-	PDCR.2	PDCR.1	-	R/W	PORTD input/output control
$1A	-	-	PECR.1	PECR.0	R/W	PORTE input/output control

PA (B/C/D/E) CR.n, (n = 0, 1, 2, 3)
0: Set I/O as an input direction. (Power on initial)
1: Set I/O as an output direction.

Equivalent Circuit for a Single I/O Pin:



Port Configuration Function Block Diagram

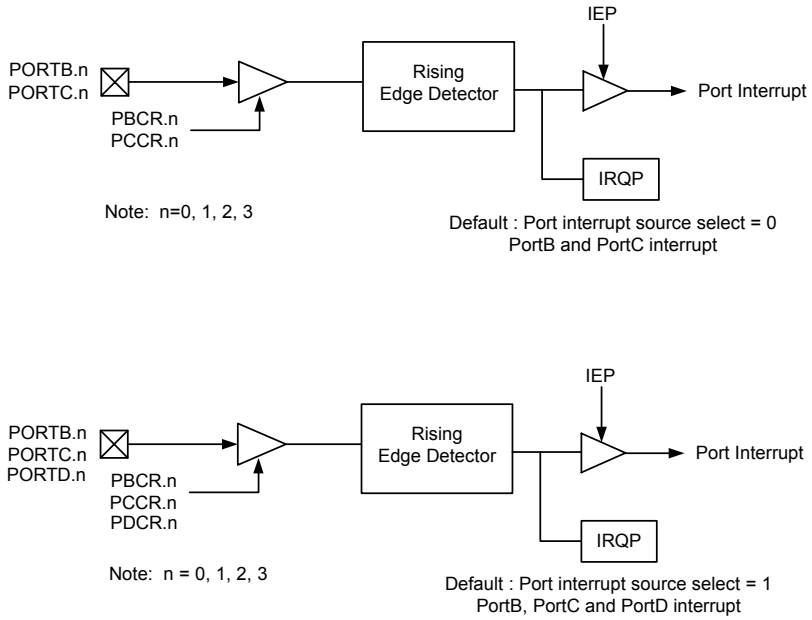
System Register $13:

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	PPULL	CPS2	CPS1	CPS0	R/W	Bit3: Port Pull-low enable Control

To turn on the pull-low resistor, user must set PPULL to “1”, and write “0” to the port data register.

Port Interrupt

The PORTB, PORTC or PORTB, PORTC and PORTD are used as port interrupt sources. Since PORT I/O is a bit programmable I/O, therefore only the input port can generate an external interrupt. Any transition from PORTB and PORTC input pins from GND to V_{DD} will generate an interrupt request (Default). When Code Option (Port interrupt source select) is high, PORTB, PORTC and PORTD as the port interrupt source. But further rising edge transitions cannot be able to make interrupt request until all of the pins return to GND. The following is the port interrupt function block-diagram.



PORT Interrupt Block Diagram

Port Interrupt PROGRAMMING NOTES:

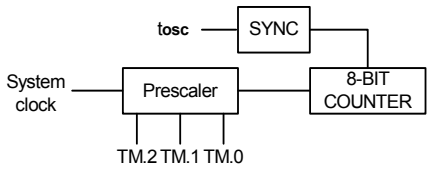
If user wants to generate an interrupt when a rising edge from GND to V_{DD} emerges in the port, the following must be executed.
1. Set the port as input port, fill port data register with “0” and avoid port floating.
2. Pull-low the port (Use external pull-low resistance or set PPULL to “1”).
3. Set port interrupt enable flag (Set IEP to “1” in port interrupt application.).

And further rising edge transition would not be able to make interrupt request until all of the pins return to GND in Port interrupt application.

7. Timer0

The timer/counter has the following features:
- 8-bit up-counting timer/counter.
- Automatic re-load counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:
- Programmable interval timer function.
- Read counter value.

7.1. Timer0 Configuration and Operation

The Timer0 consist of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

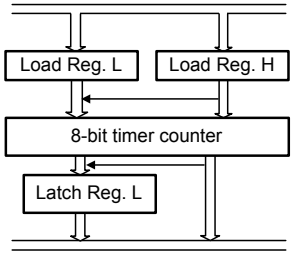
Low nibble first

High nibble to update the counter

Read Operation:

High nibble first

Low nibble followed.



7.2. Timer Mode Register

The timer can be programmed in several different prescalers by setting Timer Mode register (TM0).

The 8-bit counter prescaler overflow output pulses. The Timer Mode registers (TM0) are 3-bit registers used for the timer control as shown in Table 1. These mode registers select the input pulse sources into the timer.

Table 1. Timer0 Mode Register ($02)

TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

8. Interrupt

Two interrupt sources are available on SH66K33A:
- Timer0 interrupt
- Port B & Port C or Port B & Port C & Port D rising edge detection interrupt (Code option)

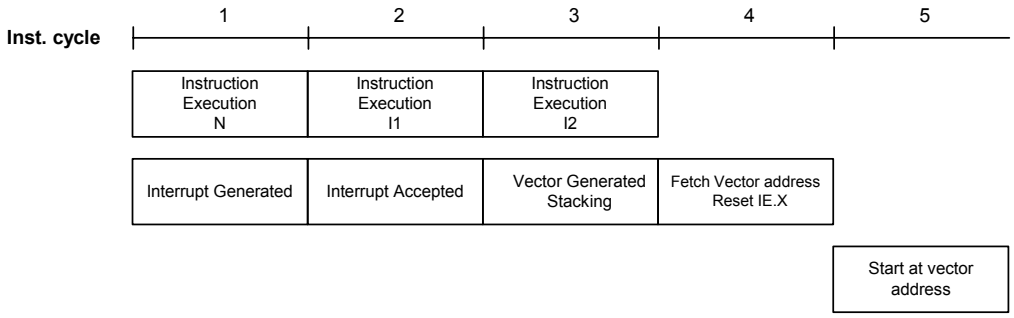
Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. These flags are cleared to “0” at initialization by chip reset.

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$00	-	IET0	-	IEP	R/W	Interrupt enable flags
$01	-	IRQT0	-	IRQP	R/W	Interrupt request flags

When IEx is set to “1” and the interrupt request is generated (IRQx is “1”), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to “0” automatically, so when IRQx is “1” and IEx is set to “1” again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting:

During the CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enabled, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

Timer Interrupt

The input clocks of Timer0 is based on system clock as Timer0 source. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 = 1), If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Port Rising Edge Interrupt

Only the input port can generate an external interrupt. The analog input cannot generate an interrupt request.

Any one of the I/O input pin transitions from GND to V_{DD} would generate an interrupt request. Further rising edge transition would not be able to make an interrupt request until all of the input pins have returned to GND. This can also be used to wake the CPU from STOP mode.

9. Remote Control Carrier Synthesizer

The device has a built-in carrier synthesizer for infrared or RF remote control circuits.

System Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$0D	-	-	-	REMO REM	W R	Bit0: REMO output data. Bit0: REM pin output status.
$13	PPULL	CPS2	CPS1	CPS0	R/W	Bit2-0: Carrier count source prescaler control

The carrier synthesizer can be programmed in several different prescaler ratios by setting CPS2 - 0.

CPS2	CPS1	CPS0	Prescaler Divide Ratio	Ratio N
0	0	0	fosc/2^{11}	2048 (initial)
0	0	1	fosc/2^{9}	512
0	1	0	fosc/2^{7}	128
0	1	1	fosc/2^{5}	32
1	0	0	fosc/2^{3}	8
1	0	1	fosc/2^{2}	4
1	1	0	fosc/2^{1}	2
1	1	1	fosc/2^{0}	1

The carrier-generating counter is an 8-bit count-up counter and two 8-bit data load registers (High level data register and Low level data register). Writing data into the data load registers can initialize the counter.

After system reset, the counter is automatically loaded with the contents of high level data register and output high level at the same time. Following when counter counts overflow from $FF to $00,the counter is automatically loaded with the contents of low level data register and output low level at the same time. When counter counts overflow again from $FF to $00 again, the counter will be loaded with the contents of high level data register again. The above sequences make up a complete loop. So the carrier synthesizer can output continuous carrier wave of certain duties and certain period.

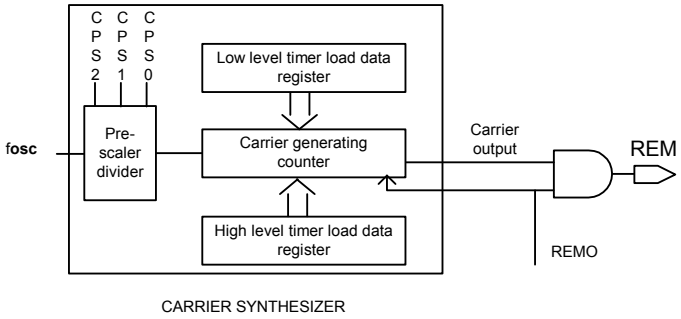
If REMO is set to “1” from “0”, the carrier counter will be initialized to load high level data register and output high level whatever states the counter is.

Load register programming: User can modify low level data register to change the width of the low level or modify high level data register to change the width of high level. In the way the carrier synthesizer can output carrier wave of different duties and different period.

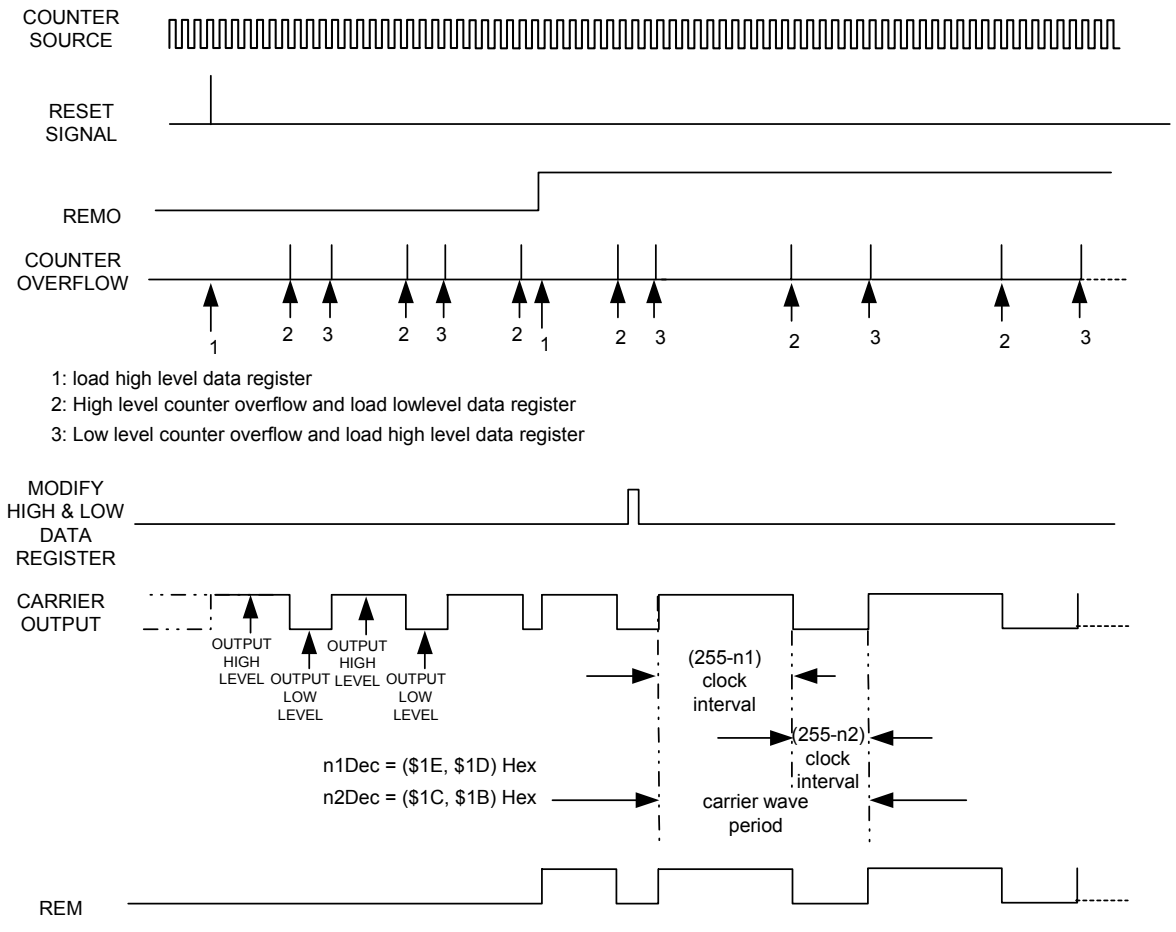
REM will remain outputting carrier wave in HALT mode, but will output GND in STOP mode.

Carrier Load Data Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$1B	CFL3	CFL2	CFL1	CFL0	R/W	Carrier low level timer load data register (low nibble)
$1C	CFL7	CFL6	CFL5	CFL4	R/W	Carrier low level timer load data register (high nibble)
$1D	CFH3	CFH2	CFH1	CFH0	R/W	Carrier high level timer load data register (low nibble)
$1E	CFH7	CFH6	CFH5	CFH4	R/W	Carrier high level timer load data register (high nibble)



Remote Control Functional Block Diagram



Carrier Synthesize Wave

10. Low Voltage Reset (LVR)

The LVR function monitors the supply voltage and applies an internal reset in the micro-controller at battery replacement. If the applied circuit satisfies the following conditions, the LVR can be incorporated by the software control.

The software enable flag controls LVR circuit on/off.

LVR circuit operating ambient temperature is T_A = -10℃ to +70℃

Functions of LVR Circuit:
The LVR circuit has the following functions:
Generates an internal reset signal when $V_{DD} \leqq V_{LVR}$.
Cancels the internal reset signal when $V_{DD} > V_{LVR}$.
Stops the oscillator operation and forces the CPU to enter STOP mode when $V_{DD} \leq V_{LVR}$.

As $V_{DD} \leqq V_{LVR}$, the LVR reset will delay about 1ms before being triggered. If V_{DD} goes back to $V_{DD} > V_{LVR}$, without any delay then cancel the LVR reset.

LVR Control Register:

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$15	LVR3	LVR2	LVR1	LVR0	R/W	LVR Enable Control (LVR3 - 0): 1010: LVR Disable Else: LVR Enable (Power-on initial 0000)

11. Watchdog Timer (WDT)

The watchdog timer is a 16-bit count-down counter, and its clock source is an independent built-in RC oscillator. But it will not run in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. To prevent it timing out and generating a device reset condition, users should write watchdog timer reset bit ($14 bit3) as “1” before timing-out. The watchdog timer has a time-out period of approx. 16ms.

System Register $14 (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	$\overline{WDT}$	-	-	-	R/W	Bit3: Watchdog timer reset bit (Write “1” to reset WDT)

Note:

The $\overline{WDT}$ bit is cleared only if the Watchdog Timer time-out occurred both in normal operation mode and in the HALT mode. The watchdog timer is cleared when the device wakes up from the STOP mode, regardless of the source of wake-up.

12. HALT and STOP Mode

After the execution of HALT instruction, SH66K33A will enter HALT mode. In HALT mode, the CPU will stop operating. But peripheral circuit (timer) will keep status.

After the execution of STOP instruction, SH66K33A will enter STOP mode. In STOP mode, the whole chip (including oscillator) will stop operating. But watchdog is still enabled.

In HALT mode, SH66K33A can be waked up if any interrupt occurs.
In STOP mode, SH66K33A can be waked up if port interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to halt/stop is executed.

13. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:

13.1. Power-on Reset

Warm-up time interval:

(1) In Internal RC oscillator mode, f**osc** = 4MHz, the warm-up counter prescaler divide ratio is $/2^{13}$ (8192) and the warm-up time interval is 2 ms.

(2) In Crystal oscillator or Ceramic resonator mode, f**osc** = 400kHz - 4MHz, the warm-up counter prescaler divide ratio is $/2^{13}$ (8192).

13.2. Wake up from Stop Mode

Warm-up time interval:

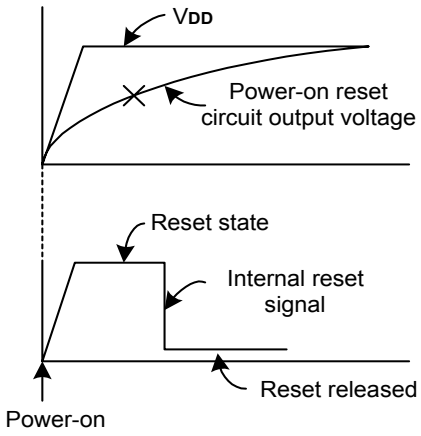
(1) In Internal RC oscillator mode, f**osc** = 4MHz, the warm-up counter prescaler divide ratio is $/2^{13}$ (8192) and the warm-up time interval is 2 ms.

(2) In Crystal oscillator or Ceramic resonator mode, f**osc** = 400kHz - 4MHz, the warm-up counter prescaler divide ratio is $/2^{13}$ (8192).

14. Reset Function

The SH66K33A has the power-on reset circuit, though it does not have $\overline{\text{RESET}}$ pin. System reset is performed automatically at power-on, and software starts program from address $000.

In order to make the built-in power-on reset circuit operate efficiently, set the voltage rising time until V_{DD} = 0V to 2.2V is obtained at power-on 1ms or less.



15. Code Option

Oscillator Type
0: 4MHz built-in RC oscillator (Default)
1: External Ceramic resonator/Crystal Oscillator: 400kHz - 4MHz

Port Interrupt Source Select
0: PORTB, PORTC interrupt (Default)
1: PORTB, PORTC, PORTD interrupt

Instruction Cycle Time:
0: Instruction cycle time = 4/f**osc** (Default)
1: Instruction cycle time = 16/f**osc**

Instruction Set

All instructions are one cycle and one-word instructions. The characteristics are memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC <- Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx <- Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC <- Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx <- Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC <- Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx <- Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC <- Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx <- Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC <- Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx <- Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC <- Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx <- Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC <- Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx <- Mx & AC	
SHR	11110 0000 000 0000	0 -> AC[3], AC[0] -> CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X, I	01000 iiii xxx xxxx	AC <- Mx + I	CY
ADIM X, I	01001 iiii xxx xxxx	AC, Mx <- Mx + I	CY
SBI X, I	01010 iiii xxx xxxx	AC <- Mx + -I +1	CY
SBIM X, I	01011 iiii xxx xxxx	AC, Mx <- Mx + -I +1	CY
EORIM X, I	01100 iiii xxx xxxx	AC, Mx <- Mx ⊕ I	
ORIM X, I	01101 iiii xxx xxxx	AC, Mx <- Mx | I	
ANDIM X, I	01110 iiii xxx xxxx	AC, Mx <- Mx & I	

1.3. Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx <- Decimal adjust for add	CY
DAS X	11001 1010 xxx xxxx	AC, Mx <- Decimal adjust for sub	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC <- Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx <- AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx <- I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC <- X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC <- X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC <- X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC <- X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC <- X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC <- X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC <- X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC <- X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST <- CY, PC +1 PC <- X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC <- ST; TBR <- hhhh, AC <- lll	
RTNI	11010 1000 000 0000	CY, PC <- ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC <- X (Include p)	
TJMP	11110 1111 111 1111	PC <- (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . .-0.3V to +3.6V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . -10℃ to +70℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.8	3.0	3.6	V	400kHz ≤ f_{OSC} ≤ 4MHz Instruction cycle time = 16/4 (4μs) or 4/4 (1μs)
RAM Retention Voltage	V_{RAM}	1.1	-	3.6	V	
LVR Voltage	V_{LVR}	-	1.7	1.95	V	
Operating Current	I_{OP}	-	0.3	1	mA	f_{OSC} = 4MHz All output pins unloaded, execute NOP instruction, V_{DD} = 3.0V
HALT Current	I_{SB1}	-	200	-	μA	f_{OSC} = 4MHz All output pins unloaded (HALT mode), V_{DD} = 3.0V
STOP Current	I_{SB2}	-	-	1.5	μA	All output pins unloaded (STOP mode), V_{DD} = 3.0V, LVR on
RESET Current	I_{RESET}	-	-	1.5	μA	Power on Reset or LVR reset, V_{DD} = 3.0V
Power-on reset circuit valid power source rising time	T_{PON}	-	-	1	ms	V_{DD} = 0 to 2.2V

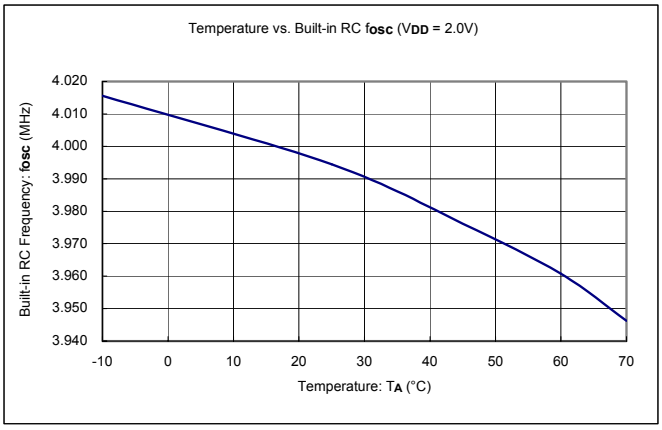
DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, f_{OSC} = 4MHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
REM sink current	I_{REML}	0.3	-	-	mA	V_{REM} = 0.3V
REM driving current	I_{REMH}	-5	-9	-	mA	V_{REM} = 1V
Input Low Voltage	V_{IL}	GND	-	V_{DD} X 0.3	V	I/O ports pins tri-state
Input High Voltage	V_{IH}	V_{DD} X 0.7	-	V_{DD}	V	I/O ports pins tri-state
High-level Input Current	I_{IH}	-	-	0.2	μA	I/O ports; $V_{I/O}$ = V_{DD}
Low-level Input Current	I_{IL1}	-50	-	-15	μA	I/O ports with pull-low; $V_{I/O}$ = V_{DD}
Low-level Input Current	I_{IL2}	-	-	-0.2	μA	I/O ports without pull-low; $V_{I/O}$ = GND
Output High Voltage	V_{OH}	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = -2mA (V_{DD} = 3.0V)
Output Low Voltage	V_{OL}	-	-	GND + 0.6	V	I/O ports, I_{OL} = 0.4mA (V_{DD} = 3.0V)

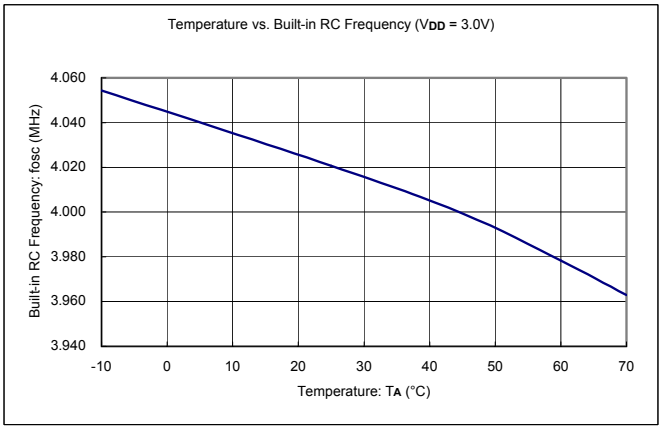
AC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25℃, built-in RC oscillator, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator Start time	T_{OST}	-	-	20	ms	455kHz Ceramic Oscillator
Frequency Variation	f_{OSC1}	3.84	4	4.16	MHz	V_{DD} = 2.0 to 3.6V,T_A = +5℃ to +45℃
Frequency Variation	f_{OSC2}	3.80	4	4.20	MHz	V_{DD} = 2.0 to 3.6V,T_A = -10℃ to +70℃
Note: Different with SH67P33A						

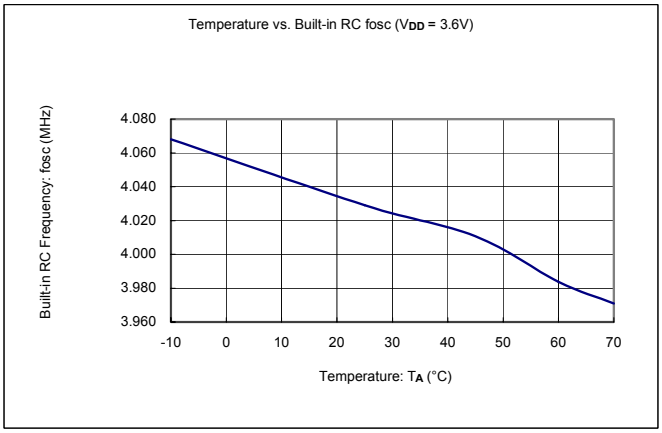
RC Oscillator Characteristics Graphs (for reference only)



Temperature vs. Built-in RC frequency (V_{DD} = 2.0V)



Temperature vs. Built-in RC frequency (V_{DD} = 3.0V)



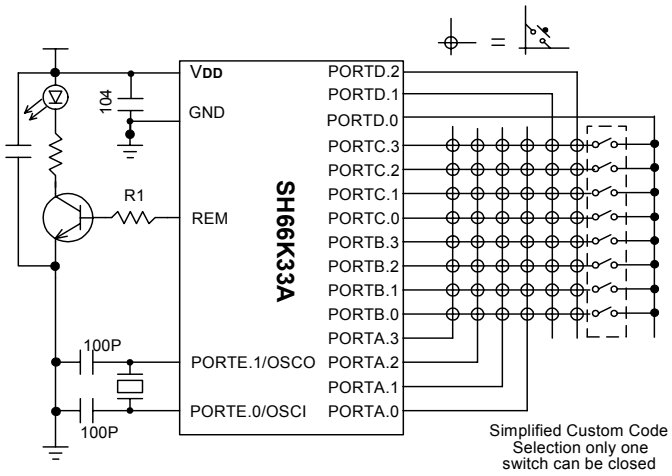
Temperature vs. Built-in RC frequency (V_{DD} = 3.6V)

Application Circuit (for reference only)

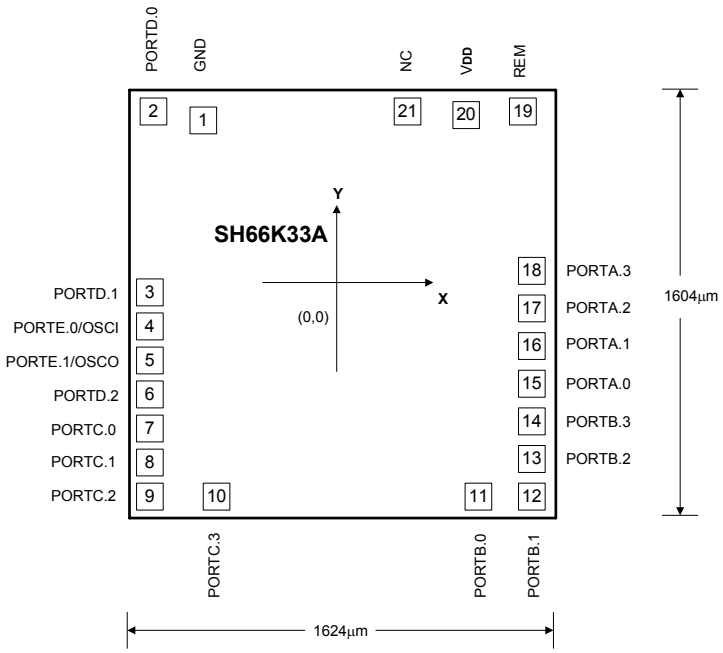
AP1:

Remote Control (48 Keys)

(1) Operating voltage: 3.0V
(2) Oscillator: Ceramic 455kHz (PORTE.0 - 1 shared to OSCI & OSCO)
(3) PORTA, PORTD.1, PORTD.2: I/O Buffers
(4) PORTB, C and PORTD.0: Input Buffers
(5) R1 = 0 is possible, but the REM specification is revised to reduce power consumption
(6) Since PORTD.0 is input only, PORTB or PORTC can be scanned out to detect PORTD.0 option.



Bonding Diagram



*. Substratum connects to ground.

Pad Location unit: μm

Pad No	Designation	X	Y	Pad No	Designation	X	Y
1	GND	-573.35	708.00	12	PORTB.1	742.00	-732.00
2	PORTD.0	-730.10	732.00	13	PORTB.2	742.00	-607.00
3	PORTD.1	-742.00	-12.00	14	PORTB.3	742.00	-482.00
4	PORTE.0/OSCI	-742.00	-132.00	15	PORTA.0	742.00	-357.00
5	PORTE.1/OSCO	-742.00	-252.00	16	PORTA.1	742.00	-232.00
6	PORTD.2	-742.00	-372.00	17	PORTA.2	742.00	-107.00
7	PORTC.0	-742.00	-492.00	18	PORTA.3	742.00	18.00
8	PORTC.1	-742.00	-612.00	19	REM	713.40	710.00
9	PORTC.2	-742.00	-732.00	20	VDD	445.15	704.90
10	PORTC.3	-526.00	-732.00	21	NC	261.95	719.90
11	PORTB.0	526.00	-732.00				

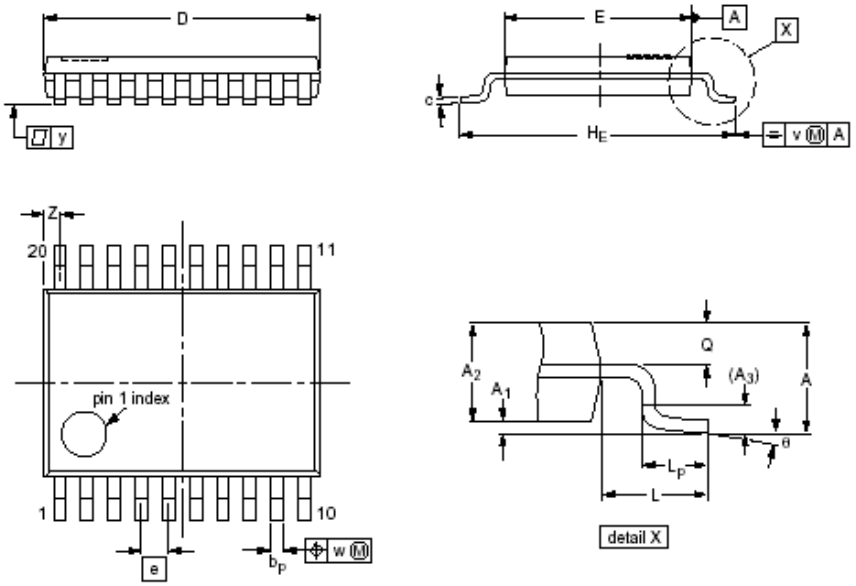
Ordering Information

Part No.	Package
SH66K33AH	Chip Form
SH66K33AX	20L TSSOP
SH66K33A	20L DIP
SH66K33AM	20L SOP

Package Information

TSSOP 20L Outline Dimensions

unit: inches/mm

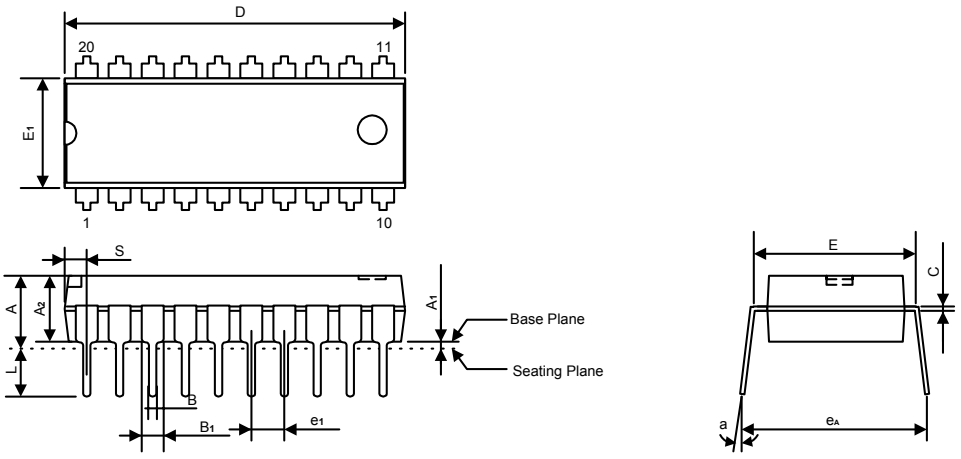


Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.1	---	---	0.044
A1	0.05	---	0.15	0.002	---	0.006
A2	0.80	---	0.95	0.032	---	0.038
A3	---	0.25	---	---	0.01	---
bp	0.19	---	0.30	0.008	---	0.012
c	0.1	---	0.2	0.004	---	0.008
D(1)	6.4	---	6.6	0.256	---	0.264
E(2)	4.3	---	4.5	0.172	---	0.18
e	---	0.65	---	---	0.026	---
HE	6.2	---	6.6	0.248	---	0.264
L	---	1	---	---	0.04	---
Lp	0.5	---	0.75	0.02	---	0.03
Q	0.3	---	0.4	0.012	---	0.016
v	---	0.2	---	---	0.008	---
w	---	0.13	---	---	0.005	---
y	---	0.1	---	---	0.004	---
Z(1)	0.2	---	0.5	0.008	---	0.02
θ	0°	---	8°	0°	---	8°

Notes:

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlaid protrusions of 0.25 mm maximum per side are not included.

P-DIP 20L Outline Dimensions unit: inches/mm

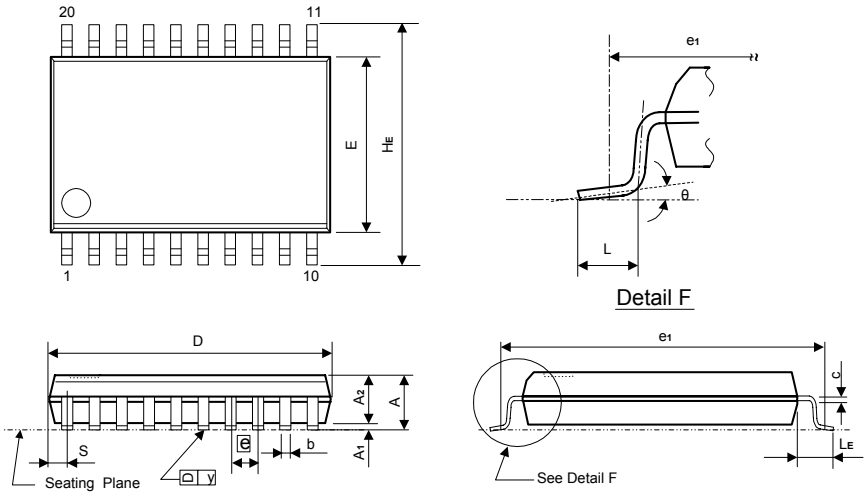


Symbol	Dimensions in inches	Dimensions in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130 ± 0.010	3.30 ± 0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.057± 0.008	1.45± 0.2
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	1.026 Typ. (1.046 Max.)	26.06 Typ. (26.57 Max.)
E	0.300 ± 0.010	7.62 ± 0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100 ± 0.010	2.54 ± 0.25
L	0.130 ± 0.010	3.30 ± 0.25
α	0° - 15°	0° - 15°
e_A	0.345 ± 0.035	8.76 ± 0.89
S	0.078 Max.	1.98 Max.

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

SOP 20L (W.B.) Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.106 Max.	2.69 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.092 ± 0.005	2.33 ± 0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.500 ± 0.02	12.80 ± 0.51
E	0.295 ± 0.010	7.49 ± 0.25
e	0.050 ± 0.006	1.27 ± 0.15
e_1	0.376 NOM.	9.50 NOM.
H_E	0.406 ± 0.012	10.31 ± 0.31
L	0.032 ± 0.008	0.81 ± 0.20
L_E	0.055 ± 0.008	1.40 ± 0.20
S	0.042 Max.	1.07 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch. Designer reference only.
4. Dimension S includes end flash.

Data Sheet Revision History

Version	Content	Date
2.2	Updated “DC Electrical characteristics”	Sep. 2007
2.1	Package information update	Apr. 2007
2.0	Change RC Range, Remove Internal RC application, change LPD to LVR	Aug. 2006
1.0	Original	Feb. 2006