SH6611A

Preliminary

1K 4-bit Microcontroller with LCD Driver

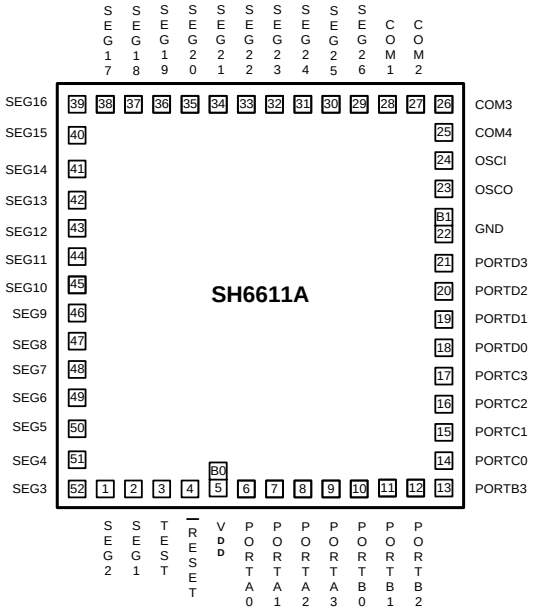
Features

- SH6610C-based single-chip 4-bit microcontroller with LCD driver
- ROM: 1024 × 16 bits
- RAM: 256 × 4 bits (data memory)
- Operation Voltage Range: 2.2V - 5.4V (3V typically)
- 16 CMOS I/O pins (PORTA - D, CMOS or Open Drain by code option)
- 4 level subroutine nesting (including interrupts)
- Two 8-bit timers with pre-divider circuit
- Oscillator warm-up timer
- 4 priority interrupt sources:
  - External interrupt (falling edge)
  - Timer0 interrupt
  - Timer1 interrupt
  - PortB interrupt (falling edge)
- Clock source: 32.768KHz crystal or 262K RC (code option)
- Instruction cycle time:
  4/32.768KHz (≈ 122μs) for 32.768KHz crystal
  4/262KHz (≈ 15μs) for 262KHz RC
- LCD driver:
  4 × 26 (1/4 duty , 1/3 bias or 1/3 duty , 1/2 bias)
- Two low power operation modes - HALT or STOP mode
- Built-in alarm generator (carrier frequency: 2KHz or 4KHz code option)
- Low power consumption (Iop < 10μA, 32.768KHz, 3V)
- Bonding option for multi-code software
- Available in CHIP FORM

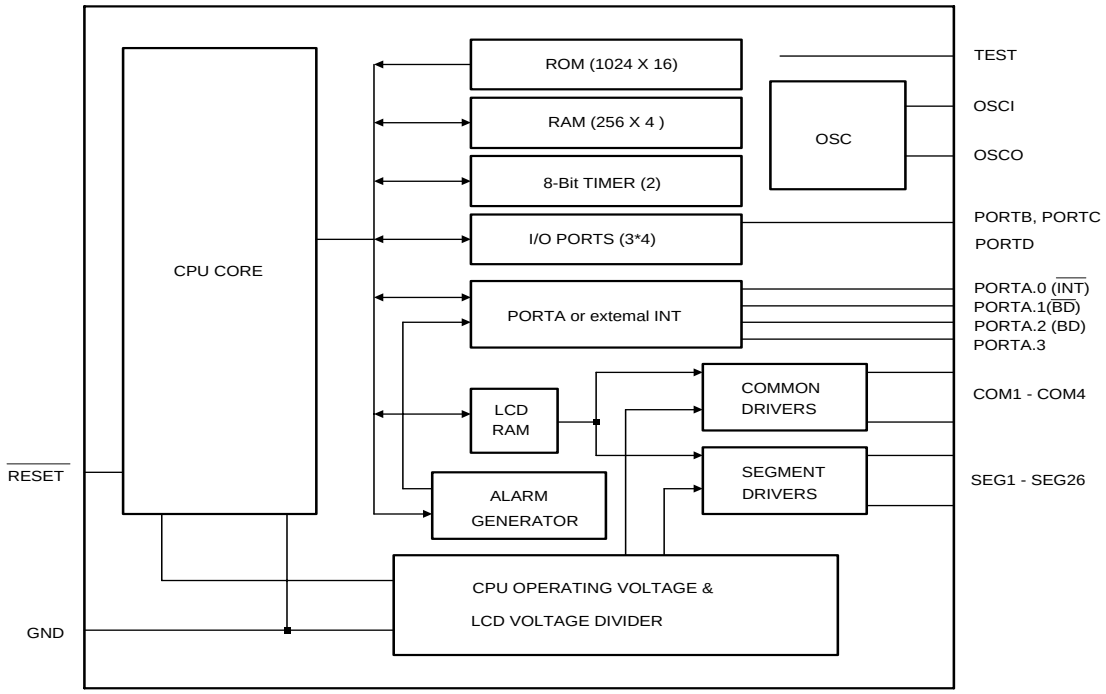
General Description

SH6611A is a single-chip microcontroller integrated with an SH6610C CPU core, SRAM, timer, alarm generator, LCD driver, I/O port, and program ROM.

Pad Configuration



Block Diagram



Pad Description

Pad No.	Designation	I/O	Description
2 - 1, 52 - 29	SEG1 - 26	O	Segment signal output for LCD display. Seg1 - 4 as output
3	TEST	I	Test pin internally pull-down (No connect for user)
4	$\overline{\text{RESET}}$	I	Pad reset input
5	V_{DD}	P	Power pin
5	B0	I	Bonding option, internally pull-low
6 - 9	PORTA0 - 3	I/O	Bit programmable I/O PA.0 could be external interrupt input($\overline{\text{INT}}$) PA.1, PA.2 could be buzzer output PA.1 (BD), PA.2 ($\overline{\text{BD}}$)
10 - 13	PORTB0 - 3	I/O	Bit programmable I/O, vector interrupt (active falling edge)
14 - 17	PORTC0 - 3	I/O	Bit programmable I/O
18 - 21	PORTD0 - 3	I/O	Bit programmable I/O
22	GND	P	Ground pin
22	B1	I	Bonding option, internally pull-high
23	OSCO	O	Oscillator output pin, connected to crystal oscillator
24	OSCI	I	Oscillator input pin, connected to crystal or external resistor
28 - 25	COM1 - 4	O	Common signal output for LCD display

Total 52 pads for mask type.

Functional Description

1. CPU

The CPU contains the following function blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register (TBR), Data Pointer (INX, DPH, DPM, and DPL), and Stacks.

1.1 PC (Program Counter)

The PC is used to address 1K Programmable ROM. It consists of 12-bits:

Page Register (PC11), and Ripple Carry Counter (PC10 - PC0).

The program counter normally increases by one (+1) with every execution of an instruction except in the following cases:

(1) When executing a jump instruction (such as JMP, BA0, BC);

(2) When executing a subroutine call instruction (CALL);

(3) When an interrupt occurs;

(4) When the chip is at the INITIAL RESET mode.

The program counter is loaded with data corresponding to each instruction.

1.2 ALU and CY

ALU performs arithmetic and logic operations.

The ALU provides the following functions:

Binary addition/subtraction (ADC, SBC, ADD, SUB, ADI, SBI)

Decimal adjustment for addition/subtraction (DAA, DAS)
Logic operations (AND, EOR, OR, ANDIM, EORIM, ORIM)

Decision (BA0, BA1, BA2, BA3, BAZ, BC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow, which the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and restored back from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3 Accumulator

Accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with ALU, data transfers between the accumulator and system register or data memory can be performed.

1.4 Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bits), DPM (3-bits) and DPL (4-bits). The addressing range can have 3FFH locations. Pseudo index address (INX) is used to read or write Data memory, then RAM address bit9 - bit0 comes from DPH, DPM and DPL.

1.5 Stack

This group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. It is organized 13 bits X 4 levels. The MSB is saved for CY. 4 levels are the maximum allowed total for subroutine calls and interrupts.

Note:

The contents of Stack are returned sequentially to the PC with the return instructions (RTNI/RTNW). Stack is operated on a first-in, last-out basis. This 4-level nesting includes both subroutine calls and interrupts requests. Note that program execution may enter an abnormal state if the number of calls and interrupts requests exceeds 4, then the bottom of stack will be shifted out.

2. ROM

The SH6611A can address 1K × 16 bit words of program area from $000 to $3FF.
ROM SPACE in the system is 1024 X 16 bits.

(a) Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
000H	JMP instruction	Jump to RESET service routine
001H	JMP instruction	Jump to External interrupt service routine
002H	JMP instruction	Jump to TIMER0 service routine
003H	JMP instruction	Jump to TIMER1 service routine
004H	JMP instruction	Jump to PB service routine (PORTB)

*JMP instruction can be replaced by any instruction.

(b) Table Data Reference

Table Data can be stored in the program memory and can be referenced by using the Table Branch (TJMP) and the Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (A) are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, A)). The address is determined by RTNW to return look-up value into (TBR, A). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into A.

3. RAM

Built-in SRAM contains of general-purpose data memory, LCD RAM and system register.

(a) RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:
$000 - $01F: System register and I/O
$020 - $11F: Data memory (256 × 4 bits, divided into 2 banks).
$300 - $319: LCD RAM space (26 × 4 bits).

(b) Data Memory

Data memory is organized as 256 X 4 bits ($020 - $11F). Because of its static nature, the RAM can keep data after the CPU enters STOP or HALT.

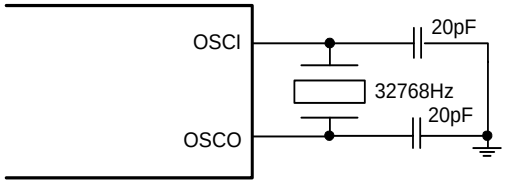
(c) The configuration of system register:

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags
$02	-	T0M.2	T0M.1	T0M.0	R/W	Bit0-2: Timer0 Mode register
$03	-	T1M.2	T1M.1	T1M.0	R/W	Bit0-2: Timer1 Mode register
$04	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter register low nibble
$05	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter register high nibble
$06	T1L.3	T1L.2	T1L.1	T1L.0	R/W	Timer1 load/counter register low nibble
$07	T1H.3	T1H.2	T1H.1	T1H.0	R/W	Timer1 load/counter register high nibble
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD
$0C	-	-	-	-	-	Reserved
$0D	-	-	B1	B0	R	Bonding option
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch Register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble
$13	O/S	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm O/P Bit1: HEAVY LOAD Mode Bit2: LCD off Bit3: set LCD segment as outport
$14	AEC3	AEC2	AEC1	AEC0	R/W	Alarm Envelope Control
$15	-	-	-	DUTY	R/W	Bit0: change LCD duty to 1/4 duty, 1/3 bias
$16 ~ $1F	-	-	-	-	-	Reserved

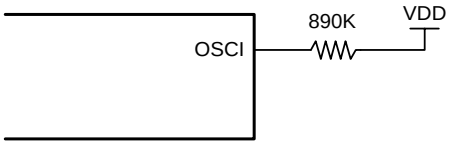
4. System Clock and Oscillator

SH6611A has one clock source. Oscillator is determined by code option. The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock = FOSC/4.
(a) Instruction cycle time:
(1) 4/32768Hz (≈122.1μs) for 32768Hz oscillator.
(2) 4/262KHz (≈15μs) for 262KHz oscillator.

(b) Oscillator type
(1) Crystal oscillator: 32768Hz



(2) RC oscillator: 262KHz



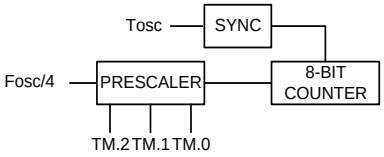
5. Timer0 & Timer1

SH6611A has two 8-bit timers.

The timer / counter has the following features:

- 8-bit up-counting timer/counter.
- Automatic re-loads counter.
- 8-level prescaler.
- Interrupt on overflow from $FF to $00.

The following is a simplified timer block diagram.



The timers provide the following functions:

- Programmable interval timer function.
- Read counter value.

(a) Timer0 and Timer1 Configuration and Operation

Both the Timer0 and Timer1 consist of an 8-bit write-only timer load register (TL0L, TL0H; TL1L, TL1H) and an 8-bit read-only timer counter (TC0L, TC0H; TC1L, TC1H). Each of them has low order digits and high order digits. Writing data into the timer load register (TL0L, TL0H; TL1L, TL1H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high order digit is written or counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations. Please follow these steps:

Write Operation:

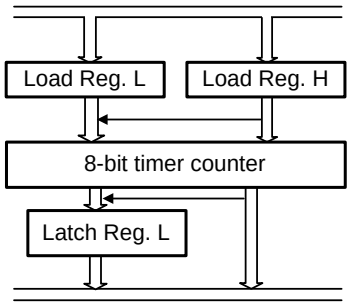
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed.



(b) Timer Mode Register

The timer can be programmed in several different prescaler ratios by setting Timer Mode register (TM0, TM1).

The 8-bit counter prescaler overflow output pulses. The Timer Mode registers (TM0, TM1) are 3-bit registers used for the timer control as shown in Table 1 and Table 2. These mode registers select the input pulse sources into the timer.

Table 1: Timer0 Mode Register ($02)

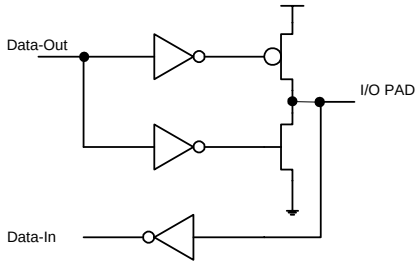
TM0.2	TM0.1	TM0.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

Table 2: Timer1 Mode Register ($03)

TM1.2	TM1.1	TM1.0	Prescaler Divide Ratio	Clock Source
0	0	0	$/2^{11}$	System clock
0	0	1	$/2^{9}$	System clock
0	1	0	$/2^{7}$	System clock
0	1	1	$/2^{5}$	System clock
1	0	0	$/2^{3}$	System clock
1	0	1	$/2^{2}$	System clock
1	1	0	$/2^{1}$	System clock
1	1	1	$/2^{0}$	System clock

6. I/O Port

SH6611A has 16 CMOS quasi-I/O ports, PORTA, PORTB, PORTC, PORTD. All I/O ports are bit programmable.
If PORTA,B,C,D are pull-high internally, it is weak drive.
The equivalent circuit is below:



Port I/O Data Register: (PDR)

Address	Bit3	Bit2	Bit1	Bit0
$08	PORT A.3	PORT A.2	PORT A.1	PORT A.0
$09	PORT B.3	PORT B.2	PORT B.1	PORT B.0
$0A	PORT C.3	PORT C.2	PORT C.1	PORT C.0
$0B	PORT D.3	PORT D.2	PORT D.1	PORT D.0

7.Interrupt

Four interrupt sources are available on SH6611A:

- External interrupt ($\overline{INT}$ shared with PA.0)
- Timer0 interrupt
- Timer1 interrupt
- PortB interrupts (falling edge)

Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remark
$00	IEX	IET0	IET1	IEP	R/W	Interrupt enable flags
$01	IRQX	IRQT0	IRQT1	IRQP	R/W	Interrupt request flags

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.

External Interrupt ($\overline{INT}$)

External interrupt is shared with the bit0 of PORTA. When bit3 of system register 0 (IEX) is set to 1, the external interrupt will be enabled, and a falling edge signal on PA.0 will generate an external interrupt. (Note: while external interrupt is enabled, writing a "0" to bit0 of PORTA will generate an external interrupt).

Port falling edge Interrupt

The PortB are used as port interrupt sources. Any one of the PortB pin transitions from VDD to GND would generate an interrupt request (IRQP=1). Further falling edge transition would not be able to make a new interrupt request until all of the input pins have returned to VDD. Port Interrupt can be used to wake the CPU from HALT or STOP mode.

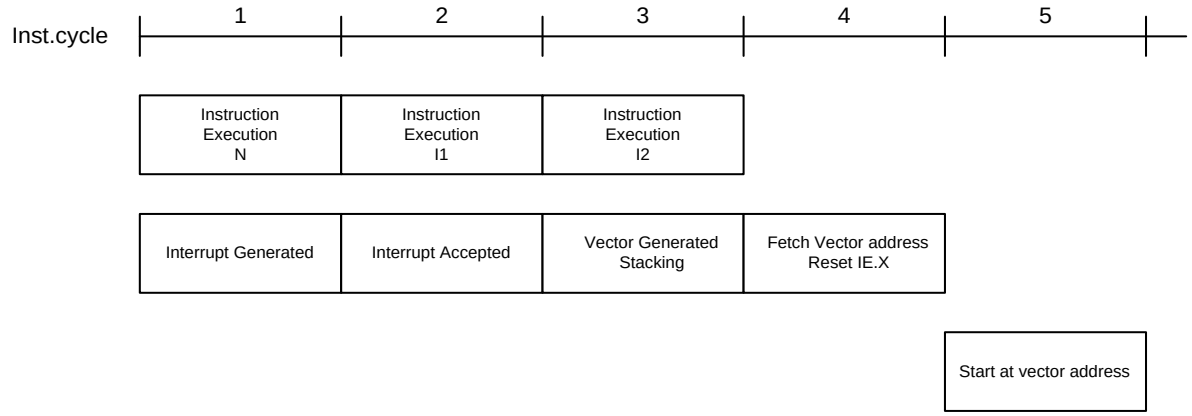
Timer Interrupt

The input clock of Timer0 and Timer1 are based on system clock. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 or IRQT1=1), If the interrupt enable flag is enabled (IET0 or IET1=1), a timer interrupt service routine will start. Timer interrupt can also be used to wake the CPU from HALT mode.

Interrupt Nesting:

During the SH6610C CPU interrupt service, the user can enable any INTERRUPT enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

Interrupt Servicing Sequence Diagram:



8. LCD Driver

The LCD driver contains a controller, a voltage generator, 4 common signal pins and 26 segment driver pins. There are two different driving modes programmable: one is 1/4 duty and 1/3 bias, the other is 1/3 duty and 1/2 bias. The driving mode is controlled by system register $15 and the power on initialization status is 1/3 duty, and 1/2 bias. The controller consists of display data RAM and a duty generator. The LCD data RAM is a dual port RAM that transfers data to segment pins automatically without a program control.

The LCD SEG1 - 4 can also be used as output port, it is selected by the bit 3 of the system register $13. When SEG1 - 4 are output ports, data can be written to bit 0 of the same addresses (300H-303H). LCD RAM could be used as data memory if needed. When the "STOP" instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the same value before executing the "STOP" instruction.

(a) LCD Control Register

System Register $13

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description
$13	O/S	LCDOFF	HLM	PAM	R/W	Bit0: set PA.1, PA.2 as Alarm O/P Bit1: HEAVY LOAD Mode Bit2: LCD off Bit3: set LCD segment as outport

PAM: PORTA Mode control:
0: PORTA.1, PORTA.2 as I/O port 1: PORTA.1, PORTA.2 as ALARM output

HLM: Heavy load mode control:
0: No heavy load 1: HEAVY LOAD mode

LCDOFF: LCD Power control:
0: LCD signal on 1: LCD signal off

O/S: Seg1 – 4 control:
0: Seg1 - 4 as LCD output 1: Seg1 - 4 as output ports

System Register $15

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Description
$15	-	-	-	DUTY	R/W	LCD duty control

DUTY: LCD duty control
0: 1/3 duty, 1/2 bias 1: 1/4 duty, 1/3 bias

(b) LCD divider resistance control (code option)

Low LCD Driving Capability :
Total Internal LCD divider resistance is 1.44M.
Normal LCD Driving Capability :
Total Internal LCD divider resistance is 360K.
High LCD Driving Capability :
Total Internal LCD divider resistance is 165K.
Higher LCD Driving Capability :
Total Internal LCD divider resistance is 120K.

When large LCD panel is used, user can select smaller divider resistance through code option to increase the bias current for better LCD performance. But it will cost more power, when smaller divider resistance is used.

(c) Configuration of LCD RAM area

(1) When segments 1 - 4 are used as output ports:

Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1
300H	-	-	-	DATA_BIT
301H	-	-	-	DATA_BIT
302H	-	-	-	DATA_BIT
303H	-	-	-	DATA_BIT

(2) When segments 1 - 4 are used as segment outputs:

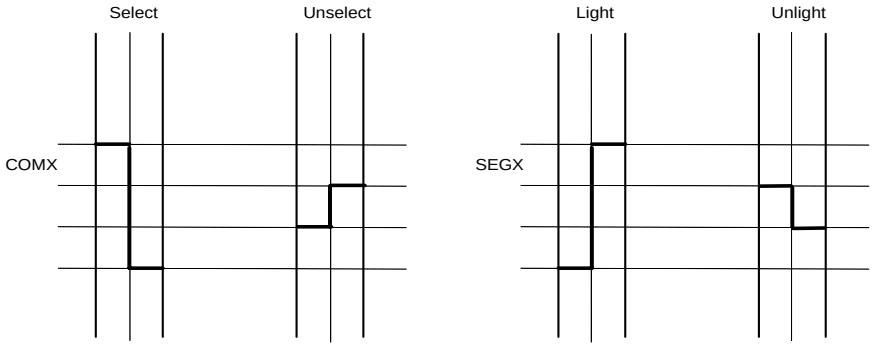
Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1
301H	SEG2	SEG2	SEG2	SEG2
302H	SEG3	SEG3	SEG3	SEG3
303H	SEG4	SEG4	SEG4	SEG4

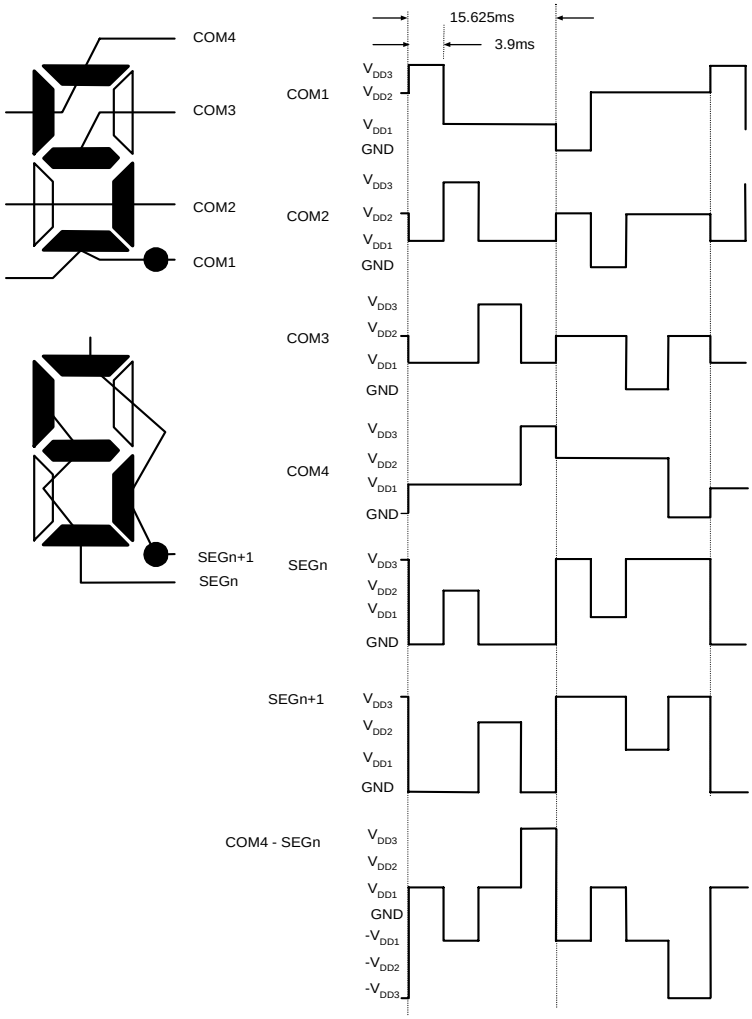
(3) Segments 5 - 26

Address	Bit 3	Bit 2	Bit 1	Bit 0	Address	Bit 3	Bit 2	Bit 1	Bit 0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
304H	SEG5	SEG5	SEG5	SEG5	30FH	SEG16	SEG16	SEG16	SEG16
305H	SEG6	SEG6	SEG6	SEG6	310H	SEG17	SEG17	SEG17	SEG17
306H	SEG7	SEG7	SEG7	SEG7	311H	SEG18	SEG18	SEG18	SEG18
307H	SEG8	SEG8	SEG8	SEG8	312H	SEG19	SEG19	SEG19	SEG19
308H	SEG9	SEG9	SEG9	SEG9	313H	SEG20	SEG20	SEG20	SEG20
309H	SEG10	SEG10	SEG10	SEG10	314H	SEG21	SEG21	SEG21	SEG21
30AH	SEG11	SEG11	SEG11	SEG11	315H	SEG22	SEG22	SEG22	SEG22
30BH	SEG12	SEG12	SEG12	SEG12	316H	SEG23	SEG23	SEG23	SEG23
30CH	SEG13	SEG13	SEG13	SEG13	317H	SEG24	SEG24	SEG24	SEG24
30DH	SEG14	SEG14	SEG14	SEG14	318H	SEG25	SEG25	SEG25	SEG25
30EH	SEG15	SEG15	SEG15	SEG15	319H	SEG26	SEG26	SEG26	SEG26

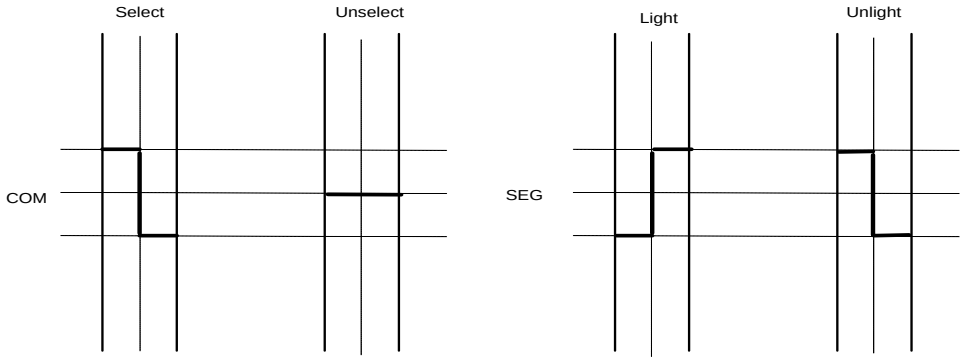
LCD Timing Waveforms

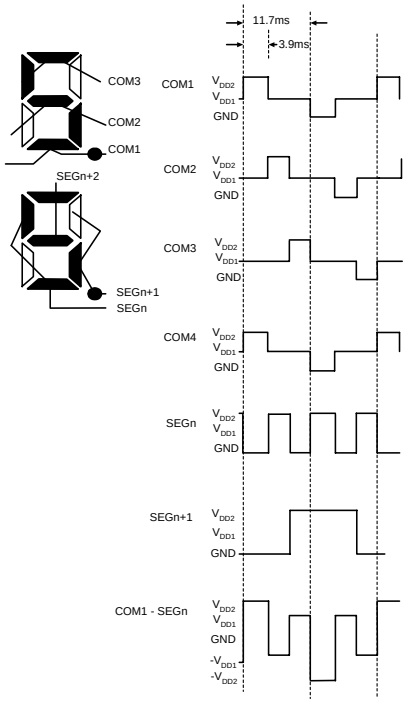
1/4 duty, 1/3 bias LCD waveform





1/3 duty, 1/2 bias LCD waveform



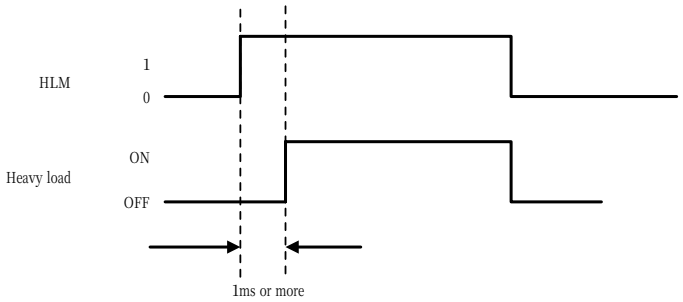


9. HEAVY LOAD Mode(HLM) When set , more current will be provide to oscillator circuit to avoid supply current drop that usually takes place in heavy output load. Perform heavy load driving only after setting up at least 1ms wait time through the software, after switching to the heavy load mode.

This mode is designed for the 32KHz crystal oscillator, so that the oscillation can be maintained in a noisy power environment. The power might drop suddenly when the ALARM is driving a speaker. The HLM is designed to control this power variation. The consumption of power will increase during the use of the HLM mode, but it will not affect the RC oscillator.

Note: The HLM needs about 5 instruction cycles to set-up the oscillation for 32.768KHz crystal oscillator.

HLM waveform



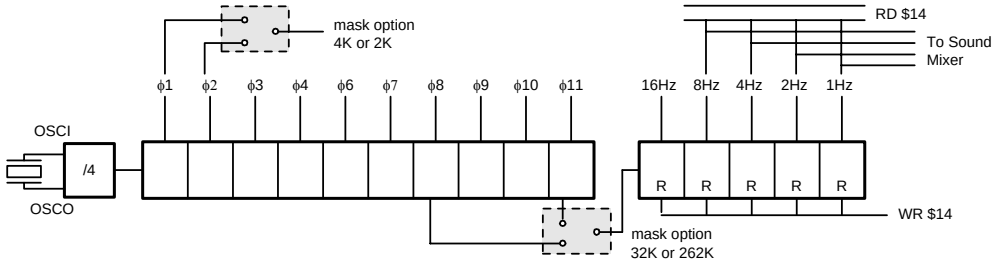
10. ALARM envelope control

System Register $14:

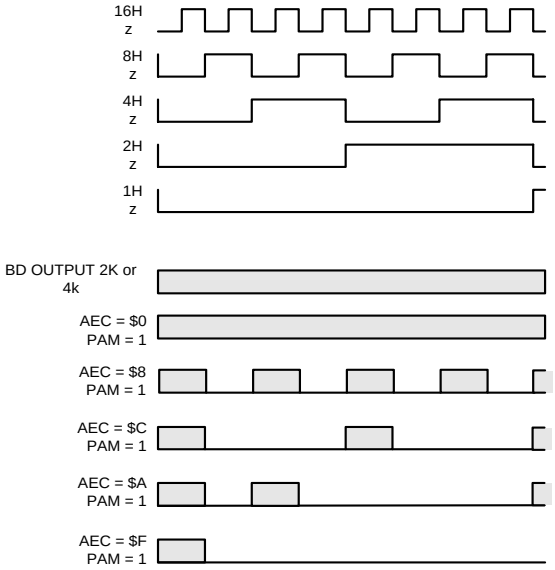
	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power On
$14	AEC3	AEC2	AEC1	AEC0	R/W	ALARM envelope control	
	0	0	0	0		DC envelope	Yes
	X	X	X	1		1Hz envelope	
	X	X	1	X		2Hz envelope	
	X	1	X	X		4Hz envelope	
	1	X	X	X		8Hz envelope	

Default carrier frequency is 4KHz. Can be selected to 2KHz by code option.
WRITE mode: control the envelop selection.
READ mode can read out current envelope wave forms.

Below is the ALARM functional block equivalent circuit diagram. To activate the ALARM function, first switch the PAM to ALARM OUTPUT mode. After setting PAM equal to 1, then set the proper envelope. When the data writes into AEC, the envelope counter will be synchronized at the same time. The programmer can read back the envelope from AEC register and make any pattern changes needed by programmer. The Read operation will not affect the alarm output waveform.



The programming alarm waveform is shown below (32.768KHz crystal or 262K RC):

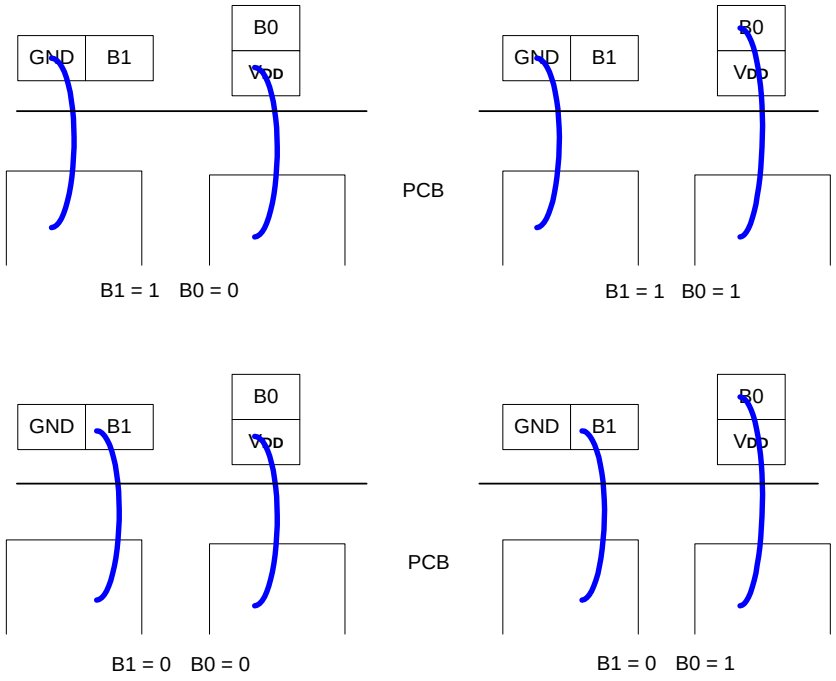


11. Option

Bonding Option

System Register 0DH (Bonding option)

	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks	Power-on
$0DH	-	-	B1	B0	R	Bit0: Bonding option 0, internal weak drive Bit1: Bonding option 1, internal weak drive	Pull low Pull high
	X	X	1	0			Yes
	X	X	0	0		B1 bond to GND	
	X	X	1	1		B0 bond to V_{DD}	
	X	X	0	1		B1 bond to GND and B0 bond to V_{DD}	



SH6611A Bonding Option

Up to 4 different bonding options are possible for the user's needs. The chip's program has 4 different program flows that will vary depending on which bonding option is used. The readable contents of B1 and B0 will differ depending on bonding.

12. HALT and STOP mode

After the execution of HALT instruction, SH6611A will enter halt mode.
In halt mode, CPU will stop operating. But peripheral circuit (Timer, Alarm and LCD) will keep operating.
After the execution of STOP instruction, SH6611A will enter stop mode.
In stop mode, the whole chip (including oscillator) will stop operating.
In HALT mode, SH6611A can be waked up if any interrupt occurs.
In STOP mode, SH6611A can be waked up if port interrupt occurs or external interrupt occurs.

Instructions

All instructions are one cycle and one word instructions. The characteristics is memory oriented operation.

Arithmetic and Logical Instruction

Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X(,B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X(,B)	00000 1bbb xxx xxxx	AC,Mx ← Mx + AC + CY	CY
ADD X(,B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X(,B)	00001 1bbb xxx xxxx	AC,Mx ← Mx + AC	CY
SBC X(,B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X(,B)	00010 1bbb xxx xxxx	AC,Mx ← Mx + -AC + CY	CY
SUB X(,B)	00011 0bbb xxx xxxx	AC ← Mx + -AC + 1	CY
SUBM X(,B)	00011 1bbb xxx xxxx	AC,Mx ← Mx + -AC +1	CY
EOR X(,B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X(,B)	00100 1bbb xxx xxxx	AC,Mx ← Mx ⊕ AC	
OR X(,B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X(,B)	00101 1bbb xxx xxxx	AC,Mx ← Mx | AC	
AND X(,B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X(,B)	00110 1bbb xxx xxxx	AC,Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3]; AC[0] → CY; AC shift right one bit	CY

Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X,I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X,I	01001 iiii xxx xxxx	AC,Mx ← Mx + I	CY
SBI X,I	01010 iiii xxx xxxx	AC ← Mx + -I +1	CY
SBIM X,I	01011 iiii xxx xxxx	AC,Mx ← Mx + -I + 1	CY
EORIM X,I	01100 iiii xxx xxxx	AC,Mx ← Mx ⊕ I	
ORIM X,I	01101 iiii xxx xxxx	AC,Mx ← Mx | I	
ANDIM X,I	01110 iiii xxx xxxx	AC,Mx ← Mx & I	

* In the assembler ASM66 V1.0, EORIM memonic is EORI. However, EORI has the same operation identical with EORIM. Same for the ORIM with respect to ORI, and ANDIM with respect to ANDI.

Decimal Adjust

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC;Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC;Mx ← Decimal adjust for sub.	CY

Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X(,B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X(,B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X,I	01111 iiii xxx xxxx	AC,Mx ← I	

Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X if AC=0	
BNZ X	10000 xxxx xxx xxxx	PC ← X if AC≠0	
BC X	10011 xxxx xxx xxxx	PC ← X if CY=1	
BNC X	10001 xxxx xxx xxxx	PC ← X if CY≠1	
BA0 X	10100 xxxx xxx xxxx	PC ← X if AC(0)=1	
BA1 X	10101 xxxx xxx xxxx	PC ← X if AC(1)=1	
BA2 X	10110 xxxx xxx xxxx	PC ← X if AC(2)=1	
BA3 X	10111 xxxx xxx xxxx	PC ← X if AC(3)=1	
CALL X	11000 xxxx xxx xxxx	ST ← CY; PC +1 PC ← X(Not include p)	
RTNW H;L	11010 000h hhh llll	PC ←ST; TBR ← hhhh; A ← llll	
RTNI	11010 1000 000 0000	CY;PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X(Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (A)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank=000
p	ROM page =0		
ST	Stack	TBR	Table Branch Register

***Absolute Maximum Ratings**

DC Supply Voltage . . . . . -0.3V to +5.5V

Input Voltage. . . . . -0.3V to V_{DD}+0.3V

Operating Ambient Temperature. . . -10°C to +70°C

Storage Temperature . . . . . -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	2.2	3	3.4	V	
Operating Current	I_{OP}	-	5	10	μA	All output pins unload execute NOP instruction
Standby Current	I_{SB1}	-	1.5	2.5	μA	All output pins unload (HALT mode) exclude LCD current
Standby Current	I_{SB2}	-	-	1	μA	All output pins unload (STOP mode) LCD off, no current
Input High Voltage	V_{IH}	0.7 ×V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	GND - 0.3	-	0.2 ×V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Output High Voltage	V_{OH1}	2.3	-	-	V	PORTA, PORTB, PORTC, PORTD (I_{OH} = 15μA)
Output Low Voltage	V_{OL1}	-	-	0.2	V	PORTA, PORTB, PORTC, PORTD (I_{OL}= 300μA)
Output High Voltage	V_{OH2}	2.1	-	-	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OH} = 2mA
Output Low Voltage	V_{OL2}	-	-	0.9	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OL} = 2mA
Output High Voltage	V_{OH3}	2.8	-	-	V	SEGx, I_{OH} = 3μA , SEG1 - 4 to be output port (for reference only)
Output Low Voltage	V_{OL3}	-	-	0.2	V	SEGx, I_{OL} = 3μA , SEG1 - 4 to be output port (for reference only)
Output High Voltage	V_{OH4}	2.8	-	-	V	COMx, I_{OH} = 8μA (for reference only)
Output Low Voltage	V_{OL4}	-	-	0.2	V	COMx, I_{OL} = 8μA (for reference only)
Pull high Resistor	Rp	-	180	-	KΩ	Pull high resistor for RESET pin
LCD Lighting Current	I_{LCD1}	-	6	-	μA	HALT mode (low driving capability)
LCD Lighting Current	I_{LCD2}	-	12	-	μA	HALT mode (normal driving capability)
LCD Lighting Current	I_{LCD3}	-	20	-	μA	HALT mode (high driving capability)
LCD Lighting Current	I_{LCD4}	-	26	-	μA	HALT mode (higher driving capability)

DC Electrical Characteristics (V_{DD} = 5.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V_{DD}	4.5	5.0	5.4	V	
Operating Current	I_{OP}	-	15	30	μA	All output pins unload execute NOP instruction
Standby Current	I_{SB1}	-	4.5	7.5	μA	All output pins unload (HALT mode) exclude LCD current
Standby Current	I_{SB2}	-	-	1	μA	All output pins unload (STOP mode) LCD off, no current
Input High Voltage	V_{IH}	0.7 ×V_{DD}	-	V_{DD} + 0.3	V	PORTA, PORTB, PORTC, PORTD
Input Low Voltage	V_{IL}	GND - 0.3	-	0.2 ×V_{DD}	V	PORTA, PORTB, PORTC, PORTD
Output High Voltage	V_{OH1}	4.3	-	-	V	PORTA, PORTB, PORTC, PORTD (I_{OH} = 15μA)
Output Low Voltage	V_{OL1}	-	-	0.3	V	PORTA, PORTB, PORTC, PORTD (I_{OL}= 300μA)
Output High Voltage	V_{OH2}	4.1	-	-	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OH} = 2mA
Output Low Voltage	V_{OL2}	-	-	1.0	V	BD/$\overline{BD}$ (set PA.1and PA.2 to be ALARM output), I_{OL} = 2mA
Output High Voltage	V_{OH3}	4.8	-	-	V	SEGx, I_{OH} = 3μA , SEG1 - 4 to be output port (for reference only)
Output Low Voltage	V_{OL3}	-	-	0.3	V	SEGx, I_{OL} = 3μA , SEG1 - 4 to be output port (for reference only)
Output High Voltage	V_{OH4}	4.8	-	-	V	COMx, I_{OH} = 8μA (for reference only)
Output Low Voltage	V_{OL4}	-	-	0.3	V	COMx, I_{OL} = 8μA (for reference only)
Pull high Resistor	Rp	-	90	-	KΩ	Pull high resistor for RESET pin
LCD Lighting Current	I_{LCD1}	-	10	-	μA	HALT mode (low driving capability)
LCD Lighting Current	I_{LCD2}	-	20	-	μA	HALT mode (normal driving capability)
LCD Lighting Current	I_{LCD3}	-	34	-	μA	HALT mode (high driving capability)
LCD Lighting Current	I_{LCD4}	-	44	-	μA	HALT mode (higher driving capability)

Note:

1. Operation frequency vs. I_{SB1}
   I_{SB1x} = (Frequency/32.768KHz) ×I_{SB1}×0.8
2. Operation frequency vs. I_{op}
   I_{opx} = (Frequency/32.768KHz) × I_{op}×0.8
3. HLM vs. I_{op}, I_{sb1} and I_{sb2}
   If HLM = 1, I_{opx} = I_{op}×2, I_{SB1x} = I_{SB1}×2, I_{SB2x} = I_{SB1}×2

GND = 0V, TA = 25°C, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage	V_{LVR}	-	1.9	-	V	LVR enable

Note:
This function of LVR is always enable, user can't disable it.

AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A = 25°C, F_{OSC} = 32.768KHz , unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{STT}	-	2	5	s	
Halt Time	t_{HTT}	-	0	-	s	I_{DD} reduces to I_{sb1} after instruction executing
Stop Time	t_{SPT}	-	0	-	s	I_{DD} reduces to I_{sb2} after instruction executing
Frequency Stability	$\Delta f / f$	-	-	1	ppm	[f(3.0)- f(2.4)]/ f(3.0), crystal oscillator (for reference only)
Frequency Variation	$\Delta f / f$	-	-	10	ppm	C1 = 5 - 25P (for reference only)

AC Characteristics (V_{DD} = 3.0V, GND = 0V, T_A= 25°C, F_{OSC}= 262KHz, unless otherwise specified)

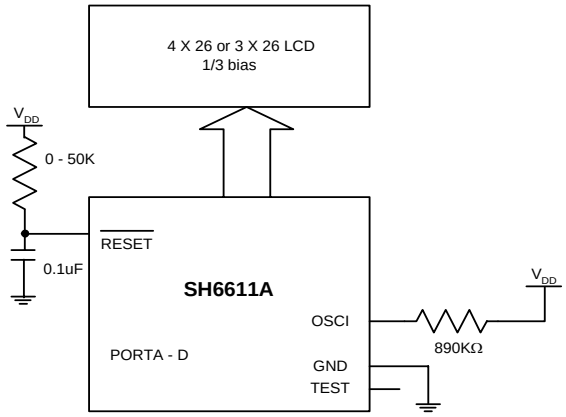
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Oscillation Start Time	t_{STT}	-	-	2	ms	
Halt Time	t_{HTT}	-	0	-	s	I_{DD} reduces to I_{sb1} after instruction executing
Stop Time	t_{SPT}	-	0	-	s	I_{DD} reduces to I_{sb3} after instruction executing
Frequency Stability	$\lvert\Delta f\rvert / f$	-	-	10	%	$\lvert f$(3.0)- f(2.4)$\rvert$ / f(3.0), RC oscillator (for reference only)
Frequency Variation	$\lvert\Delta f\rvert / f$	-	-	15	%	variation caused by process variation (for reference only)

Application Circuits (for reference only)

SH6611A chip substrate connects to system ground.

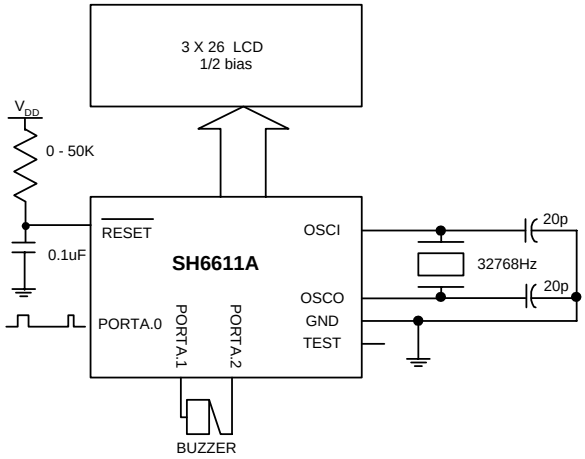
AP1

OSC : RC: 262K (code option)
LCD Panel: 1/4 duty, 1/3 bias; (S/W select 1/4 duty, auto 1/3 bias)
LCD Panel: 1/3 duty, 1/3 bias; (S/W select 1/4 duty, auto 1/3 bias; ignore duty 4 segments)
PORTA - D : I/O



AP2

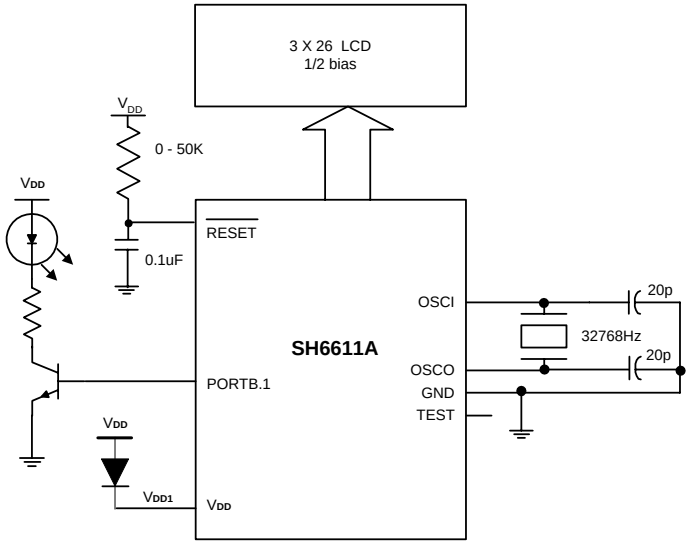
OSC: 32.768KHz crystal (code option)
LCD: 1/3 duty, 1/2 bias
PORTB - D: I/O
PORTA.0: external interrupt
PORTA.1, PORTA.2: ALARM output (carrier frequency: 2KHz or 4KHz code option) (code option)



Application Circuits (continued)

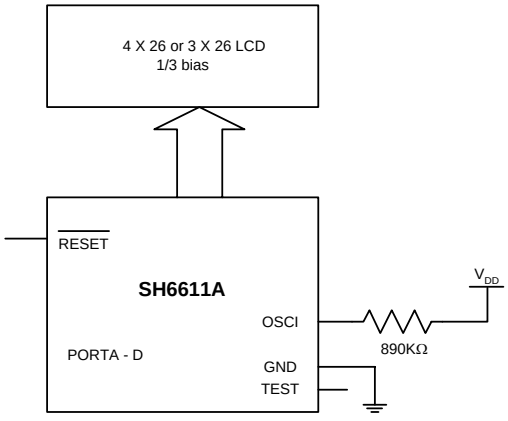
AP3

OSC: 32.768KHz
LCD: 1/3 duty, 1/2 bias
PORTB.1 = Output
When V_{DD} is higher than V_{LCD}, reducing V_{DD} to V_{DD1} can regulate the voltage.

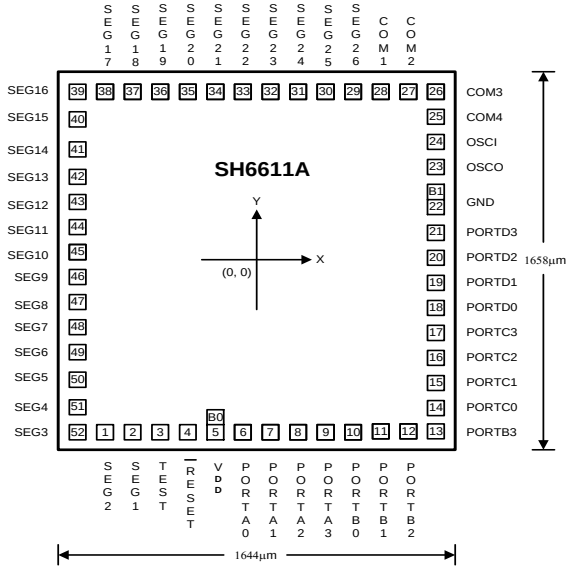


AP4

OSC : RC: 262K (code option)
LCD Panel: 1/4 duty, 1/3 bias; (S/W select 1/4 duty, auto 1/3 bias)
LCD Panel: 1/3 duty, 1/3 bias; (S/W select 1/4 duty, auto 1/3 bias; ignore duty 4 segments)
PORTA - D : I/O
Use Internal pull high resistor for RESET pin (Code Option)



Bonding Diagram



* Substrate connects to GND.
The bonding wire with diameter of 1.0mil is recommended.

unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	SEG2	-630	-758.8	26	COM3	752	758.8
2	SEG1	-510	-758.8	27	COM2	630	758.8
3	TEST	-395	-758.8	28	COM1	510	758.8
4	$\overline{\text{RESET}}$	-280	-758.8	29	SEG26	390	758.8
5	VDD	-165	-758.8	30	SEG25	275	758.8
	B0	-152.4	-662.95	31	SEG24	165	758.8
6	PORTA0	-50	-758.8	32	SEG23	55	758.8
7	PORTA1	60	-758.8	33	SEG22	-55	758.8
8	PORTA2	170	-758.8	34	SEG21	-165	758.8
9	PORTA3	280	-758.8	35	SEG20	-275	758.8
10	PORTB0	390.1	-758.8	36	SEG19	-390	758.8
11	PORTB1	505	-758.8	37	SEG18	-510	758.8
12	PORTB2	625	-758.8	38	SEG17	-630	758.8
13	PORTB3	752	-758.8	39	SEG16	-752	758.8
14	PORTC0	752	-638.8	40	SEG15	-752	633.3
15	PORTC1	752	-526.8	41	SEG14	-752	513.3
16	PORTC2	752	-416.8	42	SEG13	-752	393.3
17	PORTC3	752	-308.8	43	SEG12	-752	278.3
18	PORTD0	752	-200.8	44	SEG11	-752	170.3
19	PORTD1	752	-92.8	45	SEG10	-752	62.3
20	PORTD2	752	15.2	46	SEG9	-752	-45.7
21	PORTD3	752	123.2	47	SEG8	-752	-153.7
22	GND	752	233.65	48	SEG7	-752	-263.7
	B1	752	316.15	49	SEG6	-752	-373.7
23	OSCO	752	413.8	50	SEG5	-752	-488.7
24	OSCI	752	523.8	51	SEG4	-752	-623.8
25	COM4	752	638.8	52	SEG3	-752	-758.8

Notice:

The Pad Locations of SH6611A are different from the SH6611. Please pay attention.

Ordering Information

Part No.	Package
SH6611AH	CHIP FORM

Data sheet Version History

SH6611A Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Feb.2004