DQ8051

Revolutionary Quad-Pipelined Ultra High Performance 8-bit Microcontroller ver 6.00

OVERVIEW

DQ8051 is a **ultra high performance, speed optimized** soft core of a single-chip 8-bit embedded controller dedicated for operation with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern about **performance to power consumption** ratio. This ratio is extended by an advanced power management unit **PMU**.

DQ8051 soft core is 100% binary-compatible with the industry standard 8051 8-bit microcontroller. DQ8051 has build-in configurable **DoCD-JTAG on chip debugger** supporting Keil µVision development platform and standalone DoCD debug software. Dhrystone 2.1 benchmark program runs from **19.69 to 26.62** times faster than the original 80C51 at the same frequency. This performance can also be exploited to great advantage in **low power** applications where the core can be clocked over ten times more slowly than the original implementation for no performance penalty.

DQ8051 is **fully customizable**, which means it is delivered in the exact configuration to meet users' requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- 100% software compatible with industry standard 8051
- **Quad-Pipelined** architecture enables to execute **26.62** times faster than the original 80C51 at the same frequency
- Up to 25.053 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster addition
- 2 Data Pointers (DPTR) for faster memory blocks copying
  - *Advanced INC & DEC modes*
  - *Auto-switch of current DPTR*
- Up to 256 bytes of internal (on-chip) Data Memory - IDM
- Up to 64K bytes of Program Memory
- Up to 16M bytes of external (off-chip) Data Memory - XDM
  - *Synchronous interface for up to 64K bytes of (on-chip) fast external Data Memory - (SXDM)*
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory

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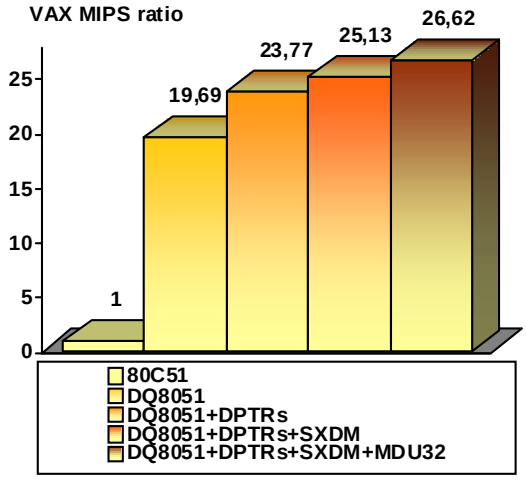
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with no internal tri-states
- Scan test ready

PERFORMANCE

One of the most important performance parameter is real application speed improvement comparing to well known 80C51 architecture. The Dhrystone Benchmark Version 2.1 was used to measure 80C51 and DQ8051 core performance. The following table gives a survey about the DQ8051 performance in terms of Dhrystone VAX MIPS per 1 MHz and its improvement comparing to 80C51.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DQ8051	0,18527	19,69
DQ8051+DPTRs	0,22369	23,77
DQ8051+DPTRs+SXDM	0,23650	25,13
DQ8051+DPTRs+SXDM+MDU32	0,25053	26,62

Core performance in terms of DMIPS per MHz



The following tables give a survey about the DQ8051 core area in ASICs Devices (CPU features and peripherals have been included):

Device	Speed	Min area	F_{max}
0,35 um	typical	10500 gates	70 MHz
0.25 um	typical	11000 gates	125 MHz
0.18 um	typical	10500 gates	180 MHz
0.13 um	typical	10700 gates	260 MHz
0.09 um	typical	9900 gates	430 MHz

DQ8051 core area and performance in ASIC devices. Results given for working system with two DPTRs and connected 256B IDM, 8kB CODE and 2kB SXDM memories.

Area utilized by the each unit of DQ8051 core in vendor specific technologies is summarized in table below.

Component	Area [Gates]
CPU*	7250
DPTR1 register	400
DPTR0 decrement	50
DPTR1 decrement	50
DPTR's auto-switch and auto-update	150
SXDM	75
Interrupt Controller	150
Power Management Unit	75
I/O ports	200
Timers	700
UART0	800
Total area	9900

Core components area utilization

*CPU – consisted of ALU, Opcode Decoder, Control Unit, User SFRs i**nterface,** IDM interface, XDM interface and Code Memory interface.

PERIPHERALS

- DoCD™ debug unit
  - *Processor execution control*
    - *Run, Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Code execution breakpoints*
    - *two real-time PC breakpoint*
    - *unlimited number of real-time OPCODE breakpoints*
  - *Hardware execution watch-points at*
    - *Internal (direct) Data Memory*

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  - *Special Function Registers (SFRs)*
  - *External Data Memory*

- *Hardware watch-points activated at a certain*
  - *address by any write into memory*
  - *address by any read from memory*
  - *address by write into memory a required data*
  - *address by read from memory a required data*

- *Automatic adjustment of debug data transfer speed rate between HAD and Silicon*
- *JTAG Communication interface*

- Power Management Unit
  - *Power management mode*
  - *Switchback feature*
  - *Stop mode*
- Extended Interrupt Controller
  - *2 priority levels*
  - *2 external interrupt sources*
  - *3 interrupt sources from peripherals*
- Four 8-bit I/O Ports
  - *Bit addressable data direction for each line*
  - *Read/write of single line and 8-bit group*
- Two 16-bit timer/counters
  - *Timers clocked by internal source*
  - *Auto reload 8-bit timers*
  - *Externally gated event counters*
- Full-duplex serial port
  - *Synchronous mode, fixed baud rate*
  - *8-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, variable baud rate*

CONFIGURATION

The following parameters of the DQ8051 core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

• Second Data Pointer (DPTR1)	- used - unused
• DPTR0 decrement	- used - unused
• DPTR1 decrement	- used - unused
• Data Pointers auto-switch	- used - unused
• Data Pointers auto-update	- used - unused
• Interrupts	- subroutines location
• Power Management Mode	- used - unused
• Stop mode	- used - unused
• Peripherals	- used - unused
• Synchronous XDM	- - size
• DoCD™ debug unit	- used - unused

Besides mentioned above parameters all available peripherals and external interrupts can be excluded from the core by changing appropriate constants in package file.

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DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - FPGA netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

DESIGN FEATURES

PROGRAM MEMORY:

The DQ8051 soft core is dedicated for operation with Internal or External Program Memory. Program Memory can be implemented as ROM, RAM or FLASH.

INTERNAL DATA MEMORY:

The DQ8051 can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as synchronous RAM.

EXTERNAL DATA MEMORY:

The DQ8051 soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

SYNCHRONOUS XDM:

The DQ8051 soft core can address up to 64 kB of fast on-chip Synchronous External Data Memory. All reads and writes are executed in one clock cycle.

USER SPECIAL FUNCTION REGISTERS:

Up to 60 External (user) Special Function Registers (ESFRs) may be added to the DQ8051 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

WAIT STATES SUPPORT:

The DQ8051 soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

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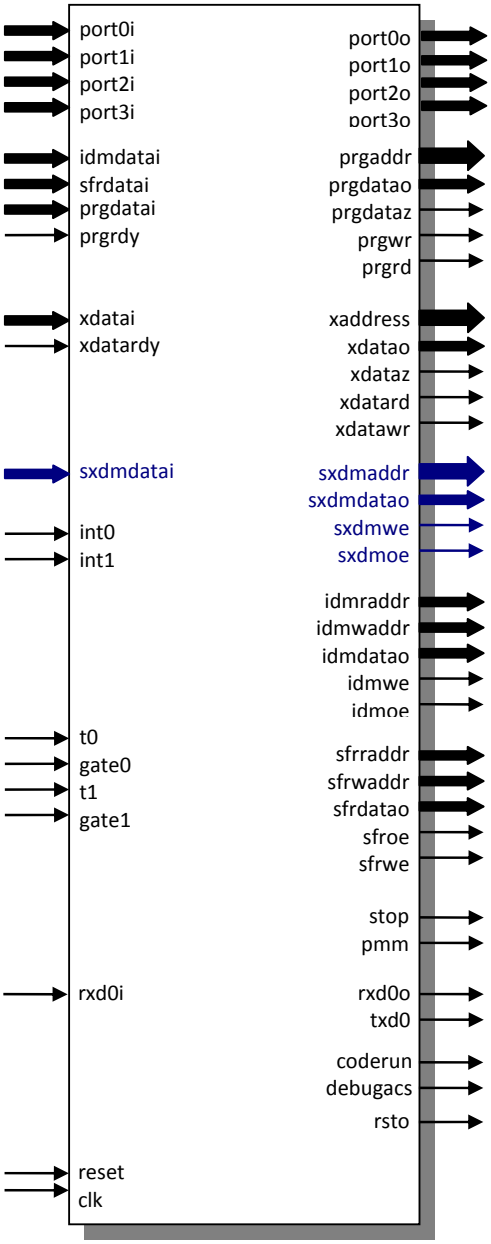
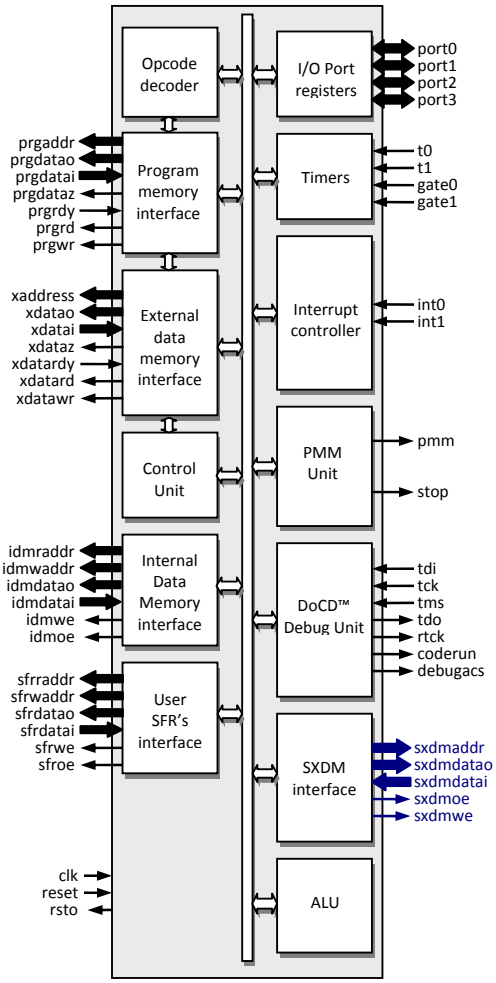
SYMBOL



BLOCK DIAGRAM



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PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset
port0i	input	Port 0 input
port1i	input	Port 1 input
port2i	input	Port 2 input
port3i	input	Port 3 input
prgdatai	input	Data bus from program memory
prgrdy	input	Program memory ready
sxdmdatai	input	Data bus from synchronous external data memory (SXDM)
xdatai	input	Data bus from external memories
xdatardy	input	External data memory ready
idmdatai	input	Data bus from internal data memory
sfrdatai	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
t0	input	Timer 0 input
t1	input	Timer 1 input
gate0	input	Timer 0 gate input
gate1	input	Timer 1 gate input
rxdi0	input	Serial receiver input 0
tdi	input	DoCD™ TAP data input
tck	input	DoCD™ TAP clock input
tms	input	DoCD™ TAP mode select input
rsto	output	Reset output
port0o	output	Port 0 output
port1o	output	Port 1 output
port2o	output	Port 2 output
port3o	output	Port 3 output
prgaddr	output	Internal program memory address bus
prgdatao	output	Data bus for internal program memory
prgdataz	output	Turn prgdata bus into 'Z' state
prgwr	output	Program memory write
prgrd	output	Program memory read
sxdmaddr	output	Synchronous XDATA memory address bus
sxdmdatao	output	Data bus for Synchronous XDATA memory
sxdmoe	output	Synchronous XDATA memory read
sxdmwe	output	Synchronous XDATA memory write
xaddress	output	Address bus for external data memory
xdatao	output	Data bus for external data memory
xdataz	output	Turn xdata bus into 'Z' state
xdatard	output	External data memory read
xdatawr	output	External data memory write
idmraddr	output	IDM read address bus
idmwaddr	output	IDM write address bus
idmdatao	output	Data bus for internal data memory
idmoe	output	Internal data memory output enable
idmwe	output	Internal data memory write enable
sfrraddr	output	Read address bus for user SFR's
sfrwaddr	output	Write address bus for user SFR's
sfrdatao	output	Data bus for user SFR's
sfroe	output	User SFR's read enable
sfrwe	output	User SFR's write enable
tdo	output	DoCD™ TAP data output
rtck	output	DoCD™ return clock line
debugacs	output	DoCD™ accessing data
coderun	output	CPU is executing an instruction
pmm	output	Power management mode indicator
stop	output	Stop mode indicator
rxd0o	output	Serial receiver output 0
txd0	output	Serial transmitter output 0

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UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic such as arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader loading new program into RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States, and allows core to work with different speed program memories.

External Data Memory Interface - Contains memory access related registers such as Data Page High (DPH), Data Page Low (DPL) and Data Pointer eXtended (DPX) registers. It performs the External Data Memory addressing and data transfers. Memory read and write cycle length can be programmed by user. It allows core to work with different speed ram memories.

Synchronous eXternal Data Memory (SXDM) Interface – contains XDATA memory access related logic allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used to store large variables frequently accessed by CPU, improving overall performance of application.

Internal Data Memory Interface – Internal Data Memory interface controls access into the internal 256 bytes memory. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) using all direct addressing mode instructions.

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers such as Interrupt Enable (IE), Interrupt Priority (IP), and (TCON) registers.

I/O Ports – Block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, and P3.

Power Management Unit – Block contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode) to significantly reduce power consumption. Switchback feature allows UART, and interrupts to be processed in full speed mode if enabled. It is very desired when microcontroller is planned to use in portable and power critical applications.

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. Two additional pins CODERUN, DEBUGACS indicate the sate of the debugger and CPU. CODERUN is active when CPU is executing an instruction. DEBUGACS pin is active when any access is performed by DoCD™ debugger. The DoCD™ system includes **JTAG interface** and complete set of tools to communicate and work with core in real time debugging. It is built as

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scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

Timers – System timers' module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 CLK periods when appropriate timer is enabled. In the counter mode the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

UART0 – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. It works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1 or Timer 2.

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The main features of each DQ8051 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I\O Ports	Compare/Capture	Watchdog	Master I²C Bus Controller	Slave I²C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DQ8051CPU	25.1	64k	64k	64k	256	256	16M	✓	✓	✓	2	2	2	-	-	-	-	-	-	-	-	-	-
DQ8051	25.1	64k	64k	64k	256	256	16M	✓	✓	✓	5	2	2	2	1	4	-	-	-	-	-	-	-
DQ8051XP	26.6	64k	64k	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

DQ8051 family of Pipelined High Performance Microcontroller Cores

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