HM9264B Series

64 k SRAM (8-kword × 8-bit)

HITACHI

ADE-203-618C (Z)
Rev. 3.0
Nov. 1997

Description

The Hitachi HM9264B is 64k-bit static RAM organized 8-kword × 8-bit. It realizes higher performance and low power consumption by 1.5 µm CMOS process technology. The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, is available for high density mounting.

Features

- High speed
  - — Fast access time: 85/100 ns (max)
- Low power
  - — Standby: 10 µW (typ)
  - — Operation: 15 mW (typ) (f = 1 MHz)
- Single 5 V supply
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - — Three state output
- Directly TTL compatible
  - — All inputs and outputs
- Battery backup operation capability

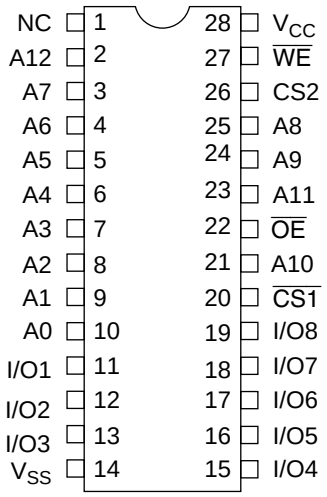
Note: HM9264B series can't be applied for Aerospace, Aircraft, Nucleus Plants, Main Flame Computers, Medical Life-support System, and Automobile Engine Control and Industrial machines. (e.g. Communication Hubs, NC, and others.)

Ordering Information

Type No.	Access time	Package
HM9264BLFP-8L HM9264BLFP-10L	85 ns 100 ns	450-mil, 28-pin plastic SOP(FP-28DA)
HM9264BLP-8L HM9264BLP-10L	85 ns 100 ns	600-mil, 28-pin plastic DIP (DP-28)

Pin Arrangement

HM9264BLFP/BLP Series

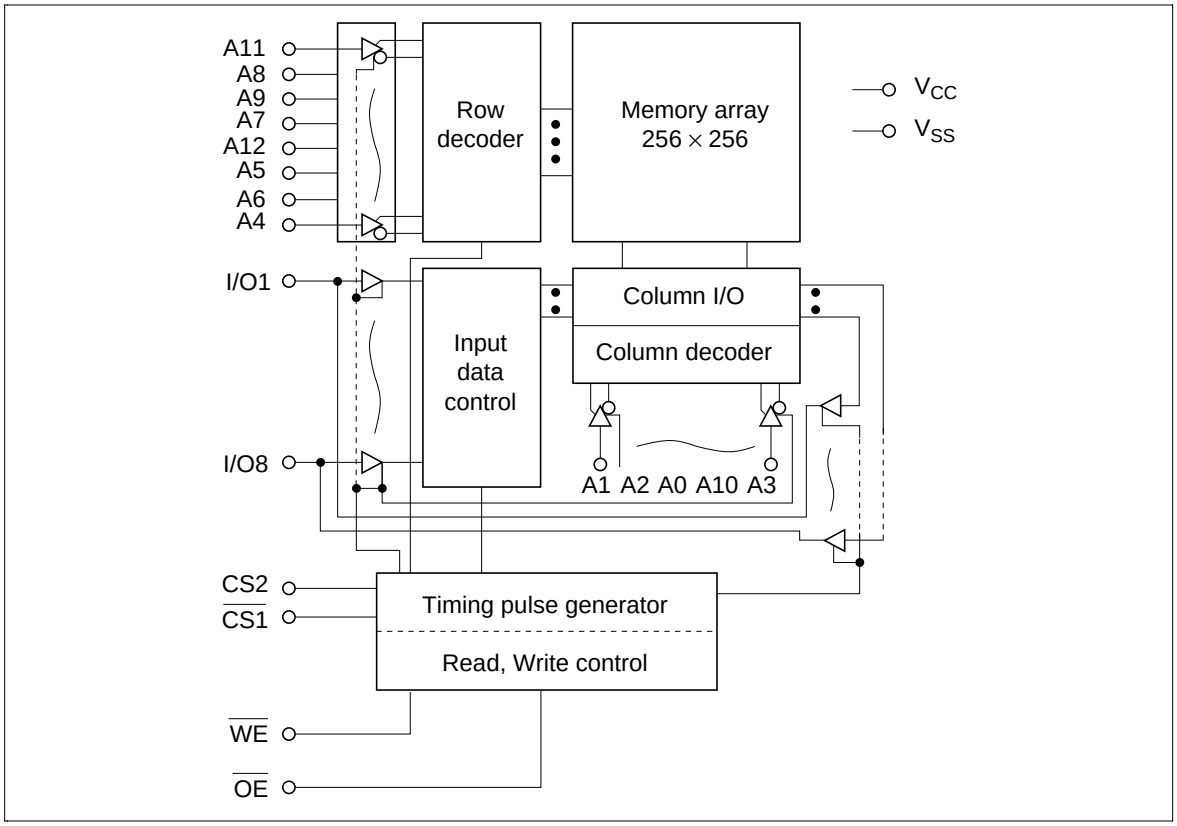


(Top view)

Pin Description

Pin name	Function
A0 to A12	Address input
I/O1 to I/O8	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
×	H	×	×	Not selected (power down)	I_{SB}, I_{SB1}	High-Z	—
×	×	L	×	Not selected (power down)	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle (1)–(3)
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage[*1]	V_{CC}	–0.5 to +7.0	V
Terminal voltage[*1]	V_T	–0.5[*2] to V_{CC} + 0.3[*3]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. Relative to V_{SS}
2. V_T min: –3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 7.0 V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3[*1]	—	0.8	V

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CCDC}	—	7	15	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA others = V_{IH}/V_{IL}
Average operating power supply current	I_{CC1}	—	30	45	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, $I_{I/O}$ = 0 mA others = V_{IH}/V_{IL}
	I_{CC2}	—	3	5	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IL}
	I_{SB1}	—	2	50	µA	$\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V, 0 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance[*1]	Cin	—	—	5	pF	Vin = 0 V
Input/output capacitance[*1]	$C_{I/O}$	—	—	7	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

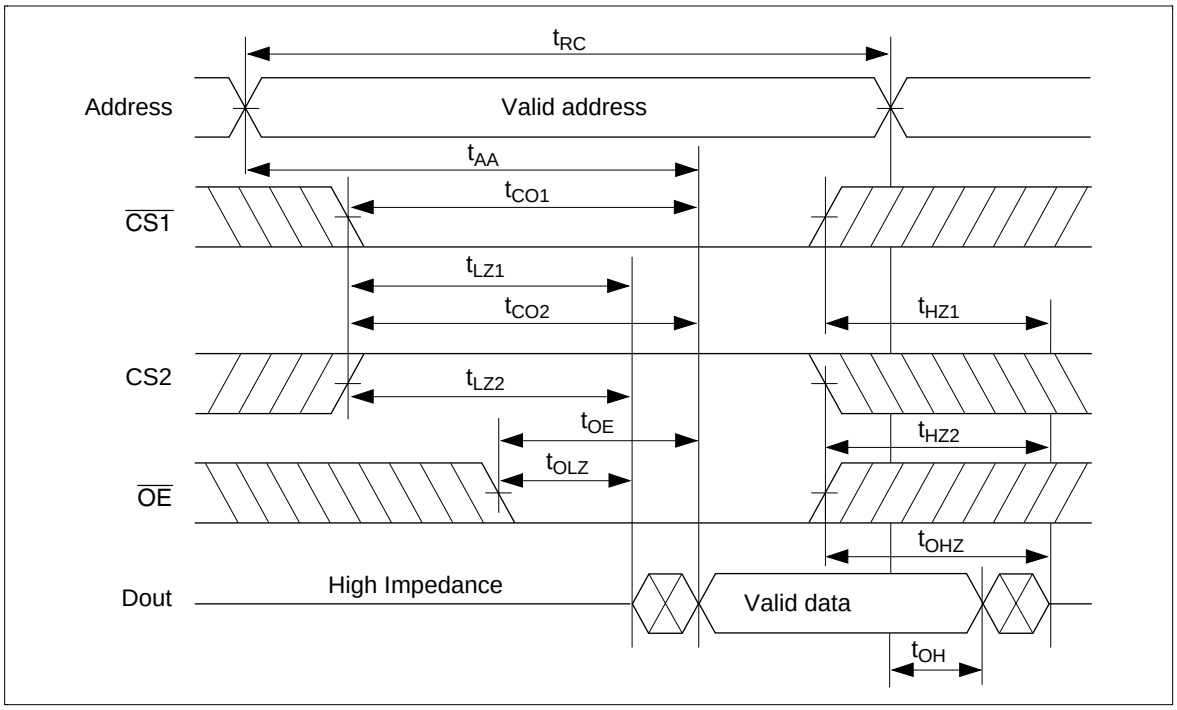
- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

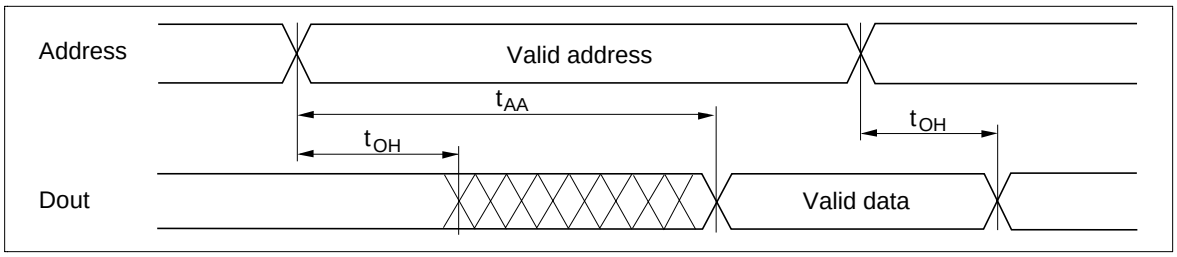
			HM9264B-8L		HM9264B-10L			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time		t_{RC}	85	—	100	—	ns	
Address access time		t_{AA}	—	85	—	100	ns	
Chip select access time	$\overline{CS1}$	t_{CO1}	—	85	—	100	ns	
	CS2	t_{CO2}	—	85	—	100	ns	
Output enable to output valid		t_{OE}	—	45	—	50	ns	
Chip selection to output in low-Z	$\overline{CS1}$	t_{LZ1}	10	—	10	—	ns	2
	CS2	t_{LZ2}	10	—	10	—	ns	2
Output enable to output in low-Z		t_{OLZ}	5	—	5	—	ns	2
Chip deselection in to output in high-Z	$\overline{CS1}$	t_{HZ1}	0	30	0	35	ns	1, 2
	CS2	t_{HZ2}	0	30	0	35	ns	1, 2
Output disable to output in high-Z		t_{OHZ}	0	30	0	35	ns	1, 2
Output hold from address change		t_{OH}	10	—	10	—	ns	

Notes: 1. t_{HZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.
3. Address must be valid prior to or simultaneously with $\overline{CS1}$ going low or CS2 going high.

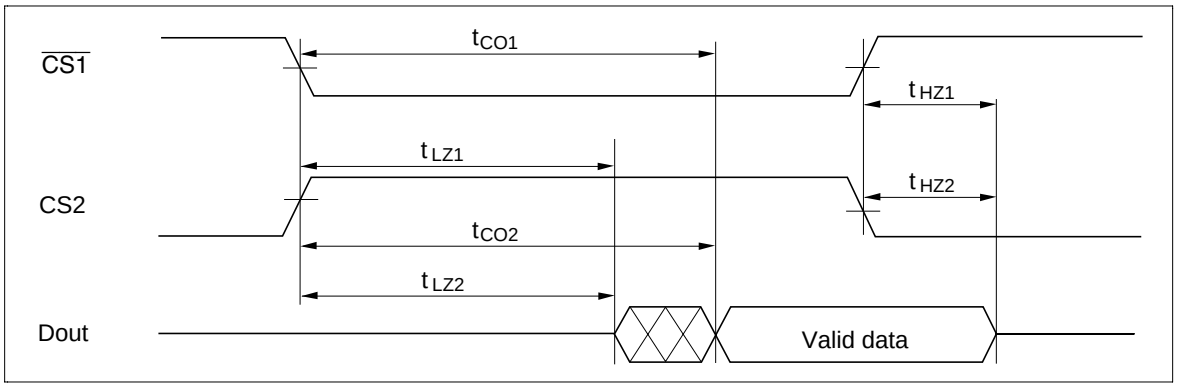
Read Timing Waveform (1) ($\overline{WE}$ = V_{IH})



Read Timing Waveform (2) ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})



Read Timing Waveform (3) ($\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL})[*3]



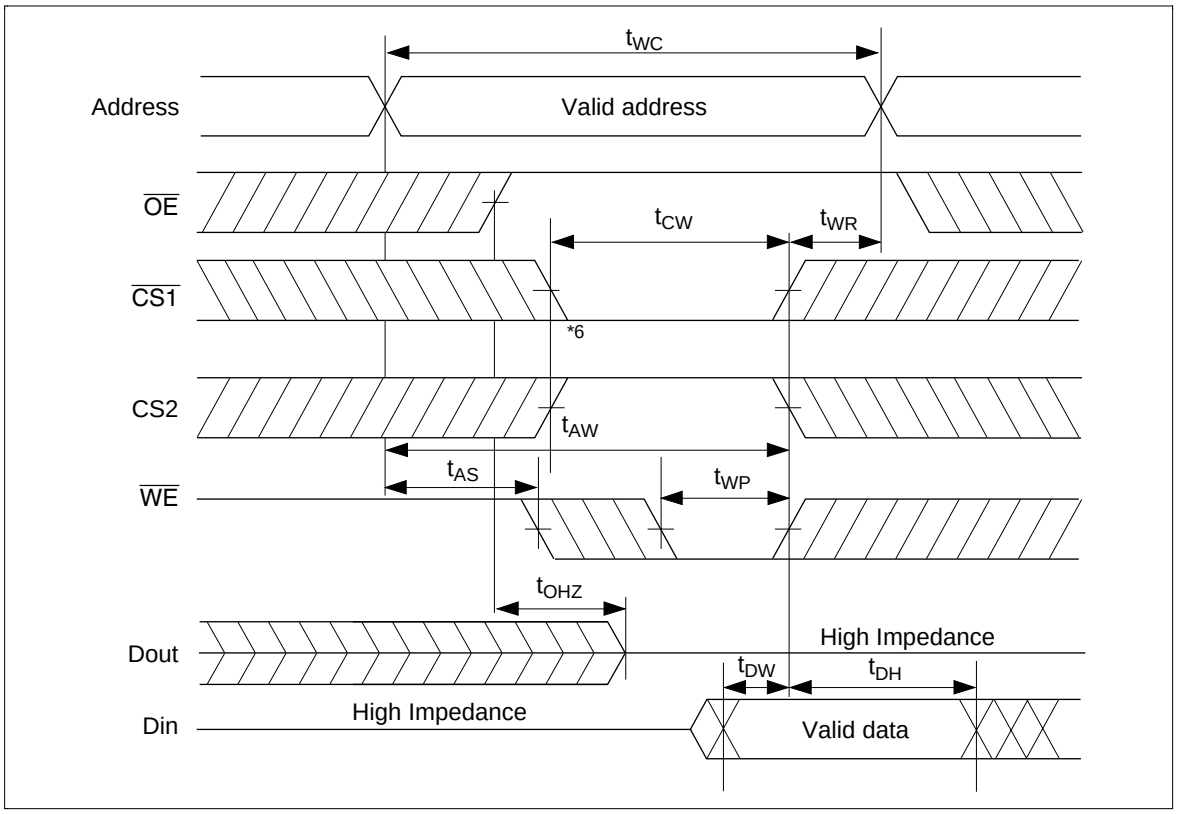
Write Cycle

Parameter	Symbol	HM9264B-8L Min	HM9264B-8L Max	HM9264B-10L Min	HM9264B-10L Max	Unit	Notes
Write cycle time	t_{WC}	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	ns	2
Address setup time	t_{AS}	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	75	—	80	—	ns	
Write pulse width	t_{WP}	55	—	60	—	ns	1, 9
Write recovery time	t_{WR}	0	—	0	—	ns	4
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	30	0	35	ns	5
Data to write time overlap	t_{DW}	40	—	40	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	5

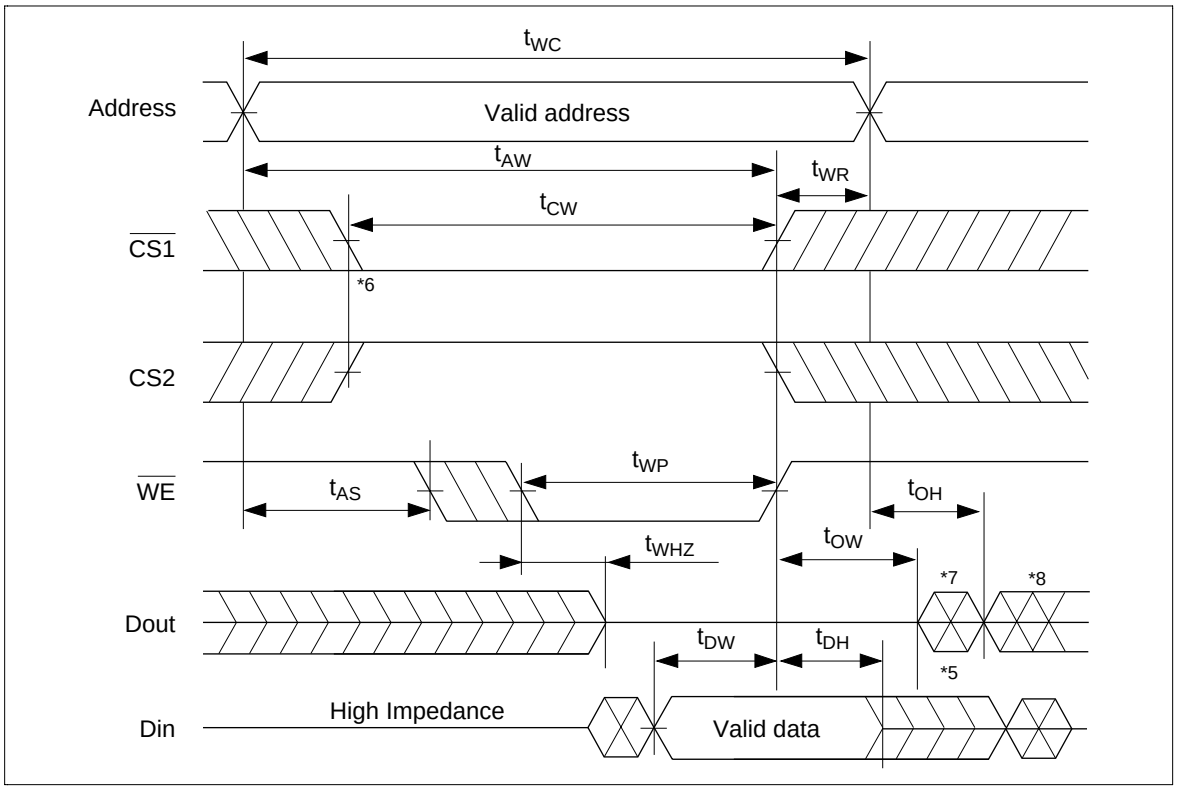
Notes:
1. A write occurs during the overlap of a low $\overline{CS1}$, and high CS2, and a high $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low,CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high CS2 going low and $\overline{WE}$ going high. Time t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low after $\overline{WE}$ goes low, the outputs remain in high impedance state.
7. Dout is the same phase of the written data in this write cycle.
8. Dout is the read data of the next address
9. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention

   $t_{WP} \geq t_{WHZ}$ max + t_{DW} min.

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed) ($\overline{OE}$ = V_{IL})

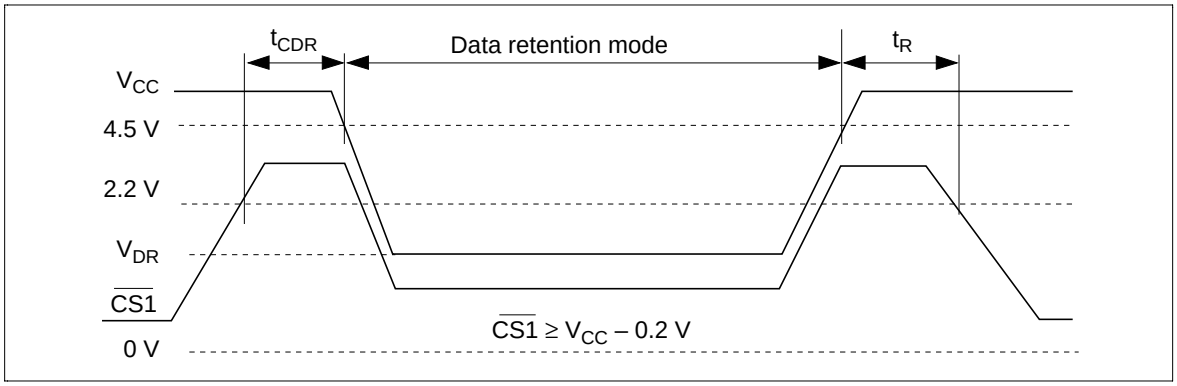


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

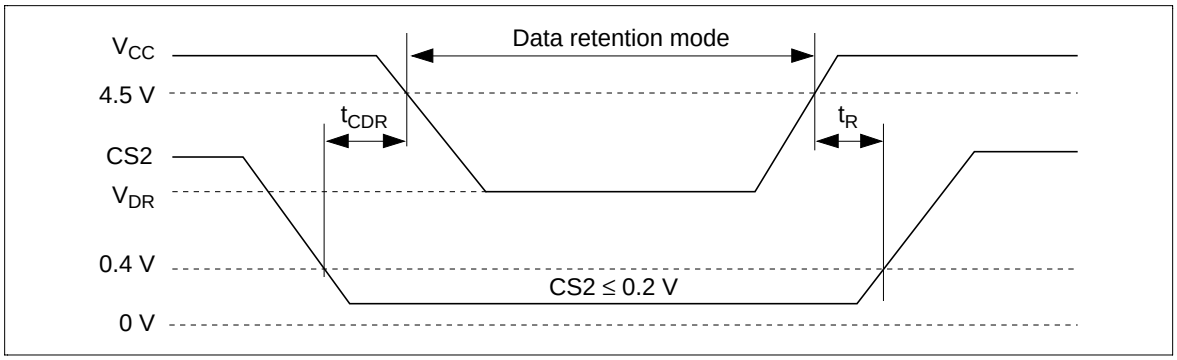
Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions[*4]
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V_{CC} –0.2 V or CS2 ≤ 0.2 V
Data retention current	I_{CCDR}	—	1[*1]	25[*2]	µA	V_{CC} = 3.0 V, 0 V ≤ Vin ≤ V_{CC} $\overline{CS1} \geq V_{CC}$ –0.2 V, CS2 ≥ V_{CC} –0.2 V or 0 V ≤ CS2 ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[*3]	—	—	ns	

Notes: 1. Reference data at Ta = 25°C.
2. 10 µA max at Ta = 0 to + 40°C.
3. t_{RC} = read cycle time.
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)

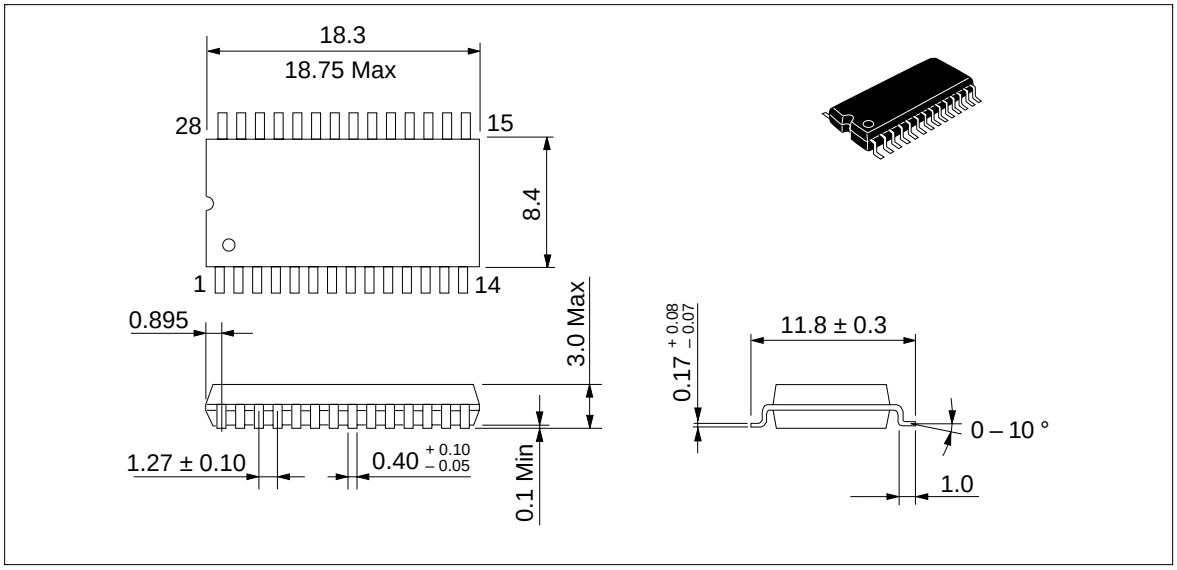


Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)

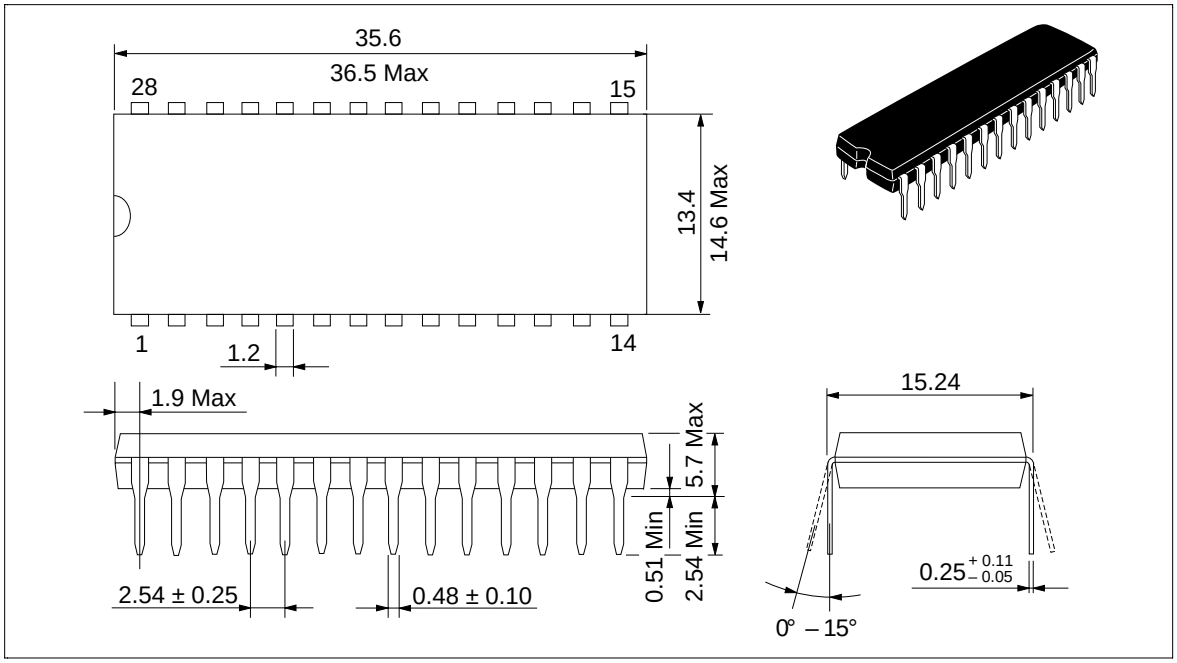


Package Dimensions

HM9264BLFP Series (FP-28DA) Unit: mm



HM9264BLP Series (DP-28) Unit: mm



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