

3V 1900MHz LINEAR AMPLIFIER MODULE

Typical Applications

- 3V CDMA US-PCS Handsets
- 3V CDMA2000/1X PCS Handsets
- Spread-Spectrum Systems

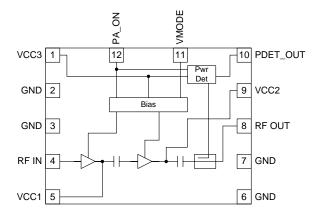
 Designed for Compatibility with Qualcomm Chipsets

Product Description

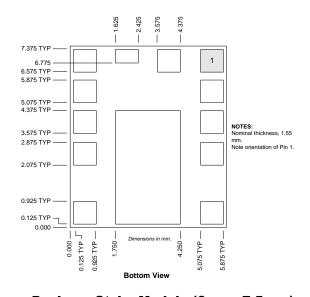
The RF3300-3 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1850MHz to 1910MHz band. The RF3300-3 has a digital control line for low power application to reduce the current drain. The device is self-contained with 50Ω input and output that is matched to obtain optimum power, efficiency, and linearity characteristics. This amplifier contains a temperature compensating bias circuit for improved performance over temperature.

Optimum Technology Matching® Applied

☐ Si BJT ☐ GaAs HBT ☐ GaAs MESFET☐ Si Bi-CMOS☐ ☐ SiGe HBT ☐ Si CMOS☐ ☐ InGaP/HBT ☐ GaN HEMT ☐ SiGe Bi-CMOS☐



Functional Block Diagram



Package Style: Module (6mmx7.5mm)

Features

- Single 3V Supply with Internal V_{REF}
- Integrated Power Detector
- 25dB Linear Gain
- 40mA Idle Current (Low Power Mode)
- Temperature Compensating Bias Circuit
- Integrated PA Enable Switch

Ordering Information

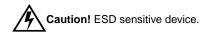
RF3300-3 3V 1900MHz Linear Amplifier Module RF3300-3 PCBA Fully Assembled Evaluation Board

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Absolute Maximum Ratings

<u> </u>						
Parameter	Rating	Unit				
Supply Voltage (RF off)	+8.0	V_{DC}				
Supply Voltage (P _{OUT} ≤28dBm)	+5.2	V_{DC}				
Control Voltage (PA_ON)	+3.6	V_{DC}				
Mode Voltage (V _{MODE})	+3.6	V_{DC}				
Input RF Power	+10	dBm				
Operating Case Temperature	-30 to +100	°C				
Storage Temperature	-30 to +150	℃				



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Parameter	Specification		Unit	Condition		
Parameter	Min.	Тур.	Max.	Unit	Condition	
High Dawes Ctata					Typical Performance at V _{CC} =3.2V,	
High Power State					PA_ON=High, T _{AMB} =25°C,	
(V _{MODE} Low)					Frequency=1850MHz to 1910MHz (unless otherwise specified)	
Frequency Range	1850		1910	MHz	(unicas otriciwise specifica)	
Linear Gain	24	25		dB		
Second Harmonic		-45		dBc		
Third Harmonic		-45		dBc		
Maximum Linear Output Power (CDMA Modulation)	28			dBm		
Total Linear Efficiency		35		%	P _{OUT} =28dBm	
Adjacent Channel Power Rejection		-47	-46	dBc	ACPR @ 1.25MHz, P _{OUT} =28dBm	
•		-61	-58	dBc	ACPR@2.25MHz, P _{OUT} =28dBm	
Input VSWR		1.5:1				
Output VSWR			10:1		No damage.	
			6:1		No oscillations. >-70dBc	
Noise Power		-141		dBm/Hz	At 80MHz offset.	
					Typical Performance at V _{CC} =3.2V,	
Low Power State					PA_ON=High, T _{AMB} =25°C,	
(V _{MODE} High)					Frequency=1850MHz to 1910MHz	
					(unless otherwise specified)	
Frequency Range	1850		1910	MHz		
Linear Gain	17	20		dB		
Second Harmonic		-45		dBc		
Third Harmonic		-45		dBc		
Maximum Linear Output Power (CDMA Modulation)	16			dBm		
Adjacent Channel Power Rejection		-49	-47	dBc	ACPR@1.25MHz, P _{OUT} =16dBm	
		-64	-59	dBc	ACPR@2.25MHz, P _{OUT} =16dBm	
Input VSWR		2:1				
Output VSWR			10:1		No damage.	
			6:1		No oscillations. >-70dBc	

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Donomotor	Specification		11!4	Condition		
Parameter	Min.	Тур.	Max.	Unit	Condition	
DC Supply					T _{AMB} =25°C	
Supply Voltage	3.2	3.7	4.2	V		
Quiescent Current		150	180	mA	V_{MODE} =Low	
		40	55	mA	V _{MODE} =High	
PA_ON Current		0.1		μΑ		
V _{MODE} Current		0.1		μΑ		
Turn On/Off Time			<40	μS	PA_ON switched from low to high, I_{CC} to	
					within 90% of the final value, P _{OUT} within	
					1 dB of the final value.	
Total Current (Power Down)		5		μΑ	PA_ON=Low	
PA_ON "Low" Voltage Range	0		0.5	V		
PA_ON "High" Voltage Range	1.7	2.7	3.6	V	Must not exceed V _{CC} .	
V _{MODE} "Low" Voltage Range	0		0.5	V		
V _{MODE} "High" Voltage Range	1.7	2.7	3.6	V	Must not exceed V _{CC} .	
Gain Settling Time			6	μS	PA_ON switched from low to high, POUT within 1 dB of the final value.	
			6	μS	PA_ON switched from high to low, POUT within 1dB of the final value.	
Internal Power Detector						
PDET Output Voltage		1.35		V	P _{OUT} =28dBm, V _{MODE} =Low	
		0.6		V	P _{OUT} =16dBm, V _{MODE} =High	

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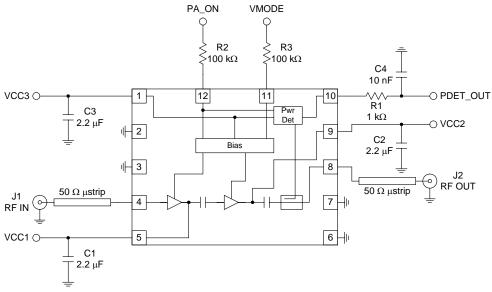
Pin	Function	Description	Interface Schematic
1	VCC3	Bias circuit and HDET power supply. A low frequency decoupling capacitor (2.2 μ F) is required. Type: P	
2	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
3	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
4	RF IN	RF input internally matched to 50Ω . This input is internally AC-coupled at the IC; however a shunt inductor used in the input matching network will provide a DC path to ground for components connected to the RF IN pin. A DC blocking capacitor may be required at this pin. Type: A, I	RF IN OFFICE Stage
5	VCC1	First stage power supply. A low frequency decoupling capacitor (2.2 $\mu\text{F})$ is required. Type: P	
6	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
7	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
8	RF OUT	RF output internally matched to 50Ω . This input is internally AC-coupled. Type: A, O	
9	VCC2	Output stage power supply. A low frequency decoupling capacitor $(2.2\mu F)$ is required. Type: P	
10	PDET_OUT	Power detector output. Type: A, O	
11	VMODE	Gain step control. When this pin is High, the module is in low power mode, and the amplifier's current is reduced. When this pin is Low, the module is in high power mode. Voltage should not be applied to this pin before VCC3 is applied. Type: D, I	
12	PA_ON	Device enable control. When this pin is High, the device is on. When this pin is Low, the device is off. Voltage should not be applied to this pin before VCC3 is applied. Type: D, I	
13	GND_SLUG	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane. Type: P	

Note: Where Type code is: I=Input; O=Output; A=Analog; D=Digital; P=Power

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Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



NOTE:

Resistors R2 and R3 are provided on the evaluation board to protect against power sequencing issues. (Refer to pin descriptions 11 and 12.) These resistors are not needed when the VCC3 is connected to the handset battery.

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