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RF3158

QUAD-BAND GSM/EDGE/GSM850/EGSM900 /DCS/PCS POWER AMPLIFIER MODULE

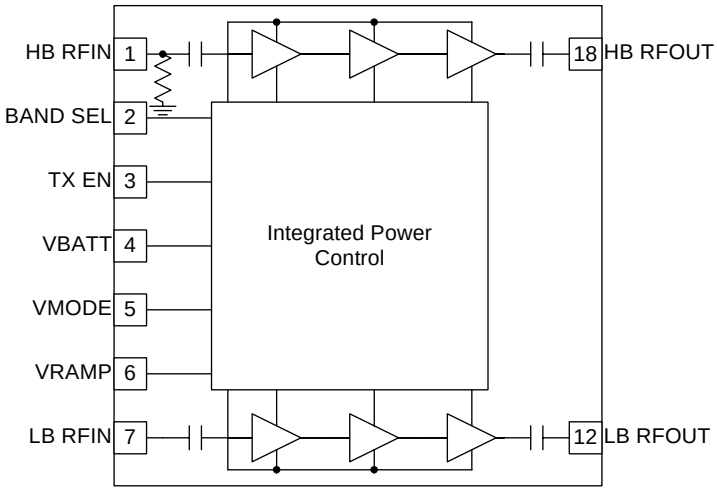
RoHS Compliant & Pb-Free Product
Package Style: Module (6mmx6mm)

Features

- Linear EDGE and GSM Operation
- PowerStar® GSM/GPRS Power Control
- Digital Band Select Enables a Single PA Lineup
- Single Supply Voltage; Requires no External Reference Voltage
- Automatic V_{BATT} Tracking Circuit avoids Switching Transients at Low Supply Voltage
- Low Power Mode for Reduced EDGE Current
- Analog Bias Control allows External Optimization of EDGE Current
- Compact 6mmx6mm Package

Applications

- Quad-Band GSM/EDGE Handsets
- GSM/EDGE Transmitter Lineups
- Portable Battery-Powered Equipment
- GSM850/EGSM900/DCS/PCS Products
- GPRS Class 12 Compatible Products
- Mobile EDGE/GPRS Data Products



Functional Block Diagram

Product Description

The RF3158 is a high power, dual-mode amplifier module with integrated power control. The input and output terminals are internally matched to 50Ω. The amplifier devices are manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (GaAs HBT) process, which is designed to operate either in saturated mode for GMSK signaling or linear mode for 8PSK signaling. The module is designed to be the final amplification stage in a dual-mode GSM/EDGE mobile transmit lineup operating in the 824MHz to 915MHz (low) and 1710MHz to 1910MHz (high) bands (such as a cellular handset). Band selection is controlled by an input on the module which selects either the low or high band. The device is packaged on a 6mmx6mm laminate module with a protective plastic overmold.

Ordering Information

RF3158	Quad-Band GSM/EDGE/GSM850/EGSM900 /DCS/PCS Power Amplifier Module
	Power Amplifier Module, 5 Piece Sample Pack
RF3158PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +6.0	V
Power Control Voltage (V_{RAMP})	-0.5 to +3.0	V
Band Select	3.0	V
TX Enable	3.0	V
V_{MODE}	3.0	V
RF - Input Power	12.0	dBm
Max Duty Cycle	50	%
Output Load VSWR	10:1	
Operating Case Temperature	-20 to +85	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

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RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
V_{RAMP} Power Control (GMSK Mode)					
Power Control Range	0.30		2.10	V	
V_{RAMP} Input Current			40	uA	$V_{RAMP}=V_{RAMP,MAX}$
V_{RAMP} Bias Control (8PSK Mode)					
High Bias Mode	2.1	2.15		V	High Bias Mode
Low Bias Mode	0.4	0.6	2.0	V	Low Bias Mode
V_{RAMP} Input Current			40	uA	$V_{RAMP}=V_{RAMP,MAX}$
V_{MODE} Switch					
V_{MODE} “HIGH”	1.5			V	8PSK Mode
V_{MODE} “LOW”	0		0.7	V	GMSK Mode
V_{MODE} Input Current	-10		10	uA	
Band Switch					
BAND_SEL “HIGH”	1.5			V	High Band (DCS/PCS)
BAND_SEL “LOW”	0		0.7	V	Low Band (GSM850/GSM900)
BAND_SEL Input Current	-10		10	uA	
TX_EN Switch					
TX_EN “HIGH”	1.5			V	PA “ON”
TX_EN “LOW”	0		0.7	V	PA “OFF”
TX_EN Input Current	-10		10	uA	
Overall Power Supply					
V_{CC} Range	3.2	3.6	4.5	V	Performance specified
	3.0		4.8	V	Functional with performance degraded
Off Current			10	uA	TX_EN low

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Impedance					
LB_RF IN		50		Ω	
LB_RF OUT		50		Ω	
HB_RF IN		50		Ω	
HB_RF OUT		50		Ω	
Cellular 850MHz Band GMSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25 °C, V_{CC}=3.6V, V_{MODE}="Low", Freq=824MHz to 849MHz, 25% Duty Cycle, Pulse Width=1154µs, Over Pin Range, BAND_SEL="Low", TX_EN="High"
Operating Frequency Range	824		849	MHz	
Input Power Range, P_{IN}	+1.0	+4.0	+6.5	dBm	
Maximum Output Power	34.5	35.0		dBm	Temp=25 °C, V_{CC}=3.6V, V_{RAMP}=$V_{RAMP,MAX}$
	32.5			dBm	Temp=85 °C, V_{CC}=3.2V, V_{RAMP}=$V_{RAMP,MAX}$
			-10	dBm	V_{RAMP}=0.3V
Power Droop	-0.25		0.25	dB	P_{OUT}≤34.5dBm, 50% Duty Cycle, Pulse Width=2308µs
Power Control Slope		300		dB/V	Maximum Slope, P_{OUT}=0dBm to 5dBm
		200		dB/V	Maximum Slope, P_{OUT}=5dBm to 15dBm
		60		dB/V	Maximum Slope, P_{OUT}≥15dBm
Total Efficiency (PAE)	47	50		%	V_{RAMP}=$V_{RAMP,MAX}$
Output Noise Power		-87	-82	dBm	RBW=100kHz, 869MHz to 894MHz, f_0=849MHz, P_{OUT}≤+34.5dBm
Forward Isolation			-25	dBm	TX_EN=0V, V_{RAMP}=0.3V, P_{IN}=+6dBm
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤34.5dBm
$3f_0$ Harmonics			-10	dBm	P_{OUT}≤34.5dBm
Fundamental Cross Band Coupling			0	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}=34.5dBm at LB_RFOUT pin.
$2f_0$, $3f_0$ Cross Band Coupling			-18	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}=34.5dBm at LB_RFOUT pin.
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤34.5dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, P_{IN}=+4dBm, set V_{RAMP} where P_{OUT}≤34.5dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where P_{OUT}≤34.5dBm into 50Ω load, no damage or permanent degradation to part.

Note: $V_{RAMP,MAX}$=2.1V

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Cellular 850MHz Band 8PSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25 °C, V_{CC}=3.6V, V_{RAMP}=2.1V, V_{MODE}="High", Freq=824MHz to 849MHz, 25% Duty Cycle, Pulse Width=1154µs, BAND_SEL="Low", TX_EN="High"
Operating Frequency Range	824		849	MHz	
Maximum Output Power Meeting EVM and ACPR Spectrum	28.5	29		dBm	High Bias mode (V_{RAMP}=2.1V)
	26.5			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, High Bias mode (V_{RAMP}=2.1V)
	13.5			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, Low Bias mode (V_{RAMP}=0.6V)
Low Power Current Consumption		350	575	mA	P_{OUT}≤13.5dBm, Low Bias mode (V_{RAMP}=0.6V)
Total Efficiency (PAE)	17	20		%	P_{OUT}=28.5dBm, High Bias mode (V_{RAMP}=2.1V)
		2.0		%	P_{OUT}=13.5dBm, Low Bias mode (V_{RAMP}=0.6V)
Gain	28.0	30.0	32.0	dB	
Gain Temperature Coefficient		-0.037		dB/K	Temp=+25°C to +85°C, V_{CC}=3.6V
		-0.025		dB/K	Temp=-20°C to +25°C, V_{CC}=3.6V
EVM RMS			3.5	%	P_{OUT}≤28.5dBm
			5.0	%	P_{OUT}≤26.5dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C
ACPR and Spectrum Mask			-57	dBc	At 400kHz in 30kHz BW, P_{OUT}≤28.5dBm
			-63	dBc	At 600kHz in 30kHz BW, P_{OUT}≤28.5dBm
ACPR and Spectrum Mask, Extreme Conditions			-57	dBc	At 400kHz in 30kHz RBW, P_{OUT}≤26.5dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C.
			-63	dBc	At 600kHz in 30kHz RBW, P_{OUT}≤26.5dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C.
Output Noise Power		-82	-80	dBm	RBW=100kHz, 869MHz to 894MHz, f_0=849MHz, P_{OUT}≤+28.5dBm
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤28.5dBm
$3f_0$ Harmonics			-10	dBm	P_{OUT}≤28.5dBm
Fundamental Cross Band Coupling			0	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}≤28.5dBm at LB_RFOUT pin.
$2f_0$, $3f_0$ Cross Band Coupling			-18	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}≤28.5dBm at LB_RFOUT pin.
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤28.5dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, set P_{IN} where P_{OUT}≤28.5dBm into 50Ω load.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM 900MHz Band GMSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25 °C, V_{CC}=3.6V, V_{MODE}="Low", Freq=880MHz to 915MHz, 25% Duty Cycle, Pulse Width=1154µs, Over Pin Range, BAND_SEL="Low", TX_EN="High"
Operating Frequency Range	880		915	MHz	
Input Power Range, P_{IN}	+1.0	+4.0	+6.5	dBm	
Maximum Output Power	34.5	35		dBm	Temp=25 °C, V_{CC}=3.6V, V_{RAMP}=$V_{RAMP,MAX}$
	32.5			dBm	Temp=+85°C, V_{CC}=3.2V, V_{RAMP}=$V_{RAMP,MAX}$
			-10	dBm	V_{RAMP}=0.3V
Power Droop	-0.25		0.25	dB	P_{OUT}≤34.5dBm, 50% Duty Cycle, Pulse Width=2308µs
Power Control Slope		300		dB/V	Maximum Slope, P_{OUT}=0dBm to 5dBm
		200		dB/V	Maximum Slope, P_{OUT}=5dBm to 15dBm
		60		dB/V	Maximum Slope, P_{OUT}≥15dBm
Total Efficiency (PAE)	47	50		%	V_{RAMP}=$V_{RAMP,MAX}$
Output Noise Power		-83	-80	dBm	RBW=100kHz, 925MHz to 935MHz, f_0=915MHz, P_{OUT}≤+34.5dBm
		-87	-83	dBm	RBW=100kHz, 935MHz to 960MHz, f_0=915MHz, P_{OUT}≤+34.5dBm
Forward Isolation			-25	dBm	TX_EN=0V, V_{RAMP}=0.3V, P_{IN}=+6dBm
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤34.5dBm
$3f_0$ Harmonics			-10	dBm	P_{OUT}≤34.5dBm
Fundamental Cross Band Coupling			0	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}=34.5dBm at LB_RFOUT pin.
$2f_0$, $3f_0$ Cross Band Coupling			-18	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}=34.5dBm at LB_RFOUT pin.
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤34.5dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, P_{IN}=+4dBm, set V_{RAMP} where P_{OUT}≤34.5dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where P_{OUT}≤34.5dBm into 50Ω load, no damage or permanent degradation to part.

Note: $V_{RAMP,MAX}$=2.1V

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM 900MHz Band 8PSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25 °C, V_{CC}=3.6V, V_{MODE}="High", V_{RAMP}=2.1V, Freq=880MHz to 915MHz, 25% Duty Cycle, Pulse Width=1154µs, BAND_SEL="Low", TX_EN="High"
Operating Frequency Range	880		915	MHz	
Maximum Output Power Meeting EVM and ACPR Spectrum	28.5	29		dBm	High Bias mode (V_{RAMP}=2.1V)
	26.5			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, High Bias mode (V_{RAMP}=2.1V)
	13.5			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, Low Bias mode (V_{RAMP}=0.6V)
Low Power Current Consumption		350	575	mA	P_{OUT}≤13.5dBm, Low Bias mode (V_{RAMP}=0.6V)
Total Efficiency (PAE)	16.5	22.0		%	P_{OUT}=28.5dBm, High Bias mode (V_{RAMP}=2.1V)
		2.0		%	P_{OUT}=13.5dBm, Low Bias mode (V_{RAMP}=0.6V)
Gain	28.0	29.5	32.0	dB	
Gain Temperature Coefficient		-0.037		dB/K	Temp=+25°C to +85°C, V_{CC}=3.6V
		-0.026		dB/K	Temp=-20°C to +25°C, V_{CC}=3.6V
EVM RMS			3.5	%	P_{OUT}≤28.5dBm
			5.0	%	P_{OUT}≤26.5dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C
ACPR and Spectrum Mask			-57	dBc	At 400kHz in 30kHz BW, P_{OUT}≤28.5dBm
			-63	dBc	At 600kHz in 30kHz BW, P_{OUT}≤28.5dBm
ACPR and Spectrum Mask, Extreme Conditions			-57	dBc	At 400kHz in 30kHz RBW. P_{OUT}≤26.5dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C.
			-63	dBc	At 600kHz in 30kHz RBW. P_{OUT}≤26.5dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C.
Output Noise Power		-83	-82	dBm	RBW=100kHz, 925MHz to 935MHz, f_0=915MHz, P_{OUT}≤+28.5dBm
		-83	-80	dBm	RBW=100kHz, 935MHz to 960MHz, f_0=915MHz, P_{OUT}≤+28.5dBm
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤28.5dBm
$3f_0$ Harmonics			-10	dBm	P_{OUT}≤28.5dBm
Fundamental Cross Band Coupling			0	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}≤28.5dBm at LB_RFOUT pin.
$2f_0$, $3f_0$ Cross Band Coupling			-18	dBm	Measured at HB_RF_{OUT} pin, P_{OUT}≤28.5dBm at LB_RFOUT pin.
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤28.5dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, set P_{IN} where P_{OUT}≤28.5dBm into 50Ω load.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS 1800MHz Band GMSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25 °C, V_{CC}=3.6V, V_{MODE}="Low", Freq=1710MHz to 1785MHz, 25% Duty Cycle, Pulse Width=1154µs, P_{IN}=Over Range, BAND_SEL="High", TX_EN="High"
Operating Frequency Range	1710		1785	MHz	
Input Power Range, P_{IN}	2.0	5.0	8.5	dBm	
Maximum Output Power	32	33		dBm	Temp=25 °C, V_{CC}=3.6V, V_{RAMP}=$V_{RAMP,MAX}$
	30			dBm	Temp=+85°C, V_{CC}=3.2V, P_{IN}≥3dBm, V_{RAMP}=$V_{RAMP,MAX}$
			-10	dBm	V_{RAMP}=0.3V
Power Droop	-0.25		0.25	dB	P_{OUT}≤32dBm, 50% Duty Cycle, Pulse Width=2308µs
Power Control Slope		350		dB/V	Maximum Slope, P_{OUT}=-5dBm to 0dBm
		250		dB/V	Maximum Slope, P_{OUT}=0dBm to +10dBm
		100		dB/V	Maximum Slope, P_{OUT}≥10dBm
Total Efficiency (PAE)	45	49		%	V_{RAMP}=$V_{RAMP,MAX}$
Output Noise Power		-80	-79	dBm	RBW=100kHz, 1805MHz to 1880MHz, f_0=1785MHz, P_{OUT}≤32dBm
Forward Isolation			-32	dBm	TX_EN=0V, V_{RAMP}=0.3V, P_{IN}=+6dBm
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤32dBm
$3f_0$ Harmonics			-7	dBm	P_{OUT}≤32dBm
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤32dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, P_{IN}=+5dBm, set V_{RAMP} where P_{OUT}≤32dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where P_{OUT}≤32dBm into 50Ω load, no damage or permanent degradation to part.

Note: $V_{RAMP,MAX}$=2.1V

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS 1800MHz Band 8PSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25 °C, V_{CC}=3.6V, V_{MODE}="High", V_{RAMP}=2.1V, Freq=1710MHz to 1785MHz, 25% Duty Cycle, Pulse Width=1154µs, BAND_SEL="High", TX_EN="High"
Operating Frequency Range	1710		1785	MHz	
Maximum Output Power Meeting EVM and ACPR Spectrum	28.0			dBm	High Bias mode (V_{RAMP}=2.1V)
	26.0			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, High Bias mode (V_{RAMP}=2.1V)
	12.5			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, Low Bias mode (V_{RAMP}=0.8V)
Low Power Current Consumption		350	550	mA	P_{OUT}≤12.5dBm, Low Bias mode (V_{RAMP}=0.8V)
Total Efficiency (PAE)	18.5	23.0		%	P_{OUT}=28dBm, High Bias mode (V_{RAMP}=2.1V)
		1.6		%	P_{OUT}=12.5dBm, Low Bias mode (V_{RAMP}=0.8V)
Gain	32.0	34.5	37.0	dB	
Gain Temperature Coefficient		-0.050		dB/K	Temp=+25°C to +85°C, V_{CC}=3.6V
		-0.040		dB/K	Temp=-20°C to +25°C, V_{CC}=3.6V
EVM RMS			3.5	%	P_{OUT}≤28dBm
			5.0	%	P_{OUT}≤26dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C
ACPR and Spectrum Mask			-57	dBc	At 400kHz in 30kHz BW, P_{OUT}≤28dBm
			-63	dBc	At 600kHz in 30kHz BW, P_{OUT}≤28dBm
ACPR and Spectrum Mask, Extreme Conditions			-57	dBc	At 400kHz in 30kHz RBW, P_{OUT}≤26dBm, Temp=-20°C to +85°C, V_{CC}=3.2V to 4.5V
			-63	dBc	At 600kHz in 30kHz RBW, P_{OUT}≤26dBm, Temp=-20°C to +85°C, V_{CC}=3.2V to 4.5V
Output Noise Power		-83	-81	dBm	RBW=100kHz, 1805MHz to 1880MHz, f_0=1785MHz, P_{OUT}≤28dBm,
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤28dBm
$3f_0$ Harmonics			-7	dBm	P_{OUT}≤28dBm
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤28dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, set P_{IN} where P_{OUT}≤28.0dBm into 50Ω load.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PCS 1900MHz Band GMSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25 °C, V_{CC}=3.6V, V_{MODE}="Low", Freq=1850MHz to 1910MHz, 25% Duty Cycle, Pulse Width=1154µs, P_{IN}=Over Range, BAND_SEL="High", TX_EN="High"
Operating Frequency Range	1850		1910	MHz	
Input Power Range, P_{IN}	2.0	5.0	8.5	dBm	
Maximum Output Power	32	33		dBm	Temp=25 °C, V_{CC}=3.6V, V_{RAMP}=$V_{RAMP,MAX}$
	30			dBm	Temp=+85°C, V_{CC}=3.2V, P_{IN}≥3dBm, V_{RAMP}=$V_{RAMP,MAX}$
			-10	dBm	V_{RAMP}=0.3V
Power Droop	-0.25		0.25	dB	P_{OUT}≤32dBm, 50% Duty Cycle, Pulse Width=2308µs
Power Control Slope		350		dB/V	Maximum Slope, P_{OUT}=-5dBm to 0dBm
		250		dB/V	Maximum Slope, P_{OUT}=0dBm to +10dBm
		100		dB/V	Maximum Slope, P_{OUT}≥10dBm
Total Efficiency (PAE)	45	49		%	V_{RAMP}=$V_{RAMP,MAX}$
Output Noise Power		-81	-79	dBm	RBW=100kHz, 1930MHz to 1990MHz, f_0=1910MHz, P_{OUT}≤32dBm
Forward Isolation			-32	dBm	TX_EN=0V, V_{RAMP}=0.3V, P_{IN}=+6dBm
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤32dBm
$3f_0$ Harmonics			-7	dBm	P_{OUT}≤32dBm
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤32dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, P_{IN}=+5dBm, set V_{RAMP} where P_{OUT}≤32dBm into 50Ω load
Output Load VSWR Ruggedness	10:1				Set V_{RAMP} where P_{OUT}≤32dBm into 50Ω load, no damage or permanent degradation to part.

Note: $V_{RAMP,MAX}$=2.1V

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PCS 1900MHz Band 8PSK Mode					Nominal Conditions (unless otherwise stated): Input and Output=50Ω, Temp=25°C, V_{CC}=3.6V, V_{MODE}="High", V_{RAMP}=2.1V, Freq=1850MHz to 1910MHz, 25% Duty Cycle, Pulse Width=1154µs, BAND_SEL="High", TX_EN="High"
Operating Frequency Range	1850		1910	MHz	
Maximum Output Power Meeting EVM and ACPR Spectrum	28.0			dBm	High Bias mode (V_{RAMP}=2.1V)
	26.0			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, High Bias mode (V_{RAMP}=2.1V)
	12.5			dBm	Temp=-20°C to +85°C, V_{CC}=3.2V, Low Bias mode (V_{RAMP}=0.8V)
Low Power Current Consumption		350	550	mA	P_{OUT}≤12.5dBm, Low Bias mode (V_{RAMP}=0.8V)
Total Efficiency (PAE)	18.5	24.0		%	P_{OUT}=28dBm, High Bias mode (V_{RAMP}=2.1V)
		1.6		%	P_{OUT}=12.5dBm, Low Bias mode (V_{RAMP}=0.8V)
Gain	32.0	34.5	37.0	dB	
Gain Temperature Coefficient		-0.045		dB/K	Temp=+25°C to +85°C, V_{CC}=3.6V
		-0.035		dB/K	Temp=-20°C to +25°C, V_{CC}=3.6V
EVM RMS			3.5	%	P_{OUT}≤28dBm
			5.0	%	P_{OUT}≤26dBm, V_{CC}=3.2V to 4.5V, Temp=-20°C to +85°C
ACPR and Spectrum Mask			-57	dBc	At 400kHz in 30kHz BW, P_{OUT}≤28dBm
			-63	dBc	At 600kHz in 30kHz BW, P_{OUT}≤28dBm
ACPR and Spectrum Mask, Extreme Conditions			-57	dBc	At 400kHz in 30kHz RBW, P_{OUT}≤26dBm, Temp=-20°C to +85°C, V_{CC}=3.2V to 4.5V
			-63	dBc	At 600kHz in 30kHz RBW, P_{OUT}≤26dBm, Temp=-20°C to +85°C, V_{CC}=3.2V to 4.5V
Output Noise Power		-84	-82	dBm	RBW=100kHz, 1930MHz to 1990MHz, f_0=1910MHz, P_{OUT}≤28dBm
$2f_0$ Harmonics			-7	dBm	P_{OUT}≤28dBm
$3f_0$ Harmonics			-7	dBm	P_{OUT}≤28dBm
All Other Non-harmonic Spurious			-36	dBm	P_{OUT}≤28dBm
Input VSWR			2.5:1		Over P_{OUT} Range
Output Load VSWR Stability	6:1				Spurious<-36dBm, RBW=3MHz, set P_{IN} where P_{OUT}≤28.0dBm into 50Ω load.

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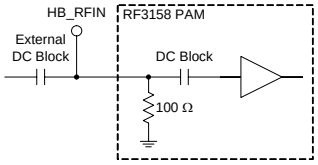
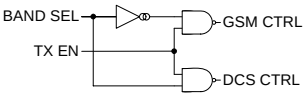
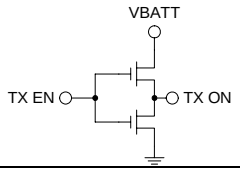
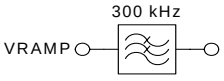
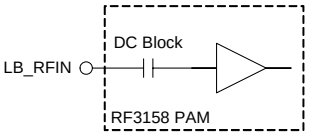
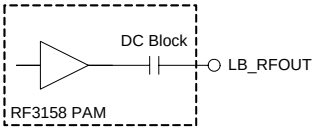
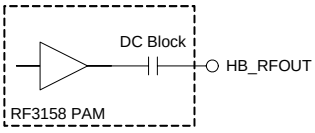
Pin	Function	Description	Interface Schematic
1	HB_RFIN	RF input to the high-band PA. There is a 100Ω shunt resistor, before the DC block inside the part, which sets the input impedance for the HB PA. When connected to a DC coupled transceiver, an external DC blocking capacitor is required.	
2	BAND_SEL	Digital input enables either the low band or high band amplifier die within the module. A logic low selects Low Band (GSM850/EGSM900), a logic high selects High Band (DCS1800/PCS1900). This pin is a high impedance CMOS input with no pull-up or pull-down resistors.	
3	TX_EN	Digital input enables or disables the internal circuitry. When disabled, the module is in the OFF state and draws virtually zero current. This pin is a high impedance CMOS input with no pull-up or pull-down resistors.	
4	VBATT	Main DC power supply for all circuitry in the RF3158. Traces to this pin will have high current pulses during operation so proper decoupling and routing to handle this should be observed.	
5	VMODE	Digital input which internally adjusts settings to optimize amplifier performance for saturated or linear mode. A logic low selects saturated mode for GMSK modulation. A logic high selects linear mode for 8PSK modulation. This pin is a high impedance CMOS input with no pull-up or pull-down resistors.	
6	VRAMP	In GMSK mode, the voltage on this pin controls the output power by varying the regulated collector voltage on the amplifiers. In EDGE mode, the voltage on this pin varies the regulated base bias of the amplifiers. An internal 300kHz filter reduces switching ORFS resulting from transitions between DAC steps. Most systems will have no need for external V_{RAMP} filtering. This pin provides an impedance of approximately 60kΩ.	
7	LB_RFIN	RF input to the low-band PA. It is DC-blocked within the part.	
8	GND	Ground.	
10	GND	Ground.	
11	GND	Ground.	
12	LB_RFOUT	RF output from the low-band PA. It is DC-blocked within the part.	
13	GND	Ground.	
14	GND	Ground.	
15	GND	Ground.	
16	GND	Ground.	
17	GND	Ground.	
18	HB_RFOUT	RF output from the high-band PA. It is DC-blocked within the part.	
19	GND	Ground.	

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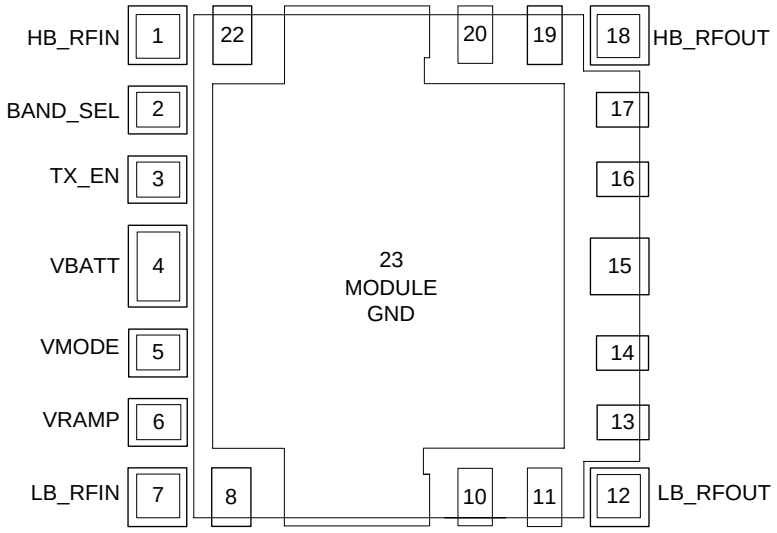
Pin	Function	Description	Interface Schematic
20	GND	Ground.	
22	GND	Ground.	
23	GND	Main ground pad in center of part. This pad should be tied to the main ground plane with as little loss as possible for optimum linearity.	

Dual Mode Operation

MODE	V_{MODE}	RF INPUT	V_{RAMP}	TX ENABLE
GSM	Low	FIXED	Analog voltage that proportionally regulates collector voltage. Controls output power level. (GSM Burst Ramp Control)	High (Normal) Low (Isolation)
EDGE	High	Ramped burst from Variable Gain Amplifier or Source (GSM Burst Ramp Control)	Analog voltage that proportionally regulates base bias. Controls amplifier bias current.	High (Normal) Low (Isolation)

Note: When V_{MODE} is low (GMSK mode), the voltage on V_{RAMP} is used to regulate the PA collector voltage which directly controls the output power. When V_{MODE} is high (8PSK mode), the PA collector voltage is regulated to 3.6V, and the supply for the PA base bias can be adjusted via the V_{RAMP} pin to optimize current drain for low or high power ranges. In addition, in 8PSK mode, the first stage of the low band PA is bypassed to decrease gain, but in high band, the PA operates with all stages.

Pin Out



Note: view from top of part.

Pins 8, 10, 11, 13, 14, 15, 16, 17, 19, 20, 22 are connected to pin 23 on the module. It is recommended that these pins be connected to module ground on the PCB as well.

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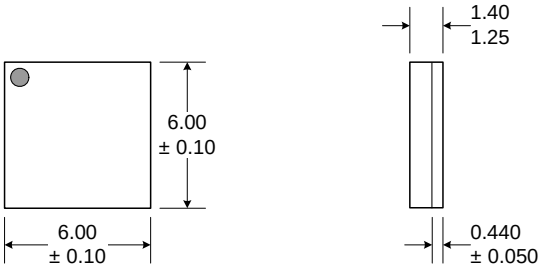
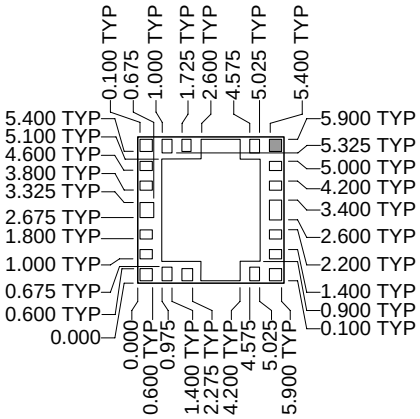
Package Drawing



Dimensions in mm.

Shaded area represents pin 1.



Note: viewed from bottom of the part.

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Theory of Operation

Overview

The RF3158 is designed for use as the final RF amplifier in GSM850, EGSM900, DCS and PCS handheld digital cellular equipment, and other applications operating in the 824MHz to 915MHz and 1710MHz to 1910MHz bands. The RF3158 is a high power, dual mode GSM/EDGE, power amplifier with PowerStar® integrated power control. The integrated power control circuitry provides reliable control of saturated power by a single analog voltage (V_{RAMP}). This V_{RAMP} can be driven directly from a DAC output. PowerStar®'s predictable power versus V_{RAMP} relationship allows single-point calibration in each band. Single point calibration enables handset manufacturers to achieve simple and efficient phone calibration during production.

The RF3158 also features an integrated saturation detection circuit, which is an industry first for standard PA module products. The saturation detection circuit automatically monitors battery voltage and adjusts the power control loop to reduce transient spectrum degradation that would otherwise occur at low battery voltage conditions. Prior to the implementation of the saturation detection circuit, handset designers were required to adjust the ramp voltage within the system software. RFMD's saturation detection circuit reduces handset design time and ensures robust performance over broad operating conditions.

The design of a dual mode power amplifier module is a challenging process involving many performance tradeoffs and compromises to allow it to perform well in both saturated and linear operating regions. This is most noticeable in the RF3158 GSM efficiency. A GSM only part can have its load line (output match) adjusted for maximum efficiency. In a dual mode module, tuning of the load line must be balanced between GSM efficiency and EDGE linearity. The result is slightly lower GSM efficiency than a single mode (saturated only) power amplifier module. In addition, the RF3158 uses a special GaAs Heterojunction Bipolar Transistor (HBT) process technology which is not used in the most efficient GSM only power amplifiers. The special HBT process allows the RF3158 to provide excellent linear performance, Error Vector Magnitude (EVM), and Adjacent Channel Power Ratio (ACPR), yet maintain competitive GSM efficiency.

Modes of Operation

The RF3158 is a dual mode saturated GSM and linear EDGE Power Amplifier. In GSM mode, the RF3158 is a traditional PowerStar® module, which means that the output power is controlled by the V_{RAMP} voltage. In EDGE mode, the RF3158 acts as a gain block where the output power is controlled by the input RF power. The input RF drive level is reduced from GSM mode to prevent saturation and limit output power. Figure 1 shows the Power Amplifier operating regions in GSM and EDGE mode.

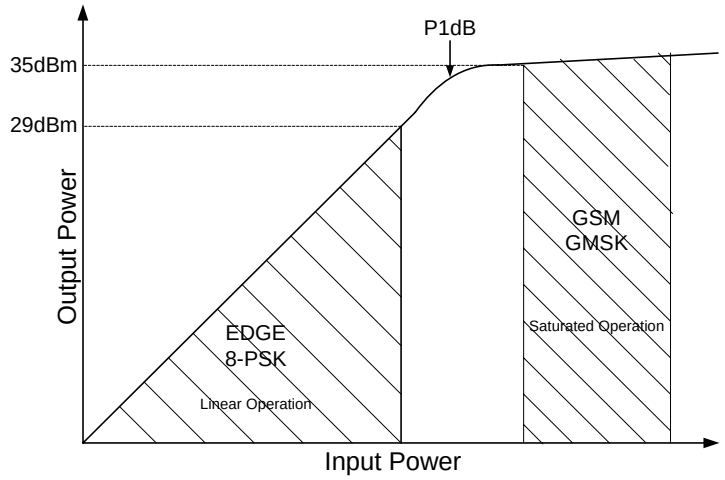

Figure 1. RF3158 Power Amplifier Operating Regions in GSM/EDGE Mode

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GSM applications typically require an input RF drive that is 3dB to 4dB higher than the 1dB compression point. GSM mode involves GMSK modulation, which is a constant envelope modulation and is not sensitive to amplitude non-linearities caused by the PA. Since the useful data in the GMSK modulation is entirely included in the phase, the amplifier may be operated in saturated mode (deep class AB) for optimum efficiency. Saturated output power for the RF3158 is controlled by the voltage on the V_{RAMP} pin.

Linear EDGE applications require a linear power amplifier to transfer 8PSK modulation with minimal distortion. Since an 8PSK signal has information encoded in both amplitude and phase, the use of a saturated PA is not trivial and requires a more complex system. The traditional way to design a transmitter that is required to convey both phase and amplitude modulation is through the use of a linear power amplifier (Class A). In RF3158, the bias is held at a constant level such that the device is operating in linear region, and the output RF level is directly proportional to the input RF level. The RF3158 is used as a linear amplifier by fixing the voltage on the V_{RAMP} pin and reducing the input power to the PA such that the device enters a linear operational region. Output power is controlled by applying the proper amplitude signal to the RFIN Pin. The voltage on the V_{RAMP} pin controls bias current and can be fixed at various levels to optimize current consumption for the desired output power range.

GSM (Saturated) Mode

In GSM mode, RF3158 operates as a traditional PowerStar® module. The incorporated control loop regulates the collector voltage of the amplifiers while the stages are held at a constant bias. The basic circuit diagram is shown in Figure 2.

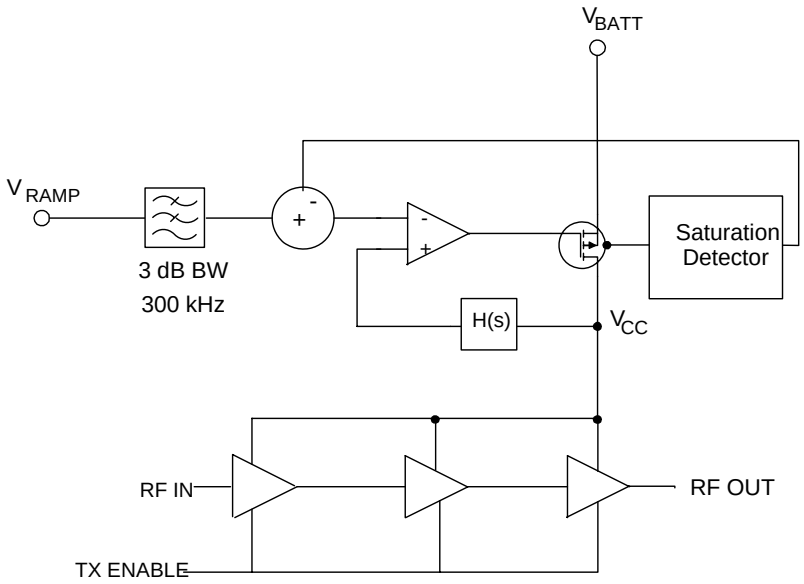

Figure 2. RF3158 Basic Circuit Diagram

By regulating the collector voltage (V_{CC}), the stages are held in saturation across all power levels. As V_{CC} is decreased, output power decreases as described by Equation 1. The equation shows that load impedance affects output power, but to a lesser degree than V_{CC} supply variations. Since the RF3158 regulates V_{CC}, the dominant cause of power variation is eliminated.

$$P_{OUT_{dBm}} = 10 \cdot \log \frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot Rl \cdot 10^{-3}} \quad \text{(Eq. 1)}$$

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RF3158 power is ramped up and down through the V_{RAMP} control voltage which in turn controls the collector voltage of the amplifier stages. The RF signal applied at the RFIN pin must be a constant amplitude signal and should be high enough to saturate the amplifier in the GSM mode. The input power (P_{IN}) range is indicated in the specifications. Power levels below this range will result in reduced maximum output power and the potential for more variation of output power over extreme conditions. Higher input power is unnecessary and will require more current in the circuitry driving the power amplifier and will increase the minimum output power of the RF3158.

The saturation detector circuit monitors the V_{BATT} and V_{CC} voltages and adjusts the power control loop to prevent the series-pass FET regulator from entering saturation. If the V_{CC} regulator were to saturate, the response time would increase dramatically. This is undesirable because the V_{CC} regulator must accurately follow the burst ramp up or ramp down applied to the V_{RAMP} pin, or the transient spectrum will degrade.

EDGE (Linear) Mode

In EDGE mode, V_{CC} is fixed and the bias currents are controlled by V_{RAMP}. The low band gain is significantly reduced from GMSK mode in order to improve receive band noise performance. The RF3158 then operates as a linear amplifier where output power is directly controlled by input power. The RF signal applied to the RFIN pin must be accurately controlled to produce the desired output amplitude and burst ramping. The RFIN power must be maintained so that the amplifier is operating in its linear region. If the input drive is too high, the amplifier will begin to saturate causing the ACPR and EVM performance to degrade. The most sensitive of these on the RF3158 is the +/-400kHz offset ACPR. As the amplifier approaches saturation, this will be the first parameter to show significant degradation.

During production calibration of a system containing the RF3158, the PA gain and other parameters must be determined. After that, the RF3158 functions as a fixed gain block while the system adjusts input power such that the output from the transmitter meets the desired system specifications.

Since the RF3158 operates as a gain block in EDGE mode, gain variation over extreme conditions must be considered when determining the output power that a specific input power will produce. Typical Gain versus Temperature is shown in Figure 3. Special attention must be given to ensure that the output power of the PA does not go higher than the maximum linear output that the PA can provide with acceptable EVM and ACPR performance.

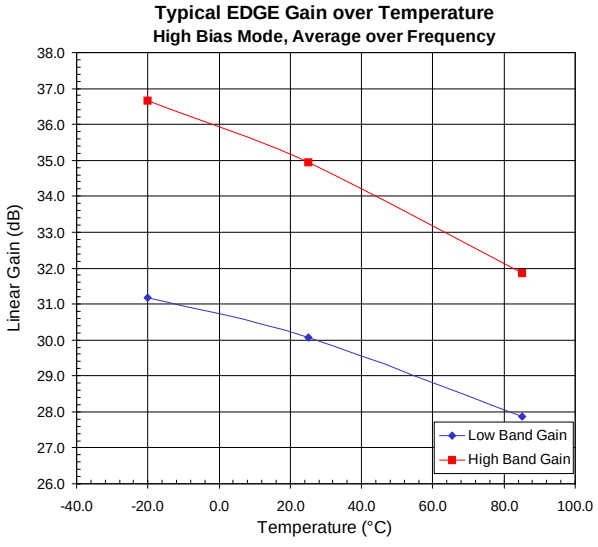

Figure 3. EDGE Gain over Temperature

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A large portion of the total current in a linear amplifier is necessary to bias the transistors so that the output remains linear. In an EDGE system where there are a range of output power levels used (PCLs), an amplifier biased to operate at a high power will be very inefficient at low power levels. Conversely, an amplifier biased to operate at a low power will not be linear at high power levels. The maximum linear power of an amplifier is determined during design, but can be adjusted to some extent by the quiescent current through the amplifier transistors.

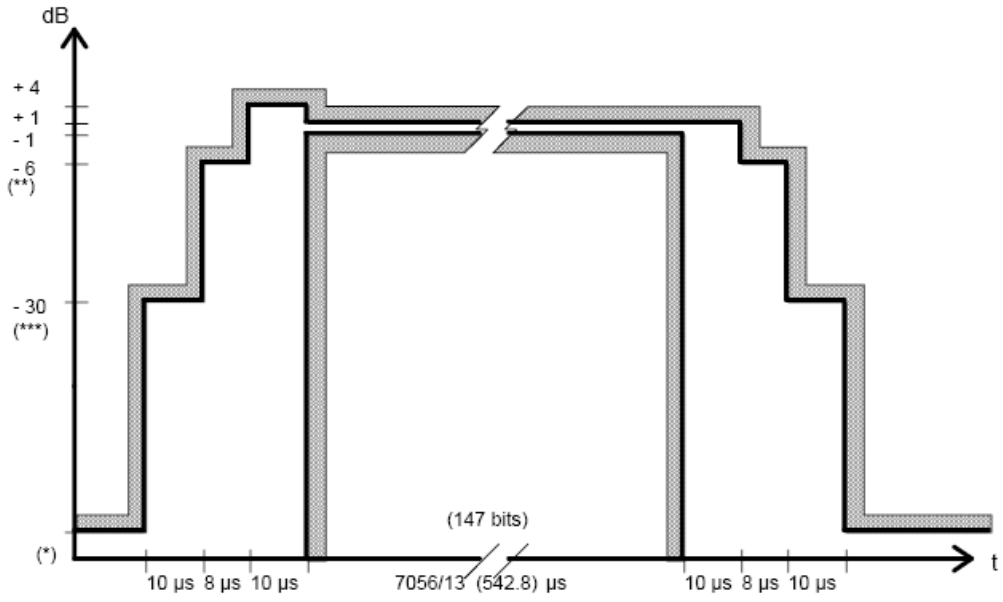
The RF3158 incorporates an analog bias control in EDGE mode. This allows the system designer to reduce quiescent current in the power amplifier when operating at lower output power levels, resulting in improved efficiency. Low bias mode for the RF3158 is basically a specific setting of the analog bias control for which characterization and test data has been collected. In low bias mode the PA can only be operated at or below a specified output power level while maintaining linearity. It is conceivable that a system designer could select a separate bias setting (V_{RAMP} voltage) for each PCL to optimize efficiency across all operating levels. However, as bias changes, so does the gain, linearity, and temperature response. Balancing all these parameters across extreme operating conditions and process variation would likely be impossible in a volume production environment. At minimum, careful system characterization and planning would be required.

Power Ramping and Timing

The RF3158 should be powered on according to the Power-On Sequence provided in the datasheet. The power on sequence is designed to prevent operation of the amplifier under conditions that could cause damage to the device, or erratic operation.

In the Power-On Sequence, there are some set-up times associated with the control signals of the RF3158. The most important of these is the settling time between TXEN going high and when V_{RAMP} can begin to increase. This time is often referred to as the "pedestal" and is required so that the internal power control loop and bias circuitry can settle after being turned on. The RF3158 requires at least 1.5µs or two quarter bit times for proper settling of the power control loop.

The diagram below is the ETSI time mask for a single GSM timeslot.



The V_{RAMP} waveform used with the RF3158 must be created such that the output power falls into this power versus time mask. The ability to ramp the RF output power to meet ETSI switching transient and time mask requirements partially depends upon the predictability of output power versus V_{RAMP} response of the power amplifier. The PowerStar® control in the RF3158 is very capable of meeting switching transient requirements with the proper raised Cosine waveform applied to the V_{RAMP} input. The ramping waveform on V_{RAMP} must not start until after TX_EN is asserted. A ramp of about 12us is required to control switching transients at high power levels.

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The V_{RAMP} voltage range should be limited to min and max values in the specifications to avoid damage or undesirable operation. At some voltage below 0.35V, the CMOS controller switches off and turns off the PA. The effect of this is a discontinuity in the response curve. In order to guarantee minimum switching transients, it is recommended that the minimum ramp voltage be set slightly above the voltage where this discontinuity occurs (See Figure 3). The V_{RAMP} voltage at which the discontinuity occurs is unique to the design of the part and does not shift significantly across process. Figure 3 shows the power versus V_{RAMP} response curve for two parts which represent typical process variation of the discontinuity.

As the V_{RAMP} voltage approaches its maximum, the linear regulator in the CMOS saturates, the output power reaches its maximum level, and the V_{RAMP} versus Output Power curve levels out. The saturation point of the linear regulator is directly proportional to the V_{BATT} supply voltage applied. The V_{RAMP} voltage can be increased above the saturation level, but the PA will not produce any higher output power. It is not recommended to apply a V_{RAMP} voltage above the absolute maximum specification, as the part could be damaged.

When the FET pass-device in the linear regulator saturates, the response time of the regulated voltage slows significantly. If the control voltage changes (as in ramp-down) the saturated linear regulator does not react fast enough to follow the ramp-down curve. The result is a discontinuity in the output power ramp and degraded switching transients. This usually occurs at low V_{BATT} levels where the regulated V_{CC} voltage is very near the supply voltage. The RF3158 incorporates a saturation detection circuit which senses if the FET pass-device is entering saturation and reduces V_{CC} to prevent it. This relieves the requirement of the transceiver controller to adjust the maximum V_{RAMP} when the battery voltage is low.

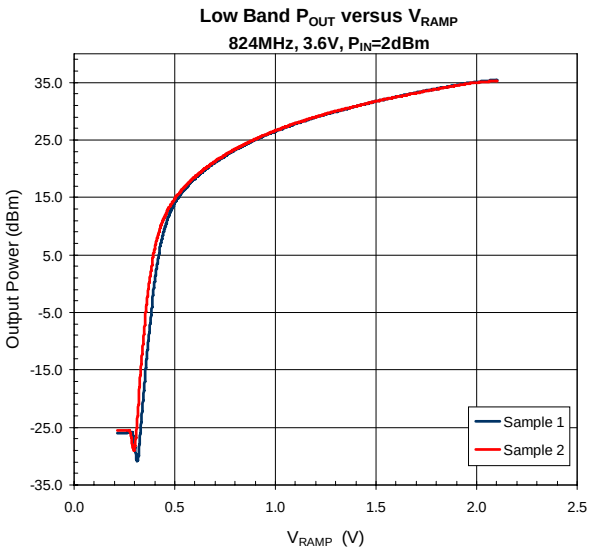

Figure 4. Output Power versus V_{RAMP}

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Design Considerations

There are several key factors to consider in the implementation of a mobile phone transmitter solution using the RF3158:

- System Efficiency

  The RF output match can be designed to improve system efficiency by presenting a non 50Ω load. Output matching circuits for the RF3158 should be a compromise between system efficiency and power as well as EDGE linearity. Optimal matching for GSM mode alone may degrade the linear performance beyond system specifications.

- Power Variation due to Supply Voltage

  Output power does not vary due to supply voltage under normal operating conditions. By regulating the collector voltage to the PA the voltage sensitivity is essentially eliminated. This covers most cases where the PA will be operated. However, as the battery discharges and V_{BATT} approaches its lower operating limit, the output power from the PA will start to drop. This cannot be avoided as a certain supply voltage is required to produce full output power. System specifications must allow for this power decrease.

  Switching Transients due to low battery conditions are reduced by the saturation detection circuit in RF3158. The saturation detection circuit consists of a feedback loop which detects FET saturation. As the FET approaches saturation, the circuit adjusts the V_{CC} voltage in order to ensure minimum switching transients. The saturation detection circuit is integrated into the CMOS controller and requires no additional input from the user.

- Power variation due to Temperature

  RF3158 output power variation due to temperature is largest at low power levels and decreases at the upper power levels. This follows the ETSI specification limits which allow a larger tolerance over extreme conditions at low power levels. Since output power is controlled by an analog input, factors other than the power amplifier will have an effect on total system power variation. The entire system containing the RF3158 should be tested to determine whether compensation is necessary. At high temperatures and low battery voltages, the PA cannot support as high of an output power. In this condition, increasing V_{RAMP} will not provide more output power, so compensation may not provide the intended result.

- Noise Power

  The bias point of the RF3158 is kept constant and the gain in the first stage is always high. This has the effect of maintaining a consistent noise power which does not increase at reduced output power levels. For that reason, noise power is at its highest when V_{RAMP} is at its maximum. The RF3158 does not create enough noise in the receive band to cause system receive band noise power failures, but it may amplify noise from other sources. Care must be taken to prevent noise from entering the power amplifier.

- Loop Stability and Loop Bandwidth Variation across Power Levels

  The design of a proper power control loop involves trade-offs affecting stability, transient spectrum and burst timing. In non-PowerStar® architectures, backing off power causes gain variation which can affect loop bandwidth. In RF3158 the loop bandwidth is determined by V_{CC} regulator bandwidth and does not change over output power. Loop stability is maintained since amplifier bias voltage is constant.

- Transient Spectrum

  Switching transients occur when the up and down power ramps are not smooth enough, or suddenly change shape. If the control slope of a PA has an inflection point within the output power control range, or if the slope is too steep, switching transients will result. In RF3158 all stages are kept constantly biased and the output power is controlled by changing the collector voltage according to Equation 1. Inflection points are eliminated by this design. In addition, the steepness of the power control slope is reduced because V_{RAMP} actively controls output power over a larger voltage range than many other power amplifiers.

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- Harmonics

  Harmonics are natural products of high efficiency, saturated power amplifiers. An ideal, class 'E', saturated power amplifier will produce a perfect square wave. Looking at the Fourier transform of a square wave reveals high harmonic content. Although this is common to all saturated power amplifiers, there are other factors that contribute to harmonic content as well. With many power control methods, a peak power detector is used to rectify and sense forward power. Through the rectification process, there is additional squaring of the waveform resulting in higher harmonics. The RF3158 has no need for the detector diode; therefore, the harmonics coming out of the PA should represent maximum power of the harmonics throughout the transmit chain. This is based on proper harmonic termination of the transmit port. The receive port termination on antenna switch as well as the harmonic impedance from the switch itself will have an impact on harmonics. These terminations should be adjusted to correct problems with harmonics.

- Multimode Operation

  When a GSM TDMA frame contains bursts of different modulation types (EDGE, GSM), a linear EDGE power amplifier must be ramped down, the mode changed, and the power ramped back up again during the guard period between bursts. This requires precise timing of control signals with less room for margin when compared to multiple timeslots with the same modulation. The RF3158 is designed to operate in different modes in adjacent timeslots provided that the control signals are properly applied. The system must be capable of controlling the RF input drive timing separately from the V_{MODE} and V_{RAMP} control signals. Failure to provide the proper timing will produce switching transients.

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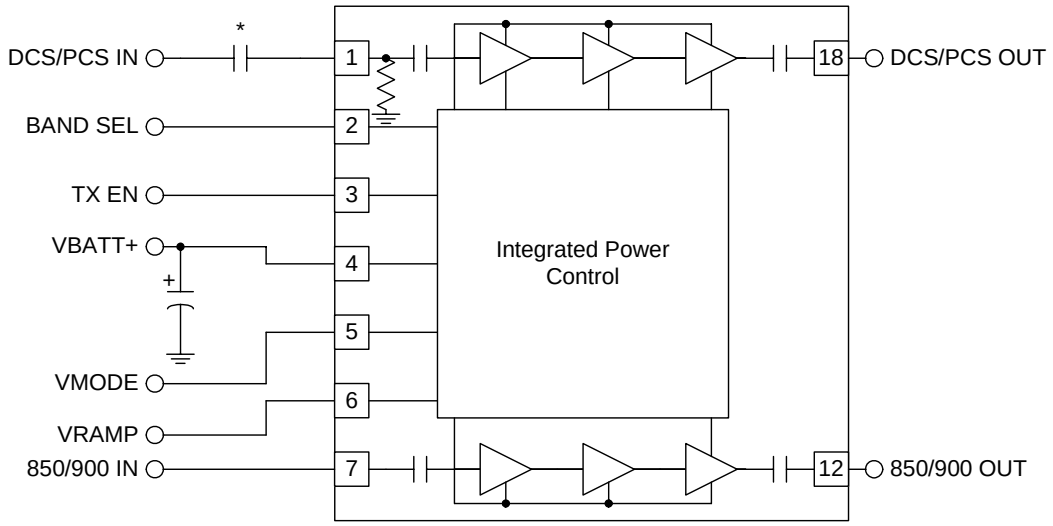
Application Schematic



*DC blocking capacitor required if Transceiver output is DC coupled.

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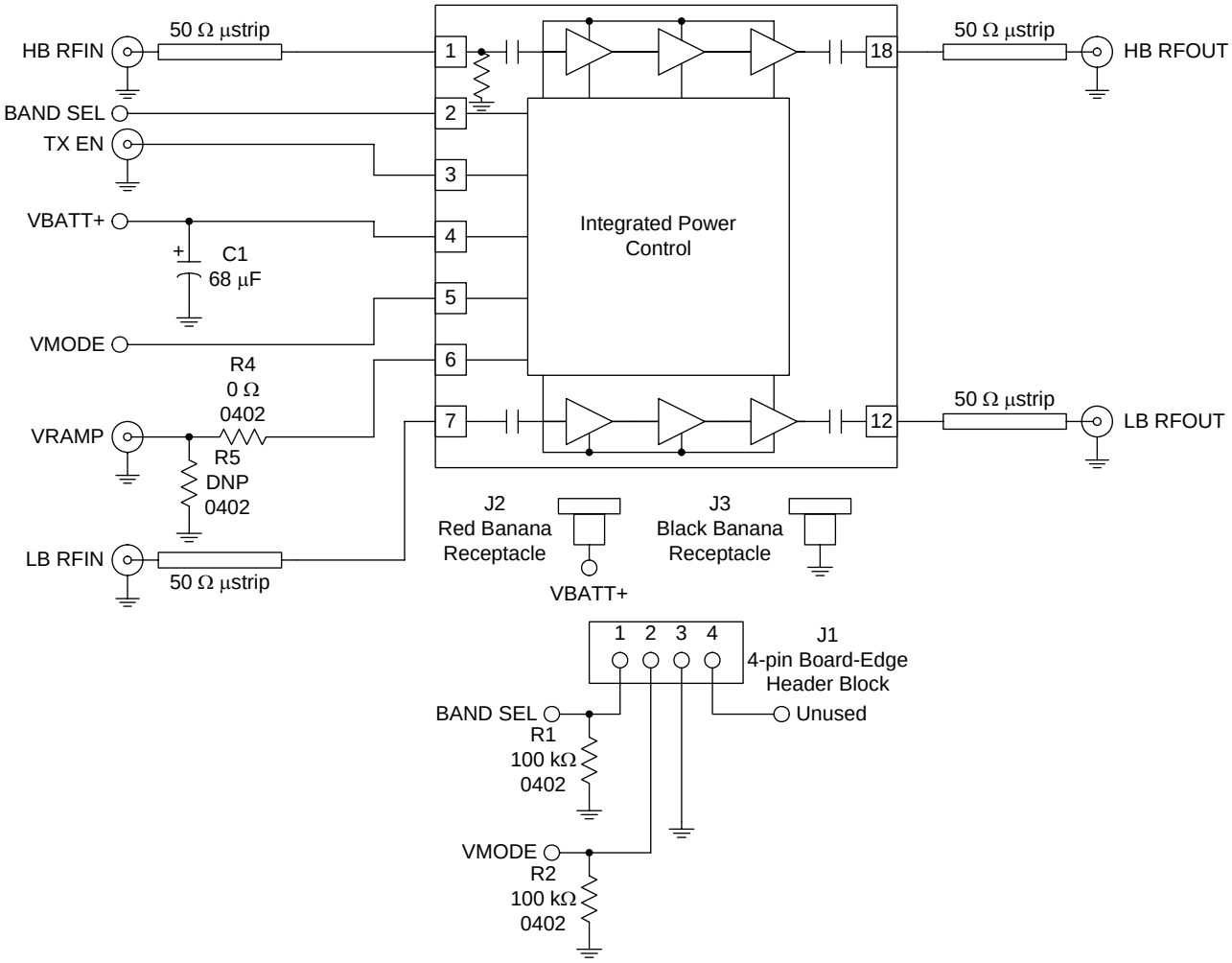
Evaluation Board Schematic



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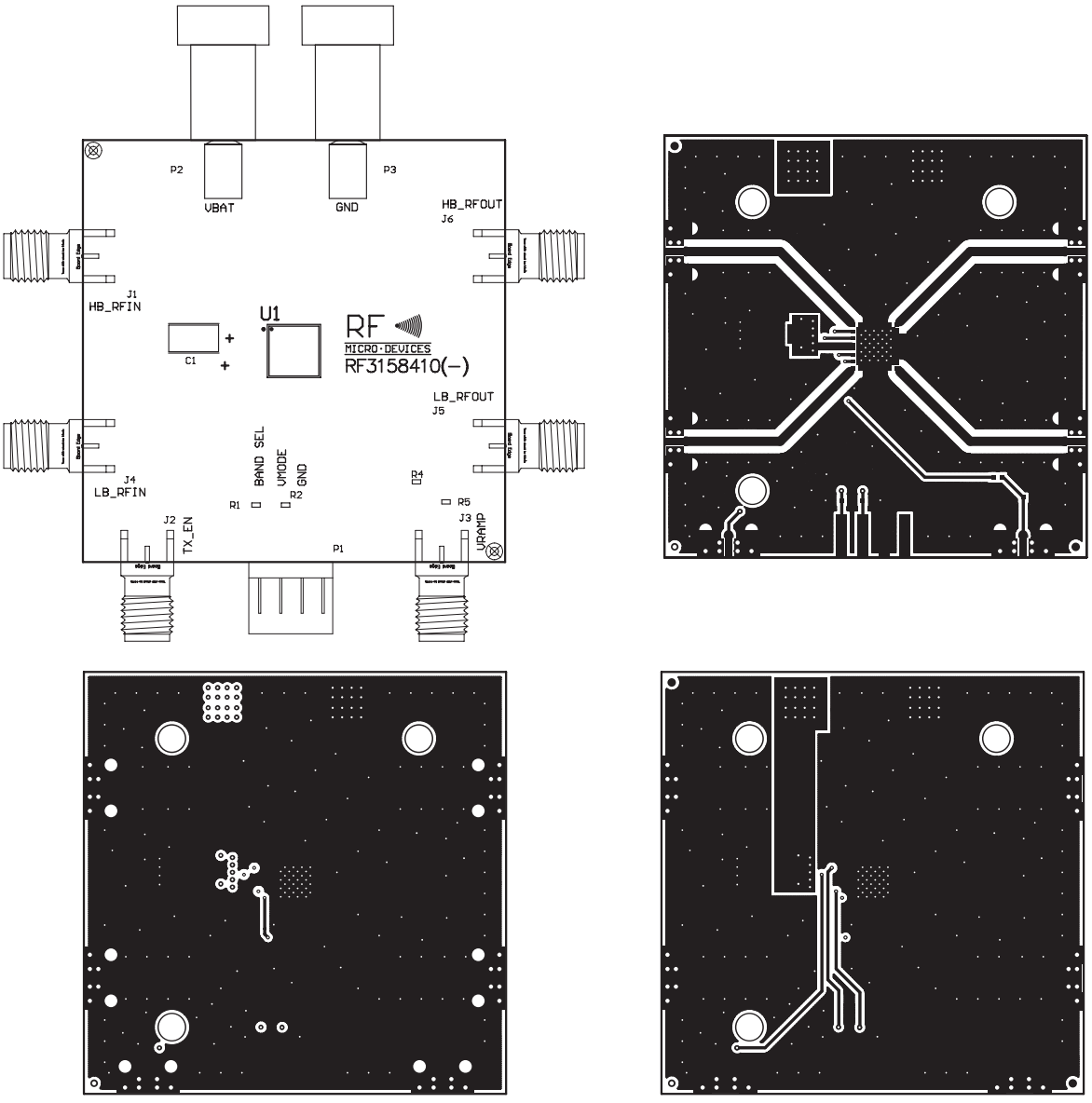
Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.046”, Board Material Rogers RO4003, Multi-Layer



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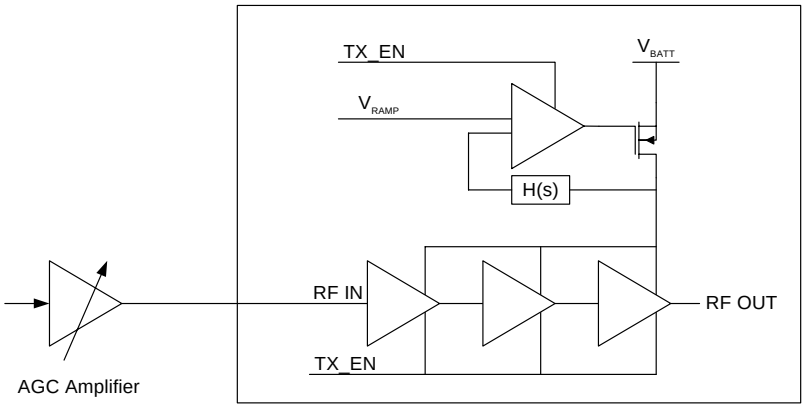
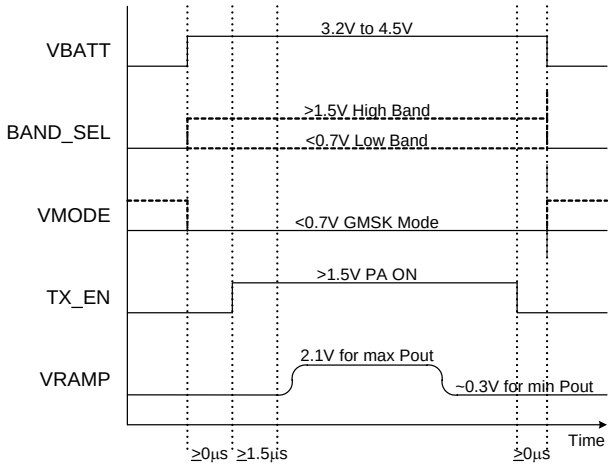
RF3158 Power Amplifier
Simplified Block Diagram of a Single Band



Power On Sequence

GMSK Power On/Off Sequence

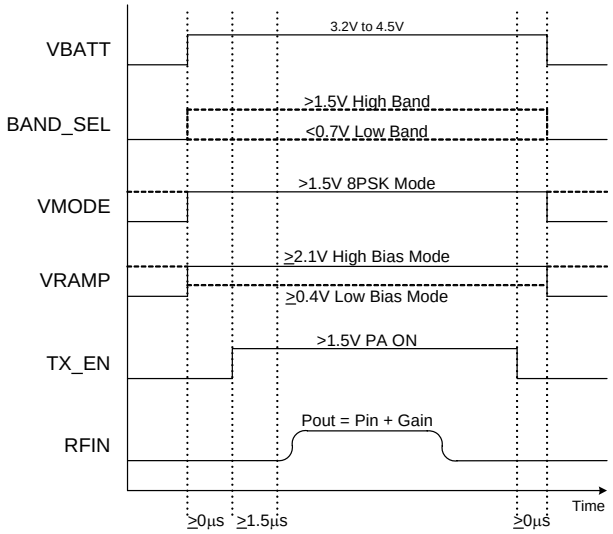


Power On Sequence:
1. Apply VBATT
2. Apply BAND_SEL
3. Apply Low on VMODE
4. Apply minimum VRAMP (~0.3V)
5. Apply TX_EN
6. Ramp VRAMP for desired output power

RFIN can be applied at any time. For good transient response it must be applied before power ramp begins.

The Power Down Sequence is the reverse order of the Power On Sequence.

8PSK Power On/Off Sequence



Power On Sequence:
1. Apply VBATT
2. Apply BAND_SEL
3. Apply High on VMODE
4. Apply bias control voltage on VRAMP
5. Apply TX_EN
6. Ramp RFIN amplitude for desired output power

The Power Down Sequence is the reverse order of the Power On Sequence.

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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

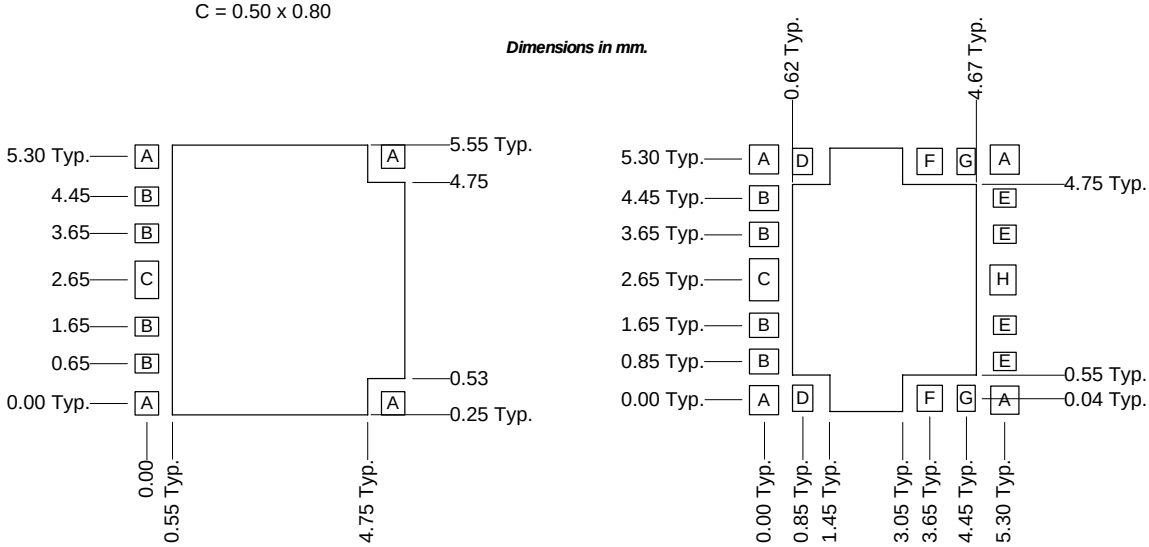
PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern

A = 0.64 Sq. Typ.
B = 0.64 x 0.54 Typ.
C = 0.64 x 0.94
D = 0.45 x 0.57 Typ.
E = 0.50 x0.40 Typ.
F = 0.55 x 0.57 Typ.
G = 0.40 x 0.57 Typ.
H = 0.57 x 0.65 Typ.

A = 0.50 Sq. Typ.
B = 0.50 x 0.40 Typ.
C = 0.50 x 0.80

Dimensions in mm.



Metal Land Pattern

Solder Mask Pattern

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RoHS* Banned Material Content

RoHS Compliant:	Yes
Package total weight in grams (g):	0.123
Compliance Date Code:	N/A
Bill of Materials Revision:	B
Pb Free Category:	e4

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Substrate	0	0	0	0	0	0
Passive Components	584	0	0	0	0	0
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

Pb noted in this material declaration is used in glass or ceramics in electronic components which is an allowed exemption from the RoHS regulations, see Annex to Directive 2002/95/EC and amendment 2005/747/EC.

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