



T-75-27-07  
**G8870-1**

## Microcircuits

### CMOS DTMF Integrated Receiver

#### Features

- CMOS technology for low power consumption—35 mW max.
- Full DTMF receiver
- Provides DTMF high and low group filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder functions
- On-chip differential amplifier, clock oscillator, and latched three-state bus.
- Uses inexpensive 3.58 MHz crystal
- Central office quality and performance
- Single +5 volt power supply
- 18-pin DIP or 20-pin PLCC package

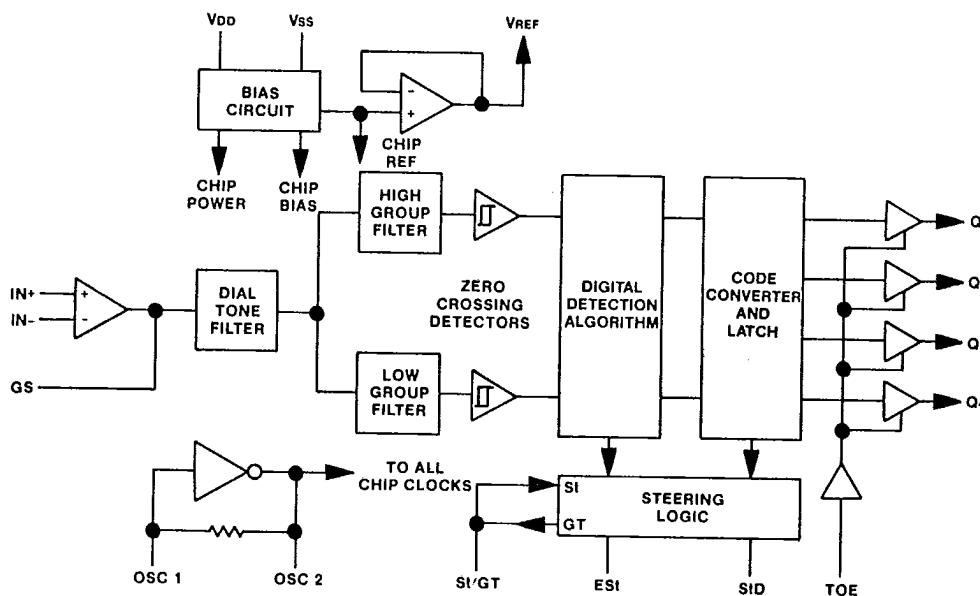
#### Applications

- PABX
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry
- Receiver system for Conference of European Postal and Telecommunications (CEPT), and British Telecom

#### General Description

The CMD G8870-1 provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP or 20-pin PLCC package. The G8870-1 is manufactured using state-of-the-art CMOS process technology for low power consumption (35 mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The G8870-1 decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The G8870-1 minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal as an external component.

#### Block Diagram





**Absolute Maximum Ratings: (Note 1)**

Parameter	Symbol	Value
Power Supply Voltage (V <sub>DD</sub> -V <sub>SS</sub> )	V <sub>DD</sub>	6.0V Max
Voltage on any Pin	V <sub>dc</sub>	V <sub>SS</sub> -0.3, V <sub>DD</sub> +0.3
Current on any Pin	I <sub>DD</sub>	10 mA Max
Operating Temperature	T <sub>A</sub>	-40° C to +85° C
Storage Temperature	T <sub>S</sub>	-65° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

**Notes:**

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

**DC Characteristics:** All voltages referenced to V<sub>SS</sub> unless otherwise noted. V<sub>DD</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 25° C.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltage	V <sub>DD</sub>	4.75		5.25	V	
Operating Supply Current	I <sub>DD</sub>		3.0	7.0	mA	
Power Consumption	P <sub>o</sub>		15	35	mW	f = 3.579 MHz; V <sub>DD</sub> = 5.0V
Low Level Input Voltage	V <sub>IL</sub>			1.5	V	
High Level Input Voltage	V <sub>IH</sub>	3.5			V	
Input Leakage Current	I <sub>IH</sub> /I <sub>IL</sub>			0.1	μA	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub> (Note 11)
Pull Up (Source) Current on TOE	I <sub>SO</sub>		6.5	15.0	μA	TOE = 0 V
Input Impedance, Signal Inputs 1,2	R <sub>IN</sub>	8	10		Meg Ω	@ 1KHz
Steering Threshold Voltage	V <sub>Tst</sub>	2.2		2.5	V	
Low Level Output Voltage	V <sub>OL</sub>			0.03	V	No Load
High Level Output Voltage	V <sub>OH</sub>	4.97			V	No Load
Output Low (Sink) Current	I <sub>OL</sub>	1.0	2.5		mA	V <sub>OUT</sub> = 0.4 V
Output High (Source) Current	I <sub>OH</sub>	0.4	0.8		mA	V <sub>OUT</sub> = 4.6 V
Output Voltage	V <sub>REF</sub>	V <sub>REF</sub>		2.7	V	No Load
Output Resistance		R <sub>OR</sub>		10	KΩ	

**Operating Characteristics:** All voltages referenced to V<sub>SS</sub> unless otherwise noted. V<sub>DD</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 25° C.

**Gain Setting Amplifier**

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current	I <sub>IN</sub>			±100	nA	V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub>
Input Resistance	R <sub>IN</sub>	10			MΩ	
Input Offset Voltage	V <sub>OS</sub>		±25		mV	
Power Supply Rejection	PSRR	50			dB	1 KHz (Note 12)
Common Mode Rejection	CMRR	55			dB	-3.0 V < V <sub>IN</sub> < 3.0V
DC Open Loop Voltage Gain	A <sub>VOL</sub>	60			dB	
Open Loop Unity Gain Bandwidth	f <sub>c</sub>	1.2	1.5		MHz	
Output Voltage Swing	V <sub>o</sub>	3.5			V <sub>p-p</sub>	R <sub>L</sub> ≥ 100KΩ to V <sub>SS</sub>
Tolerable Capacitive Load (GS)	C <sub>L</sub>			100	pF	
Tolerable Resistive Load (GS)	R <sub>L</sub>			50	KΩ	
Common Mode Range	V <sub>cm</sub>	2.5			V <sub>p-p</sub>	No Load

**AC Characteristics:** All voltages referenced to VSS unless otherwise noted. VDD = 5.0V, VSS = 0V, TA = 25°C, fCLK = 3.579545 MHz using test circuit (Fig. 1).

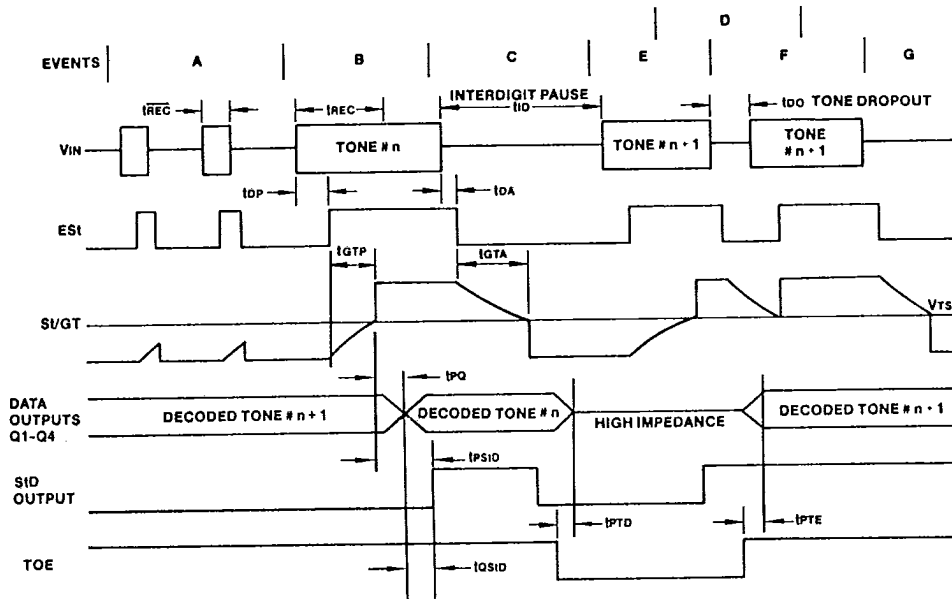
Parameter	Symbol	Min	Typ	Max	Units	Notes
Valid Input Signal Levels (each tone of composite signal)		-31		+1	dBm	1,2,3,4,5,8
		21.8		869	mVRMS	
Input Signal Level Reject		-37			dBm	1,2,3,4,5,8
		10.9			mVRMS	
Positive Twist Accept				10	dB	2,3,4,8
Negative Twist Accept				10	dB	
Freq. Deviation Accept Limit				1.5% · 2 Hz	Nom.	2,3,5,8,10
Freq. Deviation Reject Limit					Nom.	2,3,5
Third Tone Tolerance		-18.5	-16		dB	2,3,4,5,8,9,13,14
Noise Tolerance			-12		dB	2,3,4,5,6,8,9
Dial Tone Tolerance		+18	+22		dB	2,3,4,5,7,8,9
Tone Present Detection Time	tDP	5	8	14	mS	Refer to Timing Diagram
Tone Absent Detection Time	tDA	0.5	3	8.5	mS	
Min. Tone Duration Accept	tREC			40	mS	(User Adjustable) Times shown are obtained with circuit in Fig. 1
Max. Tone Duration Reject	tREJ	20			mS	
Min. Interdigit Pause Accept	tID			40	mS	
Max. Interdigit Pause Reject	tDR	20			mS	
Propagation Delay (St to Q)	tPQ		6	11	μS	TOE = VDD
Propagation Delay (St to StD)	tPSID		9		μS	
Output Data Set Up (Q to StD)	tQSID		4.0		μS	
Propagation Delay (TOE to Q)	Enable	tPTE	50	60	nS	RL = 10KΩ CL = 50pF
	Disable	tPTD	300		nS	
Crystal/Clock Frequency	fCLK	3.5759	3.5795	3.5831	MHz	
Clock Output (OSC2)	Capacitive Load	CLO		30	pF	

**NOTES:**

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE.
12. External voltage source used to bias VREF.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.



Timing Diagram



Explanation of Events

- A) Tone bursts detected, tone duration invalid, outputs not updated.
- B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.
- C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
- D) Outputs switched to high impedance state.
- E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
- F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
- G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

- VIN DTMF composite input signal.
- EST Early Steering Output. Indicates detection of valid tone frequencies.
- SVGT Steering input/guard time output. Drives external RC timing circuit.
- Q1-Q4 4-bit decoded tone output.
- STD Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
- TOE Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
- tREC Maximum DTMF signal duration not detected as valid.
- tREC Minimum DTMF signal duration required for valid recognition.
- tID Minimum time between valid DTMF signals.
- tOO Maximum allowable drop-out during valid DTMF signal.
- tDP Time to detect the presence of valid DTMF signals.
- tDA Time to detect the absence of valid DTMF signals.
- tGTP Guard time, tone present.
- tGTA Guard time, tone absent.

**Functional Description**

The CMD G8870-1 DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP or 20-pin PLCC package configuration. The G8870-1's internal architecture consists of a band-split filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

**Filter Section**

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

**Decoder Section**

The G8870-1 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (EST). Any subsequent loss of signal condition will cause Est to fall.

**Steering Circuit**

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by Est. A logic high on Est causes Vc (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (Est remains high) for the validation period (TGTF), Vc reaches the threshold (VTS1) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives Vc to VDD. GT continues to drive high as long as Est remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

**Guard Time Adjustment**

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} \approx 0.67 RC$$

The value of tDP is a parameter of the device and tREC is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a tREC of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present (tGTP) and tone-absent (tGTA). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing tREC improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short tREC with a long too would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

**Input Configuration**

The input arrangement of the G8870-1 provides a differential input operational amplifier as well as a bias source (VREF) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1 with the op-amp connected for unity gain and VREF biasing the input at 1/2VDD. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor Rs.

**DTMF Clock Circuit**

The internal clock circuit is completed with the addition of a standard television color burst crystal having a resonant frequency of 3.579545 MHz. A number of G8880 devices can be connected as shown in Figure 8 such that only one crystal is required.

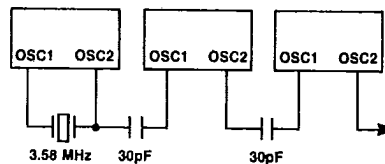


Figure 8. Common Crystal Connection



Pin Function Table

Name	Description
IN+	Non-inverting input
IN-	Inverting input
GS	Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.
VREF	Reference voltage output (nominally VDD/2). May be used to bias the inputs at mid-rail.
IC	Internal connection. Must be tied to Vss.
IC	Internal connection. Must be tied to Vss.
OSC1	Clock input
OSC2	Clock output
Vss	Negative power supply (Normally connected to 0V).
TOE	Three-state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull-up.
Q1	Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2.)
Q2	
Q3	
Q4	
StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V <sub>TSt</sub> .
ES <sub>t</sub>	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ES <sub>t</sub> to return to a logic low.
St/GT	Steering input/guard time output (bidirectional). A voltage greater than V <sub>TSt</sub> detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V <sub>TSt</sub> frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ES <sub>t</sub> and the voltage on St. (See Fig. 2.)
VDD	Positive power supply

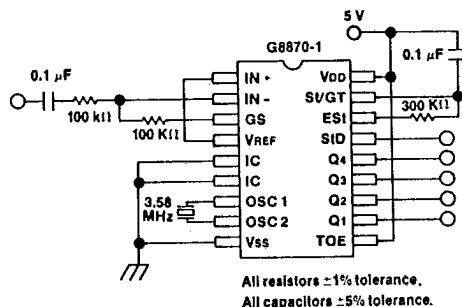


Figure 1. Single Ended Input Configuration Test Circuit

FLOW	FHIGH	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
—	—	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

Figure 2. Functional Decode Table

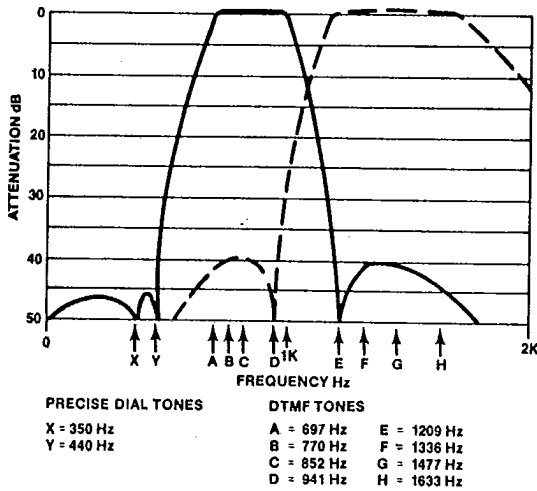


Figure 3. Typical Filter Characteristic

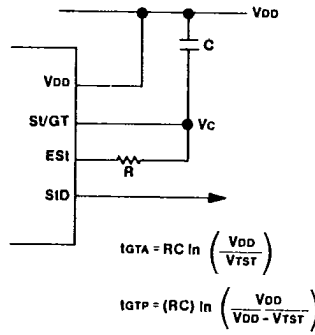


Figure 4. Basic Steering Circuit

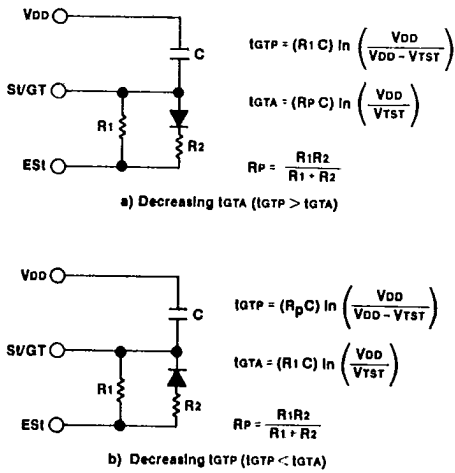
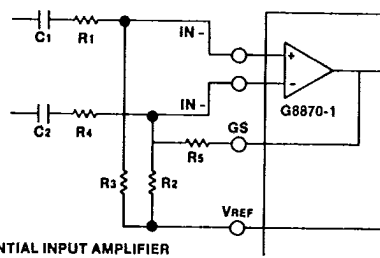


Figure 5. Guard Time Adjustment



DIFFERENTIAL INPUT AMPLIFIER

$C1 = C2 = 10 \text{ nF}$   
 $R1 = R4 = R5 = 100 \text{ K}\Omega$   
 $R2 = 60 \text{ K}\Omega, R3 = 37.5 \text{ K}\Omega$   
 $R3 = \frac{R2R5}{R2 + R5}$

VOLTAGE GAIN ( $Av \text{ diff}$ ) =  $\frac{R5}{R1}$

INPUT IMPEDANCE  
 $(Z_{INDIFF}) = 2 \sqrt{R1^2 + \left( \frac{1}{\omega C} \right)^2}$

All resistors are — 1% tolerance.  
 All capacitors are — 5% tolerance.

Figure 6. Differential Input Configuration

Application

Receiver System for British Telecom Spec POR 1151

The circuit shown in Fig. 8 illustrates the use of the G8870-1 device in a typical receiver system. The British Telecom specifications define the input signals less than -34 dBm as the non-operate level. This condition can be attained by choosing suitable values for R1 and R2 to provide 3 dB attenuation, such that the -34 dBm input signal will correspond to -37 dBm at the gain setting pin GS of the G8870-1. As shown in the diagram, the component values of R3 and C2 are the guard time requirement when the total component tolerance is 6%. For better performance, it is recommended to use the non-symmetric guard time circuit in Fig. 7.

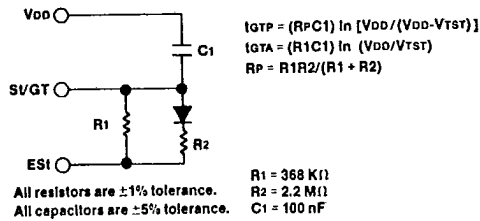


Figure 7. Non-Symmetric Guard Time Circuit

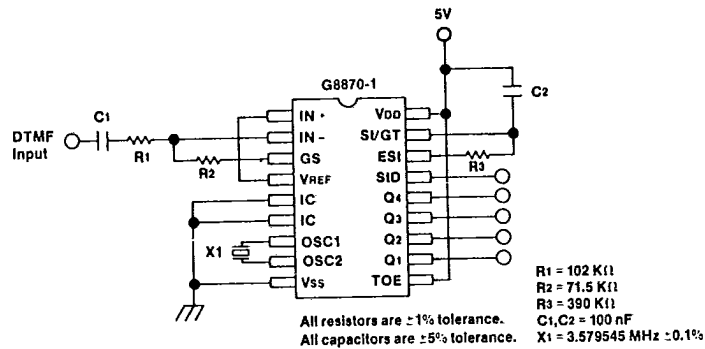


Figure 8. Single Ended Input Configuration for British Telecom or CEPT Specifications





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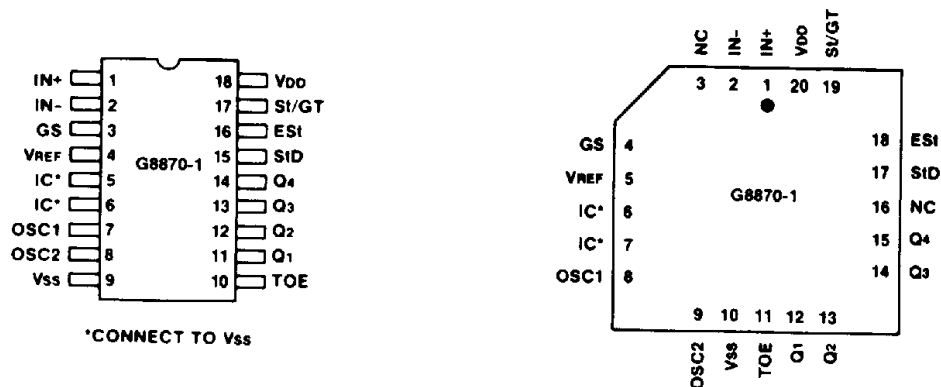
G8870-1

## Pin Function

Pin	Description
IN+	Non-Inverting Input
IN-	Inverting Input
GS	Gain Select
IC	Internal Connection
OSC1	Clock Input
OSC2	Clock Output
TOE	Three-State Output Enable

Pin	Description
Q1-4	Three-State Data Outputs
StD	Delayed Steering Output
ESi	Early Steering Output
St/GT	Steering Input/Guard Time Input
VREF	Reference Voltage Output
VSS	Negative Power Supply
VDD	Positive Power Supply

## Pin Configuration



## Ordering Information

