CMOS INTEGRATED DTMF RECEIVER- 3 VOLT VERSION

Features

- 2.7 to 3.6 volt operating range
- Full DTMF receiver
- Less than 18mW power consumption
- Industrial temperature range
- Uses quartz crystal or ceramic resonators
- Adjustable acquisition and release times
- 18-pin DIP, 20-pin QSOP, 18-pin SOIC, 20-pin PLCC, 20-pin TSSOP
- **CM88L70**
  - Power down mode
  - Inhibit mode
  - Buffered oscillator output (OSC 3) to drive other devices

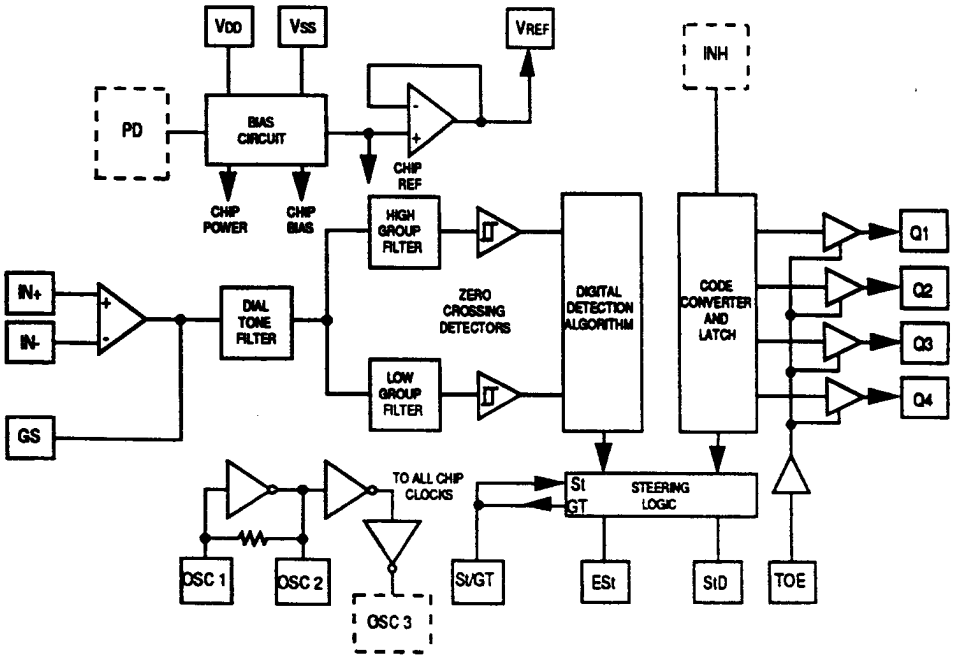
Applications

- PCMCIA
- Portable TAD
- Mobile radio
- Remote control
- Remote data entry
- Call limiting
- Telephone answering systems
- Paging systems

Product Description

The CMD CM88L70/70C provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin DIP, SOIC, or 20-pin PLCC, TSSOP, or QSOP package. The CM88L70/70C is manufactured using state-of-the-art CMOS process technology for low power consumption (35mW, max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The CM88L70/70C decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. This DTMF receiver minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal or ceramic resonator as an external component.

Block Diagram



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Absolute Maximum Ratings: (Note 1)

ABSOLUTE MAXIMUM RATINGS		
Parameter	**Symbol**	**Value**
Power Supply Voltage (V_{DD}-V_{SS})	V_{DD}	6.0V Max
Voltage on any Pin	V_t	V_{SS}-0.3V Min, V_{DD}+0.3V Max
Current on any Pin	I_t	10mA Max
Storage Temperature	T_S	-65°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to V_{SS}, V_{DD} = 3.0V + 20% / -10%, T_A = -40°C to +85°C unless otherwise noted.

DC CHARACTERISTICS							
Parameter		**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Operating Supply Voltage		V_{DD}	2.7	3.0	3.6	V	V
Operating Supply Current		I_{DD}		3.0	5.0	mA	
Standby Supply Current		I_{DDS}		5.0	10	µA	PD=V_{DD}
Low Level Input Voltage		V_{IL}			1.0	V	V_{DD}=3.0V
High Level Input Voltage		V_{IH}	2.0			V	V_{DD}=3.0V
Input Leakage Current		I_{IH}/ I_{IL}		0.1		µA	V_{IN}=V_{SS} or V_{DD} (Note #11)
Pull Up (Source) Current on TOE		I_{SO}	-12	-2.0		µA	TOE=0V
Pull down (sink) Current PD		I_{PD}		1.0	45	µA	PD=3.0V
Pull down (sink) Current INH		I_{INH}		1.0	45	µA	INH=3.0V
Input Impedance, (IN+, IN-)		R_{IN}		10		MΩ	@ 1KHz
Steering Threshold Voltage		V_{Tst}		1.5		V	
Low Level Output Voltage		V_{OL}		0.1	0.4	V	I_{OL}=1.0mA
High Level Output Voltage		V_{OH}	2.4	2.6		V	I_{OH}=-400µA
Output High (Source) Current		I_{OH}	1.0			mA	V_{OUT}=2.5V @ V_{DD}=2.7V
Output Voltage	V_{REF}	V_{REF}		1.5		V	No Load
Output Resistance	V_{REF}	R_{OR}		10		KΩ	

Operating Characteristics: All voltages referenced to V_{SS}, V_{DD} = 3.0V + 20% / -10%, T_A = -40°C to +85°C unless otherwise noted.

Gain Setting Amplifier

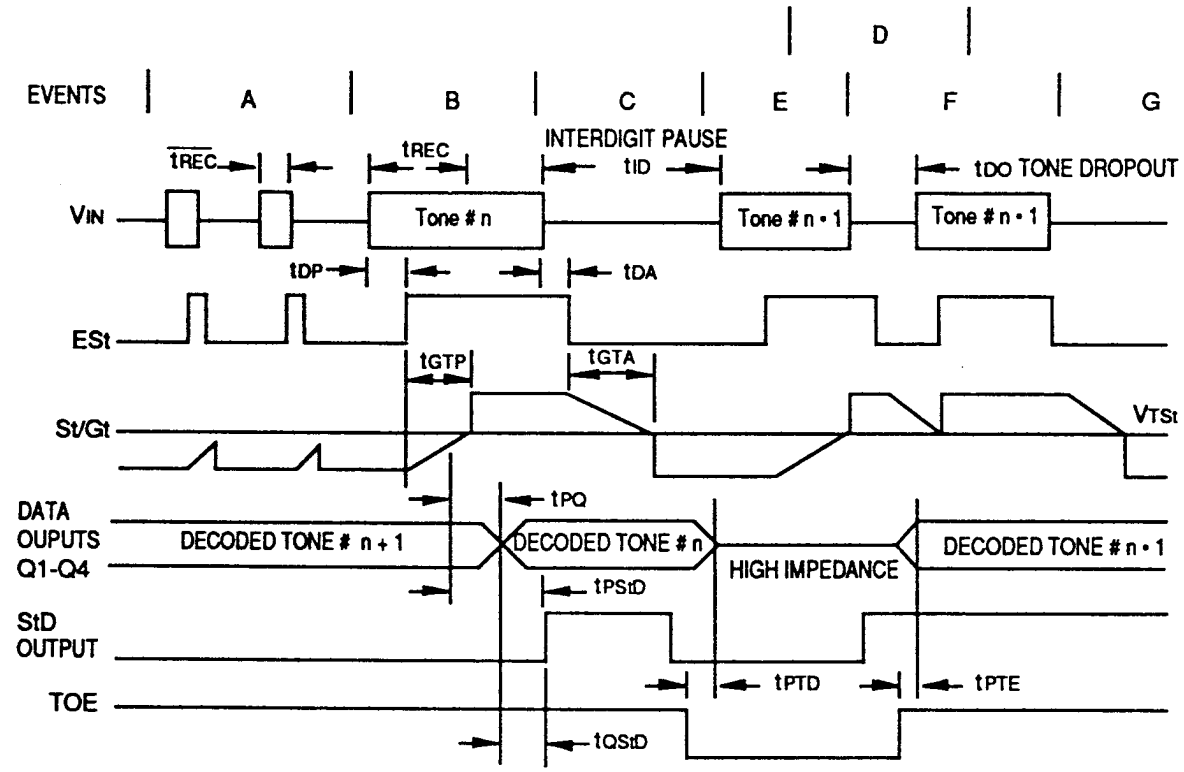
OPERATING CHARACTERISTICS						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input Leakage Current	I_{IN}		100		nA	V_{SS} < V_{IN} < V_{DD}
Input Resistance	R_{IN}		10		MΩ	
Input Offset Voltage	V_{OS}		15	25	mV	
Power Supply Rejection	PSRR	50	60		dB	1KHz (Note 12)
Common Mode Rejection	CMRR	40	60		dB	-3.0V < V_{IN} < 3.0V
DC Open Loop Voltage Gain	A_{VOL}	32	65		dB	
Open Loop Unity Gain Bandwidth	fc	0.3	1.0		MHz	
Output Voltage Swing	V_O		2.2		Vp-p	R_L ≥ 100KΩ to V_{SS}
Tolerable Capacitive Load (GS)	C_L			100	pF	
Tolerable Resistive Load (GS)	R_L				KΩ	
Common Mode Range	Vcm	5.0	1.5		Vp-p	No Load

AC Characteristics: All voltages referenced to V_{SS}, V_{DD}=3.0V + 20% / -10%, T_A=-40°C to +85°C, f_{CLK}=3.579545 MHz using test circuit (Fig. 1) unless otherwise noted.

AC CHARACTERISTICS							
Parameter		**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Valid Input Signal Levels (each tone of composite signal)			-36		-6.4	dBm	1,2,3,4,5,8
			12.3		370	mV_{RMS}	
Positive Twist Accept					6	dB	
Negative Twist Accept					6	dB	
Freq. Deviation Accept Limit					1.5%±2 Hz	Nom.	2,3,5,8,10
Freq. Deviation Reject Limit			±3.5%			Nom.	2,3,5
Third Tone Tolerance				-16		dB	2,3,4,5,8,9,13,14
Noise Tolerance				-12		dB	2,3,4,5,6,8,9
Dial Tone Tolerance				+22		dB	2,3,4,5,7,8,9
Tone Present Detection Time		t_{DP}	5	8	14	mS	Refer to Timing Diagram
Tone Absent Detection Time		t_{DA}	0.5	3	8.5	mS	
Min. Tone Duration Accept		t_{REC}			40	mS	(User Adjustable) Times shown are obtained with circuit in Fig. 1)
Max. Tone Duration Reject		t_{REC}	20			mS	
Min. Interdigit Pause Accept		t_{ID}			40	mS	
Max Interdigit Pause Reject		t_{DO}	20			mS	
Propagation Delay (St to Q)		t_{PQ}		13		µS	TOE=V_{DD}
Propagation Delay (St to StD)		$t_{PS}t_D$		8		µS	
Output Data Set Up (Q to StD)		$t_{QS}t_D$		3.4		µS	
Propagation Delay (TOE to Q)	Enable	t_{PTE}		200		nS	R_L=10KΩ C_L=50pF
	Disable	t_{PTD}		500		nS	
Crystal/Clock Frequency		f_{CLK}	3.5759	3.5795	3.5831	MHz	
Clock Output (OSC 2)	Capacitive Load	C_{LO}			30	pF	

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gaussian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%.
8. For an error rate of better than 1 in 10,000
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
11. Input pins defined as IN+, IN-, and TOE.
12. External voltage source used to bias V_{REF}.
13. This parameter also applies to a third tone injected onto the power supply.
14. Referenced to Figure 1. Input DTMF tone level at -28 dBm.

Timing Diagram



Explanation of Events

A) Tone bursts detected, tone duration invalid, outputs not updated.
B) Tone #n detected, tone duration valid, tone decoded and latched in outputs.
C) End of tone #n detected, tone absent duration valid, outputs remain latched until next valid tone.
D) Outputs switched to high impedance state.
E) Tone #n + 1 detected, tone duration valid, tone decoded and latched in outputs (currently high impedance).
F) Acceptable dropout of tone #n + 1, tone absent duration invalid, outputs remain latched.
G) End of tone #n + 1 detected, tone absent duration valid, outputs remain latched until next valid tone.

Explanation of Symbols

V_{IN}	DTMF composite input signal.
ESt	Early Steering Output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
Q1-Q4	4-bit decoded tone output.
StD	Delayed Steering Output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
TOE	Tone Output Enable (input). A low level shifts Q1-Q4 to its high impedance state.
t_{REC}	Maximum DTMF signal duration not detected as valid.
t_{REC}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid DTMF signals.
t_{DO}	Maximum allowable drop-out during valid DTMF signal.
t_{DP}	Time to detect the presence of valid DTMF signals.
t_{DA}	Time to detect the absence of valid DTMF signals.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

Functional Description

The CMD CM88L70/70C DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP, SOIC, or 20-pin PLCC, TSSOP, or QSOP package configuration. The CM88L70/70C's internal architecture consists of a bandsplit filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The CM88L70/70C decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by E_{St}. A logic high on ESt causes V_C (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives VC to V_{DD}. GT continues to drive high as long as ESt remains high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$t_{REC} = t_{DP} + t_{GTP}$
$t_{GTP} \approx 0.67\ RC$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guardtimes for tone-present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the CM88L70/70C provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1, with the op-amp connected for unity gain and VREF biasing the input at ½ V_{DD}. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R5.

Clock Circuit

The internal clock circuit is completed with the addition of a standard television color burst crystal or ceramic resonator having a resonant frequency of 3.579545 MHz. The CM8870C in a PLCC package has a buffered oscillator output (OSC3) that can be used to drive clock inputs of other devices such as a microprocessor or other CM887X's as shown in Figure 7. Multiple CM88L70/70Cs can be connected as shown in figure 8 such that only one crystal or resonator is required.

Power Down and Inhibit Mode

A logic high applied to pin 6 (PD) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C and D. The output code will remain the same as the previous detected code (see Figure 2).

Pin Function Table

Name	Description	
IN+ IN-	Non-inverting input Inverting input	Connection to the front-end differential amplifier
GS	Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.	
V_{REF}	Reference voltage output (nominally $V_{DD}/2$). May be used to bias the inputs at mid-rail.	
INH	Inhibits detection of tones represents keys A,B,C,D.	
OSC 3	Digital buffered oscillator output.	
PD	Power down	Logic high powers down the device and inhibits the oscillator.
OSC1	Clock input	3.579545 MHz crystal connected between these pins completes internal oscillator.
OSC2	Clock output	
V_{SS}	Negative power supply (normally connected to 0V).	
TOE	Three-state output enable (input). Logic high enables the outputs Q_1-Q_4. Internal pull-up.	
Q_1 Q_2 Q_3 Q_4	Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2).	
StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V_{TSt}.	
ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
St/Gt	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Fig. 2)	
V_{DD}	Positive power supply.	
IC	Internal connection. Must be tied to V_{SS} (for 8870 configuration only)	

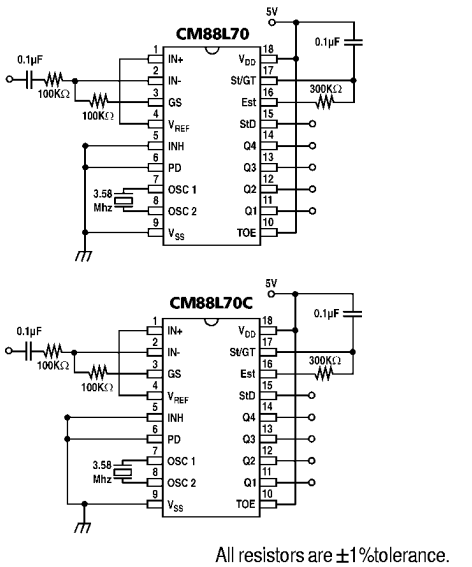


Figure 1. Single Ended Input Configuration

F_{LOW}	F_{HIGH}	KEY	TOW	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1209	0	H	1	0	1	0
941	1336	•	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z
L = Logic Low, H = Logic High, Z = High Impedance							

Figure 2. Functional Diode Table

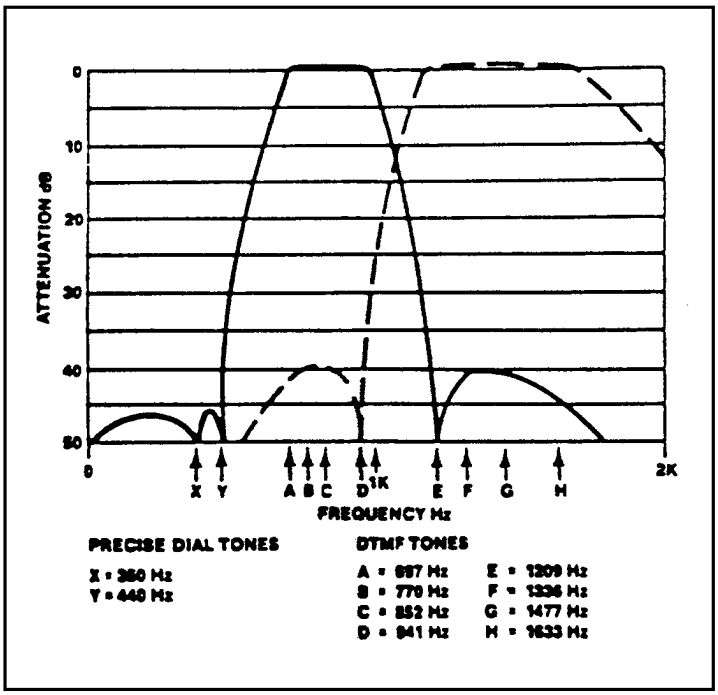


Figure 3. Typical Filter Characteristic

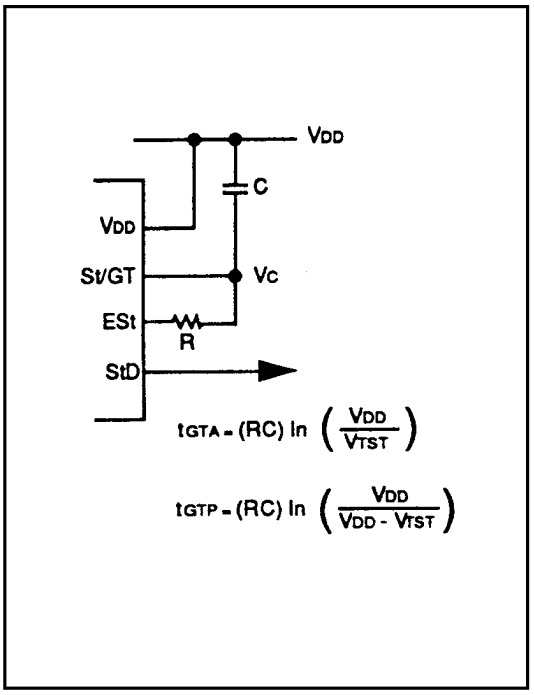


Figure 4. Basic Steering Circuit

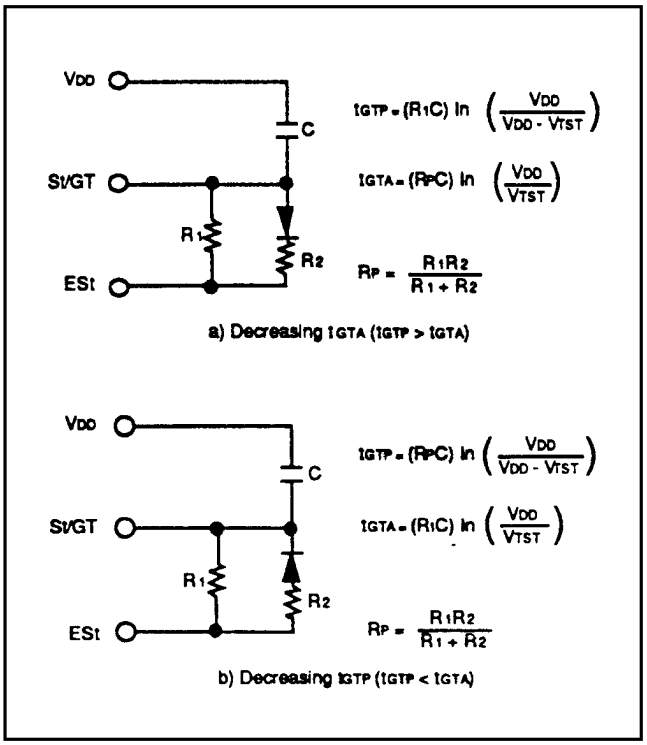


Figure 5. Guard Time Adjustment

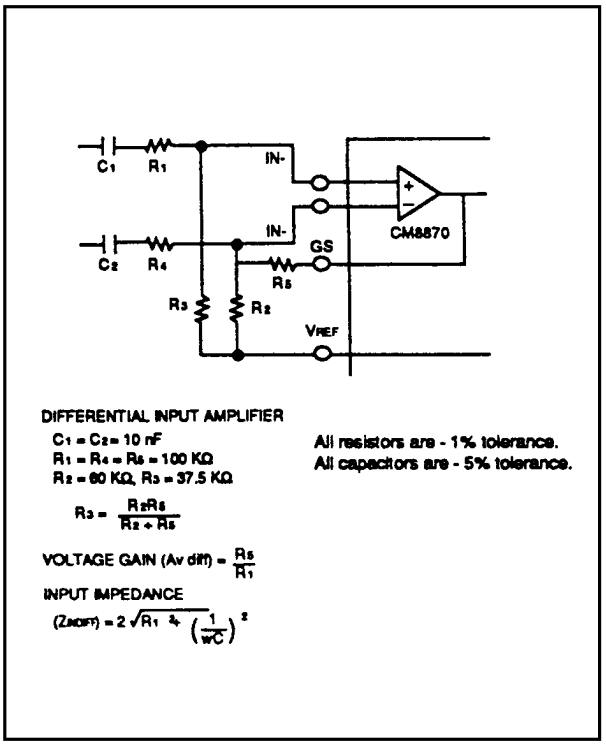


Figure 6. Differential Input Configuration

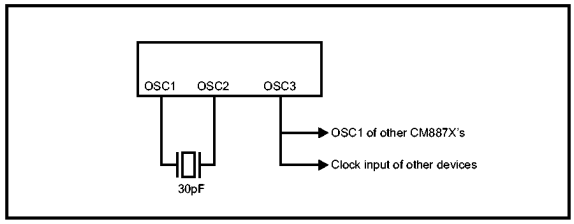


Figure 7. CM88L70C Crystal Connection (PLCC Package Only)

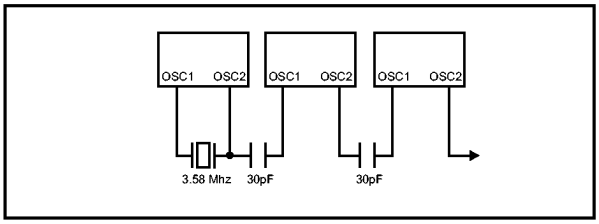
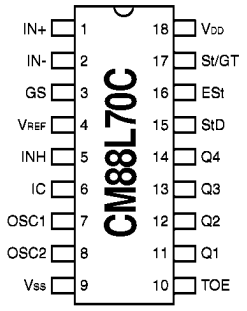
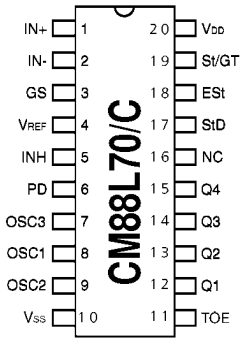


Figure 8. CM88L70/70C Crystal Connection

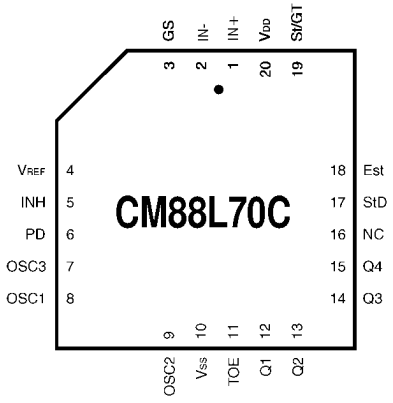
Pin Assignments



P — Plastic DIP (18)
S — SOIC (18)



TS — TSSOP (20)
Q — QSOP (20)



PE — PLCC (20)

Ordering Information

Example: CM88L70 / CM88L70C — P — I

Product Identification Number

Package

P — Plastic DIP (18)
PE — PLCC (20)
S — SOIC (18)
TS — TSSOP (20)
Q — QSOP (20)

Temperature/Processing

None — 0°C to +70°C, ±5% P.S. Tol.
I — -40°C to +85°C, ±5% P.S. Tol.