AT1212

OC-12 Multi-Service ADM

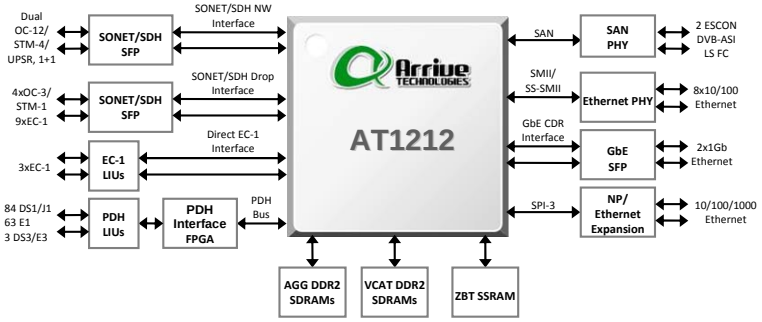
Rev. 1.3 – May 2008 **Preliminary Short Data Sheet**

INTRODUCTION

The AT1212 is a highly integrated OC-12/STM-4 Multiservice Add/Drop Multiplexer on a chip. The AT1212 has integrated cross-connects supporting DS0, VT/TU/TU3 and STS/VC level switching. The AT1212 provides a multi-format and multi-rate Ethernet and common legacy data over PDH, PDH mapped to SONET/SDH or direct SONET mapping. On the PDH side, the chip provides a parallel multiplexed PDH bus carrying 3 DS3s or 3 E3s or 84 DS1s or 63 E1s or any mixture of them. The 84/63 DS1/E1s signals can be accessed directly via the PDH bus or be multiplexed to 3 channelized DS3/E3s via 3 embedded M13/E13 engines or mapped to SONET/SDH. The chip supports a dual OC-12/STM-4 SONET/SDH interface with 1+1 or UPSR/SNCP hardware controlled protection. On the Ethernet side, the chip provides 8 Fast Ethernets via a SMII/SS-SMII bus and 2 Gigabit Ethernet ports with on-chip CDRs. It also supports an OIF SPI-3 bus to support external devices such as a Network Processor to provide extended L2+ or L3 level processing or expansion of the Ethernet ports. The AT1212 supports ATM, GFP-T/F, HDLC, PPP and LAPS encapsulation. A Traffic Aggregation and Management at Layer 2 for VLAN/MPLS with Classifying, Policing, Queuing, Shaping, and Scheduling is provided. It provides direct SONET/SDH mapping, SONET/SDH/PDH virtual concatenation (VCAT) and LCAS with 128 groups in accordance with G.7041, G.8040, G.7042 and G.7043. A serial port is provided for ESCON, DVB-ASI or low speed Fiber Channel SAN applications.

APPLICATIONS

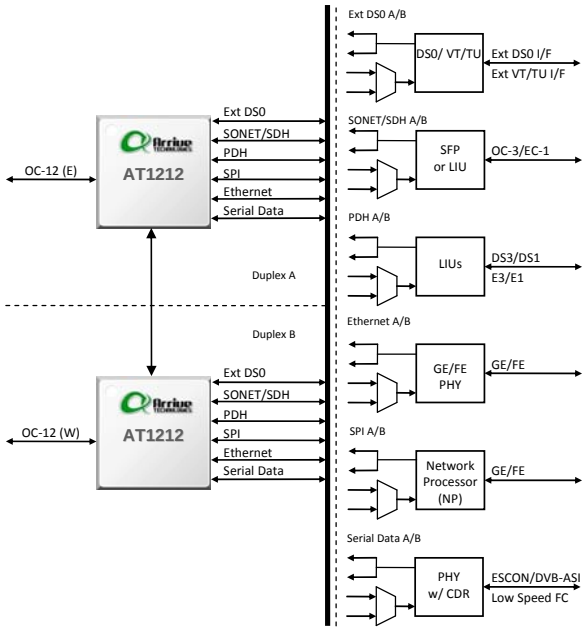
- Next Generation MSPP, MSTP or ADM systems
- Next Generation ultra low cost micro and pizza box MSPPs/ADMs
- SONET/SDH Enterprise Customer Premises Equipment with integrated ADM/MSPP
- Line-cards for SONET/SDH Switches and Cross-connects
- Multi-rate/multi-format Mapping of Ethernet over PDH or PDH/SONET/SDH
- Ideal for cost sensitive wireless backhaul and Ethernet/PDH private line backhaul systems



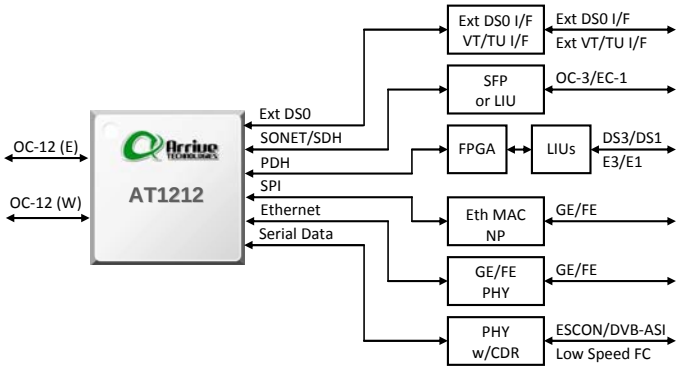
KEY FEATURES

- 622 Mbps SONET/SDH Data & PDH Multi-Service ADM on a chip
- 2xOC-12/STM-4 SONET/SDH network interfaces
- 4xOC-3/STM-1 SONET/SDH drop interfaces
- 622Mbps SONET/SDH drop muxed interface for 9xEC-1
- 3xEC-1 serial drop interfaces
- Supports Hardware based APS for Linear and UPSR/SNC
- Includes STS/VC, TU3, VT1.5/VT2/VT3/VT6/ TU11/TU12/TU2, and 8K-DS0 cross-connects
- Integrated Fast Ethernet and Gigabit Ethernet, FC/FICON/ESCON and DVB-ASI ports
- Supports 128 SONET/SDH HI/LO and PDH VCAT Groups with LCAS
- Transparent and Frame GFP mapping
- OIF SPI-3 port with up to 128 logical channels
- Integrated 3xDS3/E3 and 84/63xDS1/E1 framers
- Integrated Network side framers for 2xOC-12/STM-1s
- Integrated Drop side framers for 4xOC-3/STM-1s, and 12 EC-1s
- Traffic Aggregation and Management at Layer 2 for VLAN/MPLS with Classifying, Policing, Queuing, Shaping and Scheduling
- E-LAN/VPLS is supported via an external FPGA or ASIC connected at SPI-3 port
- Integrated system synchronization
- 2x16Mx16 DDR2 SDRAM for VCAT delay compensation (can be eliminated if VCAT is not utilized)
- 3x32Mx16 DDR2 SDRAM for Data Aggregation buffer (can be eliminated if Data Aggregation is not utilized)
- 1x512Kx36 ZBT SSRAM for hardware status
- Provided in an HFC-BGA1296 package
- Typical power consumption is 5-7 watts

Duplex Micro-MSPP



Simplex Micro-MSPP



SYSTEM FEATURES

- 2 OC-12/STM-4 Network Interface ports with on-chip CDR
- 4 individual OC-3/STM-1 ports with on-chip CDR
- 1x622Mbps drop muxed port with on-chip CDR for 9xEC-1
- 3 serial EC-1 ports with on-chip B3ZS Encoder/Decoder
- SONET/SDH Section/Line Overhead Processor
- Hardware based Line and Path APS for SONET/SDH
- SONET/SDH Line BER monitoring (10^{-3} to 10^{-9})
- Full SONET/SDH TOH Transparency
- STS/VC Pointer Processor with standard and random concatenations
- TU3 Pointer Processor
- VT/TU Pointer Processor with standard and random concatenations
- Hi-order/Lo-order 511-channel POH Processor pool
- 511-channel Tandem Connection Monitor pool
- SONET/SDH Hi-order/Lo-order 511-channel BER monitor pool (10^{-3} to 10^{-9})
- Flexible TOH and POH Add/Drop port
- 135x135 STS/VC High Order Cross-connect
- 2100x2100 VT/TU Low Order Cross-connect
- 36x36 TU3 Cross-connect
- 8K DS0s and associated Signaling Cross-connect
- 512-channel HDLC pool of DCC, PDH Facility Data Link, CCS channel, Local Data Link, and Redundancy Data Link
- Clock synthesizer and system active/standby synchronizer

DATA FEATURES

- 2 GbE ports with on-chip 1.25Gbps CDR
- 2 ESCON/DVB-ASI/FICON/Low-speed FC (200/270/540Mbps) ports with serial clock and data interface
- 8 Fast Ethernet ports via SMII or SS-SMII
- OIF SPI-3 Interface up to 128 physical ports with programmable data segmentation of 64 or 128 bytes
- Ethernet MAC controller with flow control including jumbo frame
- Support 802.3ah Ethernet OAM processing and loopback
- 128 Hi/Lo-Order/PDH VCAT channels
- Supports VCAT differential delay with up to 256ms for Hi/Lo-Order, up to 384ms for DS1s, up to 256ms for E1/E3s and up to 217ms for DS3s
- Supports LCAS with hitless add/remove and fault isolation
- GFP-T/F, PPP/HDLC, LAPS and ATM encapsulation
- TUG-3 (SDH concatenation with both VC-4-Xv and VC-3-Xv) supported
- Support EoS/EoPDH/EoPoS with or without Data Aggregation
- Traffic Aggregation and Management at Layer 2 for VLAN/MPLS with Classifying, Policing, Queuing, Shaping, and Scheduling
- Large DDR2 SDRAM for Packet Buffers

PDH FEATURES

- Multiplexed 3 DS3/E3s, or 84 DS1s, or 63 E1s or any mixed PDH bus
- 3 DS3 C-bit Parity and DS3 M13 multiplexing
- 3 E3 G.832 and E3 G.751 E13 multiplexing
- Asynchronous mapping 3 DS3/E3 to 3 STS-1/VC-3 SPE
- 84 DS1 SF/ESF/SLC-96/DDS Framers supporting J1 and SF/ESF
- 63 E1 basic frame or CRC-4 multi-frame framers
- Synchronous/Asynchronous mapping 84/63 DS1/E1 to VT1.5/VT2 (or TU-11/TU-12)
- 8064-DS0 Signaling Processor for Signaling Scan and Dial Pulse Collection
- DS3/E3, DS1/E1 LCV-based BER monitoring (10^{-3} to 10^{-9})
- PDH thru path Jitter Attenuation
- PDH transmultiplexing to/from SONET/SDH
- PDH VCAT and LCAS in compliance with G.7043

BLOCK DIAGRAM