AT1230

OC-12/3 PDH Mapper/ADM

Rev. 1.0 – Jan 2009 **Preliminary Short Data Sheet**

INTRODUCTION

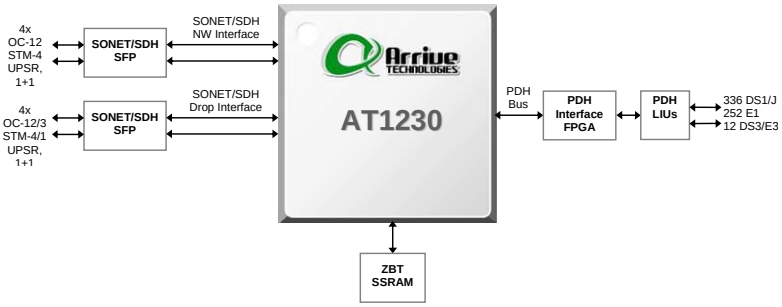
The AT1230 is a highly integrated OC-12/STM-4 or OC-3/STM-1 Add/Drop Multiplexer and PDH Mapper on a chip. The AT1230 has integrated cross-connects supporting DS0, VT/TU/TU3 and STS/VC level switching. On the SONET/SDH side, the chip provide 4 OC-12/STM-4 and 4 OC-12/3/STM-4/1 interfaces with on-chip CDR. On the PDH side, the chip provides a parallel multiplexed PDH bus carrying 12 DS3s or 12 E3s or 336 DS1s or 252 E1s, or any mixture of them. A simple FPGA is used to convert parallel DS1/E1/DS3/E3 signals on the PDH bus to the serial signals required for the LIUs for pin count expansion. The 336DS1/252E1s signals can be accessed directly on the PDH bus or be multiplexed to 12 channelized DS3/E3s via 12 embedded M13/E13 engines or mapped to SONET/SDH. The chip supports SONET/SDH interface with 1+1 protection, UPSR and mapping of DS1/E1/DS3/E3 to SONET/SDH. The AT1230 includes flexible channel assignment for all applicable SDH and SONET mappings.

APPLICATIONS

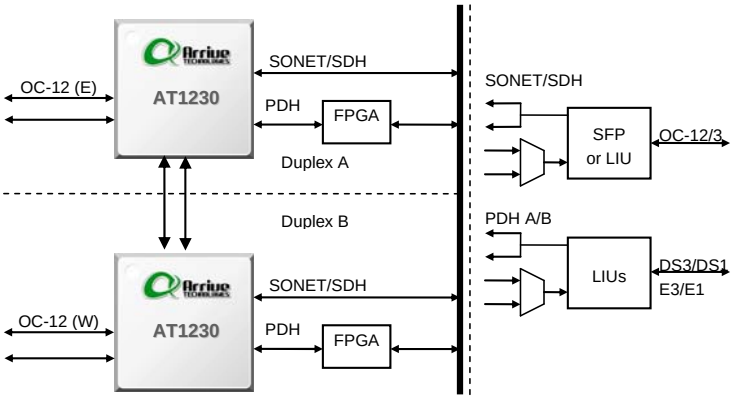
- Wireless Backhaul
- PDH Private Line Backhaul Systems
- Low cost micro and pizza box ADM
- SONET/SDH Enterprise CPE
- SONET/SDH Cross Connects
- SONET/SDH Switches
- Multi-rate/multi-format Mapping of PDH over SONET/SDH
- RNC and Voice Gateways

KEY FEATURES

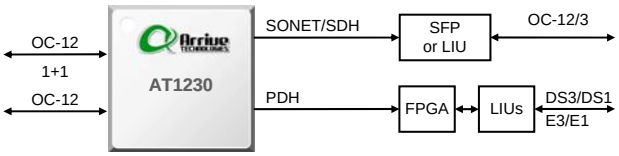
- 2.5Gbps/622Mbps SONET/SDH PDH ADM/Mapper on a chip
- 4xOC-12/STM-4 SONET/SDH network interfaces
- 4xOC-12/STM-1 or OC-3/STM-1 SONET/SDH drop interfaces
- Supports Hardware based APS for Linear and Ring networks including UPSR/SNCP
- Includes STS/VC, TU3, VT1.5/VT2/VT3/VT6/ TU11/TU12/TU2 Cross-connects
- Integrated 12xDS3/E3 and 336/252xDS1/E1 framers
- Integrated Network side framers for 4xOC-12/STM-4s
- Integrated Drop side framers for 4xOC-12/STM-4, 4xOC-3/STM-1s
- Integrated system synchronization
- 1x512Kx36 ZBT SSRAM for hardware status
- Provided in an HFC-BGA1296 package
- Typical power consumption is 4.8 watts



Duplex ADM



Simplex ADM



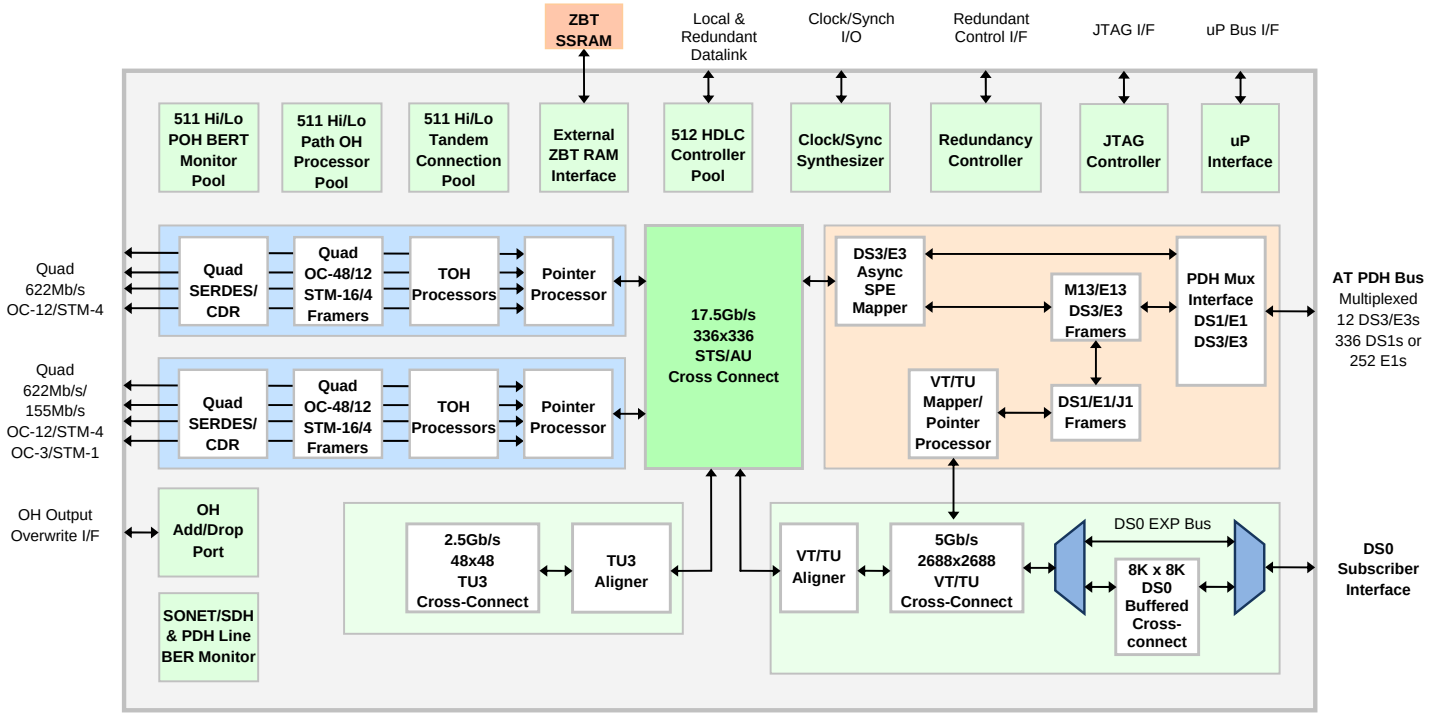
SYSTEM FEATURES

- 4 OC-12/STM-4 Network Interface ports with on-chip CDR
- 4 individual OC-12/STM-4/OC-3/STM-1 ports with on-chip CDRs
- SONET/SDH Section/Line Overhead Processor
- Hardware based Line and Path APS for SONET/SDH
- SONET/SDH Line BER monitoring (10-3 to 10-9)
- Full SONET/SDH TOH Transparency
- STS/VC Pointer Processor with standard and random concatenations
- TU3 Pointer Processor
- VT/TU Pointer Processor with standard and random concatenations
- Hi-order/Lo-order 511-channel POH processor pool
- 511-channel Tandem Connection Monitor pool
- SONET/SDH Hi-order/Lo-order 511-channel BER monitor pool (10-3 to 10-9)
- Flexible TOH and POH Add/Drop port
- 336x336 STS/VC High Order Cross-connect
- 2688x2688 VT/TU Low Order Cross-connect
- 48x48 TU3 Cross-connect
- 8K DS0s and associated Signaling Cross-connect with 168/126 DS1/E1 slip buffers
- 512-channel HDLC pool of DCC, PDH Facility Data Link, CCS channel, Local Data Link, and Redundancy Data Link
- Clock synthesizer and system active/standby synchronizer

PDH FEATURES

- Multiplexed 12 DS3/E3s, or 336 DS1s, or 252 E1s or any mixed PDH bus
- 12 DS3 C-bit Parity and DS3 M13 multiplexing
- 12 E3 G.832 and E3 G.751 E13 multiplexing
- Asynchronous mapping 12 DS3/E3 to 12 STS-1/VC-3 SPE
- 336 DS1 SF/ESF/SLC-96/DDS Framers supporting J1 and SF/ESF
- 252 E1 basic frame or CRC-4 multi-frame framers
- Synchronous/Asynchronous mapping 336/252 DS1/E1 to VT1.5/VT2 (or TU-11/TU-12)
- DS3/E3, DS1/E1 LCV-based BER monitoring (10-3 to 10-9)
- PDH through path Jitter Attenuation
- PDH transmultiplexing to/from SONET/SDH

BLOCK DIAGRAM



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