RF3000

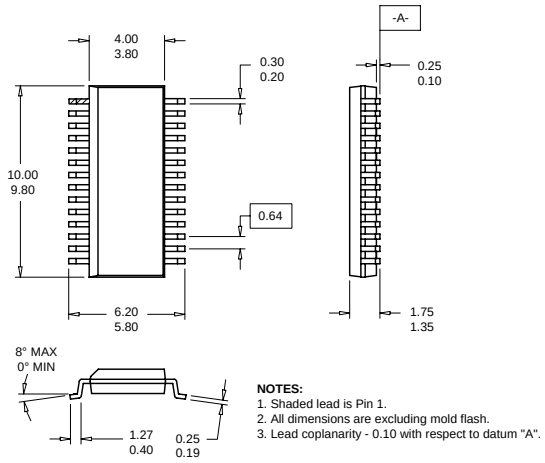
SPREAD-SPECTRUM BASEBAND MODEM

Typical Applications

- IEEE802.11b Wireless LAN Systems
- ISM Band Systems
- Direct Sequence Systems
- Wireless Modems
- Wireless Point-to-Point

Product Description

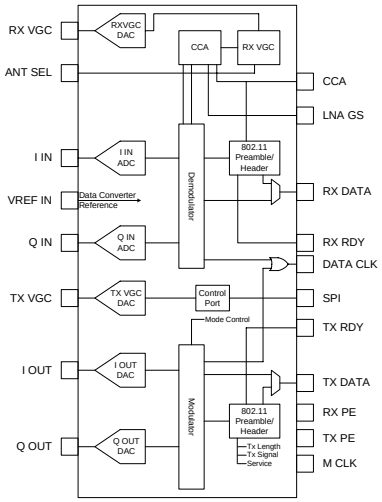
The RF3000 is a monolithic CMOS baseband processor. It is suitable for use in 11Mbps IEEE802.11b wireless LAN systems, and contains all functions required to convert a spread-spectrum signal to bit stream. The on-chip equalizer provides protection against multi-path in high data rate modes. All functions are configurable via an SPI port. A complete 2.4GHz radio reference design is available from RFMD.



Package Style: SSOP-28

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ InGaP/HBT
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaN HEMT
- ☐ GaAs MESFET
- ☑ Si CMOS
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- On-Chip ADCs and DACs, RSSI, AGC
- BPSK/QPSK/CCK
- 250nS Delay Spread Equalizer
- Supports Antenna Diversity
- Reference Design Available

Ordering Information

RF3000	Spread-Spectrum Baseband Modem
RF3000 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+4.0	V_{DC}
Input, Output or I/O Voltage	Ground-0.5 to VCC+0.5	V_{DC}
Voltage	2.7 to 3.6	V
VDDD Output	2.7	V_{DC}
Max. Storage Temperature	-65 to +150	°C
Max. Junction Temperature	+150	°C
Operating Ambient Temperature	-40 to +85	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC Electrical					See Figures 15 and 16. V_{CC}=3.0V to 3.3V±10%, T_Z=-40°C to +85°C
Power Supply Voltage	2.7	3.3	3.6	V	VDDA
	TBD	2.2	TBD	V	VDDD, Output Only.
V_{REF}	1.6	1.7	1.8	V	No current draw.
Input Voltage	2.5		VDDA+0.2	V	Logical “1” (V_{IH})
	-0.2		+0.7	V	Logical “0” (V_{IL})
Output Voltage	TBD	VDDA-1.0	TBD	V	Logical “1” (V_{OH})
	TBD	0.2	0.7	V	Logical “0” (V_{OL})
Current Consumption		25	TBD	mA	Transmit Mode (I_{TX})
		50	TBD	mA	Receive Mode (I_{RX})
Sleep Mode		500	500	µA	Mode 1, Reset Active, No Clocks (I_{S1})
		1.5	1.5	mA	Mode 2, Reset Inactive, No Clocks (I_{S2})
Input Leakage Current			10	µA	I_I
Output Leakage Current			10	µA	I_O
Output Loading		20	20	pF	
AC Electrical					V_{CC}=3.0V to 3.3V±10%, T_A=-40°C to +85°C. See Note 1.
M CLK Duty Cycle	40/60		60/40	%	
Rise/Fall	-		10	nS	All outputs. See Notes 2 and 3.
TXPE to I_{OUT}/Q_{OUT}	3.0		3.1	µS	1st valid chip. 802.11 modes.
TXDATA to I/Q_{OUT}			1.0	µS	
TXPE Inactive Width	1			µS	See Notes 2 and 4.
TXRDY Active to 1st DATACLK Hi	500			nS	
Setup TXDATA to DATACLK	10			nS	
Hold TXDATA to DATACLK Hi	10			nS	
Reset to TXPE	100			µS	
Reset to RXPE	100			µS	
TXDATA Modulation Extension	2			µS	See Notes 2 and 5.
RXPE Inactive Width	0			nS	See Notes 2 and 6.
DATACLK Period	90			nS	11Mbps Mode
DATACLK Width Hi or Low	22	44	68	nS	11Mbps Mode
DATACLK to RX Data	30			nS	
RXRDY to 1st DATACLK	40			nS	See Note 2.
RXDATA to 1st DATACLK	40			nS	
Setup RXDATA to DATACLK	30			nS	
RESET Width Active	40			nS	See Note 2.
RXPE to CCA Valid			15	µS	See Note 2.
RXPE to RSSI Valid			15	µS	See Note 8.
I/Q_{IN} to RXDATA			2.25	µS	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
I/Q ADC					
Full Scale Input Voltage		0.7	+10%	V_{P-P}	See Note 7.
Input Bandwidth		11		MHz	
Input Capacitance		5		pF	
Input Impedance	50			kΩ	
I/Q DAC					
Full Scale Output Voltage		200		mV	See Note 7.
Sample Rate		11		MHz	
Resolution		6		bits	
DNL		0.5		LSB	
INL		0.5	1.0	LSB	Tested for monotonicity.
TX VGC DAC					
Maximum Gain Output Voltage		1.2		V	
Minimum Gain Output Voltage		2.0		V	
Resolution		6		bits	
DNL		0.5		LSB	
INL		0.5	1.0	LSB	Tested for monotonicity.
RX VGC DAC					
Maximum Gain Output Voltage		1.2		V	
Minimum Gain Output Voltage		2.0		V	
Resolution		6		bits	
DNL		0.5		LSB	
INL		0.5	1.0	LSB	Tested for monotonicity.
Control Port Timing Characteristics					
SPI Mode					Mode Switching Characteristics. See Figure 3.
C CLK Clock Frequency			6	MHz	f_{CLK}
CS High Time Between Transmissions	1.1			µS	t_{CSH}
CS Falling to C CLK Edge	22			nS	t_{CSS}
C CLK Low Time	68			nS	t_{CLKL}
C CLK High Time	68			nS	t_{CLKH}
CD IN to C CLK Setup Time	42			nS	t_{DSU}
C CLK Rising to Data Hold Time	16			nS	t_{DHLD}
C CLK Falling to CD OUT Stable			47	nS	t_{PD}

Notes:

1. AC tests performed with C_L=20pF, I_{OL}=2mA, and I_{OH}=-1mA. Input reference level all inputs V_{CC}/2. Test V_{IH}=V_{CC}, V_{IL}=0V; V_{OH}=V_{OL}=V_{CC}/2.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Measured from V_{IL} to V_{IH}.
4. TX PE must be inactive before going active to generate a new packet.
5. I_{OUT}/Q_{OUT} are modulated after last chip of valid data to provide ramp-down time for RF/IF circuits.
6. A new search will begin after last bit of 802.11 packet in 802.11 modes.
7. Centered about 1.7V V_{REF}.
8. Accurate to within ±3dB of final gain setting.

For more information on Figure 1, see parameter table (on previous pages).

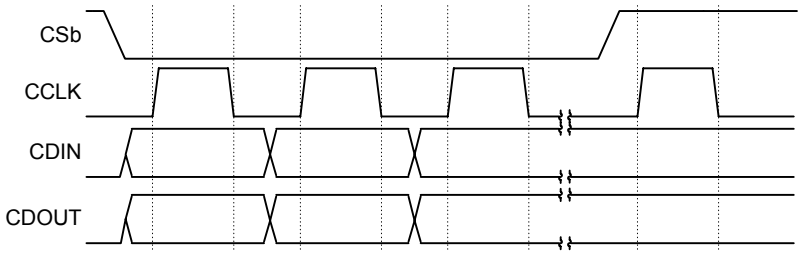


Figure 1. SPI Timing Transition Detail

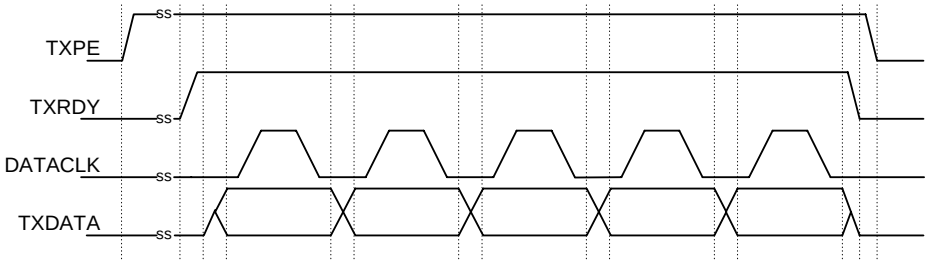


Figure 2. Transmit Port Detail Timing

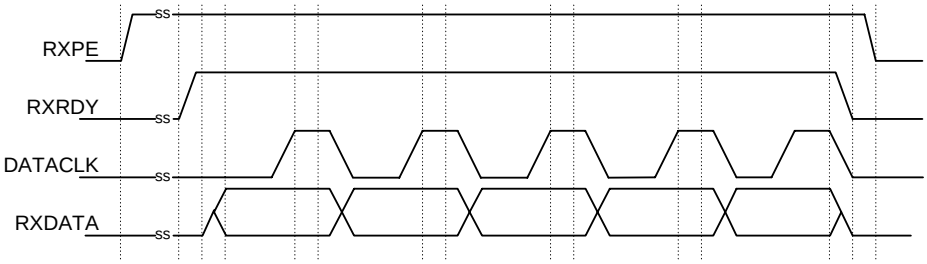


Figure 3. Receiver Port Detail Timing

Index

Pin	Function	Description	Interface Schematic
1	TXPE	Input from the external network processor. The rising edge of TX PE places the transmitter into an active state. The falling edge of TX PE indicates the end of transmission.	
2	RXPE	When active (value '1'), the receiver is powered up and CCA circuitry is active.	
3	MCLK	Master clock. This should be a 44MHz for IEEE802.11b and is used to generate other internally used clocks.	
4	TXRDY	Indicates that the chip is ready to accept data from the MAC for Tx.	
5	RXRDY	Indicates that the chip is ready to deliver data to the MAC from Rx.	
6	VDDD	Output from 2.2V internal voltage regulator for digital sections of RF3000. This pin should not be connected to anything.	
7	GNDD	Ground signal for digital power.	
8	CCA	Clear channel assessment per IEEE802.11b standard. “1” indicates “clear”.	
9	LNAGS	LNA gain select. “1” indicates “high gain”.	
10	TXDATA	TX data stream input.	
11	DATACLK	Data clock for TX and RX data.	
12	RXDATA	RX data stream output.	
13	CSb	In SPI mode this pin serves as serial port chip select.	
14	CCLK	Serial port clock. This clock is used for SPI mode.	
15	CDIN	In SPI mode this pin serves as CDIN input.	
16	CDOUT	In SPI mode this pin serves as CDOUT output.	
17	RXVGC	Analog receive variable gain control output: 1.2V to 2.0V.	
18	NC	Not connected.	
19	IIN	Analog I input.	
20	QIN	Analog Q input.	
21	VDDA	DC power for analog sections 3.3V.	
22	GNDA	Ground signal for analog power.	
23	IOUT	Analog I output: 1.6V to 1.8V.	
24	QOUT	Analog Q output: 1.6V to 1.8V.	
25	TXVGC	Analog voltage for transmitter variable gain control: 1.2V to 2.0V.	
26	ANTSEL	Antenna selection signal for diversity receiver.	
27	RESET	Pin='1' chip reset. Pin='0' standard operation.	
28	VREF	Reference voltage for internal data converters. Connect to RF2948 V_{REF} or set to 1.7V_{DC}.	

General Description

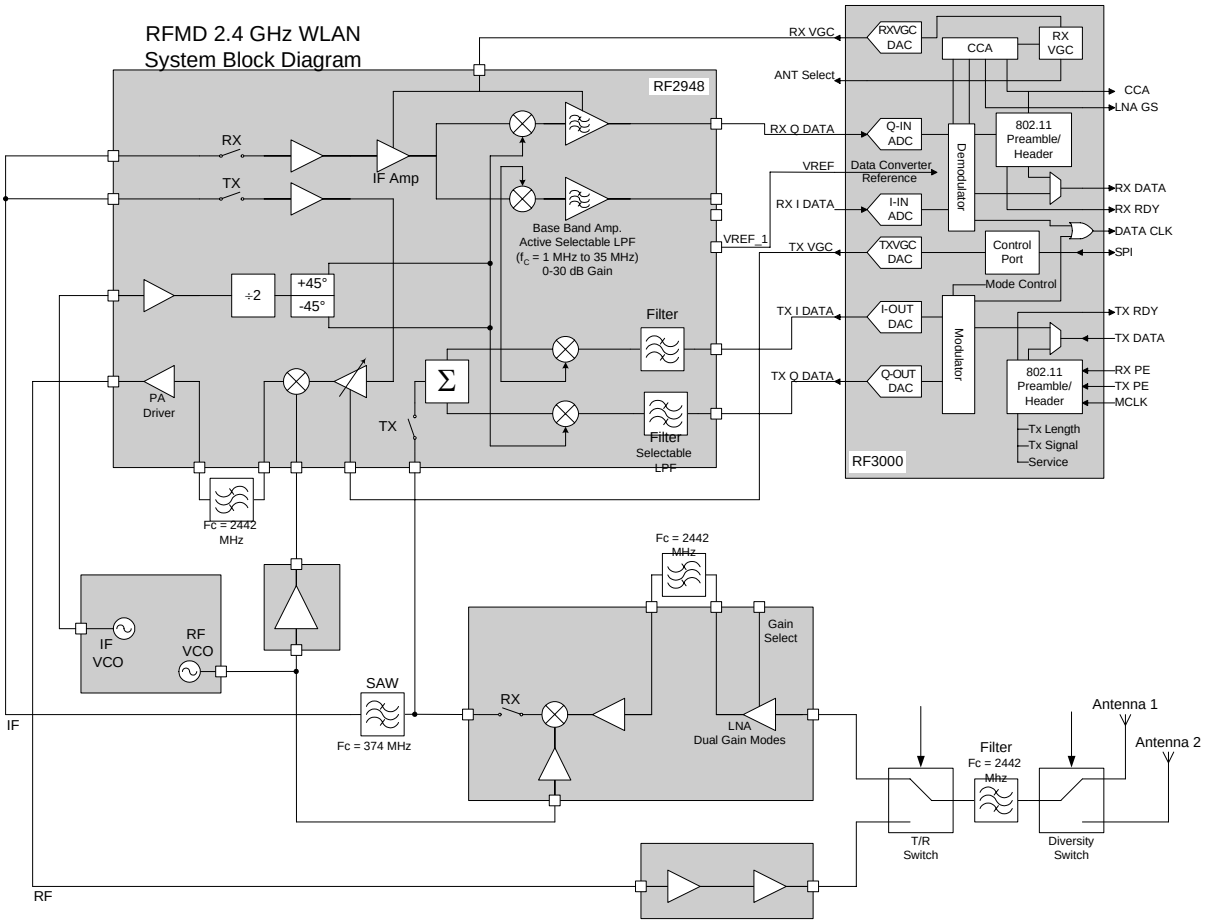


Figure 4. 2.4GHz IEEE802.11b Chipset Diagram

Figure 4 shows the complete 2.4GHz chipset, and where the RF3000 fits into the system. Figure 5 shows a simplified block diagram of the RF3000. The RF3000 is a complete spread-spectrum transceiver, allowing PSK system operation. The RF3000 performs all of the functions necessary to modulate a digital data source for transmission in a wireless environment. The RF3000: handles preamble and header generation and extraction; automatic gain control; clear channel assessment; antenna diversity; and, implements an equalizer to handle multi-path events at high data rates.

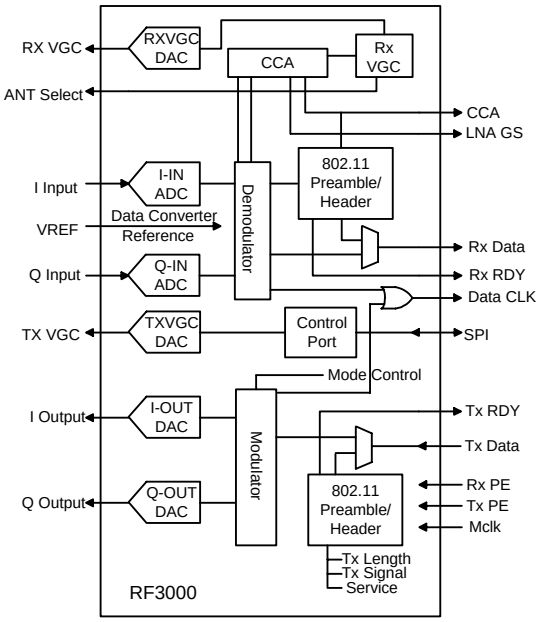


Figure 5. RF3000 Block Diagram

SPI Control Port

The control port is used by the Media Access Controller (MAC) to set up and modify the multiple operation modes of the RF3000. The port is set to SPI mode, with the RF3000 acting as Slave. Note that if no setup information is programmed into the RF3000's registers, it will default to a BPSK 1Mbps IEEE802.11b DSSS mode. If an IEEE802.11b mode is selected in Register 1, other waveform registers are ignored and the appropriate, standards compliant features are enabled (e.g., PN code, preamble/header, etc.). TX length is required for all IEEE802.11b modes.

All Registers, as defined in the Register Definition section of this datasheet, can be read in real time through this control port. Selected registers, as indicated in the Register section are read-only.

The control port of the RF3000 contains a mode to automatically increment the register pointer, allowing reading or writing of adjacent bytes without the need to stop and restart control port access.

SPI Mode Description

SPI mode pin definitions.

Pin Name	Description
$\overline{CS}$	Serial port chip select. A value of '0' is port enabled.
C CLK	Control port-bit clock input from serial port master.
CD IN	Serial data input to the RF3000. Data is clocked in on the rising edge of C CLK.
CD OUT	Serial data output from the RF3000. Data is clocked out on the falling edge of C CLK.

SPI Method of Operation

Write:

To Write into a register of the RF3000, the accessing SPI master needs to simply bring $\overline{CS}$ low, then Address the RF3000 (0100000_2) and provide a '0' for the Read/Write-bit. The user should note that all data transfers to/from the RF3000 are msb first. This should be followed by the Auto-increment-bit and the Memory address pointer (MAP), this is an 7-bit value to indicate the initial address for the write process. Register data is to immediately follow the MAP. If the Auto-Increment-bit is set RF3000 will continue to write data 1 byte at a time into the address pointed to by the MAP, and increment the MAP after each byte. When the SPI Master is finished filling registers, it must raise $\overline{CS}$ to indicate the cycle end.

Read:

Reading the contents of the RF3000 internal registers, the procedure is actually a write process followed by the read. The SPI Master must bring $\overline{CS}$ low, to prepare the RF3000 to look for its address. The SPI Master now addresses the RF3000, by placing the RF3000 base address (0100000_2) on the data bus and append a '0' for the Read/Write-bit. The SPI Master must now set the Auto-increment-bit and initialize the 7-bit MAP to the value of the register to be read. The user should raise $\overline{CS}$, to end the write portion of the cycle. To complete the Write/Read cycle the SPI Master now needs to lower $\overline{CS}$ again, and readdress the RF3000 providing a '1' for the Read/Write-bit. Once this is completed the RF3000 will begin outputting the register contents. As long as the $\overline{CS}$ remains low, and the auto-increment bit is set, the RF3000 will auto-increment the MAP. When the RF3000 reaches Address 31, the MAP will be reset to Register 0 and the process continues.

SPI Operation Summary

To Write:

9. Bring $\overline{CS}$ low.
10. Chip Address (7-bits) - This should match the RF3000 chip address of 0100000_2.
11. Read/Write-bit = '0'
12. Auto-Increment-bit - Value of '1' enables auto-increment
13. Memory Address Pointer (MAP) (7-bits) - This is the address of the register to be written to, MSB first.
14. Register Data (8-bits) - MSB First
15. Repeat step 6 if Auto-Increment or bring $\overline{CS}$ HIGH to end operation.

To Read:

1. Bring $\overline{CS}$ low.
2. Chip Address (7-bits) - This should match the RF3000 chip address of 0100000_2.
3. Read/Write-bit = '0'
4. Auto-Increment-bit - Value of '1' enables auto-increment
5. Memory Address Pointer (MAP) (7-bits) - This is the address of the register to be written to, MSB first.
6. Bring $\overline{CS}$ high.
7. Bring $\overline{CS}$ low.
8. Chip Address (same as step 2) - MSB First
9. Read/Write-bit = '1'
10. RF3000 will output 8-bit register value, MSB First, and Increment MAP, if Auto increment enabled.
11. Repeat step 10 for polling or Auto-Increment or bring $\overline{CS}$ high to end operation.

SPI Mode Functional Timing Diagrams

Write

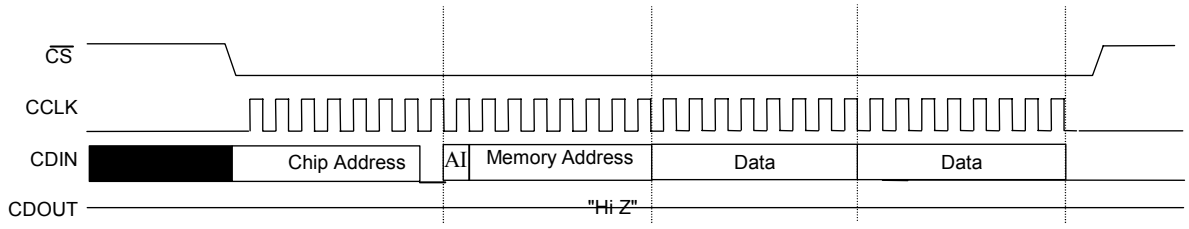


Figure 6. SPI Write Functional Timing Diagram

Read

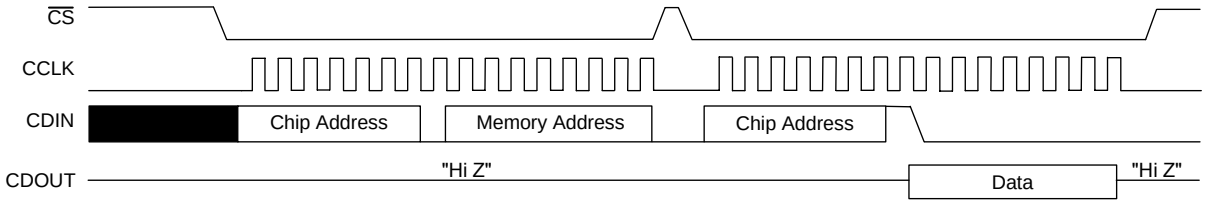


Figure 7. SPI Read Functional Timing Diagram

RF3000 Method of Operation

The transmitter power enable (TX PE) input enables the transmitter process. (Note: Transmit has priority over receive.) When TX PE is high, the LNA GS signal will be driven low. The TX RDY output indicates the readiness of the RF3000 to receive data for transmit. Transmitted data is passed into the RF3000 through the TX DATA input and clocked by the DATA CLK output. The receiver power enable (RX PE) input enables the receiver, and the receive data ready (RX RDY) signal indicates that received data is upcoming. The RF3000 generates the received data clocks, and outputs the received data, through the RX DATA output. The receiver port also provides a clear channel assessment (CCA) to the MAC.

The table below summarizes the operation of the chip. The user should note that RX PE must be High to perform CCA.

TX PE	RX PE	Operation
0	0	Standby mode.
0	1	RX is powered up. CCA circuity is active.
1	0	TX is powered up. Begin TX. CCA is inactive.
1	1	RESERVED

IEEE802.11b Transmit Modes

IEEE802.11b DSSS Transmit Modes

The RF3000 supports PSK and CCK DSSS modes defined in IEEE802.11b specification. The RF3000 also supports the optional short preamble and header format as defined in IEEE802.11b.

The following section describes IEEE802.11b DSSS data transmission. The user must first prepare the applicable control port registers to determine the mode of operation and the transmission length. The mode of operation must be written into Register 1, followed by setting the transmission length (in microseconds). The length is to be written into Registers 17 (bit 0 only), 18 and 19. Mode byte values for IEEE802.11b modes are summarized below

IEEE802.11 DSSS Mode	Mode Byte Value
1Mbps DBPSK	$0x00_{16}$
2Mbps DQPSK Long preamble	$0x20_{16}$
2Mbps DQPSK Short preamble	$0x30_{16}$
5.5Mbps CCK Long preamble	$0x40_{16}$
5.5Mbps CCK Short preamble	$0x50_{16}$
11Mbps CCK Long preamble	$0x60_{16}$
11Mbps CCK Short preamble	$0x70_{16}$

Once the control port values are written, the RF3000 is ready to transmit data. Optionally, the TX length value can be written during the 128μS of preamble. When the user is ready to transmit, TX PE is driven High. This signals the RF3000 to assemble and transmit the 802.11 preamble and header, as described below.

Preamble		Header				Data
128 1's	SFD (16-bits)	Service (8-bits)	Signal (8-bits)	Length (16-bits)	CRC (16-bits)	Data (x-bits)

The preamble and header for 1Mbps mode is always transmitted as 1Mbps BPSK. However for 2Mbps, 5.5Mbps and 11Mbps modes, IEEE802.11b allows a short preamble, which has the preamble, transmitted as 1Mbps BPSK and the header transmitted as 2Mbps QPSK. The usage of the optional short preamble is selected when the transmission mode is written to the control port.

The RF3000 signals that it is nearing the end of the preamble and header transmission by driving TX RDY high. This signals the user that transmission data clocks are coming. When the RF3000 is ready to transmit data it will begin clocking transmit data. Data to be transmitted should be present on TX DATA on the rising edge of DATA CLK. The RF3000 will only clock in the number of data-bits to fill the specified transmission time.

IEEE802.11b DSSS Transmission Summary

1. TX Mode different:
   Write value to the mode register according to table.
2. TX Length different:
   Write the number of uS to transmit in the TX length registers.
3. Drive TX PE High and wait for TX RDY to go High.
4. Transmit data must be valid on the rising edge of DATA CLK.

Figure 8 shows the primary interface mode for the RF3000 TX Data port.

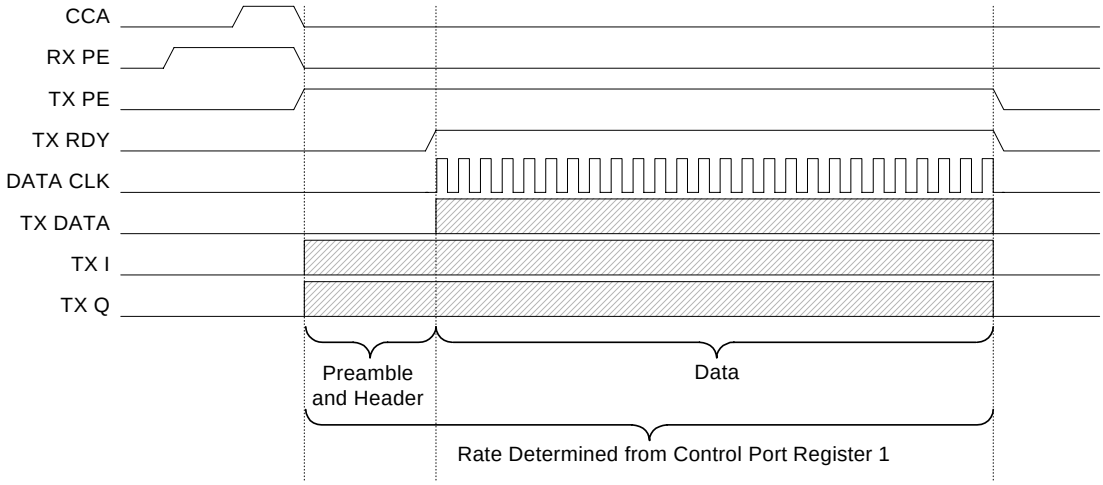


Figure 8. IEEE802.11b Transmit Timing Overview

The RF3000 has provision for an alternate Transmit Data port interface. In the transmit interface an extra clock is asserted after TXRDY goes 'high' and before the first TX data clock on DATA CLK, see Figure 8a. The alternate Transmit interface is enabled by writing 0x08 into RF3000 Register 0x1C.

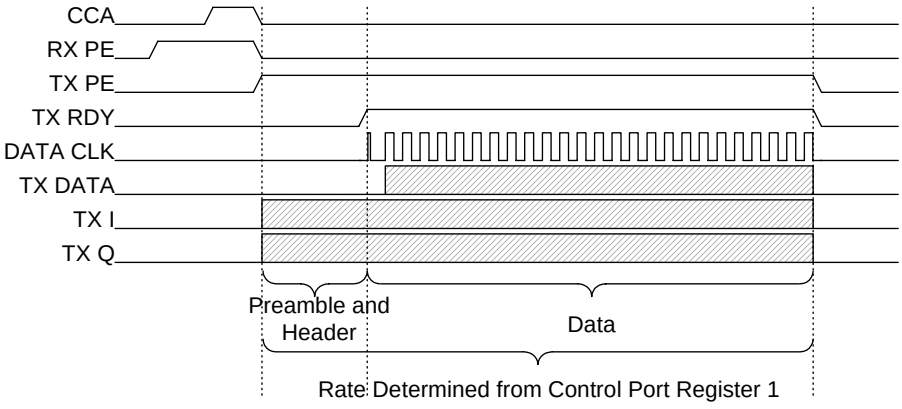


Figure 8a. Alternate Transmit Interface

IEEE802.11b Receive Mode

The RF3000 receiver has an interface similar to the transmit port, and provides link support data through the control port. The user drives RX PE High to enable the receiver circuitry. The RF3000 then begins to watch the incoming data stream for a valid Barker code PN sequence.

The RF3000 contains logic to perform AGC when used in conjunction with the RF2948 and RF2494 as in the RF031X reference designs for IEEE802.11b. The following sections will explain the method of AGC and the calibration hooks that exist inside the RF3000 to compensate for manufacturing tolerances in total system gain of an IEEE802.11b radio.

Diversity

The RF3000 makes diversity decisions every 1mS while looking for A/D saturation according to the state machine in Figure 9.

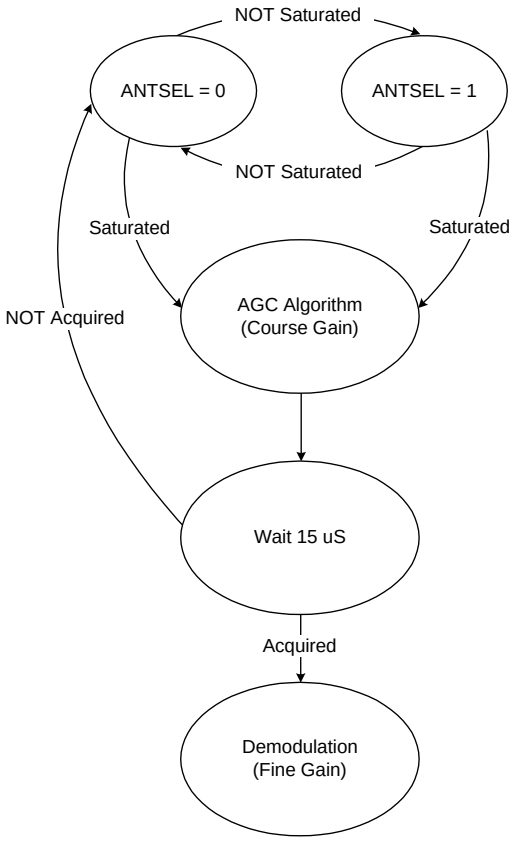


Figure 9. Diversity and AGC Algorithm

AGC Algorithm

The RF3000 AGC algorithm is implemented to automatically control both the RXVGC of the RF2948 and the LNAGS pin of the RF2494. The RF3000 is programmed to search the possible gain settings of LNAGS and RXVGC in a binary fashion to quickly determine the final gain setting needed to optimize the inputs to the A/D converters for demodulation. The AGC algorithm is completely controlled by detection of saturation of the A/D converters.

The RF3000 begins the algorithm by setting the RXVGC and LNAGS pins to a predetermined maximum gain condition. Upon detection of A/D saturation, the RF3000 will decrease the system gain (via the RXVGC pin) to a predetermined “mid-point”. This mid point is chosen to allow the RF3000 to determine the correct setting of the LNAGS pin. If the RF3000 detects saturation at this “mid-point”, the RF3000 will place the RF front end into a low gain mode, and will begin searching for the correct RXVGC setting in a binary tree fashion. If the RF3000 does not detect saturation on the A/D converters while at this “mid-point”, the RF3000 will leave the LNAGS pin in high gain mode and proceed with the binary search of RXVGC. This binary tree representation of the gain algorithm can be seen in Figure 9. It is important to note that once the RF3000 makes a decision on the LNAGS setting, that setting will remain for the entire duration of the packet and cannot be altered until the next packet.

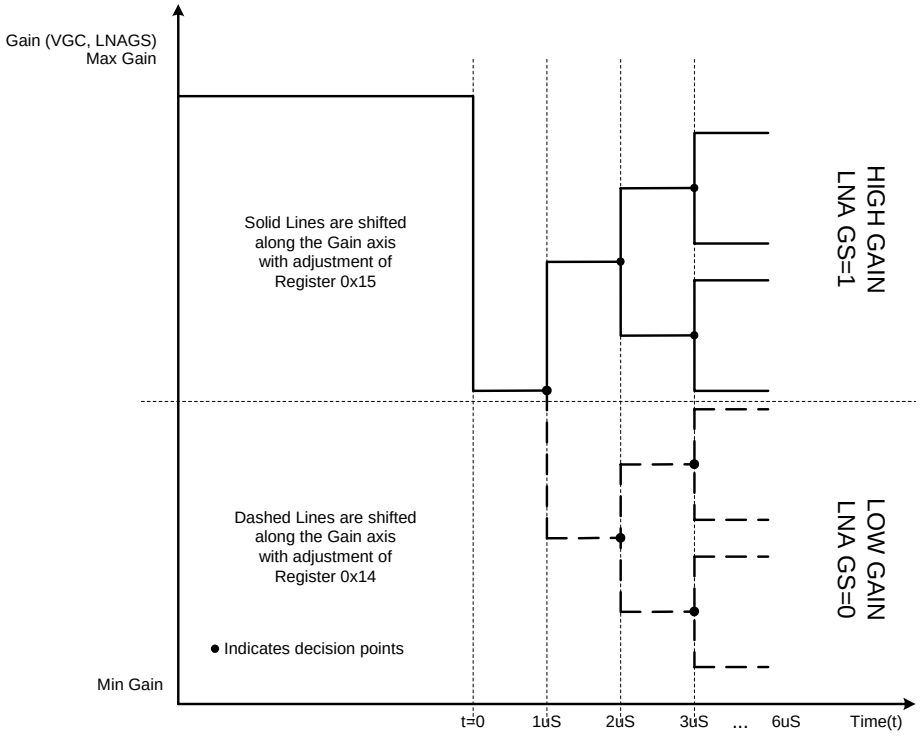


Figure 10. AGC Decision Structure

RSSI is a function of RXVGC and LNAGS. RSSI is updated every 1μS during the AGC algorithm. While demodulating data, the demodulator will make fine tuning adjustments to RSSI based on the value of RXVGC.

An optional AGC algorithm is available, enabled by writing a '1' into bit 4 of Register 0x1C. In this mode the AGC may be kicked off after it has already settled if a large signal is present. This addresses a scenario in which an interferer (which may be noise) initially kicks off the AGC. The AGC then chooses the gain setting to accommodate this level of signal. Subsequently, a desired signal is incident on the antenna. This signal may be larger than the interferer and, because of the gain setting of the radio, may be difficult to demodulate. Under the optional AGC mode, the gain would be re-optimized to the desired signal. We believe that this will help radio performance in many environments. When using the new AGC algorithm, Register 0x1C should be written to 0x78. The values of 0, 1, 1 in b7, b6, b5 respectively increases the saturation requirement for the AGC algorithm. This has the effect of biasing the algorithm to produce a higher gain setting to give the baseband processor an optimum input amplitude for robust demodulation.

Another optional mode has been added to the AGC algorithm. This mode adds a delay into the algorithm after the LNA gain select is changed to allow enough time for the radio to settle properly. The delay eliminates the possibility of a 'dead zone' where there is a small range of input power levels with a probability that the AGC will settle to an incorrect gain setting. To enable this mode, Register 0x1D is written to 0x80. In addition, the 6 lsb's of reg20 must be set to 4 higher the 6 lsb's of reg21 because the outcome of the AGC decision step will change. If this mode is not to be used, Register 0x1D should be written to 0x00.

AGC Calibration

The RF3000 is preprogrammed for a “typical” radio. The default settings of the RF3000 may be used without modification, but the conditions of the AGC algorithm may be modified by writing to register 21 and register 20 of the control port. Register 21 controls an offset to the RXVGC DAC for LNAGS=1 (high gain mode), and register 20 controls an offset to the RXVGC DAC for LNAGS=0 (low gain mode). Caution should be taken when setting these registers; incorrect settings can create a “dead zone” between the high/low gain trees. The following figure shows the “typical” settings for the RXVGC output of the RF3000 during LNAGS=1. Also shown are the expected production variances of an IEEE802.11 radio, and the calibration ranges of the RF3000. Writing to register 21 of the RF3000 will move the range of AGC operation on the RXVGC pin. For example, if the six LSB's in register 21 are written to 000100b (4 decimal), the starting point for the AGC algorithm (max gain) will be with a DAC code of 8+4=12 codes, and the LNAGS decision will be made at a code of 47+4=51 codes. This has the overall effect of decreasing the gain provided by the RF2948 by four D/A codes or approximately 5dB for both initial AGC setting for detection of saturation and for determining LNAGS. Likewise if the six LSB's of register 21 are written to 1111000 (-4 decimal), the initial condition that the RF3000 uses to look for saturation is 8-4=4 codes, and the LNAGS decision is determined at 47-4=43 codes.

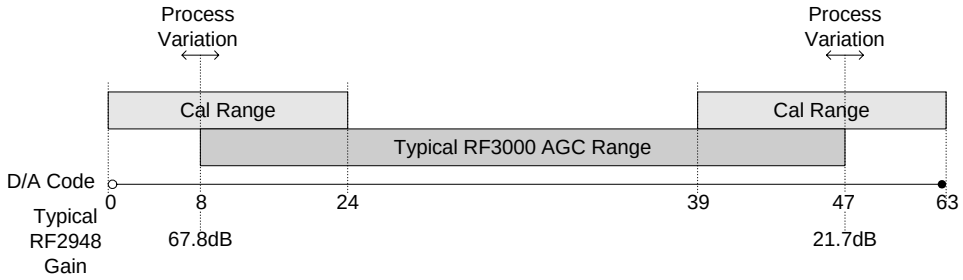


Figure 11. High Gain Mode (LNAGS=1) Plot of RXVGC Showing Normal Operation and Calibration Ranges

Similar to the high gain calibration, register 20 controls an offset into the LNAGS=0 (low gain mode) values that are applied to the D/A converter. The figure below shows the normal operation range of the RF3000 and the calibration range that is provided.

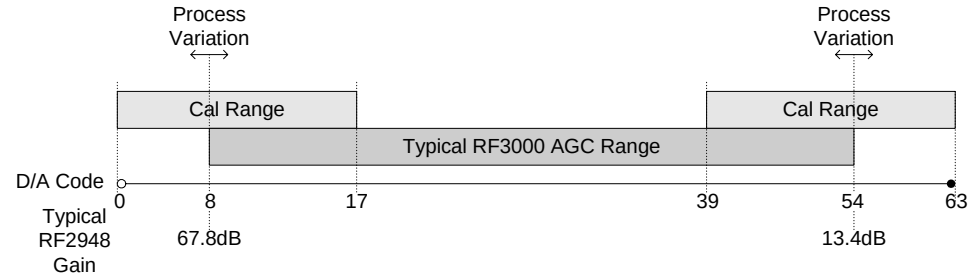


Figure 12. Low Gain Mode (LNAGS=0) Plot of RXVGC Showing Normal Operation and Calibration Ranges

High Gain Calibration Procedure

Calibration of an IEEE802.11b radio can be accomplished by sending a repetitive pattern to the radio at a known input power, and adjusting the register settings until all packets are correctly received without errors or missing packets. A simple procedure is contained outlined as follows.

1. Write the six LSB's of register 21 to the value 011000 (24 decimal). This will decrease the total system gain.
2. Apply an 1Mbps IEEE802.11b signal to the input of the radio of a known input power (-75dBm).
3. Decrease the six LSB's of register 21 by one LSB until all packets are received correctly without dropping any packets.
4. Since the input power of the reference signal was set to -75dBm (to eliminate effects of thermal noise), calculate the final register 21 setting by subtracting a known predetermined value from the value found in step 3 of the calibration procedure.

Low Gain Calibration Procedure

Similar techniques can be applied to calibrate the Low gain settings of the RF3000. As an initial value, the register setting in register 20 should be equal to the value of register 21. Register 20 is provided to allow manufacturing calibration to account for reverse isolation variances in the T/R switch if used as an additional pad.

Post-AGC

When the Barker code is acquired, the RF3000 assigns the ACQ-bit in the mode register to a 1 and proceeds to extract the header information. When the start frame delimiter is identified, the RF3000 will assign a 1 to the SFD-bit in the mode register. The RF3000 will now decode the transmission mode and data length from the header, and check the header via the 16-bit CRC. The RF3000 will then clock-out 32 bits of header information. This will be the 8-bit RX signal field, followed by the 8-bit RX service field, and then the 16-bit RX length field. The MAC can also read these values through the serial port registers 0x04 through 0x07.

The header data will be followed by 16 bit times of no clock transitions.

Immediately before providing data, the RF3000 will drive RX RDY High. The received data will be stable on the rising edge of DATA CLK. In the event the header CRC is incorrect, the RF3000 will bring RX RDY high for the duration of the packet, but no DATA CLK or RX DATA transitions will occur.

IEEE802.11b DSSS Receive Summary

1. Drive RXPE High.
2. RF3000 looks for incoming valid Barker Code.
3. RF3000 sets ACQ bit in Register 0x01.
4. When the Start Frame Delimiter is identified, the RF3000 sets the SFD bit in Register 0x01.
5. RF3000 Extracts Header information.
   This information is copied into the RF3000 RX Status, Service fields and presented on the RXDATA Pin with Clocks on DATA CLK.
6. This will be followed by 16 bit times of no clock transitions.
7. RF3000 Drives RXRDY high, and clocks Received Data on the rising edge of DATA CLK.
8. RF3000 Drives RXRDY low at the end of the data packet.

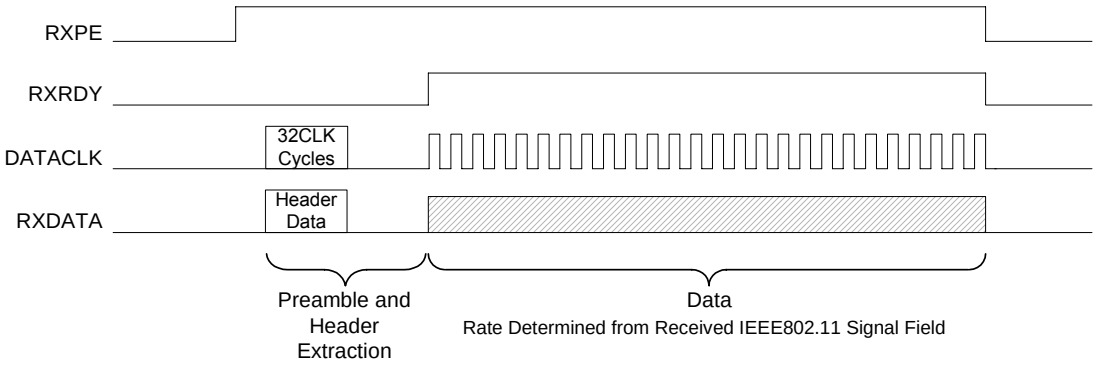


Figure 13. IEEE802.11b Receive Timing Overview

The RF3000 has provision for an alternate Receive Data port interface. In the receiver interface, the DATACLK is inverted, and an extra clock is asserted after RXRDY goes 'low' indicating the end of the received packet, see Figure 13a. The alternate Transmit interface is enabled by writing 0x08 into RF3000 Register 0x1C.

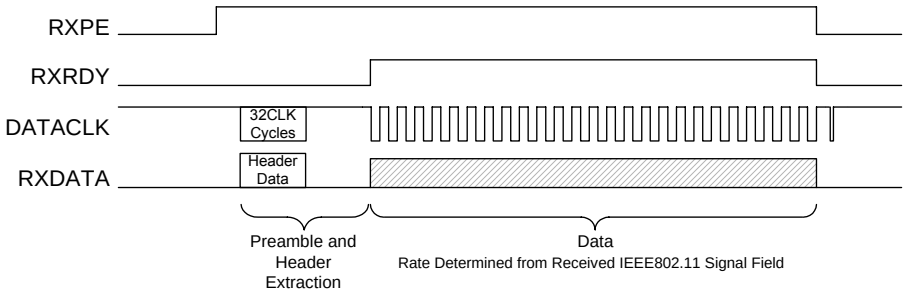


Figure 13a. Alternate Receiver Interface

Block Diagram Breakout

The following sections describe each of the blocks, as indicated in the block diagram, that comprise the RF3000.

Modulator

PSK Modes

The RF3000 uses a proprietary architecture that allows the modulation of PSK signals by simply reprogramming the part via the control port. The transmitted data stream is first spread and the resulting data stream is modulated.

CCK Mode

IEEE802.11b Preamble/Header Creation and Assembly

The RF3000 provides circuitry to generate and assemble a preamble and header as specified in the IEEE802.11b specification. The short preamble option for 2Mbps, 5.5Mbps and 11Mbps, as specified in IEEE802.11b, is selectable in the mode control register. The RF3000 will transmit these fields along with a protective CRC-16 for error detection. For other protocols, the preamble/header circuitry is disabled, and packet structures should be generated externally.

Demodulator

PSK Modes

The RF3000 uses a proprietary architecture that allows the demodulation of PSK signals by simply reprogramming the part via the control port. The received signal is first de-spread and the PSK signal is recovered.

CCK Mode

In order to perform CCK demodulation, circuitry is provided to pass the output of the A/D converters to a fast Walsh transform (FWT). The output of the FWT is then passed to decision circuitry to determine the received signal.

IEEE802.11b Preamble/Header Detection and Extraction

Circuitry is provided to search the incoming data for start frame delimiter (SFD) and to obtain length field information as well as modulation type. In 802.11 modes, this circuitry is always active since the preamble and header tells the PHY which modulation type the data packet is using. The RF3000 will also check the preamble/header field for errors by checking the CRC-16 field for errors.

Data Converters

The RF3000 contains all A/D converters and D/A converters required to implement a transceiver.

A/D Converters

I/Q A/Ds - These are 4-bit analog-to-digital converters used to sample the data according to the mode of the RF3000.

D/A Converters

Four (4) digital-to-analog converters are present for transmitter VGC, receiver VGC, I Out, and Q Out.

RSSI, CCA and AGC

Scramblers

Scramblers for whitening the spectrum are provided, as specified in IEEE802.11b.

SCRAMBLER NOTE: The data scrambler defined by IEEE802.11b has a probability of 1/128, to lock up scrambling when random data is followed by a repetitive pattern. The patterns identified are: all 0's; all 1's; repetitive 01's; repeated 0011's; and, repeated 000111's. Once the pattern ceases the scrambler will resume its normal operation.

Diversity
Switching and detection at beginning of Receive.

Equalizer
Proprietary architecture, active only in 5.5Mbps and 11Mbps CCK modes. For multipath cancellation, the RF3000 defines the path with the largest magnitude as the main path and all others as secondary paths. The RF3000 equalizer can cancel the two most significant secondary paths. these can either be two (2) post-cursor, echo paths, or they can be one (1) post-cursor and one (1) pre-cursor paths. Pre-cursor delay can be up to one-quarter symbol period. Post-cursor delay can be up to one (1) symbol period. The magnitude of cancelled multipaths up to -3dBc, normalized to the main path.

Control Port Register Definitions for RF3000

Register 0x00 - Reserved

R7	R6	R5	R4	R3	R2	R1	R0

This register is reserved.

Register 0x01 - Modem Control and RX Status

Mode 3	Mode 2	Mode 1	Mode 0	Short Preamble*	ACQ *	SFD *	CRC *

***** - Read Only

This register is used to setup primary operation of the modem.

NOTE: The four (4) LSB's are read-only and reflect the receiver status.

Mode (3-0) - TX Mode

Mode 3	Mode 2	Mode 1	Mode 0	Mode ID	Notes
0	0	0	0	802.11 1Mbps DSSS	***Default Mode***
0	0	0	1	Reserved	Reserved
0	0	1	0	802.11 2Mbps DSSS	Long preamble
0	0	1	1	802.11 2Mbps DSSS	Short preamble
0	1	0	0	802.11 5.5Mbps CCK	Long preamble
0	1	0	1	802.11 5.5Mbps CCK	Short preamble
0	1	1	0	802.11 11Mbps CCK	Long preamble
0	1	1	1	802.11 11Mbps CCK	Short preamble
1	0	0	0	BPSK	Reserved
1	0	0	1	QPSK	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved

Default 802.11 1Mbps DSSS, RX mode detected automatically.

NOTE: In 802.11 modes, the received data rate will be accepted from the received header and therefore will be selected automatically.

Short Preamble - READ ONLY

0 - Long Preamble Received

1 - Short Preamble Received

ACQ - Receiver acquisition status - READ ONLY

0 - Not locked

1 - acquired

SFD - 802.11 SFD status - Read Only

0 - Not found

1 - SFD detected

CRC - 802.11 RX CRC - Read Only

0 - CRC valid

1 - CRC error

Register 0x02 - CCA Control

CCA1	CCA0	RSSI_t5	RSSI_t4	RSSI_t3	RSSI_t2	RSSI_t1	RSSI_t0

CCA1, CCA0 - 802.11 CCA Mode:

CCA1	CCA0	CCA Mode
0	0	RSSI Threshold Sensitive
0	1	Acquisition Sensitive
1	X	Both

RSSI_t - 6-bit RSSI threshold value for CCA.

Register 0x03 - Diversity and RSSI Value

Diversity	Cpantsel	RSSI5 *	RSSI4 *	RSSI3 *	RSSI2 *	RSSI1 *	RSSI0 *

***** - Read Only

NOTE: The six (6) LSB's are read-only and reflect the receiver status.

Diversity - RX diversity enable bit.
Default - 0

0 - No diversity, ANT SEL pin is forced to Cpantsel.
1 - Diversity active, RF3000 automatically selects ANT SEL pin.

Cpantsel - Antenna selection bit in non-diversity mode.
Default - 0

0 - ANT SEL forced to 0.
1 - ANT SEL forced to 1.

RSSI5-0 - Output of the RSSI A/D - Read Only

Register 0x04 - RX Signal Field (Read only)

RX_Sig7	RX_Sig6	RX_Sig5	RX_Sig4	RX_Sig3	RX_Sig2	RX_Sig1	RX_Sig0

In DSSS modes, this value is the received byte of the received signal field. In FHSS, only the four (4) LSB's are used.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Received Mode
0	0	0	0	1	0	1	0	1Mbps DSSS
0	0	0	1	0	1	0	0	2Mbps DSSS
0	0	1	1	0	1	1	1	5.5Mbps DSSS
0	1	1	0	1	1	1	0	11Mbps DSSS
0	0	0	0	0	0	0	0	Reserved
0	0	0	0	0	0	0	1	1.5Mbps FSK***
0	0	0	0	0	0	1	0	Reserved
0	0	0	0	0	0	1	1	2.5Mbps FSK***
0	0	0	0	0	1	0	0	3Mbps FSK***
0	0	0	0	0	1	0	1	3.5Mbps FSK***
0	0	0	0	0	1	1	0	4Mbps FSK***
0	0	0	0	0	1	1	1	4.5Mbps FSK***

*** - IEEE802.11b proposed modulation rates not currently supported.

Register 0x05 - RX Length Field MSB's (Read only)

RX_LN15	RX_LN14	RX_LN13	RX_LN12	RX_LN11	RX_LN10	RX_LN9	RX_LN8

The upper byte of the length field received.
In DSSS mode, this value is the length in microseconds of the received data packet.

Register 0x06 - RX Length Field LSB's (Read only)

RX_LN7	RX_LN6	RX_LN5	RX_LN4	RX_LN3	RX_LN2	RX_LN1	RX_LN0

The lower byte of the length field received.

Register 0x07 - RX Service Field (Read only)

RX_SER7	RX_SER6	RX_SER5	RX_SER4	RX_SER3	RX_SER2	RX_SER1	RX_SER0

This register is used per IEEE802.11b specification.
RX_SER7 is length field extension in high data rate proposal 802.11b.
RX_SER3 is modulation selection bit for high rate transmission.
0 - CCK
RX_SER2 signifies Synth Clock to Signal Clock per 802.11 specification.

Register 0x08 - Reserved

Register 0x09 - Reserved

Register 0x0A - Reserved

Register 0x0B - Reserved

Register 0x0C - Reserved

Register 0x0D - Reserved

Register 0x0E - Reserved

Register 0x0F - Reserved

Register 0x10 - Reserved

Register 0x11 - TX Variable Gain and TX Length Field Extension

TXVGC5	TXVGC4	TXVGC3	TXVGC2	TXVGC1	TXVGC0	SCRAMBLER	TX_LN16

TXVGC5-TXVGC0 - Gain setting for transmission.
000000 - Min gain
111111 - Max gain

SCRAMBLER - This bit enables and disables the IEEE802.11b data scrambler.

Bit Value	Scrambler Mode
0	Enabled
1	Disabled

TX_LN16 - TX length extension bit as defined in IEEE 802.11b specification.

Register 0x12 - TX Length Field MSB's

TX_LN15	TX_LN14	TX_LN13	TX_LN12	TX_LN11	TX_LN10	TX_LN9	TX_LN8

Register 0x13 - TX Length Field LSB's

TX_LN7	TX_LN6	TX_LN5	TX_LN4	TX_LN3	TX_LN2	TX_LN1	TX_LN0

Registers 0x12 and 0x13 indicate the number of microseconds that the RF3000 is to transmit after receiving a request to start transmission.

Register 0x14 - Low Gain Calibration

Reserved	Reserved	Low_Gain5	Low_Gain4	Low_Gain3	Low_Gain2	Low_Gain1	Low_Gain0

Bit 5 .. Bit 0:Low Gain Calibration, Range -32 to +16

Register 0x15 - High Gain Calibration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Channel 14 Filter	DSSS PAD	High_Gain5	High_Gain4	High_Gain3	High_Gain2	High_Gain1	High_Gain0

Bit 7: A value of '1' enables the channel 14 filter
Bit 6: 6dB pad of DS modes
Bit 5 .. Bit 0:High Gain Calibration, Range -8 to +31

Register 0x16 - Reserved

Register 0x17 - Reserved

Register 0x18 - Reserved

Register 0x19 - Reserved

Register 0x1A - Reserved

Register 0x1B - Reserved

Register 0x1C - Options Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SAT_THRESH [2]	SAT_THRESH [1]	SAT_THRESH [0]	ALT AGC	Enabled Alternative Data Port Interface	RESERVED '0'	RESERVED '0'	RESERVED '0'

Bit 7 .. Bit 5:Signed Magnitude Offset for all steps of course AGC. Saturation threshold is 4+ value where $V=3 \leq Value \leq 3$.
Bit 4: A value of '1' allows the AGC algorithm to retrigger with ADC saturation.
Bit 3: A value of '1' enables the alternate TX/RX data bus interface.
Bit 2: Reserved, set to '0'.

Register 0x1D - Options Register 2

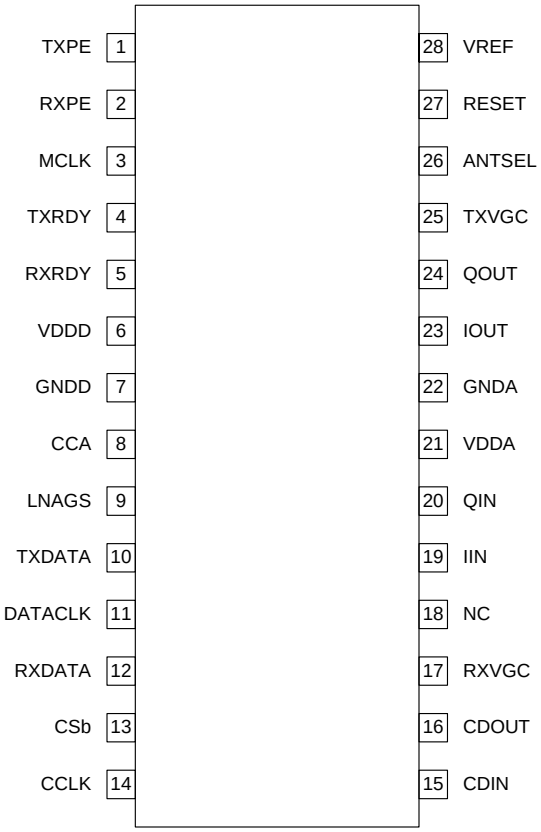
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LNAGS DELAY	RESERVED '0'	RESERVED '0'	RESERVED '0'	RESERVED '0'	AGC Re-trigger Threshold	RESERVED '0'	RESERVED '0'

Bit 7: LNAGs Delay - When set to '1', this delays the next AGC decision step an extra 1μS (total of 2μS) if a transition of the LNAGs pin from 1 to 0 occurs.
Bit 6 .. Bit 3:Reserved, set to '0'.
Bit 2: Sets threshold for AGC re-trigger.
'0' sets re-trigger threshold to high count.
'1' sets re-trigger threshold to low count.
Bit 1: Reserved, set to '0'.
Bit 0: Reserved, set to '0'.

Register 0x1E - Reserved

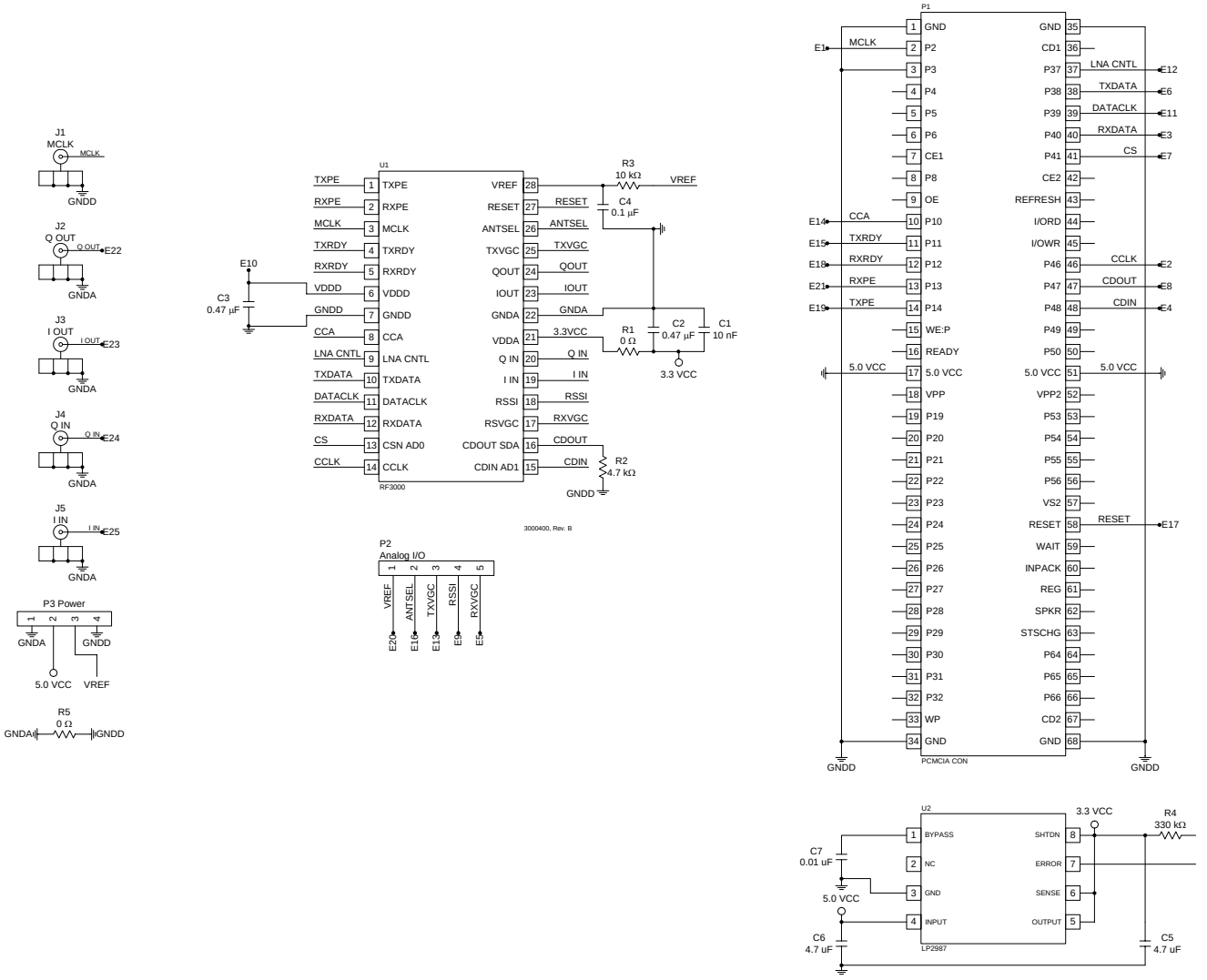
Register 0x1F - Reserved

Pin Out



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 2.12” x 3.57”

Board Thickness 0.062”, Board Material FR-4